A Simulation-Based Investigation on the Effect of Transistor Reordering on the Timing Behavior of MOS Digital Circuits[1]

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Abstract— Many CAD researchers have taken advantage of the freedom to permute series connected transistors in MOS digital circuits in an attempt to decrease layout area without addressing the effect this has on the timing performance of the circuit. Such transistor permutations (or reordering), although will not change the logical behavior of a circuit, can have significant and profound effects on the timing behavior of the circuit. Therefore, the effect of transistor reordering on the timing behavior of MOS circuits is investigated in this paper. The investigation is performed by analyzing the transient response of Series Connected MOS Structures (SCMS's) using SPICE. The investigation shows that the effect of transistor reordering on the timing performance of a MOS logic gate varies significantly depending on transistor strengths, stack height, load capacitance and critical input signal transition time. Circuits for which the effect of transistor reordering on timing is insignificant are clearly recognized. It is shown how the results of this investigation are used to optimize the performance of CMOS circuits.

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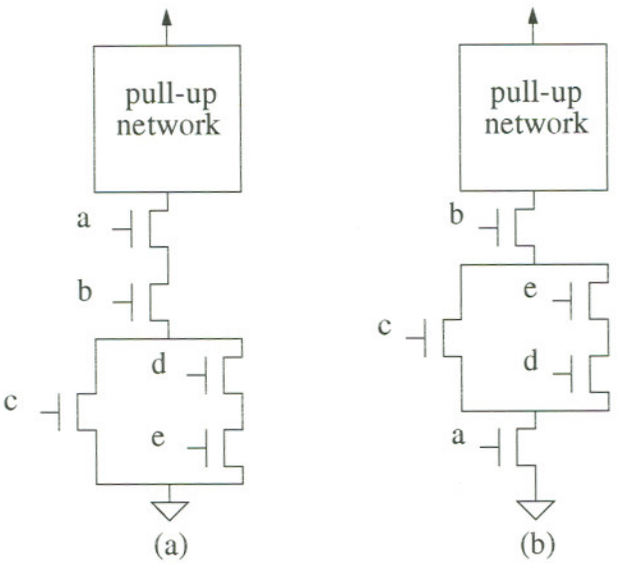


Fig. 1. Two different CMOS implementations of the function $\overline{ab(c+de)}$.

I Introduction

During the past twenty years researchers have been designing tools for the automatic design of specific subcircuits (e.g., routing channels, functional cells, PLAs, etc.) of integrated circuits. This research has led to a variety of techniques for improving different characteristics of automatically synthesized integrated circuits. The characteristics which researchers have paid particular attention to in the MOS technology include layout area, timing, power dissipation and yield. In the MOS technology logic gates may be designed to implement arbitrary switching functions [1] as shown in Fig. 1. The locations of specific transistors or groups of transistors in a MOS logic gate may be interchanged without altering the logical behavior of the circuit. For example, the circuit shown in Fig. 1(a) implements the same logic function as that of Fig. 1(b); however, some of the transistors are placed in different physical locations with respect to other transistors in the circuit. A recent trend in the design of CAD tools for layout synthesis has been to reorder the transistors in a MOS logic gate in an attempt to improve layout area. Reordering has been performed in algorithms for the solution of the channel routing problem [2], the gate matrix layout problem [3], the functional cell generation problem [4] and transistor network design [5]. An example is shown for each of these problems in which transistor reordering is used to decrease layout area. Shown

in Fig. 2(a) (respectively, (b), (c)) is an example of a channel routing problem (respectively, gate matrix layout, functional cell layout) taken from [2] (respectively, [3], [4]) in which the layout area is decreased by 43 percent (respectively, 43 percent, 54 percent) due to transistor reordering. Shown in Fig. 2(c) are the functional cell layouts and their corresponding graph representations, where the edges of the graphs correspond to the transistors of the circuit. Shown in Fig. 2(d) are the graph representations of two MOS transistor networks taken from [5] in which the number of transistors has been decreased by 37.5 percent due to transistor reordering and the elimination of redundant devices. The white nodes in the graph of Fig. 2(d) denote the input and output terminals of the MOS transistor network. The improvement in layout area due to transistor reordering is significant for all these problems; however, the researchers have ignored the impact of transistor reordering on the timing behavior of the circuit. Statistics are given in [6] which show that of all series/parallel CMOS circuits which have stack height four or less, the layout area required by implementation in a functional cell layout style may be reduced by performing transistor reordering in 61 percent of these circuits. These examples indicate that the transistor order in a MOS logic gate has a significant effect on the layout area of the circuit; however, it is not known exactly how transistor order affects other circuit characteristics such as timing and power dissipation.

It is well known that transistor reordering, although will not change the logical behavior of a circuit, will certainly transform a circuit into a new one with different analog behavior, which in turn may have a profound effect on the timing behavior (or speed) of the circuit. However, this effect on timing behavior has only been briefly mentioned in the literature [1, 7] and has never been closely examined. Concern about the effect of such transistor reordering on timing behavior has been expressed by VLSI designers and researchers. It is clear that if the transistor reordering would dramatically change the speed of a circuit, then many reorderings which slow down a circuit should not be used. On the other hand, if the effect of reordering on the timing is very insignificant, then both CAD tool developers and VLSI circuit designers need to be informed so that the use of such operations to optimize circuit parameters other than speed (e.g., layout area) is justified. This motivates the research that is presented in this paper. It is shown in the sequel that the order in which signal transitions arrive at a MOS logic gate, and hence transistor order, has a varying effect on the performance of the circuit. Circumstances where the effect of transistor reordering on timing is insignificant are clearly identified.

In this paper the effect of transistor reordering on timing behavior is investigated through extensive SPICE simulations. The effects of transistor reordering on the propagation delay of a circuit are examined under different circumstances. The purpose of this investigation is to determine

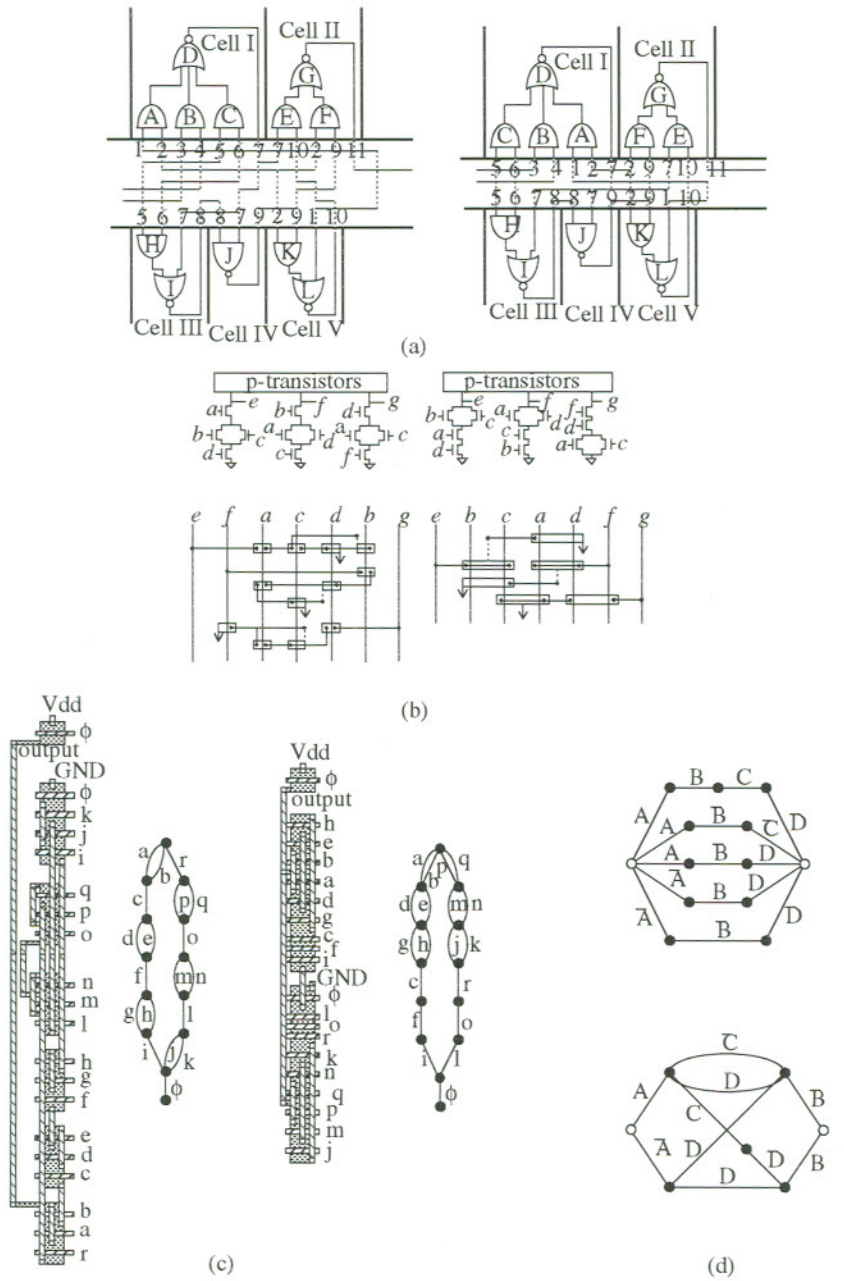


Fig. 2. Examples showing improvement in layout design due to transistor reordering.

if the transistor order significantly affects the timing behavior of CMOS complex gates. The effect of transistor reordering on the timing behavior of a Series Connected MOS Structure (SCMS) has been briefly mentioned in [7]; however, their conclusions concerning this topic are not sufficient to give the CAD tool designer a thorough understanding of the effect of transistor reordering on timing behavior. An SCMS is simply a set of MOSFET's connected in series. The major contribution of [7] is an analysis of the dependence of SCMS delay on stack height in submicrometer circuit design, and very little emphasis is placed on the effect of input signal arrival times on circuit delay.

The objective of this paper is to analyze the significance of transistor order with respect to the timing behavior of MOS digital circuits. It has been assumed in some cases (e.g., [8]) that the best way to position the transistors in a circuit is to place the transistor driven by the signal which arrives latest in time nearest to the output node of the circuit. However, it is shown in this paper that this is not always true, and furthermore, the variation in propagation delay with respect to transistor order is significant in some cases.

The effect of transistor reordering on a CMOS circuit can be determined by examining isolated complex gates, since reordering the transistors of a gate does not change the capacitive loading on preceding logic stages, and therefore, has the same effect on all the logic paths in which the gate is contained.

The analyses of the timing behavior of circuits in this paper are performed by simulation using SPICE [9] version 3 on a SUN SPARCstation 1. More than 20000 different circuits have been simulated and used to form the basis for this investigation. Presented in Section II are the objectives of this investigation, and a qualitative analysis of the behavior which shows the significance of this work. The simulations are described in detail in Section III. The results of the SPICE simulations are summarized and analyzed in Section IV. The dependence of transistor order on the sizes of transistors is analyzed in Section V, and a CAD tool which uses the knowledge obtained from this investigation to perform transistor reordering to optimize circuit delays is presented in Section VI. Finally, the paper is concluded in Section VII.

II Qualitative Analysis of Circuit Behavior

The general operation of an SCMS is to transfer charge between two nodal capacitances, one on each end of the SCMS. In the case of a CMOS NAND gate one of the nodal capacitances has value zero, since one end of the SCMS is connected to ground. The rate of transferral of charge from one capacitor to the other, or in other words the current flow through the SCMS, is dictated at a particular instant of time by the transistor which has the least capacity of all transistors in

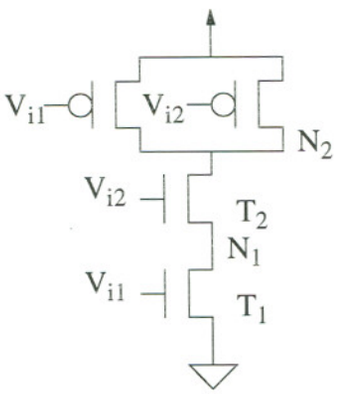


Fig. 3. (a) A 2-input CMOS NAND gate, and (b) its equivalent circuit using a basic RC-model for the MOS transistors.

the SCMS to carry current at that particular instant of time. The capacity of a transistor to carry current is indicated by the I-V characteristics of the device. the current flow through an SCMS when charge is being transferred from one capacitance to another is dependent on the internal node voltages of the circuit.

Let us take a closer look at the transient behavior of an SCMS. Consider the CMOS NAND gate shown in Fig. 3. The pull down network of this circuit is an SCMS. Assume both inputs are initially at a low voltage level, and when it is said that they arrive it is meant that they switch from low to high. Suppose the signals V_{i_1} and V_{i_2} arrive separately in time (i.e., they do not arrive simultaneously). Note that this is the situation where the worst case delay may occur. Let us consider the following two cases: signal V_{i_1} arrives prior to signal V_{i_2}, and signal V_{i_2} arrives prior to signal V_{i_1}. That is, case 1 corresponds to the situation where transistor T_1 switches first, and case 2 corresponds to the situation where transistor T_2 switches first. The propagation delay through a gate is measured relative to the latest arriving input (i.e., the input transition which causes the output to change state). It is clear that if T_1 switches prior to T_2 the charge on node N_1 is depleted prior to the requisition of signal V_{i_2} to discharge the output (i.e., node N_2). Hence the potential of node N_1 is zero prior to the time from which the propagation delay is measured (assuming the

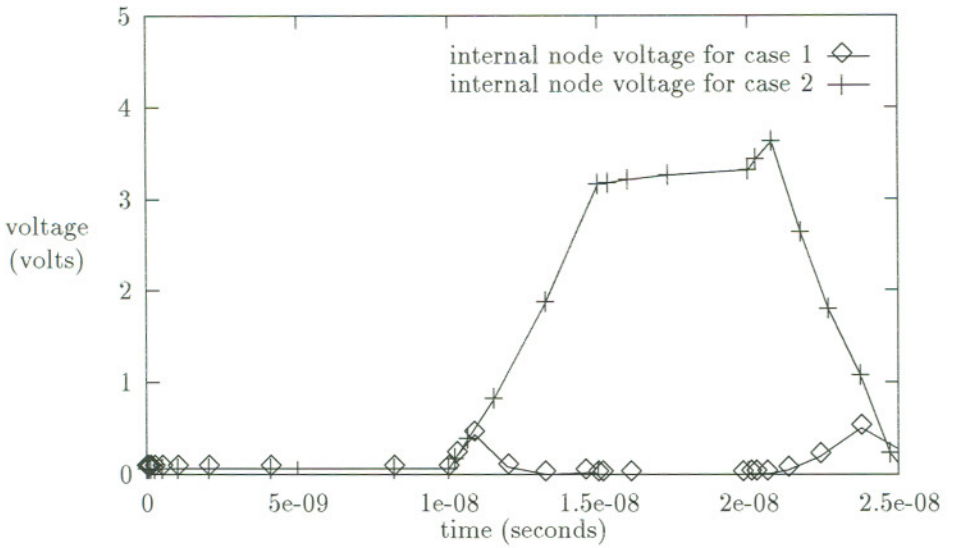


Fig. 4. Internal node voltages of a 2-input NAND gate.

time between signal transitions is sufficient to allow N_1 to reach steady state). Consider case 2 where signal V_{i_2} arrives prior to signal V_{i_1}. When signal V_{i_2} switches from low to high charge is shared between nodes N_2 and N_1, and node N_1 is charged to a voltage of $V_{gs} - V_t$, where V_{gs} and V_t are the gate to source and threshold voltages of the device, respectively. Hence, it is required that more internal charge be depleted from the circuit to switch the output from high to low for case 2. Intuitively it appears that the gate switches faster if the input arrival pattern is similar to case 1 as opposed to case 2; however, this is not true under all circumstances. The internal node voltage (V_{ds_1}) is shown in Fig. 4 for each case. For case 1 node N_1 is initially discharged and V_{ds_1} remains very small during switching. For case 2 node N_1 is charged to $V_{DD} - V_t$ when v_{i_2} arrives, and decreases monotonically after a slight initial increase when V_{i_1} arrives. In each case T_1 is initially in saturation, and therefore is dictating the current flow from the output to ground. It is difficult to see from this analysis which case will result in a greater average current flow, and hence, a faster switching output.

Consider the 4-input NAND gates shown in Figs. 5(a) and (b). If the rise time of the critical input signal is 5 ns, then the ratio of the delay of the circuit in Fig. 5(a) to the delay of the circuit in Fig. 5(b) is 1.23; however, if the rise time of the critical input signal is 2 ns, then this ratio is .99. This indicates that the transistor order is significant, and, as is indicated by the case where the input signal has a 5 ns transition time, the circuit does not behave as one's intuition would lead oneself to believe.

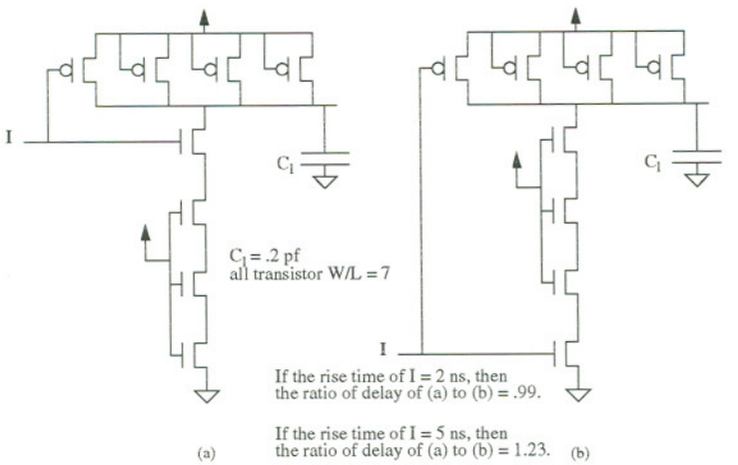


Fig. 5. (a) A top-critical and (b) a bottom-critical CMOS NAND gate.

III Description of Simulations

In order to minimize the number of simulations required for this investigation it is assumed that no two input signals of a CMOS complex gate have a state transition at the same instant of time. The *critical* input of an SCMS is the input signal which creates a conducting path through the SCMS when it changes state (i.e., it is the input signal of the transistor which switches "on" last). With this assumption there is the equivalent of only one conducting path between the output and power terminals of the CMOS complex gate. A particular CMOS complex gate may have multiple conducting paths between the output and power terminals; however, all paths contain the critical transistor (i.e., the transistor which causes the change in state of the output of the gate). Therefore, the multiple paths between the output terminal and the critical transistor may be represented by an equivalent circuit. The multiple paths between the critical transistor and the power terminal may be treated similarly. For example if two transistors are connected in parallel and conducting, the net effect is a single conducting transistor with width approximately equal to the sum of the widths of the two transistors. For example, consider the circuit shown in Fig. 6(a). Suppose the transistor driven by signal E in Fig. 6(a) is the critical transistor and all other transistors in the pull-down network are conducting. Assuming no other signal switches simultaneously with E, the

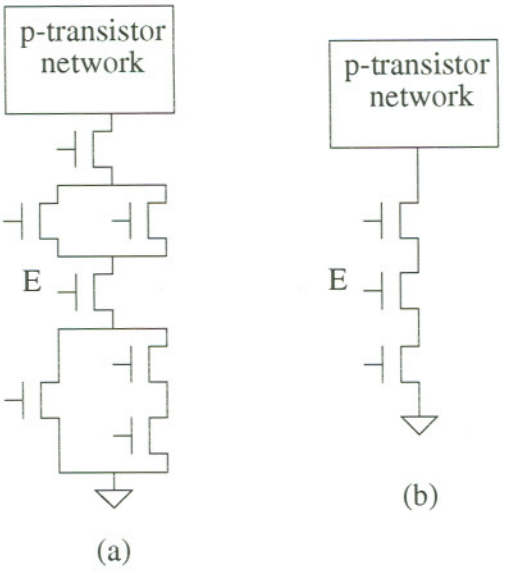


Fig. 6. (a) A CMOS complex gate and (b) its equivalent SCMS with unspecified device sizes.

circuit of Fig. 6(a) may be represented by an equivalent circuit as shown in Fig. 6(b). Hence, the behavior of the circuit may be properly analyzed by considering an SCMS. Since all the devices in the SCMS do not have the same dimensions, the effect of sizing on the timing behavior of an SCMS must be analyzed. The results of this analysis are presented in Section V. Since the analysis is performed on SCMS's over a range of transistor sizes, the investigation provides an understanding of the behavior of general series/parallel circuits. That is, the results presented here apply to series/parallel circuits whose unspecified device sizes in its equivalent SCMS are within the range of device sizes used in the simulations.

The CMOS NAND gate is used in each of the circuit simulations performed in this investigation. The use of the CMOS NOR gate in the simulations leads to similar results. The objective is to determine the difference between the propagation delays of a NAND gate for the two cases where the critical transistor is connected to the output (*top-critical*) and to the ground terminal (*bottom-critical*). These two cases represent the two extremes in the order in which transistors may be placed in the circuit. The ratio of the propagation delay of a top-critical circuit to that of a bottom-critical circuit is computed for all combinations of 20 different input signal rise times in the range of .1 ns to 10 ns and 20 different load capacitances in the range of .1 pf to 10 pf. These

simulations are performed on 2, 3, 4, 5 and 6-input NAND gates. In addition, the simulations are performed over a range of load capacitances between 10 pf and 100 pf in order to verify that the transistor order is insignificant for large loads, independent of rise time and stack height (i.e., the number of transistors between the output and ground terminals). Simulations are performed over much wider ranges of input signal rise times and load capacitances in order to determine the region in the rise time versus load capacitance plane in which the ratio of the delay of a top-critical to a bottom-critical circuit is close to one. Simulations performed to determine the effect of sizing on the behavior of an SCMS include the simulation of a 4-input NAND gate for all possible combinations of 10 transistor sizes in the range of 1 μm to 200 μm.

The transistor model used in the SPICE simulations is MOS level 2, and the transistor characteristic parameters are from the MOSIS[2] 2-μm p-well fabrication process. The options which control the convergence of the transient analysis performed by SPICE are adjusted to give greater numerical accuracy in the SPICE output.

IV Analysis of Simulation Results

The simulation results obtained during the investigation are analyzed in this section to provide an understanding of the behavior of the SCMS as a function of critical input signal rise time, load capacitance and stack height.

A subset of the simulation results is shown in Fig. 7. Plotted on the logarithmic x-axis in the graphs of Fig. 7 are either the load capacitance or input signal rise time, and plotted on the y-axis is the ratio of the propagation delay of a top-critical circuit to that of a bottom-critical circuit (*delay ratio*). If the delay ratio is less than one, then the circuit is faster when the transistor order is such that the circuit is top-critical, and if the delay ratio is greater than one, then the transistor order for which the circuit is bottom-critical is faster. The propagation delay is measured from the time at which the critical input signal is half way between its low and high voltages to the time at which the output signal is half way between its low and high voltages. Plotted in the third dimension (z-axis) in the graphs of Fig. 7 are either stack height, load capacitance or rise time. The dependence of the delay ratio is being studied as a function of three variables; therefore, for a given graph the value of one of the variables is constant. The circuits used in the simulations which produced the results summarized in Fig. 7 are composed of transistors of minimum size.

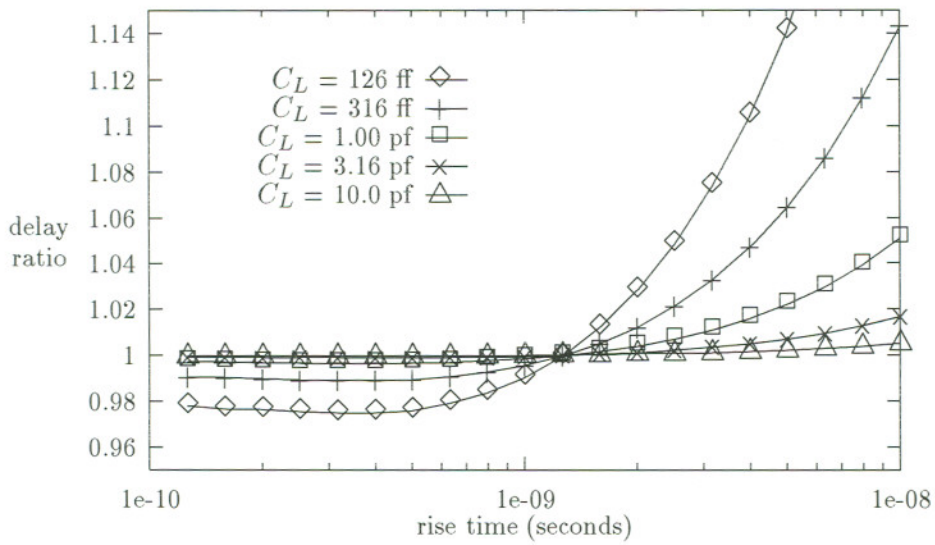
Consider the graphs shown in Figs. 7(a) and (b). Plotted in the graph of Fig. 7(a) is the delay ratio versus rise time for various load capacitances with a fixed stack height of three, and the

[2]MOSIS is the Metal-Oxide Semiconductor Implementation Service located at USC.

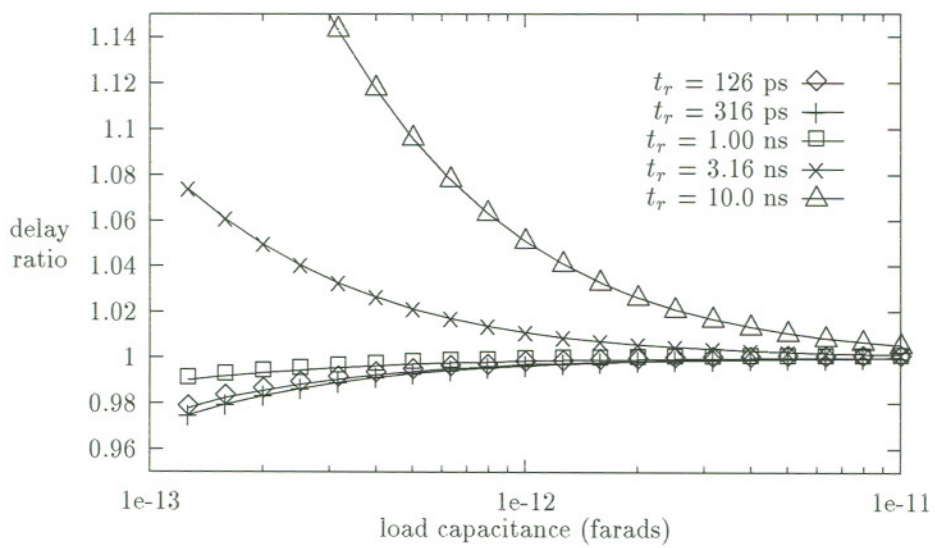
graph of Fig. 7(b) is the same as the graph of Fig. 7(a) with the x-axis and z-axis interchanged. It can be seen from Figs. 7(a) and (b) that for circuits with a small stack height (e.g., ≤ 4), the delay ratio is within 5 percent of one independent of the size of the load (for reasonable values of load capacitance) when the rise time of the critical input is small (e.g., ≤ 1 ns). Also, for circuits with a stack height less than or equal to 6, the delay ratio is within 5 percent of one for rise times between 1 ns and 10 ns, and load capacitances greater than or equal to 1 pf. For rise times in the range of 1 ns to 10 ns and load capacitances less than 1 pf, the delay ratio is much bigger than 1 (e.g., 10 to 30 percent), which indicates that the transistor order is significant and a bottom-critical reordering of the circuit has less delay.

The timing behavior of circuits having stack heights greater than four and rise times larger than 3 ns (see Figs. 7(c) and (d)) is similar to circuits with small stack heights. Circuits for which the rise time of the critical input is less than 3 ns, the stack height is larger than 4 and the load capacitance is small (e.g., $< .2$ pf) switch faster when the transistor order is such that the circuit is top-critical; however, if the load capacitance is large, then the transistor order is insignificant.

In general, for circuits with a load capacitance larger than .3 pf and rise time of the critical input signal less than 5 ns the delay ratio is within 5 percent of one independent of stack height (see Figs. 7(e) and (f)), and it is within 2 percent of one for load capacitances larger than 1 pf (see Fig. 7(g)). As can be seen from the graph shown in Fig. 7(h), independent of the rise time of the critical input signal and the stack height, the transistor order becomes less significant as the load capacitance increases.

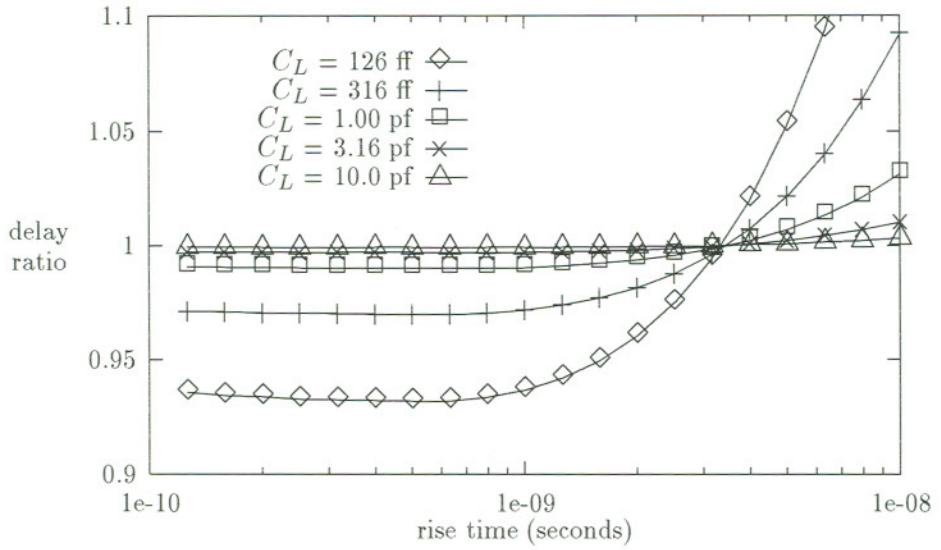


(a) stack height = 3

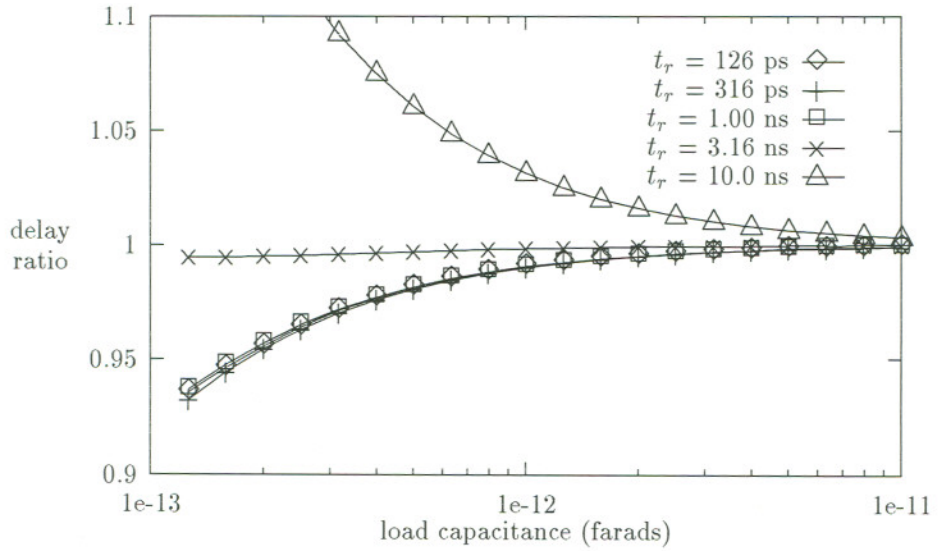


(b) stack height = 3

Fig. 7. Subset of simulation results for 2, 3, 4, 5 and 6-input NAND gates containing transistors of minimum size.

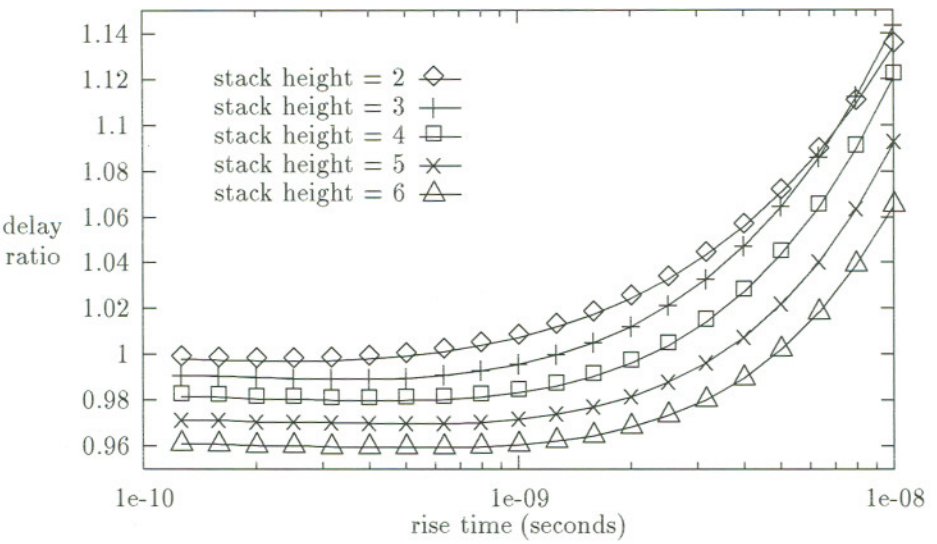


(c) stack height = 5

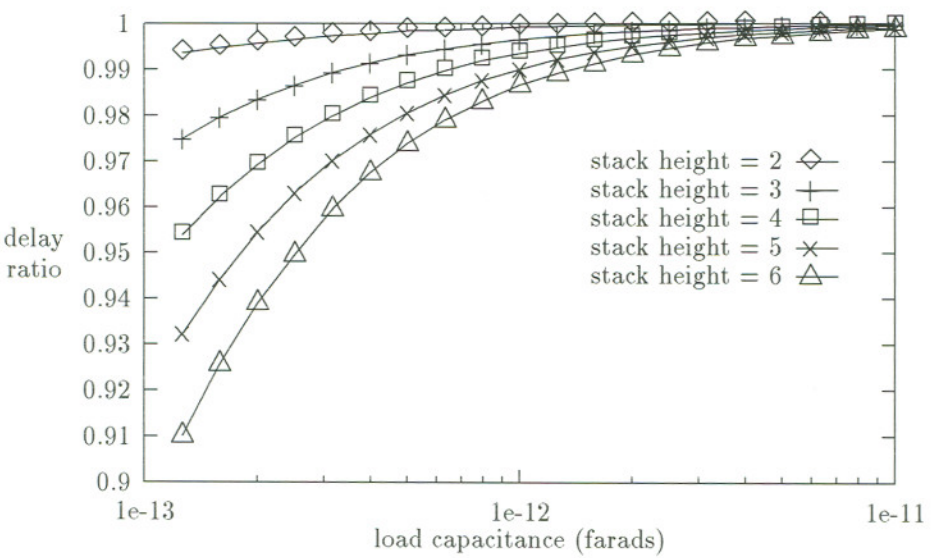


(d) stack height = 5

Fig. 7 (Continued)

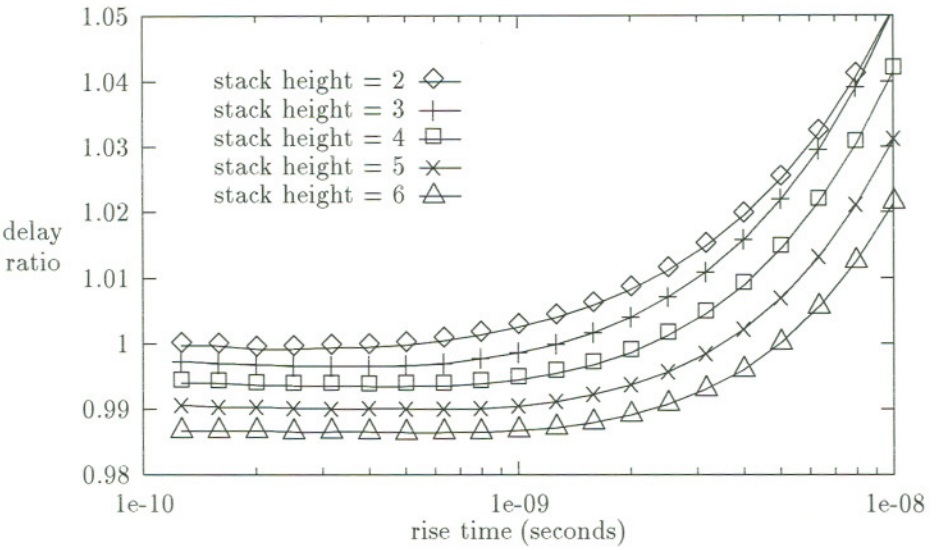


(e) C_L = 316 ff

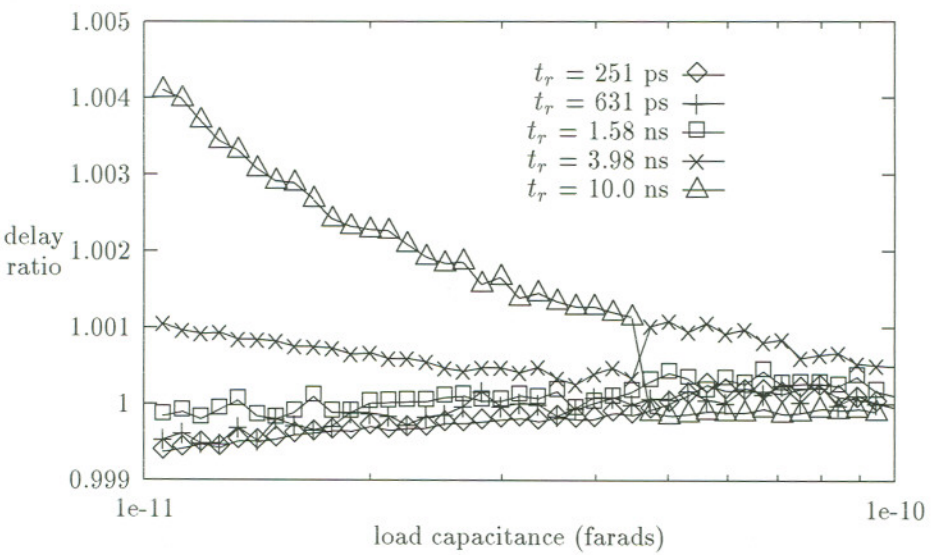


(f) t_r = 3.16 ns

Fig. 7 (Continued)



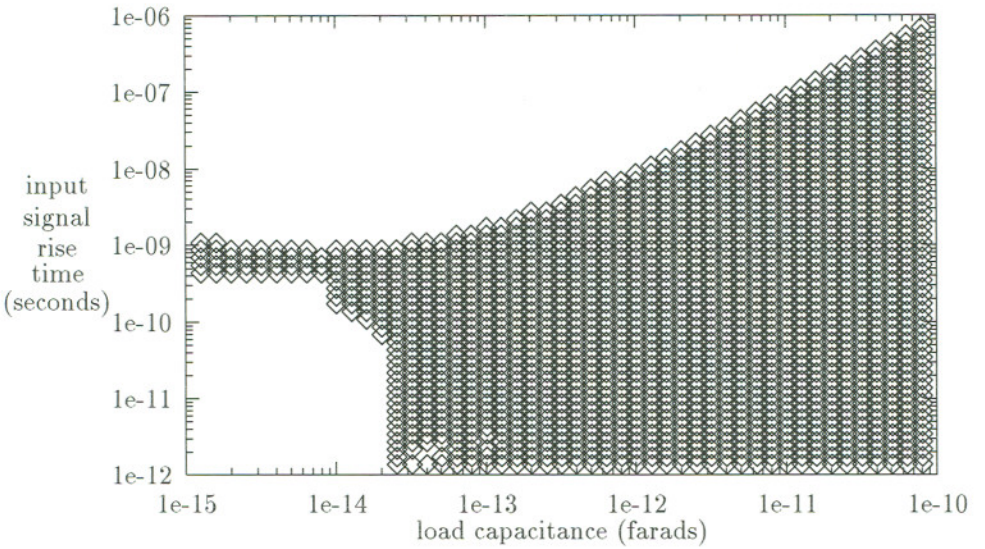
(g) C_L = 1.00 pf



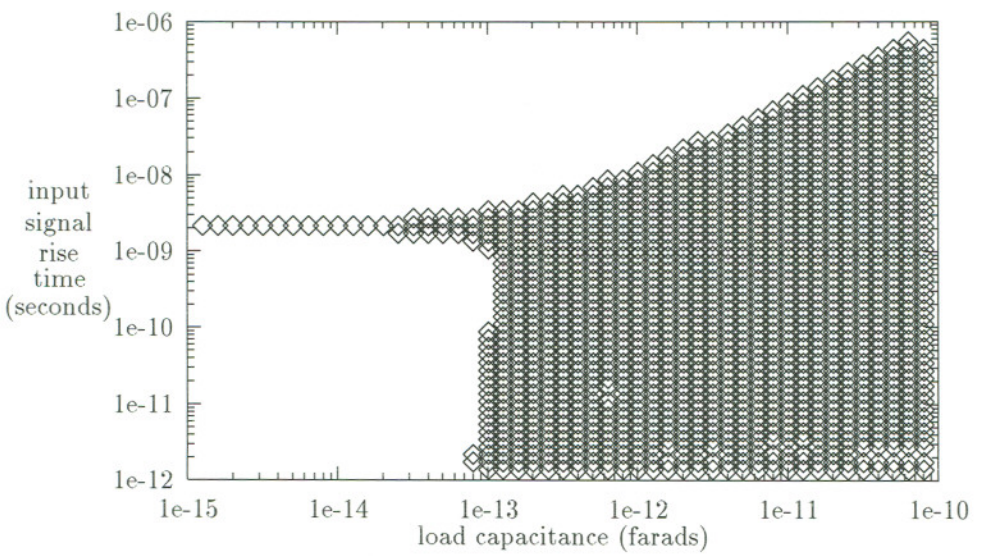
(h) stack height = 4

Fig. 7 (Continued)

The delay ratios are plotted in the plane defined by the rise time of the critical input and the load capacitance for stack heights of 2 and 4 in Figs. 8(a) and (b), respectively. The shaded regions in Fig. 8 represent circuits for which the delay ratio is within 5 percent of one. In the majority of CMOS designs the rise time of the critical input and the load capacitance for most gates are such that the circuits are within the shaded region (i.e., the effect of transistor reordering on propagation delay is less than 5 percent). Hence, for CMOS circuits which have a single conducting path between power rail and output, typical input signal transition times and load capacitances and are implemented using transistors of minimum size, the effect of transistor order on the propagation delay is insignificant. Therefore, transistor reordering may be performed on these circuits in an attempt to improve layout characteristics other than timing with little regard to the effect of reordering on the delay of the circuit.



(a) stack height = 2



(b) stack height = 4

Fig. 8. Region of the rise time versus load capacitance plane where the delay ratio is within 5 percent of one.

A graph similar to those shown in Figs. 8(a) and (b) is shown in [7]. The results obtained in our analysis differ from those in [7]. The method used to obtain the data in [7] is different from the data in this paper, and therefore it is not appropriate to compare the results. Since the data in this paper has been obtained using SPICE, it can be concluded that it is an accurate prediction of circuit behavior.

We conjecture that the results presented in this section are largely independent of the fabrication process, since they are presented as a ratio of two propagation delays. That is, a different process for which the circuits are inherently faster or slower would give similar results, since the same factors of improvement or degradation would apply to each propagation delay in the ratio.

V Effect of Transistor Size

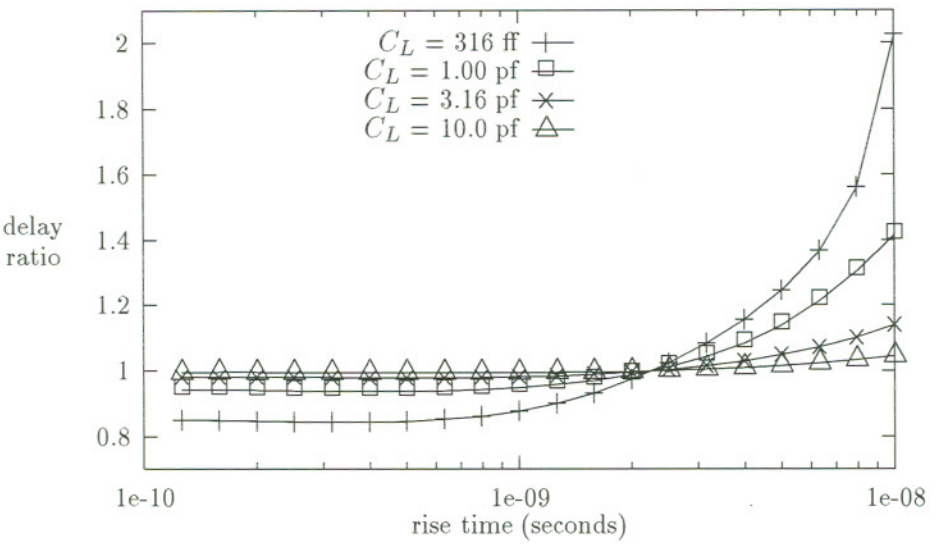
It is necessary to understand the effect of transistor sizing on the significance of transistor order in an SCMS since many circuits may contain multiple conducting paths between the output and power rail (which is similar to containing transistors of various sizes), and transistor sizing is often used to improve circuit performance [10]. Let us first examine the situation where all the transistors of an SCMS are sized uniformly.

The results of SPICE simulations of a 4-input NAND gate containing transistors with strengths ten times those of a minimum size transistor are shown in Fig. 9. The identical simulations performed on a 4-input NAND gate containing minimum size transistors are shown in Fig. 10. A qualitative comparison of Figs. 9(a) and (b) with Figs. 10(a) and (b), respectively, show that the behavior of the circuit containing wider transistors is similar to the behavior of the circuit containing the minimum size devices. Upon closer examination one notices that the results of the simulations of the stronger circuit (i.e., the circuit containing larger transistors) resemble the results of simulations of a minimum size circuit with a smaller load capacitance. The propagation delay of the gate is a function of the rate of change of charge being shared between the load capacitance and parasitic source/drain capacitances. Circuits which contain transistors of larger width have greater capacity to carry current, and therefore, the effective load capacitance is smaller for these circuits (i.e., the load "appears" smaller, since the rate of change of charge is greater). In order to verify this observation, the circuit containing the wide transistors is simulated over a range of larger load capacitances. The results of this simulation are shown in Fig. 11, and they closely resemble the results shown in Fig. 10. Analysis of the simulation results with respect to input signal transition time and stack height of an SCMS which contains uniform size devices having strengths greater

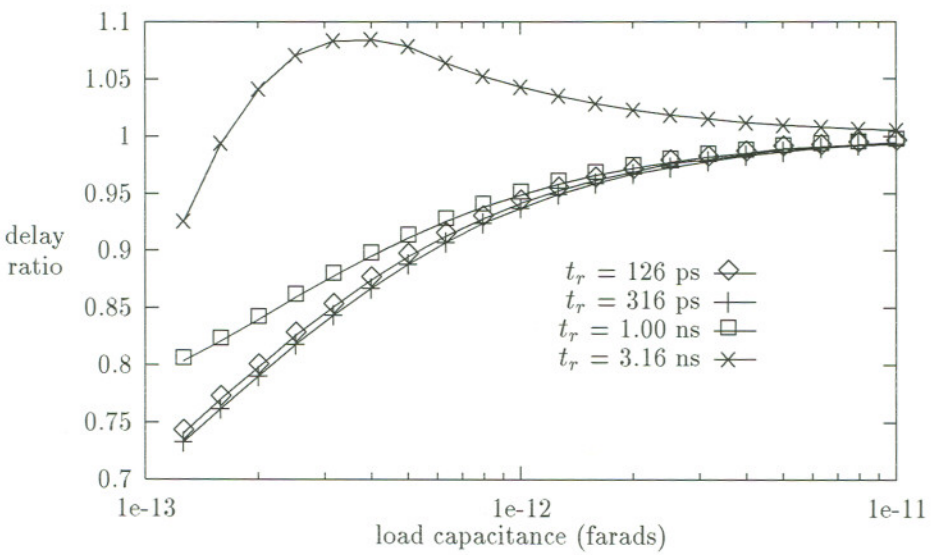
than minimum size yields similar conclusions to those of an SCMS containing devices of minimum size. Hence, the behavior of an SCMS containing transistors of uniform size is equivalent to the behavior of an SCMS containing transistors of minimum size for an appropriate load capacitance (i.e., the qualitative behavior is similar).

Consider the two 4-input NAND gates shown in Figs. 12(a) and (b). Shown in Fig. 13 (respectively, 14, 15) are the propagation delays of the circuits shown in Figs. 12(a) and (b) versus the size of transistor x (respectively, y, z) with all other devices having minimum size. The propagation delay is normalized with respect to the delay of a fanout 4 inverter designed with minimum size transistors. The delay of the fanout 4 inverter is 1.57 ns. A comparison of the propagation delays in each of these figures indicates that the transistor order is significant for SCMS's which are constructed with transistors of different sizes, and therefore, transistor order is significant in CMOS complex gates which have multiple conducting paths between the output and power rail. The delay ratios (top-critical to bottom-critical) are plotted in Fig. 16 for the data shown in Figs. 13, 14 and 15. These simulations are performed using a 1 pf load and 2 ns critical input signal rise time. One might be tempted to say, based on the data shown in Fig. 16, that a top-critical circuit performs better than a bottom-critical circuit; however, this data is for a specific load capacitance and input signal rise time, and the delay ratio varies significantly with respect to these parameters.

The data shown in Figs. 13, 14 and 15 indicates that the delay of a MOS logic gate as a function of transistor size is not necessarily monotonic, and its derivative (i.e., its slope at any given point on the curve) is a function of the position of the critical transistor. Many existing transistor sizing algorithms assume that the delay of an individual gate is a monotonically decreasing function of transistor size (i.e, the delay continuously decreases as transistor size increases), so the delay of a given logic path is a parabolic function (i.e., has only one minimum) of transistor size [10]. Since this function has only one minimum, it must be the global minimum. The results shown in Figs. 13, 14 and 15 show that it is possible to increase the delay of a gate by increasing the size of transistors in the gate; therefore, the problem of determining the minimum propagation delay through a logic path has a solution space with a contour having multiple minima (i.e., there are multiple solutions for which its derivative is zero). Therefore, it may not be the case that the first minimum found is the global minimum. This indicates that the problem of determining optimal transistor sizes in MOS digital circuits needs to be reinvestigated.

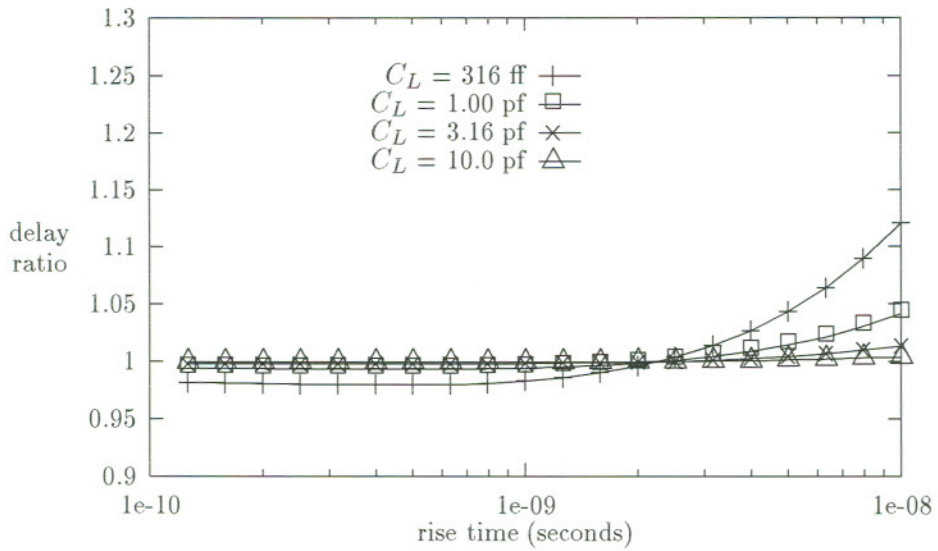


(a) stack height = 4

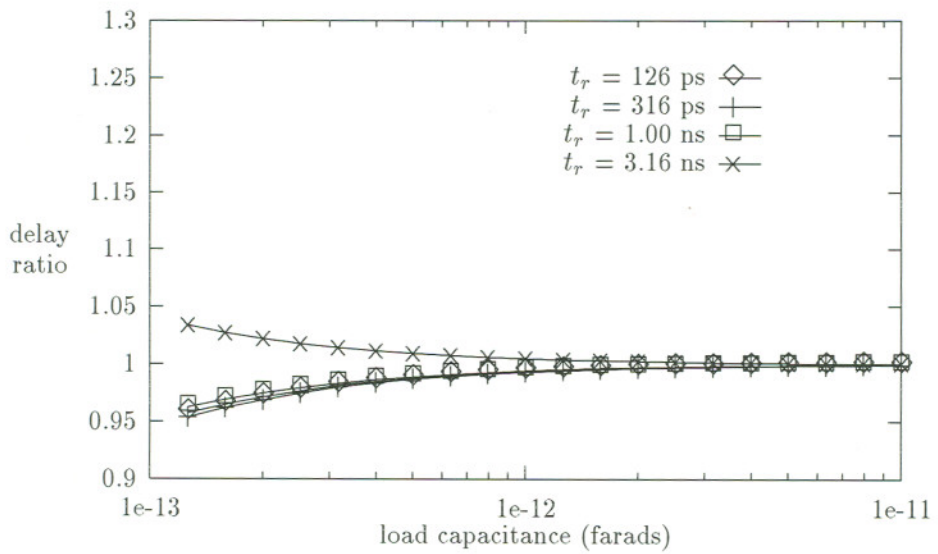


(b) stack height = 4

Fig. 9. Simulation results of circuits containing transistors which have ten times the strength of minimum size devices.

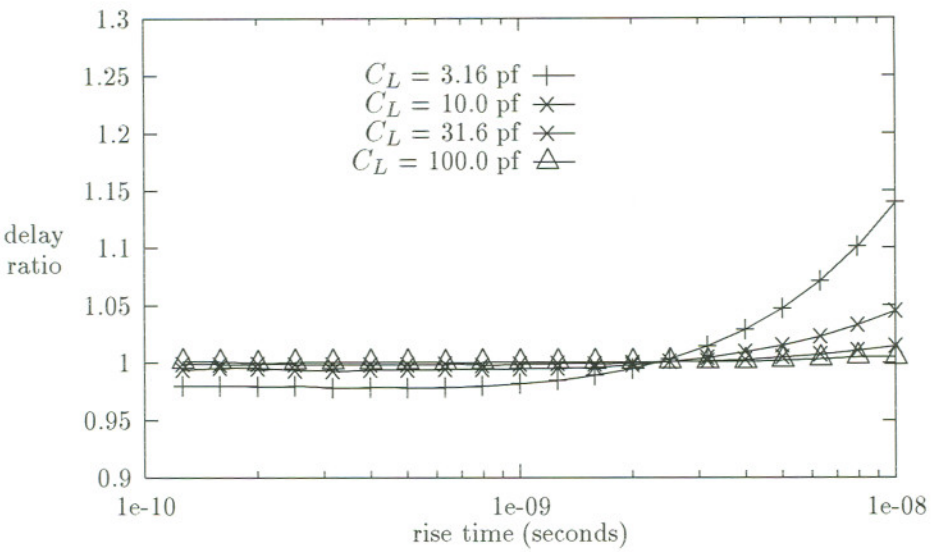


(a) stack height = 4

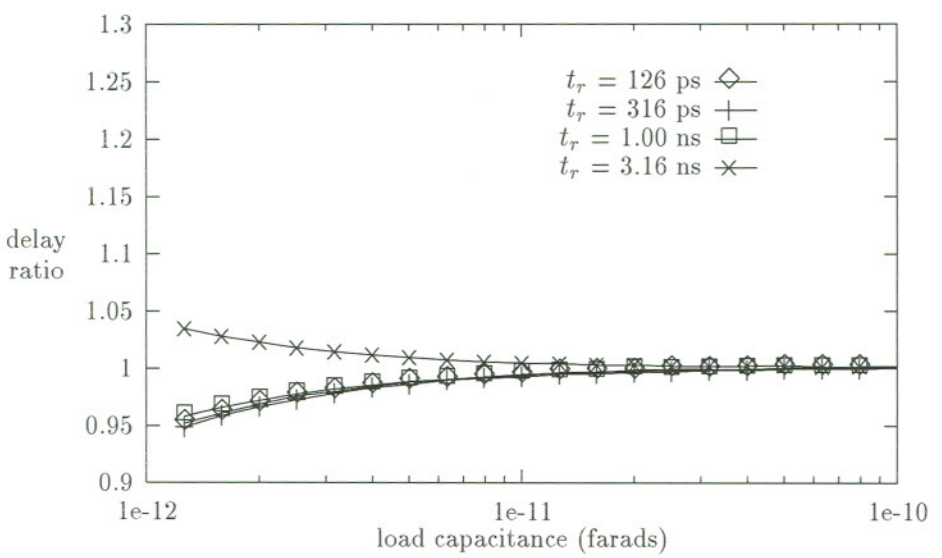


(b) stack height = 4

Fig. 10. Simulation results of circuits containing transistors of minimum size.



(a) stack height = 4



(b) stack height = 4

Fig. 11. Simulation results of circuits containing transistors which have ten times the strength of minimum size devices.

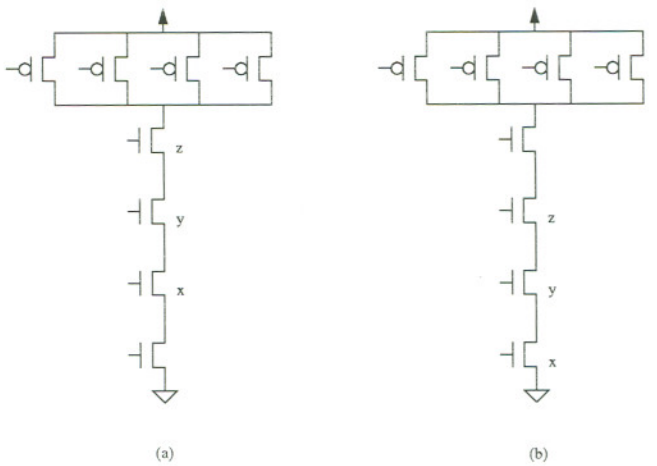


Fig. 12. NAND gates used to determine effect of sizing on transistor order.

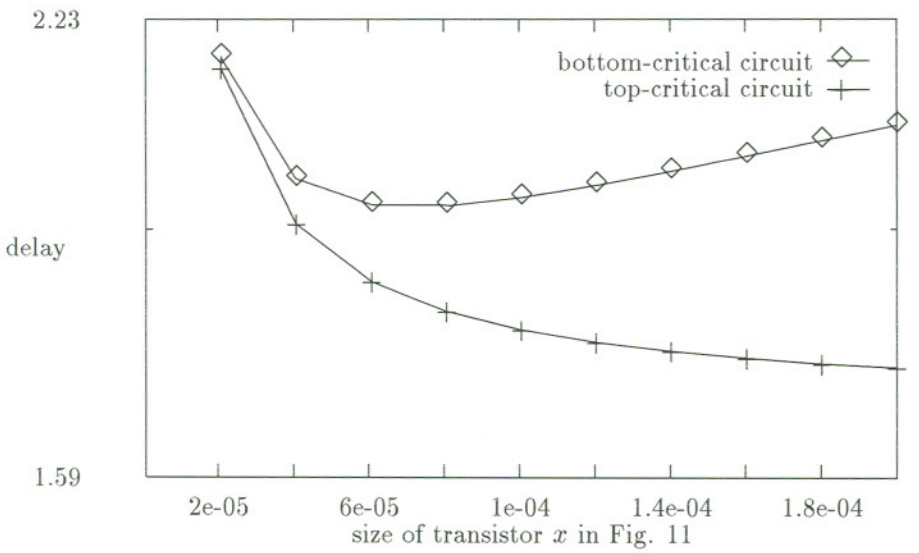


Fig. 13. Propagation delays for the circuits of Fig. 12 for various sizes of transistor x.

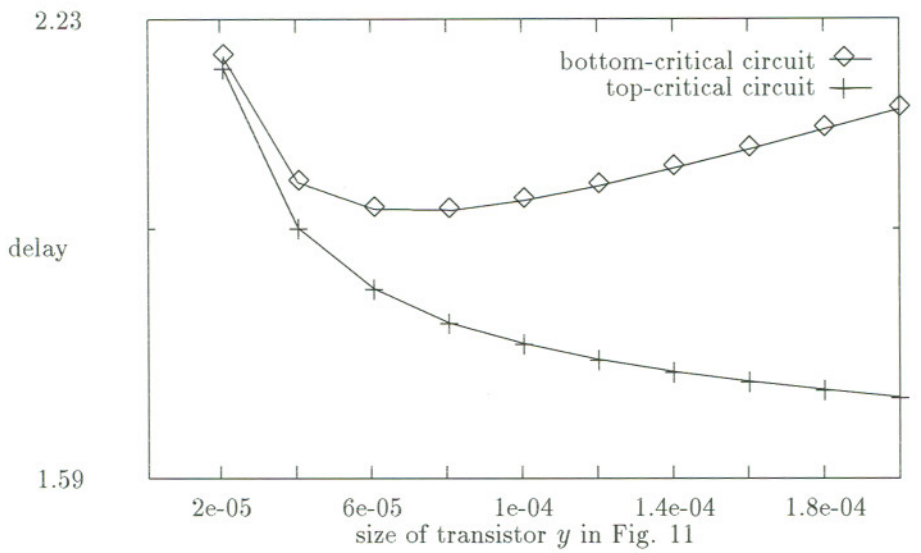


Fig. 14. Propagation delays for the circuits of Fig. 12 for various sizes of transistor y.

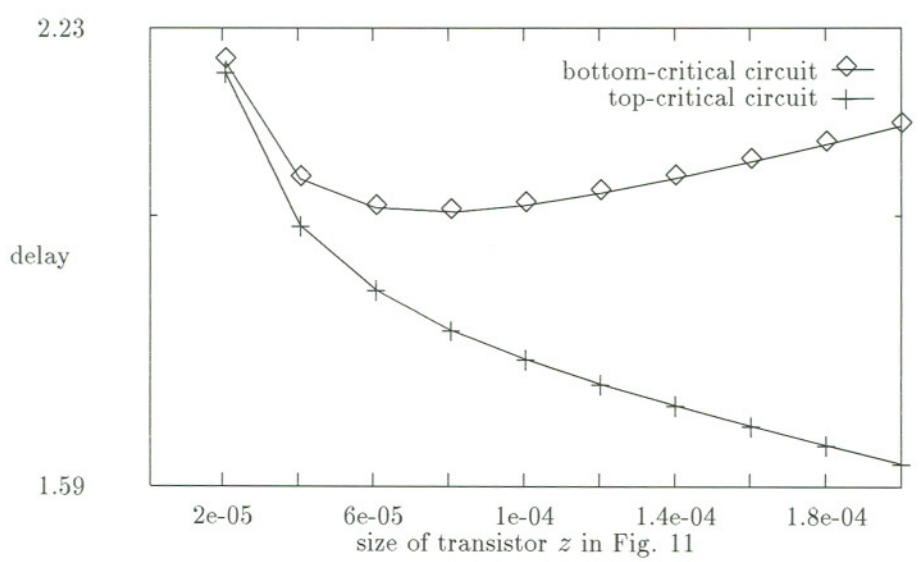


Fig. 15. Propagation delays for the circuits of Fig. 12 for various sizes of transistor z.

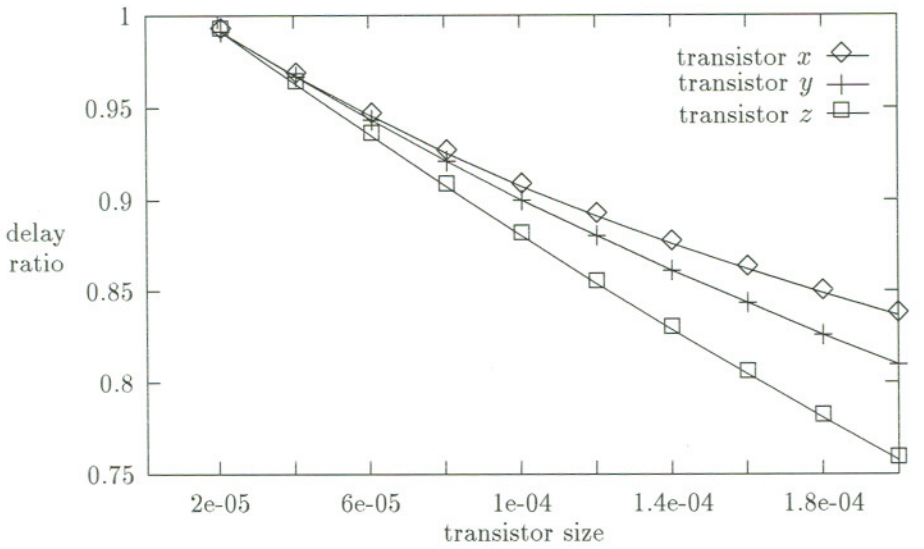


Fig. 16. Delay ratios for the circuits shown in Fig. 12 for various transistor sizes.

VI Characterizing Critical Input Position

An algorithm is presented in [11] which performs transistor reordering to improve the performance of CMOS circuits. The algorithm uses a model to determine the best transistor order which is based on the data collected in this investigation. A least square fit technique is used to fit the data from this investigation to a general form which is selected by the authors of [11]. The accuracy of the model in [11] is largely dependent on the general form, since a very large number of data points are available. The function used to model transistor order is dependent on load capacitance, critical input signal transition time, critical transistor size and non-critical transistor size. The algorithm in [11] performs a breadth first search on a combinational logic network from primary inputs and register outputs to primary outputs and register inputs. It computes the value of the delay ratio for each gate, and reorders the transistors accordingly. After the transistors of a gate have been reordered the gate is simulated to determine its propagation delay.

The results of the performance optimization algorithm in [11] are encouraging. The delay of the critical path of an 8-bit barrel shifter has been reduced by 22 percent, and greater delay reduction is expected for some other circuits [11].

VII Conclusions

Based on the previous investigation the following results may be stated concerning the effect of transistor order on the timing performance of MOS digital circuits:

- The delay ratio decreases as the stack height increases (see Figs. 7(e) and (g)).
- The delay ratio approaches one as the load capacitance increases (see Figs. 7(d) and (h)).
- The delay ratio increases as the input signal transition time increases (see Fig. 7(a)).
- The delay ratio decreases as transistor size increases (see Fig. 16).
- If a circuit is constructed of transistors of minimum size and there are few conducting paths between the output and power rail, then the transistor order has less than 5 percent effect on the propagation delay of the circuit if the load capacitance is greater than .1 pf and the input signal transition time is less than 3 ns.[3]
- For circuits constructed with transistors of greater than minimum size, say x times larger than minimum size, and the transistors are sized uniformly, the transistor order has less than 5 percent effect on the propagation delay of the circuit if the load capacitance is greater than x times .1 pf and the input signal transition time is less than 3 ns.[3]
- The significance of transistor order is independent of input signal transition time for very large load capacitances.
- For circuits containing minimum size devices and having small load capacitances, a bottom-critical reordering has less propagation delay.
- For logic gates containing nonuniformly sized devices, a top-critical reordering has less propagation delay.
- The optimal sizing of transistors in a MOS logic gate is a function of the position of the critical transistor.

Although in the current state of VLSI circuit technology timing performance is the greatest concern of a circuit designer in most applications, there remains a desire to design circuits which require as little area as possible, and therefore, transistor reordering to reduce layout area is an important area of research.

[3]These values may vary for different fabrication processes; however, the behavior pattern is similar.

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