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BOUNDS FOR A PETRI NET MODEL OF A COMPLEX MULTIPROCESSOR

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Abstract

In this paper we establish upper and lower bounds for a Petri network model of a multiprocessor with multiple memories. Most of the principles in this paper are based on those of our prior paper [4].

I Introduction

Petri network models have been used successfully to model multiprocessor systems [1]. Such models may or may not have product form solution [3]. In this correspondence, models which can generate upper and lower bounds for important performance measures of a canonical and practical dual processor model are presented.

The system of interest is shown in figure 1. It contains two common memories, M_1 and M_2, and two processors, P_1 and P_2. A stochastic Petri Net model is illustrated in figure 2. The model consists of four sequences of events called tasks. The underlying statistical assumptions are Markovian. When internally ACTIVE, (that is, externally idle,) P_1 (P_2) can request the use of M_1 (M_2) with the rate of q^{30} (q^{40}) and the use of M_2 (M_1) with the rate of q^{10} (q^{20}). Once a task sequence is in either the GLOBAL BUS REQUEST place or the LOCAL BUS(MB_1) REQUEST place, it can access the bus at rate q^{11}, q^{12}, q^{21}, q^{22}, q^{31} and q^{41}, as shown in figure 2, if the bus is free. That is, contention arises as only one processor may access the bus at one time. We assume that P_1 needs an average of $1/q^{32}$ memory access time for M_1 and $1/q^{13}$ for M_2, and that P_2 needs an average of $1/q^{42}$ memory access time for M_2 and $1/q^{23}$ for M_2. We also assume that all the transition rates are exponentially distributed.

The state transition diagram of this model is shown in figure 3. This model has no product form solution since the transitions do not all belong to integral building blocks [2]. The equilibrium state probabilities of this model can be obtained by solving the linear global balance equations. In practice, it may not be necessary to obtain equilibrium state probabilities. A quick estimation of the range of some specified performance measures may be enough. In this paper, we will use a bounding methodology, which has been described by [4], for the model in figure 1.

The organization of this paper is as follows. In section II, we will develop the upper bound and the lower bound for memory utilization. In section III, we will do the same for the blocking probability.

II Memory Utilization

Memory utilization, U, is the fraction of time that any one of the memories is being accessed by either of the processors. It corresponds to the states (–2,–2), (–2,–1), (–2,0), (–2,1), (–2,2), (–1,3), (0,3), (1,3) (3,1), (3,0), (3,–1), (2,–2), (1,–2), (0,–2) and (–1,–2) in figure 3.

1. Lower Bound Model

We modify the model in figure 2 as follows. Whenever a processor wishes to move from being ACTIVE to a BUS REQUEST, it may only do so if the corresponding memory is free. If the memory is busy at that time, then the request is lost. Since some of the requests are lost, there are fewer requests per unit time in this model. Therefore, this model can provide a lower bound for the memory utilization for the model in figure 2. The transition diagram of the modified model is like that of figure 3 except that the transitions from state (0,2) to state (1,2), from state (0,3) to state (1,3), from state (0,3) to state (–1,3), from

state (2,0) to state (2,1), from state (3,0) to state (3,1), from state (3,0) to state (3,–1), from state (–2,0) to state (–2,1), from state (–2,1) to state (–2,2), from state (0,–2) to state (1,–2) and from state (1,–2) to state (2,–2) are taken out. The resultant model is a product form model as the state transition diagram consists of integral building blocks. The equilibrium state probabilities are given by:

$$P_l(i,j) = \frac{q^{10}}{q^{1i}} \frac{q^{20}}{q^{2j}} P_l(0,0)$$

$$P_l(-i,j) = \frac{q^{30}}{q^{3i}} \frac{q^{20}}{q^{2j}} P_l(0,0)$$

$$P_l(-i,-j) = \frac{q^{30}}{q^{3i}} \frac{q^{40}}{q^{4j}} P_l(0,0)$$

$$P_l(i,-j) = \frac{q^{10}}{q^{1i}} \frac{q^{40}}{q^{4j}} P_l(0,0)$$

The lower bound of the memory utilization, U_l, is correspond to the same states.

2. Upper Bound Model

For the upper bound model, we assume that there is always a request from each processor, that is, $q^{10} = \infty$, $q^{11} = \infty$, $q^{20} = \infty$, $q^{21} = \infty$, $q^{30} = \infty$ and $q^{40} = \infty$. This model is shown in figure 4. Naturally, there are more requests per unit time in this model. Therefore, this model can provide an upper bound for the memory utilization for the model in figure 2. The transition diagram of this upper bound model is shown in figure 5. The upper bound model is also a product form model as the state transition diagram consists of integral building blocks. The equilibrium state probabilities are the same as the lower bound's except that the initial transition rates, i.e., q^{10} is replaced by q^{12}, q^{20} is replaced by q^{22}, q^{30} is replaced by q^{31} and q^{40} is replaced by q^{41}. The upper bound of the memory utilization, U_u, is corresponds to the states (–2,–2), (–2,–1), (–2,0), (–1,–2), (0,–2), (–1,1), (0,1), (1,1), (1,0) and (1,–1).

III Blocking Probability

Blocking probability, P_b, is the fraction of times that the bus requests are blocked. For the model in figure 2, it is corresponds to states (–2,0), (–2,1), (–2,2), (–1,3), (0,3), (0,2), (1,2), (1,3), (2,0), (2,1), (3,0), (3,1), (3,–1), (0,–2), (1,–2) and (2,–2). Its lower bound model can be adapted from the the lower bound model of the memory utilization. Since some of the requests are lost, this model has less requests for using the memories and hence the probability of being blocked will be smaller. The lower bound for the blocking probability, P_{bl}, corresponds to the same states.

We note that it appears to be difficult to generate an upper bound model for blocking probability. We have been unsuccessful in our attempts to do this.

IV Conclusion

We have introduced bounding methodology to a complicated stochastic Petri Net model of a multiprocessor systems. We feel that this method is convenience

in the study of non-product form systems.

Acknowledgements

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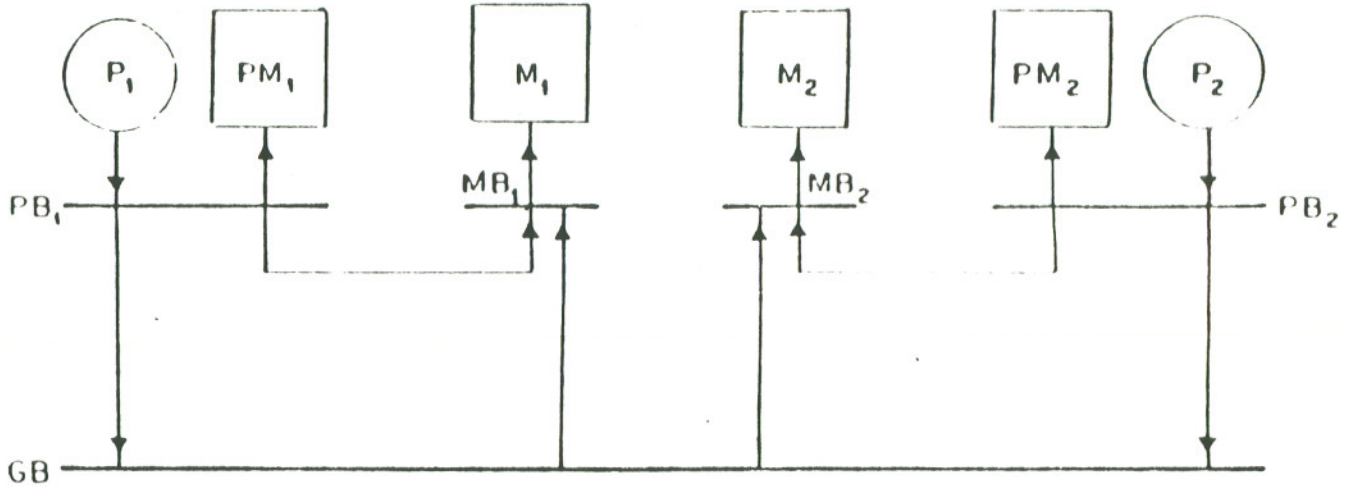
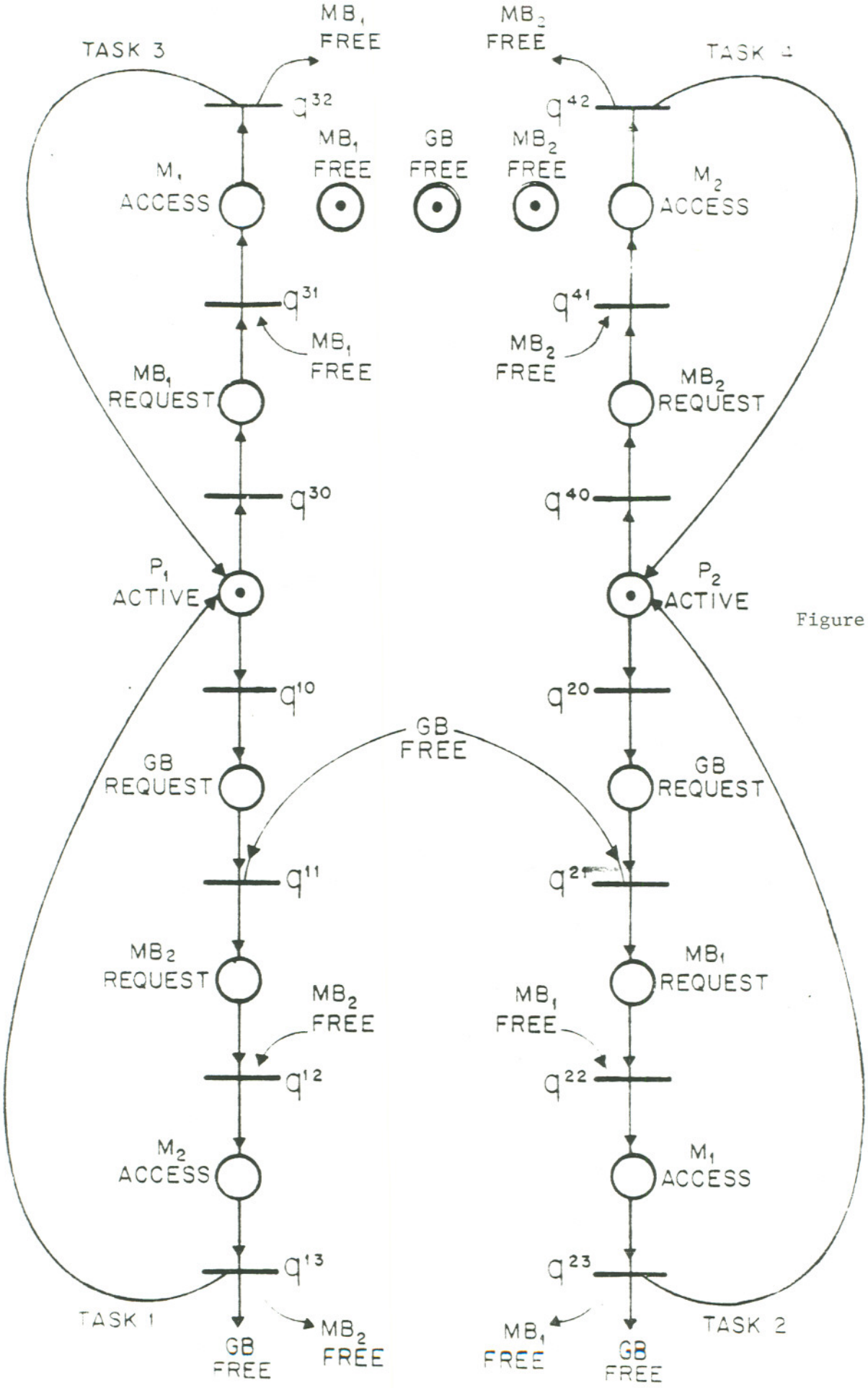


Figure 1.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q11
MB2 REQUEST
MB2 FREE
q12
M2 ACCESS
q13
TASK 1
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MB2 FREE
TASK 4
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q41
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q40
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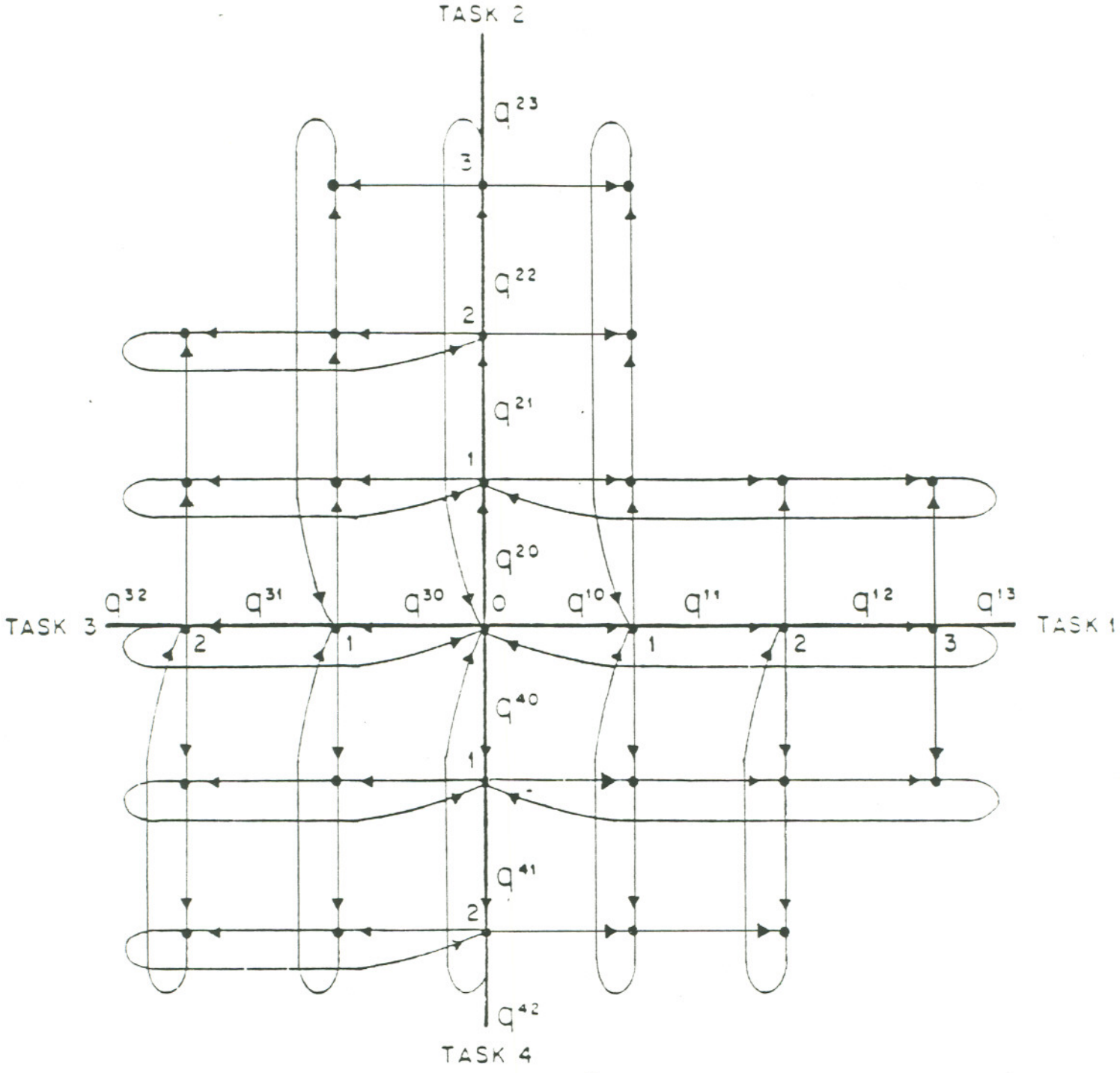
TASK 2

Figure 2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TASK 4

Figure 3

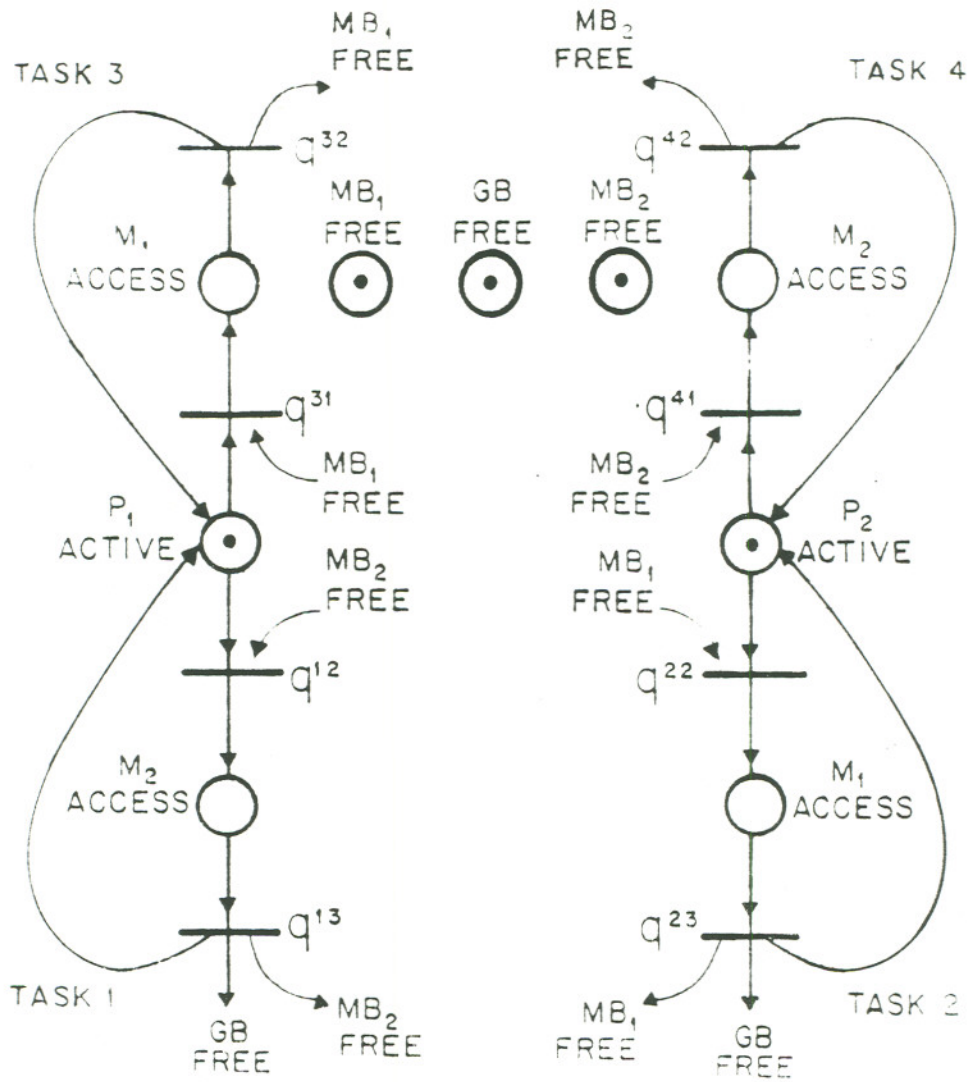
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Figure 4

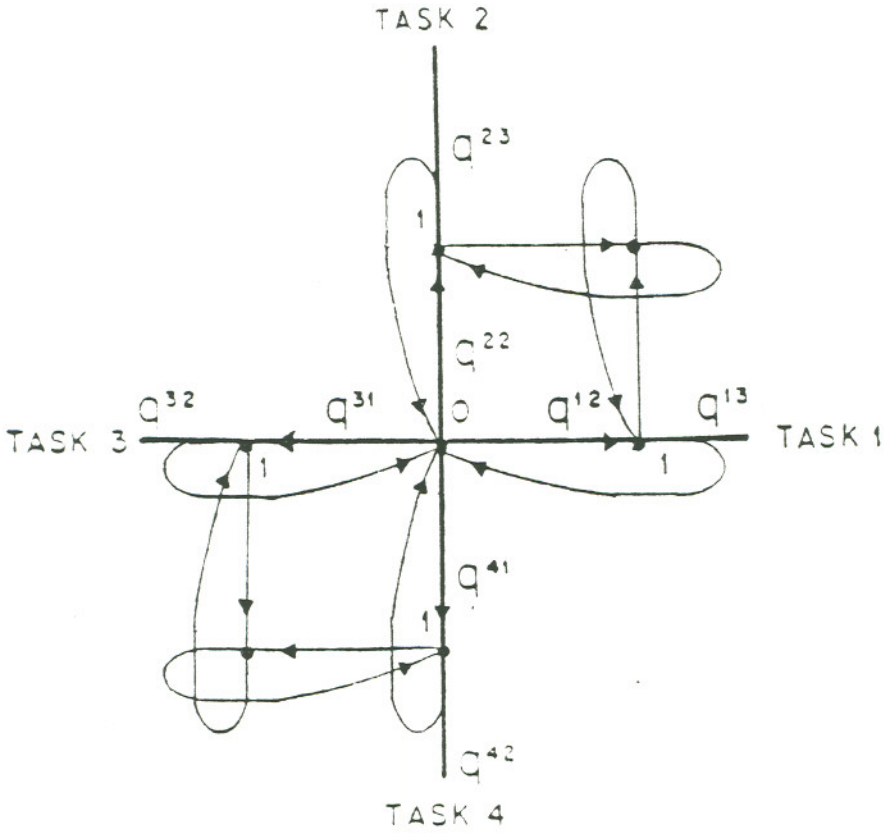

Figure 5