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POWER DISTRIBUTION IN TSV BASED 3-D PROCESSOR-MEMORY STACKS

A Thesis Presented

by

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to

The Graduate School

in Partial Fulfillment of the

Requirements

for the Degree of

Master of Science

in

Electrical Engineering

Stony Brook University

May 2012

Stony Brook University

The Graduate School

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Abstract of the Thesis

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Three primary techniques for manufacturing through silicon vias (TSVs), via-first, via-middle, and via-last, have been analyzed and compared to distribute power in a three-dimensional (3-D) processor-memory system with nine planes. Due to distinct fabrication techniques, these TSV technologies require significantly different design constraints, as investigated in this work. A valid design space that satisfies the peak power supply noise while minimizing area overhead is identified for each technology. It is demonstrated that the area overhead of a power distribution network with via-first TSVs is approximately 9% as compared to less than 2% in via-middle and via-last technologies. Despite this drawback, a via-first based power network is typically overdamped and the issue of resonance is alleviated. A via-last based power network, however, exhibits a relatively low damping factor and the peak noise is highly sensitive to number of TSVs and decoupling capacitance.

To my dearest parents,
Jayashree Krishnamurthy and
Satheesh Lakshminarayana.

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ACKNOWLEDGEMENTS

The last two years I have spent at Stony Brook University have been eventful and rewarding. Thanks to the very many people who have made it so.

I am grateful and indebted to my advisor, Professor Emre Salman for giving me an opportunity to work with him for my master's thesis. His indulgence and patience have been an inspiration to me in the last 17 months. Working with him helped me develop insights into my academic life that continue to positively influence me. Thank you Professor for everything.

I would like to thank Professor Milutin Stanacevic and Professor Mikhail Dorojevets for serving on my defense committee. Listening to their lectures was a pleasure and having them on the defense committee a privilege. A special thanks to all the members, present and past, of the Nanoscale Circuit and Systems Laboratory for being a great company in learning.

I am grateful to Dr. Sadanand Deshpande, Manager of Semiconductor Characterization and eDRAM Design at IBM Semiconductor Research and Development Center (SRDC), Bangalore, for providing me with the excellent opportunity to work with him as a research intern. I thank Raviprasad Kuloor and Santhosh Narayanaswamy for mentoring me very patiently while I was at IBM SRDC. My thesis work has been greatly influenced by the experience I gained there.

I am extremely grateful to Anuj Gupta, Senior Design Engineer at Global Foundries, New York, for being a great friend and for making himself available 24X7 for even the silliest of the doubts I have had related to my research. Insights he gave into my research have been very valuable, thank you once again. I would also like to thank Varun Subramanian, PhD candidate in the Embedded Systems Laboratory for

helping me document my work.

Prathyush Kama, a passionate person, a silent teacher, and a wonderfully warm friend, I cannot thank you enough. From cooking to computer architecture, what I have learnt from you seems to last me forever. Ganesh Kamath, I am so glad you were always available to share a story. It is so hard to imagine how life at Stony Brook would have been without you as a suite mate. Deepti Rao, I just cannot thank you enough. Your unconditional love and support have meant a lot.

Lastly and most importantly, a heartfelt thanks to my parents without whom I could not have made it anywhere. Without saying much, I would like to quote the much clichéd, yet very appropriate words, “No gift to your mother will ever equal her gift to you-Life”. Thank you.

Chapter 1

Introduction

Over the past decade, various novel technologies have emerged to alleviate the scaling challenges of traditional two-dimensional (2-D) integrated circuits. Monolithic three-dimensional (3-D) integration is a promising technology that maintains the benefits of miniaturization by enabling higher integration density and enhancing system performance [1–6]. In wafer level 3-D integration technologies, multiple wafers are thinned, aligned, and vertically bonded. Communication among the dies is achieved by high density through silicon vias (TSVs).

In 3-D technologies, global interconnect is reduced, lowering the overall power dissipation and latency. 3-D integration also provides unique advantages to develop highly heterogeneous systems where diverse functions such as analog/RF based communication, sensing circuitry, digital data processing blocks, and sensors are merged in a monolithic fashion [3, 7, 8], as illustrated in Fig. 1.1. Another important application of 3-D integration technology is stacked processor-memory systems, as described below.

3-D technology alleviates the existing gap between logic blocks and memory units in high performance microprocessors. The difference in the performance of

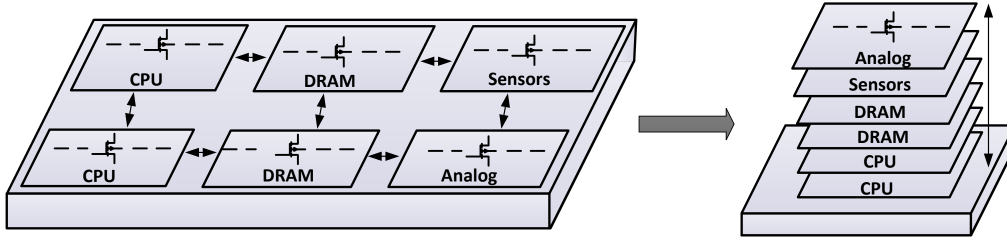

Figure 1.1: **Enabling heterogeneous integration through three-dimensional ICs.**

a processor and memory has grown due to significantly different scaling characteristics [9, 10]. This issue has been partly relieved with the introduction of multilevel cache with different size and speed [11]. The growing disparity, however, remains as a primary concern. 3-D integration technology alleviates this issue by utilizing vertically embedded dynamic random access memory (DRAM), thereby significantly increasing the memory bandwidth and reducing memory access time.

A significant circuit- and physical-level challenge in this system is to design a robust power distribution network that achieves reliable power delivery to each die. Maintaining the power network impedance smaller than target impedance is a difficult task due to reduced operating voltages, increased current magnitudes, and the existence of multiple dies and TSVs. A conservatively large number of power/ground TSVs can significantly increase the area overhead in addition to producing high inductive characteristics due to a smaller damping factor, as demonstrated in this work.

The rest of the chapters are organized as follows. The primary characteristics of the three TSV fabrication technologies and the previous work in this area are summarized in Chapter 2. Electrical models used to analyze power distribution networks for each TSV technology are described in Chapter 3. Approach and simulation results of the power supply noise analysis and power loss are provided in

Chapter 4. Finally, the thesis is concluded in Chapter 5.

Chapter 2

TSV Fabrication Techniques and Previous Work

Each TSV technology exhibits unique challenges in designing a 3-D power distribution network. These differences arise due to distinct fabrication techniques. The fabrication characteristics and relative physical dimensions of via-first, via-middle, and via-last TSVs are summarized, respectively, in Sections 2.1, 2.2, and 2.3. These properties are also listed in Table 2.1. The chapter is concluded in Section 2.4 by summarizing the previous work in this area and primary contributions of this research.

Parameter	Via-first	Via-middle	Via-last
Filling material	Doped polysilicon	Tungsten	Copper
Structure	Cylindrical	Annular and conical	Cylindrical
Processing temperature	High	Average	Low
Manufacturability	Difficult	Very difficult	Established
Formation	Before FEOL	Before BEOL	After BEOL
Electrical characteristics	Highly resistive	Resistive and inductive	Inductive
Landing metal	M_1	M_1	M_{Top}
Take-off metal	M_{Top}	M_{Top}	M_{Top}

Table 2.1: Characteristics of via-first, via-middle, and via-last TSVs [12–21].

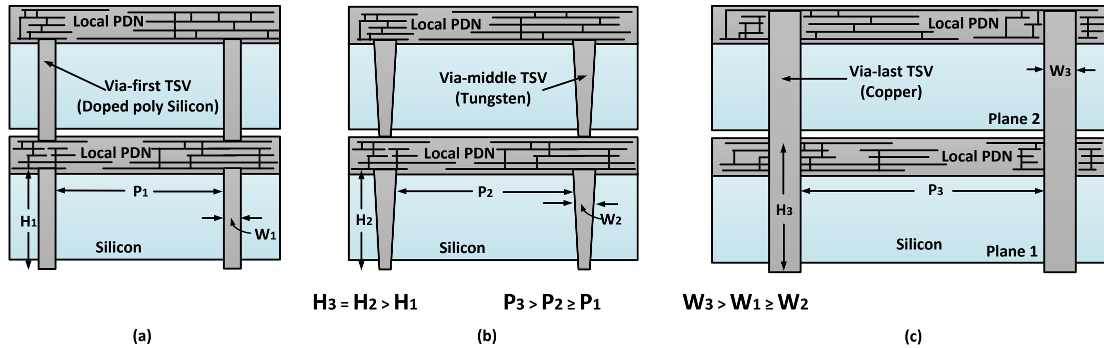

Figure 2.1: **Illustration of the three primary TSV technologies: (a) via-first, (b) via-middle, and (c) via-last.**

2.1 Via-first TSV

In the via-first method, TSVs are fabricated before the transistors are patterned in silicon, *i.e.*, prior to front-end-of-line (FEOL) [12,13,17,19]. Thus, TSVs fabricated with the via-first technique do not pass through the metallization layers, as depicted in Fig. 2.1(a). The TSV of a plane is connected between the first metal layer of the current plane and the top most metal layer of the previous plane. Polysilicon is typically used as the filling material due to its ability to withstand high temperatures [12, 13, 17, 19]. Via-first TSVs are less sensitive to contamination since both the filling and substrate materials are the same [18]. The physical dimensions of via-first TSVs are smaller than via-last TSVs [21]. Via-first TSVs, however, are highly resistive and have a lower filling efficiency due to the use of polysilicon as the filling material [18].

2.2 Via-middle TSV

In a via-middle process, the TSVs are fabricated after FEOL, but before the metallization layers are patterned, *i.e.*, prior to back-end-of-line (BEOL) [14–16, 18, 20]. Similar to via-first TSVs, via-middle TSVs connect the first metal layer of a plane with the last metal layer of the previous plane, as illustrated in Fig. 2.1(b). Since the high temperature FEOL process precedes TSV fabrication steps, via-middle process permits the use of tungsten as the filling material, which is significantly less resistive as compared to doped polysilicon. Tungsten can be used as the filling material due to low thermal expansion coefficient (4.6 ppm/K) as compared to copper (17 ppm/K) [15]. A material with low sensitivity to temperature is required since the TSV fabrication step is followed by a moderately high temperature BEOL process.

Via-middle TSVs require a relatively large (12:1 or higher) aspect ratio [14–16, 20]. Thus, the width of via-middle TSVs is comparable to the width of via-first TSVs whereas the height is comparable to via-last TSVs. This characteristic produces a relatively high inductive behavior. Also note that the fabrication process of via-middle TSVs is relatively more challenging. For example, a conformal barrier process is required for the tungsten to adhere to the dielectric in the cavity. A 20 nm titanium nitride (TiN) layer is typically deposited using metal organic chemical vapor deposition (MOCVD) [14]. TiN is a hard, dense, refractory material with sufficiently low electrical resistivity (22 $\mu\Omega$cm) [22].

Another challenge is the high stress during the deposition of the oxide layer which is exacerbated when a conformal layer is required. This challenge is partially negated with the use of a tapered TSV structure that progressively shrinks in size [14, 15]. This structure is illustrated in Fig. 2.1(b). Other challenges include sensitivity to contamination and the requirement to maintain the temperature within

500°C [18].

Novel deposition techniques such as atomic layer deposition (ALD) and time-modulated deposition alleviate some of these issues [14, 23]. From the design perspective, via-middle technology is an interesting compromise between a highly resistive via-first and a low resistive, but highly inductive via-last TSVs. Furthermore, similar to via-first TSVs, via-middle TSVs do not cause metal routing blockages. The Semiconductor Manufacturing Technology (SEMATECH) consortium has chosen via-middle TSVs as a primary focus area [24].

2.3 Via-last TSV

In the via-last approach, TSV formation occurs after the metallization layers are fabricated, *i.e.*, after BEOL [12, 18, 21]. Thus, as opposed to via-first and via-middle TSVs, via-last TSVs pass through the metal layers, causing metal routing blockages, as depicted in Fig. 2.1(c) [21, 25]. A lower resistivity filling material such as copper is used since high temperature FEOL and BEOL processes are performed before the via formation [12, 18]. The use of copper as a filling material makes the process sensitive to both temperature (should be maintained less than 230°C) and contamination [18]. Despite exhibiting relatively low resistance, the inductive characteristics of via-last TSVs are relatively more significant than via-first TSVs due to greater dimensions [21]. The physical connection between the TSV and metal layers is typically achieved at the top most metal layer.

2.4 Previous Work

Previous work on 3-D power delivery has focused on different power distribution topologies, effect of TSV geometry, and core versus coaxial TSVs [25–28]. For example, Wu and Zhang have proposed a strategy to place the TSVs and the decoupling capacitors in a processor-memory system [26]. A method to place decoupling capacitance for the processor die by exploiting the proximity between the processor die and the DRAM dies has been proposed. Khan *et al.* have performed an architectural analysis of power delivery in 3-D circuits [27]. The impact of TSV size and spacing, C4 (controlled collapse chip connection) bump spacing, and co-axial TSVs has been investigated. Both of these works, however, are based on via-last TSVs. Other TSV fabrication technologies such as via-first and via-middle have not been considered.

Existing work on different TSV technologies primarily focus on fabrication characteristics rather than circuit design requirements. For example, in [12] and [29], via-first TSV technology has been investigated with little attention on circuit design implications. Similarly, via-middle TSVs have been discussed in [14–16] focusing primarily on process characteristics. The fabrication constraints of the three TSV technologies are also compared in [30]. Furthermore, yield characteristics of these TSV technologies are analyzed and compared in [31].

Pavlidis and De Micheli have investigated the presence of alternate low impedance current paths in via-first TSVs [25]. These additional current paths have been exploited, resulting in a 22% reduction in the number of intraplane vias or alternatively, a 25% decrease in the required decoupling capacitance [25]. The same filling material, however, has been considered for both via-first and via-last TSVs. Furthermore, a simplified model has been assumed for the power distribution network

within each plane.

Via-first, via-middle, and via-last TSV technologies exhibit unique advantages and limitations, as described in this paper. Furthermore, a power distribution network in each case exhibits significantly different design requirements. These design requirements are separately evaluated for each TSV technology. A nine plane 3-D system with eight planes of embedded DRAM and a single processor plane is considered. The two primary contributions of this work are as follows: (1) via-first, via-middle, and via-last TSV technologies are explored in a comparative manner to distribute power in a 3-D processor-memory system and (2) design space that satisfies power supply noise while minimizing the overall physical area is determined for each TSV technology. The primary differences in the design space are also emphasized to determine different design requirements. Furthermore, a power loss analysis is also performed and design guidelines are provided for each technology.

Chapter 3

Electrical Models

The models that are used to analyze power supply noise for each TSV technology are described in this chapter. System level model, including the orientation of the planes and the dimensions of the dies are discussed in Section 3.1. Electrical models used for TSVs, substrate, and the power distribution network within a plane are provided, respectively, in Sections 3.2, 3.3, and 3.4. Finally, the model for the load circuit is described in Section 3.5.

3.1 System Level Model

A 3-D system in 32 nm CMOS technology consisting of eight memory planes and one plane for the processor is considered. This system is illustrated in Fig. 3.1. Each plane contains nine metal layers where the metal thickness and aspect ratio are determined according to 32 nm technology parameters [32]. The power supply voltage V_{DD} is equal to 1 volt. Each plane occupies an area of 120 mm^2, excluding the TSVs and the intentional decoupling capacitance. The system has 1 gigabyte (GB) of DRAM distributed uniformly across eight memory planes. Each memory plane has 1 gigabit (Gb) DRAM. Every DRAM plane is divided into 32 modules

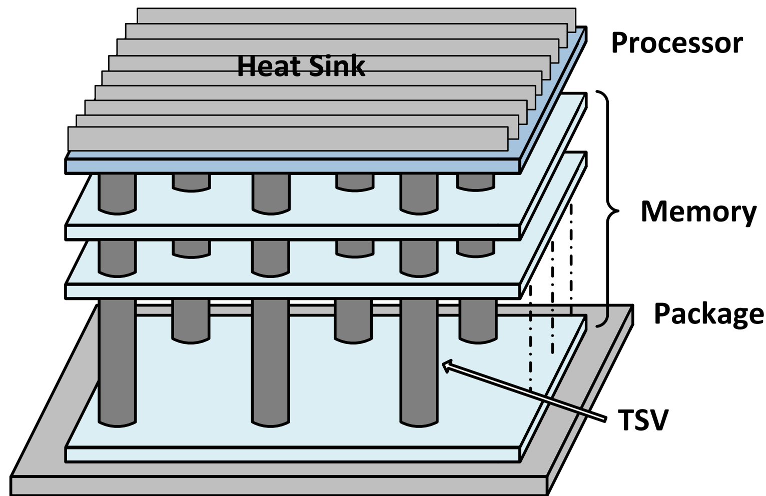

Figure 3.1: **Three-dimensional integration of dynamic random access memory with the processor core.**

of equal size, each having 32 Mb of memory. Similarly, the processor plane is also divided into 32 modules. Each of these modules consume an area of 1500×2500 μm^2. This topology is depicted in Fig. 3.2.

For via-first and via-middle technologies, the TSVs are placed beneath the active circuit, as illustrated in Fig. 3.2(a) whereas in via-last technology, the power and ground TSVs are distributed on both sides of each module, as depicted in Fig. 3.2(b). Note that although the TSVs are placed beneath the active circuit in via-first and via-middle technologies, these TSVs consume additional device area. Thus, in Fig. 3.2(a), the area represented by a 32 Mb DRAM module includes both the 1500×2500 μm^2 DRAM area and the TSV area. Note that the processor plane does not contain any TSVs, as described later in this section.

As depicted in Fig. 3.2, the processor plane is typically placed closer to the heat sink due to high switching activity. The memory planes are therefore closer to the package whereas the processor plane is farthest from the package pads. The orien-

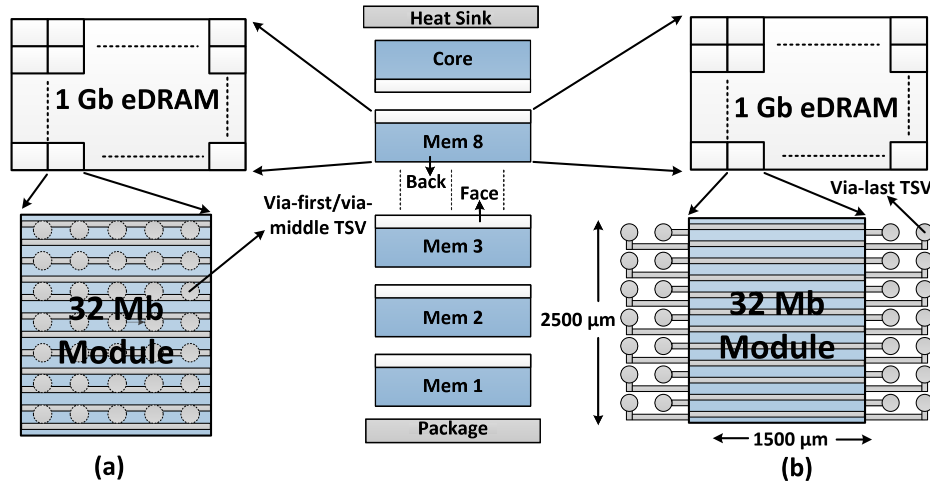

Figure 3.2: **Illustration of the 3-D processor-memory stack: (a) via-first and via-middle TSVs and (b) via-last TSVs.**

tation of the memory planes such as face-to-face or face-to-back exhibits a design tradeoff. The first memory plane can face the package where the metal layers are directly connected (without the TSVs) to the package pads. Alternatively, the first memory plane can face the adjacent DRAM plane. In the second option, as considered in this work, TSVs are required to connect the first memory plane with the package pads. First option eliminates these TSVs, but the additional current paths available in via-first and via-middle technologies [25] cannot be exploited in distributing power. These additional current paths exist only when the current flow is from the lowest to the highest metal layer in a plane, as described later. Another consideration is the orientation between the processor plane and the adjacent memory plane. A face-to-back approach maintains the symmetry of the 3-D system, but the communication bandwidth between the two planes is limited. Alternatively, in a face-to-face approach, processor and memory can communicate with the metal layers without requiring TSVs, thereby enhancing the communication bandwidth.

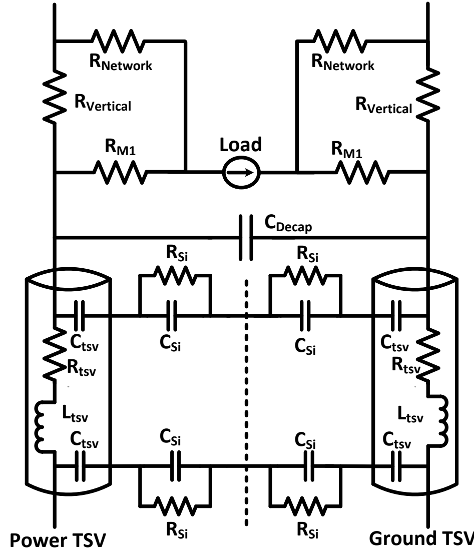

Figure 3.3: **Equivalent power distribution network that corresponds to each module.**

This scheme, as considered in this work, also reduces the overall number of TSVs, partly compensating the additional TSVs between the first memory plane and package. Thus, the processor plane does not contain any TSVs.

In the rest of this work, the analysis is performed for an area of 1500×2500 μm^2, which corresponds to a single module in both memory and processor planes. The procedure is similar for the remaining 31 modules. An equivalent electrical model corresponding to the power distribution network of this portion of the system is illustrated in Fig. 3.3. This model consists of the TSVs, substrate, power distribution network within a plane, switching load circuit, and decoupling capacitance, as described in the following sections. Note that in addition to these on-chip impedances, the parasitic package resistance and inductance are, respectively, 3 mΩ and 100 pH at both the power and ground supplies.

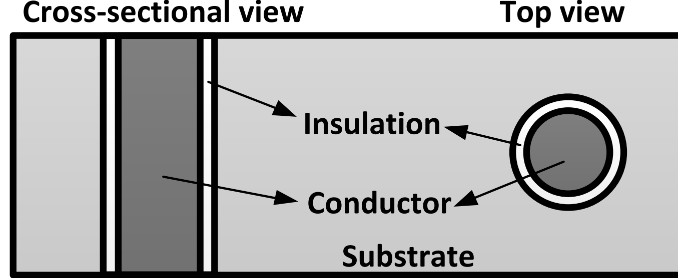

Figure 3.4: **Cross-sectional and top views of a TSV.**

3.2 TSV Model

A TSV is typically represented as a cylinder with a diameter W and depth H. Aspect ratio of a TSV is given by H/W. Cross-sectional and top views of a TSV are depicted in Fig. 3.4. The minimum distance between the two TSVs is determined by the pitch P, which is typically twice the TSV diameter [33].

The TSV model consists of a resistance R_{tsv} and inductance L_{tsv} due to the filling material, and a capacitance to the substrate C_{tsv} due to the thin dielectric layer [34]. R_{tsv} is determined by [35],

$$R_{tsv} = \sqrt{(R_{AC}^{tsv})^2 + (R_{DC}^{tsv})^2}, \tag{3.1}$$

where the DC resistance R_{DC}^{tsv} and AC resistance R_{AC}^{tsv} are, respectively,

$$R_{DC}^{tsv} = \frac{\rho_f H}{\pi (W/2)^2}, \tag{3.2}$$

$$R_{AC}^{tsv} = \frac{\rho_f H}{2\pi (W/2)\delta_{tsv}}. \tag{3.3}$$

ρ_f is the conductivity of the filling material and the skin depth δ_{tsv} is [35]

$$\delta_{tsv} = \frac{1}{\sqrt{\pi f \mu_f \rho_f}}, \tag{3.4}$$

where f is the frequency and μ_f is the permeability of the filling material. The TSV inductance L_{tsv} is [36]

$$\begin{aligned} L_{tsv} &= \frac{\mu_o}{4\pi}[2H\ln(\frac{2H+\sqrt{(W/2)^2+(2H)^2}}{W/2})+ \\ &\quad (W/2-\sqrt{(W/2)^2+(2H)^2})], \end{aligned} \tag{3.5}$$

where μ_o is vacuum permeability. The TSV capacitance C_{tsv} is determined from the cylindrical capacitor formula as [37]

$$C_{tsv} = \frac{2\pi\varepsilon_{ox}H}{\ln(\frac{W/2+t_{ox}}{W/2})}, \tag{3.6}$$

where ε_{ox} is the oxide permittivity.

Note that in via-middle technology, a tapered TSV structure is utilized to mitigate the high stress during the TSV formation, as mentioned earlier. Thus, the resistance and inductance of via-middle TSVs are determined by integrating over the maximum and minimum TSV diameter, and dividing the result by the difference between the two extremes,

$$R_{tsv,via-middle} = \int_{W_{min}}^{W_{max}} \frac{R_{tsv}}{W_{max}-W_{min}}dW, \tag{3.7}$$

$$L_{tsv,via-middle} = \int_{W_{min}}^{W_{max}} \frac{L_{tsv}}{W_{max}-W_{min}}dW. \tag{3.8}$$

For the via-middle TSV capacitance, (3.6) is utilized to calculate the arithmetic average since the effect of this capacitance is negligible when large decoupling capacitances are used, as described in Chapter 4. Also note that the skin effect is neglected for via-first and via-middle based TSVs due to sufficiently small TSV diameters. The maximum and minimum thickness for via-middle TSVs are listed in Table 3.1. The primary characteristics of the three TSV technologies are also listed in this table.

Parameter	Via-first	Via-middle	Via-last
Diameter W	4 μm	4 μm to 2.66 μm	10 μm
Height H	10 μm	60 μm	60 μm
Pitch P	8 μm	8 μm to 9.34 μm	20 μm
Oxide thickness t_{ox}	0.2 μm	0.2 μm	0.2 μm
TSV resistance R_{tsv}	5.7 Ω	858.36 mΩ	20 mΩ
TSV inductance L_{tsv}	4.18 pH	49.76 pH	34.94 pH
TSV capacitance C_{tsv}	23 fF	117.81 fF	283 fF
Tapering angle	*NA*	1°	*NA*
Aspect ratio AR	2.5:1	15:1-22:1	6:1
Material resistivity ρ_f	7.2 $\mu\Omega$m	12 $\mu\Omega$cm	16.8 nΩm
Substrate resistance R_{si}	8.81 kΩ	1.57 kΩ	1.76 kΩ
Substrate capacitance C_{si}	1.19 fF	6.72 fF	6 fF
Co-efficient of thermal expansion CTE	Low	4.6 ppm/K	17 ppm/K

Table 3.1: Model parameters for TSVs [12, 15, 36].

3.3 Substrate Model

The substrate is modeled as an RC impedance, where the substrate capacitance C_{si} and the substrate resistance R_{si} are, respectively [37],

$$C_{si} = \frac{\pi\varepsilon_{si}H}{\ln\left(\frac{2P}{W/2} + \sqrt{(\frac{2P}{W/2})^2 - 1}\right)}, \tag{3.9}$$

$$R_{si} = \frac{\varepsilon_{si}\rho_{si}}{C_{si}}. \tag{3.10}$$

$\varepsilon_{si} = 105 \times 10^{-12}$ F/m and $\rho_{si} = 10$ Ωcm are, respectively, silicon permittivity and substrate resistivity.

3.4 Power Distribution Network within a Plane

The model of a power distribution network within a plane plays an important role in analyzing power supply noise in TSV based 3-D circuits. The characteristics of this network vary depending upon the TSV technology, as described in this section.

In the proposed 3-D processor-memory stack, the two top most metal layers (M_9 and M_8) in each plane are dedicated to global power distribution. The physical

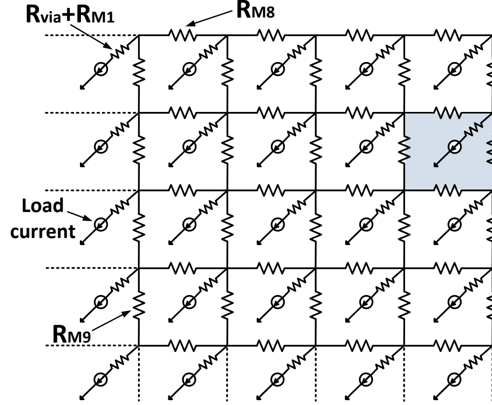

Figure 3.5: **Interdigitated power distribution network within a plane consisting of two top most metal layers, stack of vias and M_1 in each intersection.**

characteristics of the on-chip interconnects are obtained from a 32 nm CMOS technology with nine metal layers [32]. An interdigitated topology is utilized where a stack of vias, located at each intersection of M_9 and M_8, transmits the power supply voltage to the first metal layer, and ultimately to the switching devices. This topology is illustrated in Fig. 3.5. In this figure, each horizontal and vertical resistance correspond, respectively, to M_8 and M_9 resistance. The resistance due to the stack of vias and M_1 is represented by the diagonal resistance. A single stack of vias from M_1 to M_9 is assumed to be 16 Ω [38]. Note that M_9 is less resistive than M_8 due to significantly higher thickness [32]. Thus, M_9 is routed vertically since the vertical dimension is higher than the horizontal dimension, as depicted in Fig. 3.2. The number of horizontal (M_8) and vertical (M_9) lines is determined from the pitch and width of the interconnects [32]. These characteristics are listed in Table 3.2.

Referring to Fig. 3.5, the physical area determined by each set of four nodes (see shaded region) is 5.62 μm $\times$ 19.4 μm. The power supply voltage is distributed to the periphery of this region by the stack of vias. Within this area, however, power is distributed by the first metal layer M_1 of the standard cells.

Parameter	Metal 8	Metal 9
Pitch	5.616μm	19.4μm
Thickness	504nm	8μm
Width	5.33μm	5.33μm
Node to node resistance	R_{M8} = 242.65 mΩ	R_{M9} = 4.43 mΩ
Number of parallel paths	445	77

Table 3.2: On-chip metal characteristics for the global power distribution network in each plane [32].

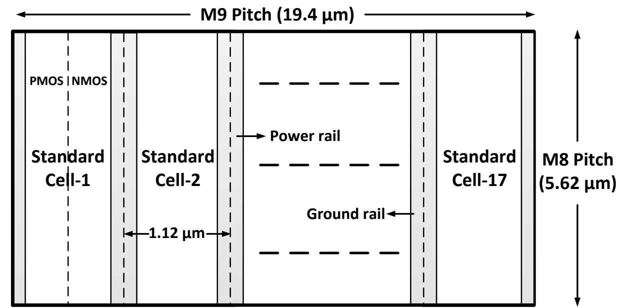

Figure 3.6: **Structure of standard cell logic in each module.**

Each standard cell has a height of approximately 10×M_1 metal lines, equal to 1.12 μm. The width of each standard cell is equal to M_8 pitch, 5.62 μm. Since M_9 pitch is 19.4 μm, 17 standard cells are located within the shaded region, as illustrated in Fig. 3.6. The minimum width and pitch of M_1 in a 32 nm technology are, respectively, 66.2 nm and 112.5 nm [32]. A metal line (M_1) of width 179 nm is utilized to distribute power and ground within a standard cell of width 5.62 μm, producing a resistance of approximately 326 mΩ.

The current flow within the power distribution network is represented in Fig. 3.7. M_8 and M_9 resistances represent the global power distribution network within a plane and the vertical resistance represents the stack of vias which is in series with the M_1 resistance. The value of these resistances varies depending upon the TSV technology, as described in the following sections.

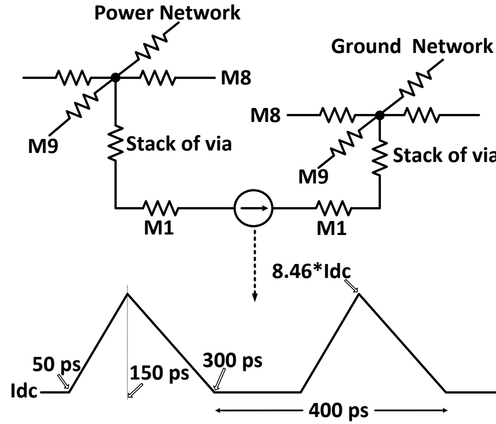

Figure 3.7: **Illustration of power distribution network and the characteristics of load current.**

3.4.1 Via-first and Via-middle TSV

In the via-first and via-middle methods, the TSVs connect the M_1 with the M_{Top} of the previous plane, as depicted, respectively, in Figs. 2.1(a) and 2.1(b). Referring to Fig. 3.3, the impedance due to the local metal layers connecting the two TSVs is modeled with $R_{Vertical}$, which is determined by the stack of via resistance. Note that the direction of current flow on the power network within a single plane is from M_1 to M_{Top}. Thus, alternative current paths exist in via-first and via-middle technologies, as also mentioned in [25]. These alternate current paths are illustrated in Fig. 3.8. The supply current is not required to flow from the top metal layer to the first metal layer. Instead, the power supply voltage can be distributed only by M_1 provided that the distance between the TSV and device is relatively small. This path is modeled by the resistance R_{M1} in Fig. 3.3. For farther distances, the current first flows toward the top metal layers through the stack of vias ($R_{Vertical}$), is then distributed by the low resistance global power network throughout the die. Subsequently, current flows back down to the first metal layer through the stack of

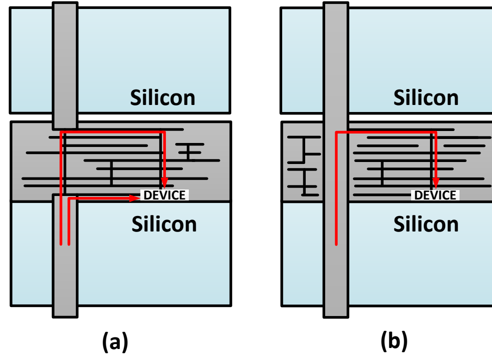

Figure 3.8: **Current flow from power supply to devices: (a) in via-first and via-middle TSV technologies, alternative current paths exist where the current can reach the devices only through the first metal layer, (b) in via-last TSV technology, current flows from the top most metal layer to the devices and alternative current paths do not exist.**

vias to reach the switching device. This path is modeled by $R_{Network}$ in Fig. 3.3. The value of these resistances is listed in Table 3.3.

3.4.2 Via-last TSV

As opposed to via-first and via-middle TSVs, via-last TSVs are located at the periphery of each module. As shown in Fig. 2.1(c), via-last TSVs pass through the metalization layers and the connection with the power network within a plane is achieved at the highest metal layer. Thus, the vertical resistance $R_{Vertical}$ is part of the TSV resistance. Furthermore, alternative current paths mentioned for via-first and via-middle TSVs do not exist in via-last TSVs since the TSV is not directly connected to the first metal layer. For via-last TSVs therefore the resistance R_{M1} in Fig. 3.3 is infinitely large. Finally, $R_{Network}$ represents the equivalent resistance between the switching load and the intersection of TSV and top metal layer. The value of these resistances is listed in Table 3.3.

Parameter	Via-first	Via-middle	Via-last
Network resistance $R_{Network}$	1.97 mΩ	1.97 mΩ	8.51 mΩ
Vertical resistance $R_{Vertical}$	1.97 mΩ	1.97 mΩ	NA
M1 Path Resistance R_{M1}	73 $\mu\Omega$	73 $\mu\Omega$	∞

Table 3.3: Power distribution network resistances within a plane.

Parameter	DRAM	Processor
Total power	3/32 W	90/32 W
Static Power	0.9/32 W	27/32 W
Dynamic Power	2.1/32 W	63/32 W
Static Current	28.125 mA	843.75 mA
Peak Current	238.125 mA	7.14 A
Operating Frquency	2.5 GHz	2.5 GHz

Table 3.4: Power characteristics [26].

3.5 Switching Circuit

The DRAM consumes 3 W of power uniformly distributed across the eight stacks [26]. Alternatively, the processor consumes 90 W of power. 30% of the overall power is due to static power dissipation whereas the remaining portion is due to dynamic power consumption [26]. As illustrated in Fig. 3.7, a triangular current waveform is assumed with 400 ps period, 100 ps rise time, and 150 ps fall time. The DC current I_{dc} and peak current I_{peak} are determined based on, respectively, the static and dynamic power consumption. The power and switching current characteristics for the DRAM and the processor are listed in Table 3.4. Note that the power and current characteristics in this table represent the 32 Mb DRAM for the memory planes and the corresponding area for the processor plane.

Chapter 4

Power Supply Noise Analysis

The simulation results demonstrating distinct power distribution network design requirements for via-first, via-middle, and via-last TSVs are investigated in this chapter. The approach to determine the design space that satisfies power supply noise and minimizes area overhead is described in Section 4.1. Both transient and AC analyses results (and corresponding design guidelines for each TSV technology) are discussed, respectively, in Sections 4.2 and 4.3.

4.1 Approach

In 3-D power distribution networks, it is important to determine an appropriate number of TSVs and decoupling capacitance that satisfy the constraint on power supply noise. From this design space, a valid pair that minimizes the physical area overhead is chosen. Note that this specific design point is dependent upon the implementation of decoupling capacitance. Two methods are considered: (1) MOS capacitance in a 32 nm technology node with a capacitance density of 39.35 fF/μm^2 as determined from the equivalent oxide thickness (EOT) of the technology [32] and (2) deep trench capacitance with two different densities: 140 fF/μm^2

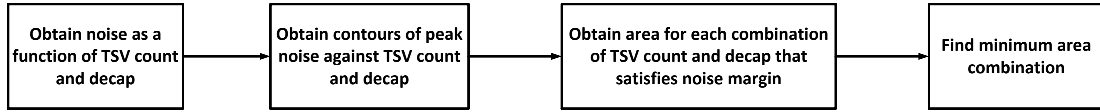

Figure 4.1: **Approach adopted to design the power distribution network with optimal number of TSVs and decoupling capacitance.**

and 280 fF/μm^2 [39].

The effect of the number of TSVs and decoupling capacitance on power supply noise is analyzed in both time and frequency domains, as described in the following sections. Note that in the rest of the thesis, number of TSVs refers to the number of power TSVs within a single module. The decoupling capacitance refers to the overall capacitance in each DRAM module. The area overhead is determined as a percentage of the area of a single module, which is 1500×2500 μm^2.

4.2 Transient Analysis Results

The dependence of peak noise on decoupling capacitance and number of TSVs, design space that satisfies the target power supply noise, and the area overhead due to TSVs and decoupling capacitance are provided. Note that the sensitivity of peak noise on number of TSVs and decoupling capacitance varies depending upon the specific design point, as described in this section. Also note that the power supply noise is observed across the current source located at the processor plane which is the farthest node from the power supply pads. In transient analysis, the tolerable power supply noise is assumed to be 100 mV, 10% of the power supply voltage.

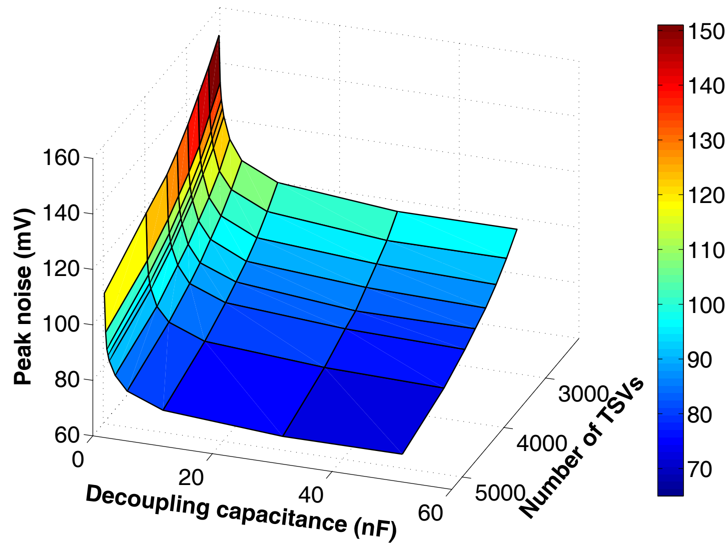

Figure 4.2: **Surface plot of peak noise as a function of number of TSVs and decoupling capacitance in via-first TSV technology.**

4.2.1 Via-fist TSV

The peak noise surface as a function of decoupling capacitance and number of TSVs is plotted in Fig. 4.2 for via-first TSVs. Since the TSV resistance is significantly higher in via-first technology, the power distribution network is overdamped, producing a monotonic response. Thus, peak noise decreases as the number of TSVs and decoupling capacitance increase. To determine the valid design space, a contour at 100 mV peak noise is extracted from the noise surface, as depicted in Fig. 4.3. Any point above the curve satisfies the noise constraint whereas the shaded region should be avoided.

Since multiple valid pairs of number of TSVs and decoupling capacitance exist, a pair that minimizes the overall area overhead can be chosen. As mentioned previously, this design point that minimizes the area overhead depends upon the implementation of the decoupling capacitance. For via-first technology, deep trench

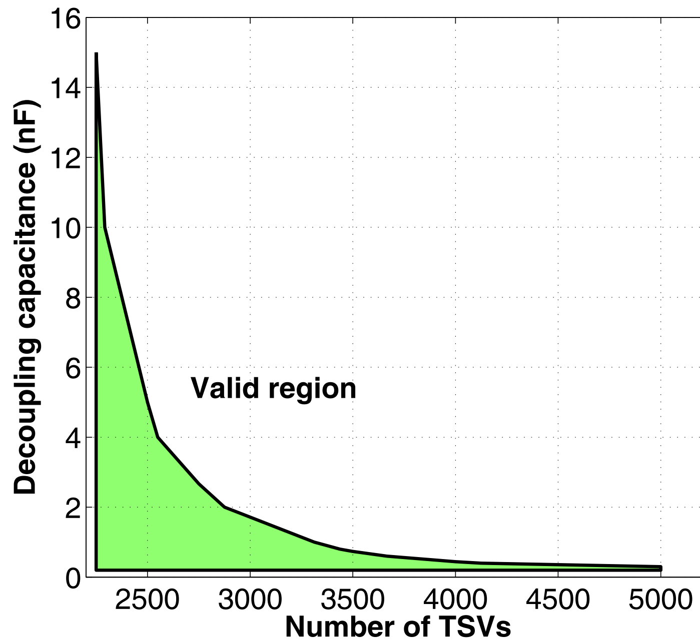

Figure 4.3: **Contour plot at 100 mV of peak noise in via-first TSV technology.**

capacitance is not considered since the substrate is thinned to approximately 10 μm. Assuming MOS decoupling capacitance with a density of 39.35 fF/μm^2, the area overhead is depicted in Fig. 4.4 for each point on the contour of Fig. 4.3.

As demonstrated in this figure, a specific design point exists that minimizes the area overhead. This design point corresponds to 2750 TSVs and 2.7 nF of decoupling capacitance, producing an area overhead of approximately 9%. Note that if an arbitrary pair is chosen from the contour in Fig. 4.3, the area overhead can be as high as 16%.

According to the transient noise results of a power distribution network with via-first TSVs, an important design requirement is to have a significantly high number of TSVs to reduce current per TSV. This requirement increases the required physical area. Note however that 6.25 times more via-first TSVs than via-last TSVs can be

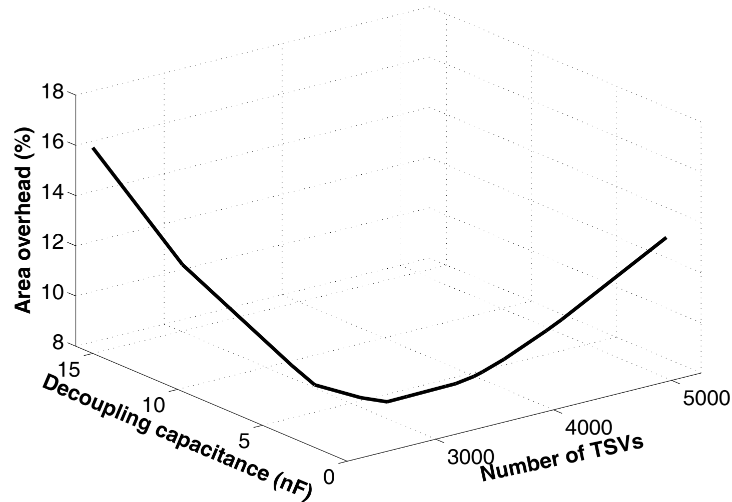

Figure 4.4: **Area overhead in via-first TSV technology. Note that each point on the curve satisfies the target power supply noise.**

placed within a constant area due to smaller via-first TSV dimensions. Also note that sufficient decoupling capacitance is required to reduce transient *IR* noise.

An advantage of a via-first based power distribution network is the high damping factor due to high TSV resistance and small TSV inductance. Thus, decoupling capacitance effectively suppresses the transient noise, producing a low peak-to-peak noise, as listed in Table 4.1. Note however that the power loss is relatively high in a via-first based power distribution network due to high TSV resistance, as listed in Table 4.1.

4.2.2 Via-middle TSV

The peak noise surface as a function of decoupling capacitance and number of TSVs is plotted in Fig. 4.5 for via-middle TSVs. The noise contour at 100 mV is illustrated in Fig. 4.6. Similar to a via-first based power network, the power supply noise monotonically decreases as the number of TSVs and decoupling capacitance

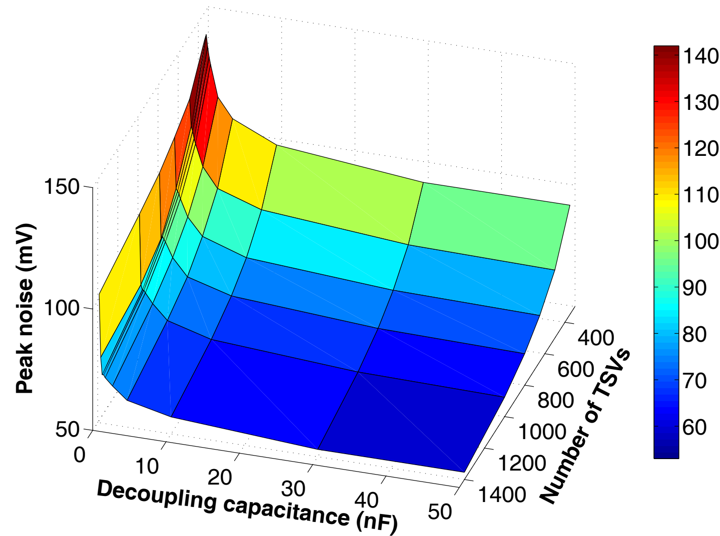

Figure 4.5: **Surface plot of peak noise a function of number of TSVs and decoupling capacitance in via-middle TSV technology.**

increase. Note that the required number of TSVs is lower than via-first TSVs since the TSV resistance is relatively less due to higher conductivity tungsten as opposed to doped polysilicon. Also note that since via-middle technology exhibits a greater substrate thickness, deep trench capacitance is considered. The area overhead is depicted in Fig. 4.7 for three different decoupling capacitance densities, as mentioned before.

Similar to a via-first technology, a specific design point exists where the physical area overhead is minimized. Also, similar to via-first TSVs, up to 6.25 times more via-middle TSVs can be placed in a given area as compared to via-last TSVs. If MOS capacitance is used, the design point that corresponds to minimum area is 620 TSVs and 0.6 nF of decoupling capacitance. If however a higher density deep trench capacitance is utilized, this optimum design point shifts to the left. In a specific small portion of the curve, the area overhead is relatively insensitive to decoupling capacitance and number of TSVs. Thus, two design points that minimize

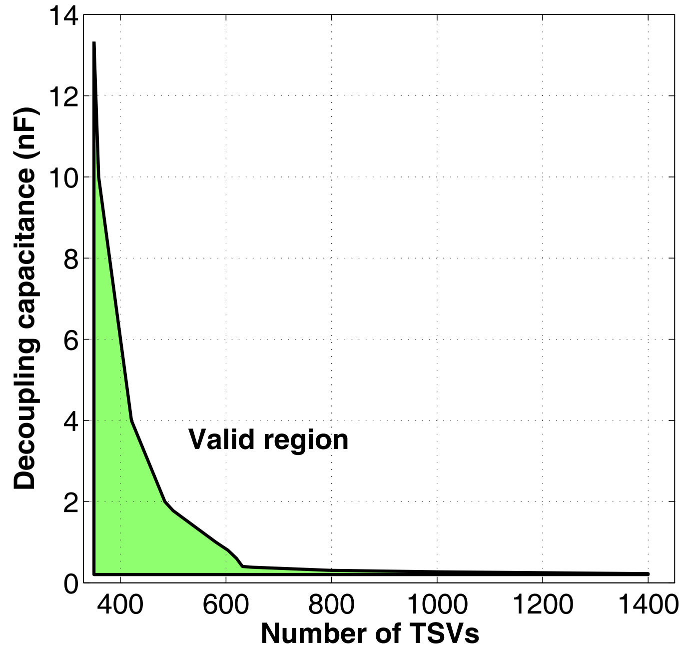

Figure 4.6: **Contour plot at 100 mV of peak noise in via-middle TSV technology.**

area overhead are determined for a low density deep trench capacitance, as listed in Table 4.1. Note that the area overhead in via-middle TSV is considerably less than via-first technology due to a smaller number of required TSVs.

An important difference between via-first and via-middle TSVs is the inductive characteristics. Via-middle TSVs exhibit higher inductance due to a greater TSV depth. Since the TSV resistance is significantly lower than via-first TSVs, the amount of decoupling capacitance plays an important role in the damping factor and therefore peak-to-peak noise. As listed in Table 4.1, the peak-to-peak noise in via-middle based power network is approximately twice as high as via-first based power network if the decoupling capacitance is low (such as the minimum area design point obtained with MOS-C). Alternatively, for the remaining minimum area design points where a deep trench capacitance is used, the peak-to-peak noise is

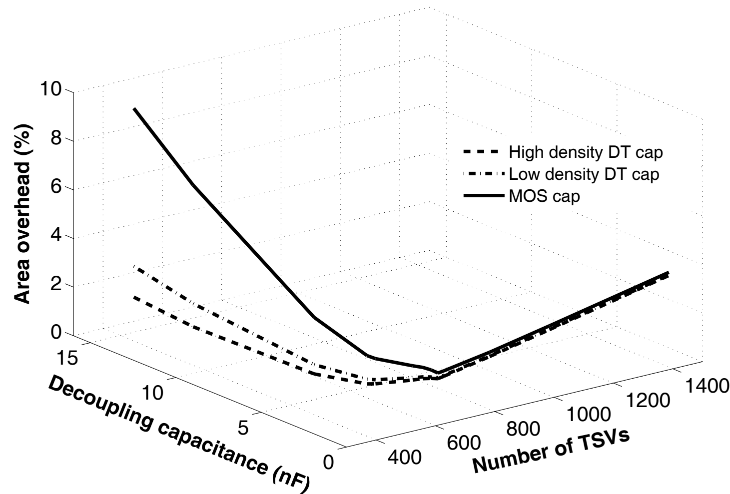

Figure 4.7: **Area overhead in via-middle TSV technology. Note that each point on the curve satisfies the target power supply noise.**

lowered due to a higher decoupling capacitance.

4.2.3 Via-last TSV

Via-last TSV technology exhibits significantly different noise characteristics as compared to via-first and via-middle technologies. Since copper is used as the filling material, the resistance of via-last TSVs is significantly less. Alternatively, the TSV inductance is higher than via-first TSVs and comparable to via-middle TSVs. Due to significantly less resistance and a relatively large inductance, a power distribution network with via-last TSVs is typically underdamped.

The peak noise surface as a function of decoupling capacitance and number of TSVs is plotted in Fig. 4.8 for via-last TSVs. As opposed to via-first and via-middle TSVs, the noise surface is nonmonotonic with multiple peaks where the noise exceeds the design objective. At specific combinations of the number of TSVs and decoupling capacitance, the power supply noise significantly increases due to the

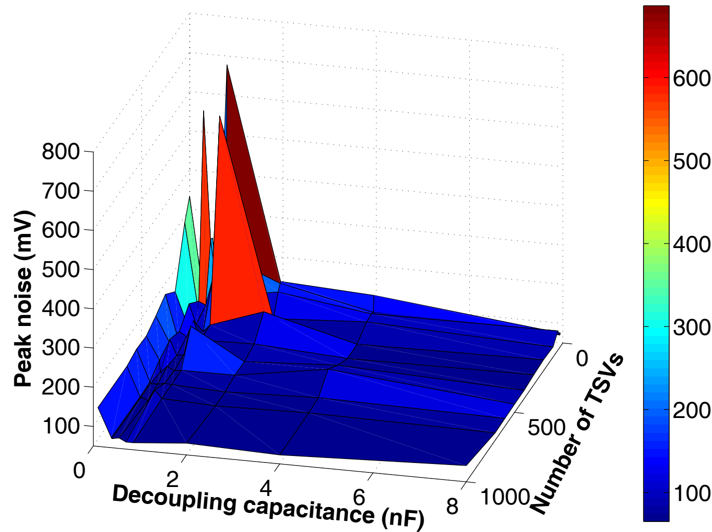

Figure 4.8: **Surface plot of peak noise as a function of number of TSVs and decoupling capacitance in via-last technology.**

resonant behavior. The noise contour at 100 mV is illustrated in Fig. 4.9 to determine the valid design space where the peak noise constraint is satisfied. The unshaded region represents a valid combination of number of TSVs and decoupling capacitance. As illustrated in this figure, at a specific decoupling capacitance, an increase in the number of TSVs can violate the noise constraint due to a lower damping factor. In this case, the decoupling capacitance should be increased. According to this figure, in via-last technology, the power supply noise is highly sensitive to number of TSVs and decoupling capacitance, particularly at relatively low decoupling capacitances. Furthermore, peak-to-peak noise is also significantly higher, as listed in Table 4.1. The area overhead, however, is the lowest in via-last TSVs since the number of required TSVs is significantly less. The power loss is also small in a via-last based power network due to a similar reason. Variation of area overhead as a function of TSVs and decoupling capacitance that satisfy the power supply

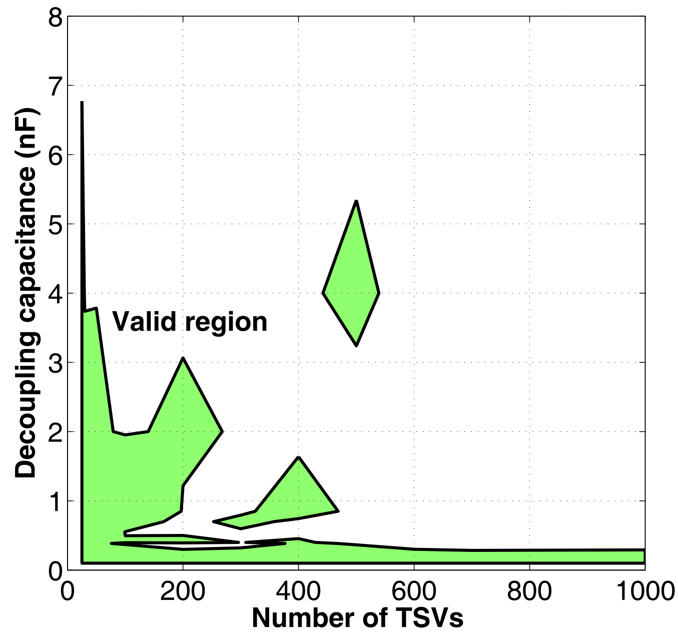

Figure 4.9: **Contour plot at 100 mV of peak noise in via-last TSV technology.**

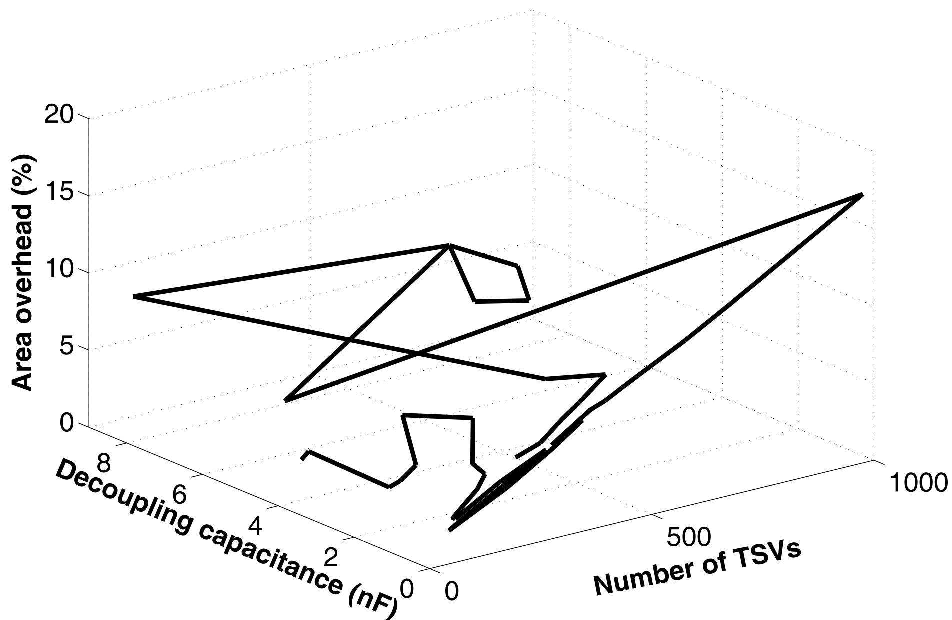

Figure 4.10: **Area overhead in via-last TSV technology when decoupling capacitance is implemented as MOS capacitors. Note that each point on the curve satisfies the target power supply noise.**

noise is shown in Fig. 4.10. The graph is plotted assuming that the decoupling capacitance is implemented as MOS capacitors. Note that the dependence of area overhead on number of TSVs and decoupling capacitance is highly complicated due to the nonmonotonic behavior of power supply noise. The design points that correspond to the minimum area overhead while satisfying the power supply noise are listed in Table 4.1 for both MOS and deep trench capacitance densities.

VIA-FIRST						
Capacitance type	Capacitance Density (fF/μm^2)	Area penalty	Number of TSVs	Decoupling capacitance (nF)	Power loss (mW)	Peak-to-peak noise (mV)
Metal-oxide-semiconductor	39.35	9.06%	2750	2.7	8.69%	33.42
VIA-MIDDLE						
Capacitance type	Capacitance Density (fF/μm^2)	Area penalty	Number of TSVs	Decoupling capacitance (nF)	Power loss (mW)	Peak-to-peak noise (mV)
Metal-oxide-semiconductor	39.35	1.96%	620	0.60	7.61%	63.56
Low density deep trench	140	1.68%	421	4	9.35%	31.33
Low density deep trench	140	1.68%	484	2	8.28%	45.13
High density deep trench	280	1.49%	421	4	9.35%	31.33
VIA-LAST						
Capacitance type	Capacitance Density (fF/μm^2)	Area penalty	Number of TSVs	Decoupling capacitance (nF)	Power loss (mW)	Peak-to-peak noise (mV)
Metal-oxide-semiconductor	39.35	1.54%	76	0.385	6.05%	134.72
Low density deep trench	140	1.21%	30	3.74	2.74%	134.67
High density deep trench	280	0.86%	30	3.74	2.74%	134.67

Table 4.1: Valid design points that satisfy the peak power supply noise while minimizing the area overhead for each TSV technology.

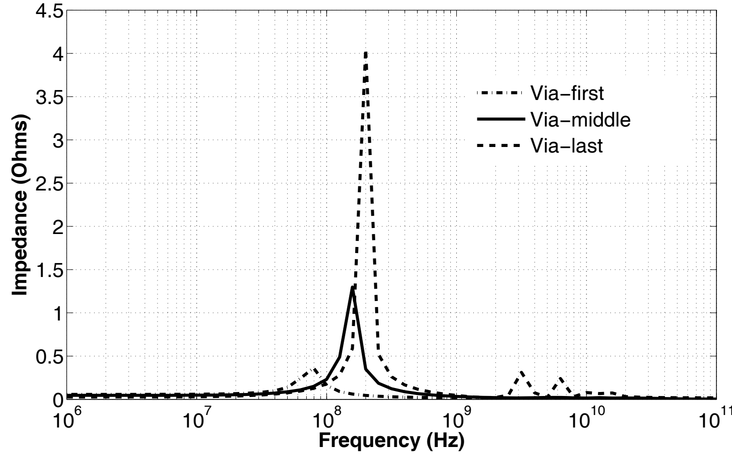

Figure 4.11: **Impedance characteristics at the design points listed in Table 4.1 when decoupling capacitance is implemented as MOS capacitors.**

4.3 AC Analysis Results

As described in the previous section, the peak noise is reduced by either increasing the number of TSVs or decoupling capacitance for both via-first and via-middle TSVs. Alternatively, for via-last TSVs, the noise exhibits a nonmonotonic relationship with these design parameters. A higher decoupling capacitance increases the damping factor, thereby reducing the peak-to-peak noise. Alternatively, the resonant frequency is shifted to lower frequencies as the decoupling capacitance increases. Thus, input independent AC analysis is useful to better understand the impedance characteristics of 3-D power distribution networks with different TSV technologies. Specifically, the impedance characteristics are investigated at the design points, as listed in Table 4.1. Note that at these design points, the power distribution network satisfies the peak noise in time domain and the area overhead is minimized, as described in the previous section. Since a separate set of design points exists depending upon the capacitance density, the impedance characteristics for both MOS capacitance and high density deep trench capacitance are investi-

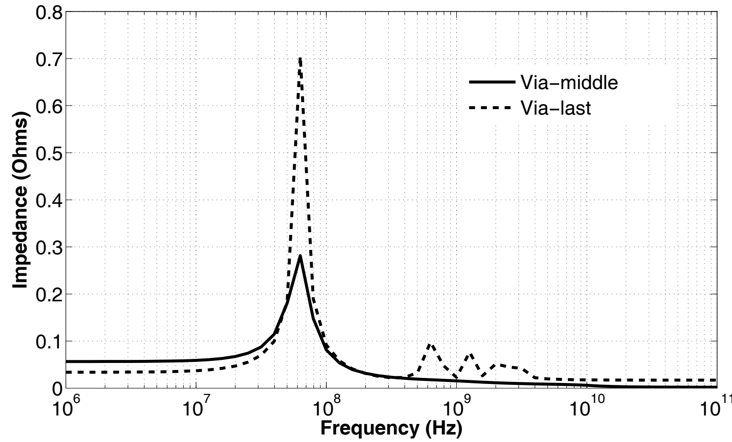

Figure 4.12: **Impedance characteristics at the design points listed in Table 4.1 when decoupling capacitance is implemented as MOS capacitors.**

gated, as illustrated, respectively, in Figs. 4.11 and Fig.4.12.

According to these figures, via-last based power networks exhibit lower impedance at relatively low frequencies. Resonance, however, is a critical issue due to a low damping factor. If a MOS capacitance is used as the decoupling capacitance, as depicted in Fig. 4.11, the minimum area is achieved at a relatively low decoupling capacitance and large number of TSVs (smaller equivalent TSV resistance). In this case, the impedance at the resonant frequency reaches 4 ohms. For a via-middle based power network, the peak impedance is less than 1.5 ohms. Alternatively, for a via-first based power network, the peak impedance is less than 0.5 ohms since high TSV resistance provides sufficient damping. Note that in a time domain analysis, the frequency is determined primarily by the rise time of the switching load. In a practical circuit, however, target impedance should be satisfied for a wide range of frequencies since the rise time varies.

In Fig. 4.12, the decoupling capacitance is implemented as a deep trench capacitance. Thus, the minimum area design point is achieved at a relatively high

decoupling capacitance and low number of TSVs. The damping factor is therefore higher and the impedance at the resonant frequency is reduced to 0.7 ohms for a via-last based power network and to 0.3 ohms for a via-middle based power network. It is therefore desirable to increase the amount of decoupling capacitance to avoid resonance even though the area overhead is not minimized. Also note that despite this reduction in the peak impedance, the resonant frequency is shifted to a lower frequency as the decoupling capacitance is increased. There is therefore a higher chance for the operating frequency to coincide with the resonant frequency. Thus, in this case, the peak impedance should be sufficiently low. Note that via-first technology is not included in Fig. 4.12 since deep trench capacitance is difficult to implement due to a low substrate thickness.

Chapter 5

Conclusion

Three different TSV technologies, via-first, via-middle, and via-last, have been evaluated to distribute power in a 32 nm 3-D system with eight memory planes and one processor plane. An electrical model has been developed that consists of power/ground TSVs, power distribution network within each plane, substrate, and the switching circuit. Different design requirements are identified for each TSV technology. A valid design space that satisfies power supply noise and minimizes physical area is determined. It is demonstrated that highly resistive via-first TSVs can be used to deliver power at the expense of approximately 9% area overhead as compared to less than 2% area overhead in via-middle and via-last technologies. Despite this higher area requirement, a power distribution network with via-first TSVs is typically overdamped and the issue of resonance is alleviated. Alternatively, for via-middle and via-last TSV technologies, the impedance at the resonant frequency should be sufficiently small. This issue is exacerbated for a via-last based power distribution network since the TSV resistance is significantly lower, and therefore the network is typically underdamped. Furthermore, the peak noise exhibits high sensitivity to number of TSVs and decoupling capacitance. Thus,

these design parameters should be carefully chosen in a via-last based power distribution network.

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