Stony Brook University

Design of Low Power Adaptive Continuous-Time Filter

A Thesis Presented

By

Yi Huang

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Abstract of the Thesis

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In this thesis, nonlinearity cancellation, low power and adaptive technologies are studied. Based on the theory and some simulation of the technology, a linear OTA is presented which has performed a good linearity in the range between -250mV and 250mV. The linear range of this OTA makes it qualify for the design of BandPass Gm-C Filter. A Charge Sensitive System whose purpose is to detect the small input signal by measuring the peak value of the output signal is built by connecting the BandPass Filter to a Charge Sensitive Amplifier. The BandPass Filter is designed properly to fulfill the linear relationship between the input signal and the peak value of output signal. Simulations in MATLAB/SIMULINK and CADENCE have proved the correction of the design.

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List of Symbols

Symbols	Description
q	Elementary charge
$U_T = (k \cdot T) / q$	Thermodynamic voltage
n_i	Intrinsic carrier concentration of Si
$\varepsilon_s, \varepsilon_{ox}$	Dielectric constant of Si and SiO2
$C'_{ox} = \varepsilon_{ox} / t_{ox}$	Gate Oxide capacitance per unit area
N_{SUB}	Doping concentration of substrate
$\phi_F = U_T \bullet \ln(N_{sub} / n_i)$	Fermi potential in the substrate
V_{FB}	Flat-band voltage
$\psi, \psi_s = \psi(y = 0)$	Electrostatic potential and surface potential
$V_{ch} = \phi_n - \phi_p = \phi_n - \phi_F$	Channel potential
Q'_{inv}	Mobile inversion charge per unit area
μ_n	Mobility of electrons in the channel
ID	MOSFET Drain Current
VGS	Gate-Source Voltage of MOSFET
VDS	Drain-Source Voltage of MOSFET

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Introduction

1.1 Introduction to the MOSFET and CMOS Technology

Nowadays, the metal oxide semiconductor field effect transistor (MOSFET) has been the main components in the semiconductor industry both in analog and digital integrated circuits.

Compared to the traditional components of semiconductor industry, the Bipolar Junction Transistor (BJT), MOS FET has some significant advantages. In high power circuits, MOSFETs sometimes have the advantage of not suffering from thermal runaway as BJTs do. Also, they can be formed into capacitors and gyrator circuits which allow Op Amps made from them to appear as inductors, thereby allowing most of the normal analog devices to be built entirely out of MOSFETs. This allows for complete analog circuits to be made on a silicon chip in a much smaller space.

As the increasing requirement of the electronic product, the criteria of the circuits' low power and high integration is higher and higher. In the application of VLSI circuits, CMOS technology has been widely used considering it provides the new method of solving the issues of the low power and high integration. The CMOS circuits consist of PMOS and NMOS, which leads to the characteristic of low power, high output swing, high input impedance, high integration, small area and so on.

In this thesis, the CMOS is the very technology in implementation

everything from the Operational Transconductance Amplifier (OTA) to the Charge Sensitive System.

1.1.1 Large and Small Signal Model of the MOSFET

1.1.1.1 Large Signal Model of the MOSFET

When the MOSFET works in DC level, its working principle can be decrypted by the large signal model. Take NMOS transistor for example, its V-I characteristic is

$$\begin{cases} I_D = \dfrac{K'W}{L}[(V_{GS} - V_T) - \dfrac{V_{DS}}{2}]V_{DS} & V_{DS} > V_T \\ I_D = 0 & V_{DS} < V \end{cases} \tag{1.1}$$

where I_D is the drain current and I_G (the gate current) is 0. V_{GS} is gate-source voltage while V_{DS} is the drain-source voltage. W, L are the width and length of the channel. K' is the transconductance constant and V_T is the threshold voltage.

For V_T, it has

$$V_T = V_{T0} \pm \gamma(\sqrt{\phi + |V_{BS}|} - \sqrt{\phi}) \tag{1.2}$$

The threshold voltage of NMOS is positive while the counterpart of PMOS is negative. V_{T0} is the threshold voltage when V_{BS} is 0 and gamma is body effect coefficient whose normal value is 0.3~0.7.

In most analog design, the large signal includes three working regions:

A. Cut-off region

In the hand calculation, analog designers always assume:

$$I_D = 0 \qquad V_{GS} < V_T \tag{1.3}$$

Actually, in this region the drain current still exists and its theory—weak inversion and moderate inversion, will be introduced in the following chapters.

B. Triode Region

In this region, the expressions are

$$I_D = \frac{K'W}{L}(V_{GS} - V_T)V_{DS} \qquad V_{GS} > V_T, V_{DS} < (V_{GS} - V_T) \tag{1.4}$$

And from (1.4) it is known that drain current has a linear relationship with drain-source voltage, this relationship can be expressed by an equivalent resistance

$$\mathrm{R}\,on = \frac{V_{DS}}{I_D} = \frac{L}{K'W(V_{GS} - V_T)} \tag{1.5}$$

In this region, the value of the resistance can be revised by changing the value of V_{GS}.

C. Saturation Region

In the saturation region, the gate-source voltage is bigger than the threshold voltage and the critical value of the drain current is

$$I_D = \frac{K'W}{2L}(V_{GS} - V_T)^2 \tag{1.6}$$

In the saturation region, the drain current almost does not change when the drain-source voltage increases. As a result, (1.6) is used as the most popular equations in analog design as a good approximation.

When the channel-length modulation effect is considered, the current can be revised as

$$I_D = \frac{K'W}{2L}(V_{GS} - V_T)^2(1 + |\lambda V_{DS}|) \tag{1.7}$$

where lambda is the channel length modulation coefficient.

Figure1.1 expresses the I-V relationship in these three regions

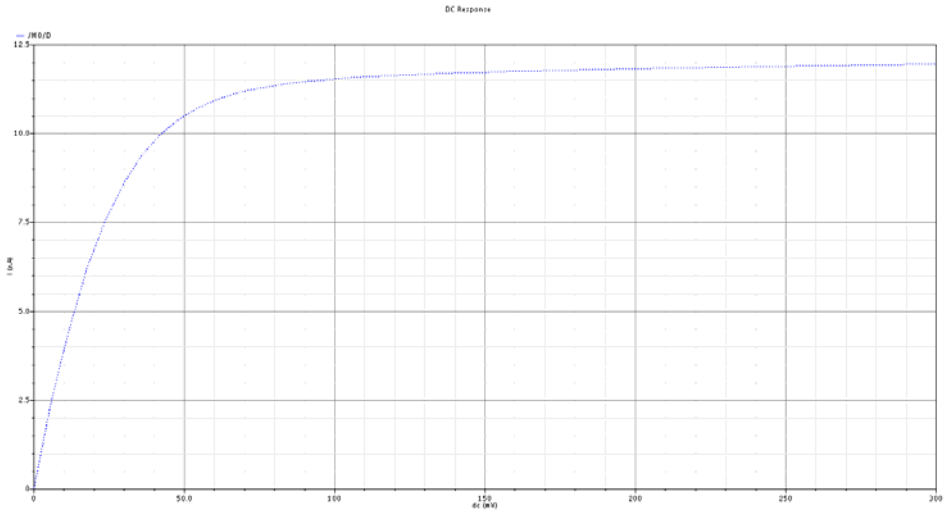


Figure 1.1 The relationship between drain current and gate-source voltage

The ideal large signal MOSFET model is just like figure1.2. The input impedance is treated as infinite and the drain terminal is a voltage-control voltage course (VCVS).

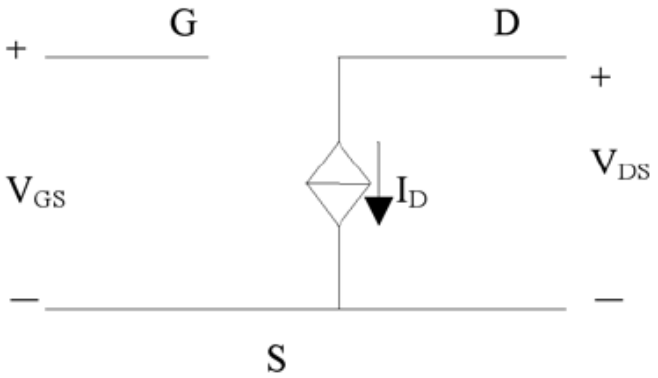


Figure 1.2 The ideal large signal model of MOSFET

1.1.1.2 Small Signal Model of the MOSFET

When the amplitude of the input signal is very small compared to the

power supply, which means that it works around the DC bias point, the MOSFET can be treated as working in the linear region of DC level. Small signal model is used to design the performance of the device and the circuits while the large signal model is employed to fix the DC operating point. For NMOS, the ransconductance and the output resistance can be derived from the I-V characteristic

$$g_m = \frac{\partial I_D}{\partial V_{GS}}\bigg|_Q = \frac{K'W}{L}(V_{GS} - V_T)(1+\lambda V_{DS})\bigg|_Q = [2\frac{K'W}{L} I_D(1+\lambda V_{DS})]^{1/2}\bigg|_Q \tag{1.8}$$

$$r_o = \frac{1}{g_{ds}} = \frac{1}{(\frac{\partial I_D}{\partial V_{DS}}\Big|_Q)} = \frac{1+\lambda V_{DS}}{\lambda I_D}\bigg|_Q \tag{1.9}$$

C_{GS}, C_{GD} and C_{DS} are the parasitic capacitance of the gate-source, gate-drain and drain-source. Hence the saturation AC small signal model can be drawn in Figure 1.3.

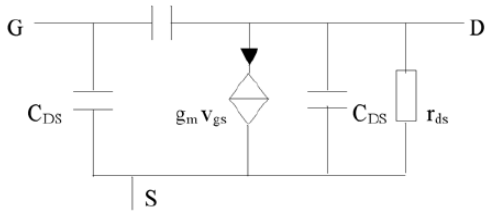


Figure 1.3 Small signal model of the MOSFET

When the circuit operates in low frequency, these capacitors can be ignored and the model can be simplified to figure 1.4.

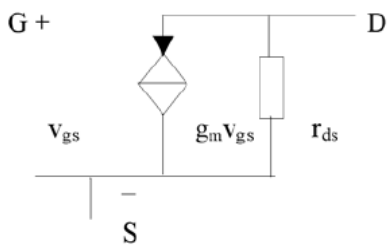


Figure 1.4 Simplified small signal model

1.1.2 Working Regions of the MOS Transistor

In the 1.1.1.1, the brief introduction of the working regions is presented based on the circuit level. In this part, some more detailed information is given from the physical perspective. The regions are named weak inversion, moderated inversion and strong inversion.

In the past few years, many people have made some contribution to the research in this field. In [85], Enz has provided a complete model in these three regions, which is mainly used in today's analog design.

In the discussion of this part, the parameters are defined in table1.1.

Symbols	Description	Units
q	Elementary charge	$A \bullet s$
$U_T = (k \cdot T)/q$	Thermodynamic voltage	V
n_i	Intrinsic carrier concentration of Si	m^{-3}
$\varepsilon_s, \varepsilon_{ox}$	Dielectric constant of Si and SiO2	F/m
$C_{ox}^{'} = \varepsilon_{ox}/t_{ox}$	Gate Oxide capacitance per unit area	F/m^2
N_{SUB}	Doping concentration of substrate	m^{-3}
$\phi_F = U_T \bullet \ln(N_{sub}/n_i)$	Fermi potential in the substrate	V
V_{FB}	Flat-band voltage	V
$\psi, \psi_s = \psi(y=0)$	Electrostatic potential and surface potential	V

$V_{ch} = \phi_n - \phi_p = \phi_n - \phi_F$	Channel potential	V
$Q_{inv}^{'}$	Mobile inversion charge per unit area	$(A \bullet s) / m^2$
μ_n	Mobility of electrons in the channel	$m^2 / (A \bullet s)$

Table 1.1 Definition used in the model

1.1.2.1 Strong Inversion Theory

Strong inversion is in the region above threshold and it is the most popularly used region in most cases of the circuit configuration.

A. Inversion Charge of Large Signal Model

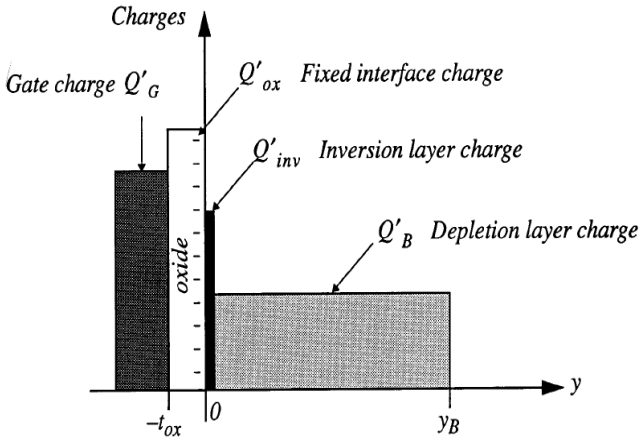


Figure 1.5 Charges appearing across the MOS Structure

The different charges appearing across the MOS structure are represented in Figure1.5. From the discussion in [85], the final equation presented is:

$$Q_{inv}^{'} \cong \frac{\partial Q_{inv}^{'}}{\partial V_{ch}}\bigg|_{V_{ch}=V_p} \bullet (V_{ch} - V_p) = -C_{ox}^{'} \bullet n \bullet (V_p - V_{ch}) \tag{1.10}$$

B. Modes of Operation of Large Signal Model

The difference modes of operation of the MOS transistor can be defined according to the source and drain voltages with respect to the pinch-off voltage, as Figure 1.6

Symmetrical forward and reverse modes are possible, de-pending on the sign of VD-VS. For VS and VD both smaller than Vp, the channel is in strong inversion from the source to the drain and the transistor is in the conduction mode.

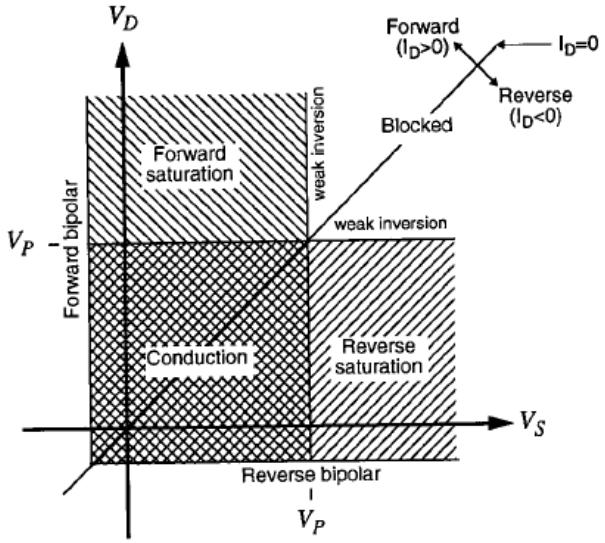


Figure 1.6 Modes of operation of the transistor

C. General Expression of the Drain Current of Large Signal Model

A general expression for the drain current that includes both the diffusion and the drift mechanism is given by:

$$I_D = W \bullet \mu_n \bullet (-Q'_{inv}) \bullet \frac{dV_{ch}}{dx} \tag{1.11}$$

The drain current can be decomposed into a forward current IF which depends on the difference Vp-Vs and a reverse current IR which depends only on Vp-VD.

After the integration of (1.10), the expression of the drain current in strong inversion is obtained:

$$I_F = \begin{cases} \frac{n \bullet \beta}{2} \bullet (V_P - V_S)^2, \ for: V_S < V_P \\ 0, \ for: V_S \geq V_P \end{cases} \tag{1.12}$$

$$I_R = \begin{cases} \frac{n \bullet \beta}{2} \bullet (V_P - V_D)^2, \; for: V_D < V_P \\ 0, \; for: V_D \geq V_P \end{cases} \tag{1.13}$$

In table 1.2 the characteristic of the drain current in strong inversion is collected.

Mode	Strong Inversion
Conduction	$n \bullet \beta \bullet [V_P - \frac{V_S + V_D}{2}] \bullet (V_D - V_S), \; for \begin{cases} V_S \leq V_P \\ V_D \leq V_P \end{cases}$
Forward Saturation	$\frac{n \bullet \beta}{2} \bullet (V_P - V_S)^2, \; for: \begin{cases} V_S < V_P \\ V_D > V_P \end{cases}$
Blocked	$0, \; for \begin{cases} V_S > V_P \\ V_D > V_P \end{cases}$

Table 1.2 Drain current in strong inversion

D. Transconductance of Small Signal Model

g_{mg} , g_{ms} and g_{md} can be used as the gate, source and drain transconductance.

Considering that:

$$\begin{aligned} g_m &\equiv \frac{\partial I_D}{\partial V_{GS}}|_{V_{BS}, V_{DS}} = g_{mg} \\ g_{mb} &\equiv \frac{\partial I_D}{\partial V_{BS}}|_{V_{GS}, V_{DS}} = g_{ms} - g_{mg} - g_{md} \\ g_{ds} &\equiv \frac{\partial I_D}{\partial V_{DS}}|_{V_{BS}, V_{GS}} = g_{md} \end{aligned} \tag{1.14}$$

From (1.13) and (1.14) the transconductance can be obtained

	Conduction	Forward Saturation
g_{mg}	$g_{mg} = \beta \bullet (V_P - V_S) = \sqrt{\frac{2\beta \bullet I_F}{n}}$	$\frac{I_D}{N \bullet U_T}$

g_{ms}	$n \bullet \beta \bullet (V_P - V_S) = \sqrt{2 \bullet N \bullet \beta \bullet I_F}$	$n \bullet \beta \bullet (V_P - V_S) = \sqrt{2 \bullet N \bullet \beta \bullet I_F}$
g_{md}	$n \bullet \beta \bullet (V_P - V_D) = \sqrt{2 \bullet N \bullet \beta \bullet I_R}$	

Table 1.3 Drain current in strong inversion

E. Intrinsic Capacitance of Small Signal Model

Using Quasi-Static Model, the intrinsic capacitance in strong inversion can be obtained:

$$C_{gs} = C_{ox} \bullet \frac{2}{3} \bullet [1 - \frac{i_r}{(\sqrt{i_f} + \sqrt{i_r})^2}] \tag{1.15}$$

$$C_{gd} = C_{ox} \bullet \frac{2}{3} \bullet [1 - \frac{i_f}{(\sqrt{i_f} + \sqrt{i_r})^2}] \tag{1.16}$$

$$C_{gb} = C_{ox} \bullet \frac{n-1}{3 \bullet n} \bullet [1 - \frac{4 \bullet \sqrt{i_f \bullet i_r}}{(\sqrt{i_f} + \sqrt{i_r})^2}] \tag{1.17}$$

1.1.2.2 Weak Inversion Theory

A. Inverison Charges of Large Signal Model

From the figure1.5 and the research in [85], a simplified expression of the inversion charge is given:

$$Q_{inv}^{'} \cong -C_{ox}^{'} \bullet \frac{\gamma}{2 \bullet \sqrt{\psi_s}} \bullet U_T \bullet e^{\frac{\psi_s - 2\phi_F - V_{ch}}{U_T}} \tag{1.18}$$

B. Modes of Operation of Large Signal Model

From the figure1.6 and the research in [85], if VS and VD are both larger than VP, the whole channel is pinch-off. The device operates in weak inversion as long as one of the source or drain voltage is still close to VP, but becomes blocked if both of them are

sufficiently larger than V_P.

C. Drain Current of Large Signal Model

Similar to the discussion in strong inversion, the expression of the drain current in weak inversion is

$$I_F = K_\omega \bullet \beta \bullet U_T^2 \bullet e^{\frac{V_P - V_S}{U_T}} \tag{1.19}$$

$$I_R = K_\omega \bullet \beta \bullet U_T^2 \bullet e^{\frac{V_P - V_D}{U_T}} \tag{1.20}$$

Mode	Weak Inversion
Conduction	$K_\omega \bullet \beta \bullet U_T^2 \bullet e^{\frac{V_P}{U_T}} \bullet [e^{-\frac{V_S}{U_T}} - e^{\frac{V_D}{U_T}}],\ for \begin{cases} V_S > V_P \\ V_D > V_P \\ V_S \cong V_D \end{cases}$
Forward Saturation	$K_\omega \bullet \beta \bullet U_T^2 \bullet e^{\frac{V_P - V_S}{U_T}},\ for: \begin{cases} V_S > V_P \\ V_D > V_P \\ V_D - V_S \gg U_T \end{cases}$
Blocked	$0,\ for \begin{cases} V_S \gg V_P \\ V_D \gg V_P \end{cases} or, V_S = V_D$

Table 1.4 Drain Current in weak inversion

D. Transconductance of Small Signal Model

Like the discussion in strong inversion, the expression of the transconductance of weak inversion can be obtained as:

$$\begin{aligned} g_{ms} &= \frac{I_F}{U_T} \\ g_{md} &= \frac{I_R}{U_T} \end{aligned} \tag{1.21}$$

E. Intrinsic Capacitance of Small Signal Model

Using Quasi-Static Model, the intrinsic capacitance in weak inversion can be obtained:

$$C_{gs} = C_{ox} \bullet i_f \tag{1.22}$$

$$C_{gd} = C_{ox} \bullet i_r \tag{1.23}$$

$$C_{gb} = \frac{n}{n-1} \bullet C_{ox} \tag{1.24}$$

1.1.2.3 Moderate Inversion Theory

The discussion on the moderate inversion focuses on the drain current of the region. Expression for the drain current have been derived in the asymptotic models of operation defined as weak and strong inversion, but they are not valid in the moderate inversion region. As a result, the expressions which define the characteristic of the moderate inversion are needed.

The normalized current in weak inversion and in strong inversion can be expressed as:

$$i_d \equiv \frac{I_D}{I_S} = i_f - i_r = F(v_p - v_s) - F(v_p - v_d) \tag{1.25}$$

Where $i_f \equiv I_F / I_S$ is the forward normalized current which is also defined as the inversion coefficient and $i_r \equiv I_R / I_S$ is the reverse normalized current. Function $F(v)$ is the interpolation function, which should have the following asymptotes:

$$F(v) = \begin{cases} (\frac{v}{2})^2, \; for: v \gg 0 \\ e^v, \; for: v \le 0 \end{cases} \tag{1.26}$$

A good and simple interpolation has been simplified in order to remove the additional coefficients:

$$F(v) = [\ln(1 + e^{v/2})]^2 \tag{1.27}$$

The forward and reverse normalized currents are then given by:

$$i_f = F(v_p - v_s) = [\ln(1 + e^{\frac{v_p - v_s}{2}})]^2$$
$$i_r = F(v_p - v_d) = [\ln(1 + e^{\frac{v_p - v_d}{2}})]^2 \quad (1.28)$$

These functions can be conveniently inverted to express the voltage in terms of the forward or reverse currents as it is generally required in analog circuit design:

$$v_p - v_s = 2\ln(e^{\sqrt{i_f}} - 1)$$
$$v_p - v_d = 2\ln(e^{\sqrt{i_r}} - 1) \quad (1.29)$$

1.2 Introduction to the Continuous Time Analog Filter

In circuit theory, a filter is an electrical network that alters the amplitude and/or phase characteristics of a signal with respect to frequency. Figure 1.7 gives out an overview of how the filters work.

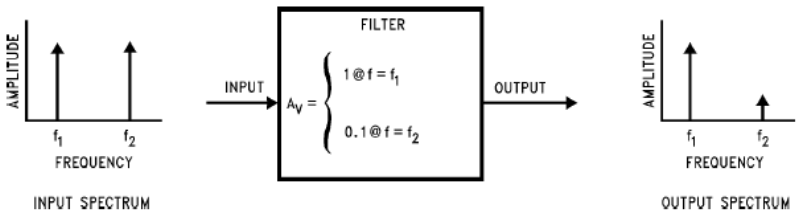


Figure1.7 The operation of the filter

1.2.1 RLC Filter

RLC Filter is the passive analog filter. It includes RC circuit, RL circuit, LC circuit and RLC circuit. Figure 1.7 is an example of the classic RLC Filter.

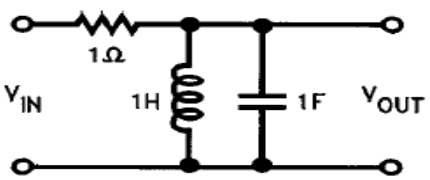


Figure1.8 RLC Filter

The passive filters have some advantages. It is the simplest (in terms of the number of necessary components) implementation of a given transfer function. Passive filters have other advantages as well. Because they have no active components, passive filters require no power supplies. Since they are not restricted by the bandwidth limitations of op amps, they can work well at very high frequencies. They can be used in applications involving larger current or voltage levels than can be handled by active devices. Passive filters also generate little noise when compared with circuits using active gain elements. The noise that they produce is simply the thermal noise from the resistive components, and, with careful design, the amplitude of this noise can be very low.

However, it also has some shortcomings. Since they use no active elements, they cannot provide signal gain. Input impedances can be lower than desirable, and output impedances can be higher the optimum for some applications, so buffer amplifiers may be needed. Inductors are necessary for the synthesis of most useful passive filter characteristics, and these can be prohibitively expensive if high accuracy (1% or 2%, for example), small physical size, or large value are required. Standard values of inductors are not very closely spaced, and it is difficult to find an off-the-shelf unit within 10% of any arbitrary value, so adjustable inductors are often used. Tuning these to the required values is time-consuming and expensive when producing large quantities of filters. Furthermore, complex passive filters (higher than 2nd-order) can be difficult and time-consuming to design.

1.2.2 OP AMP RC Filter

Op Amp RC Filter first emerged in 1940's as the Active RC filter. Resistors and capacitors locate in the feed back loop of the operational amplifier.

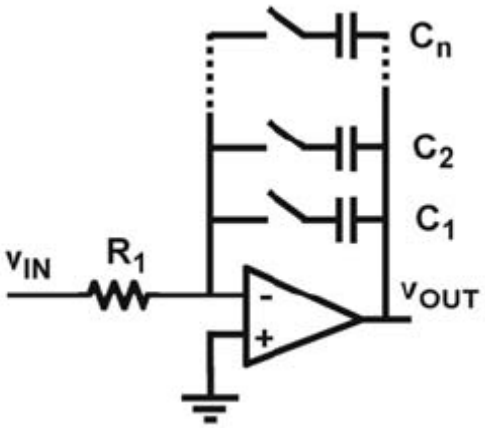


Figure1.9 Op Amp RC Filter

The OP AMP RC Filter has some advantages. If a low-noise Op Amp is used, large Signal-to-Noise ratios (SNR) can also be achieved, large input signals can be applied with very little distortion. The Signal-to-Noise-and Distortion ratio (SNDR) can also be fairly high. Actually, this filter is capable of the highest SNDR values possible, depending on the power consumption.

However, this is obviously only correct for the frequencies where the loop gain is high. So the OP AMP RC filters are not suitable for high frequencies. That is one of its disadvantages.

Another disadvantage is that passive components are used, which usually have a low absolute accuracies. The absolute errors can be as high as 15 ... 20%. People will therefore need to tune the filter sections. However, in such an OTA-RC filter no component can be tuned. The only way out is to use resistor or capacitor banks, as shown in figure 1.9. For an 8-bitbinary bank of capacitances, the absolute error can be

reduced to 0.4%.

1.2.3 MOSFET-C Filter

For MOSFET-C filter, the triode region MOSFETs are used as well as Op Amp and capacitors. Figure 1.10 is a sketch map of this kind of filter.

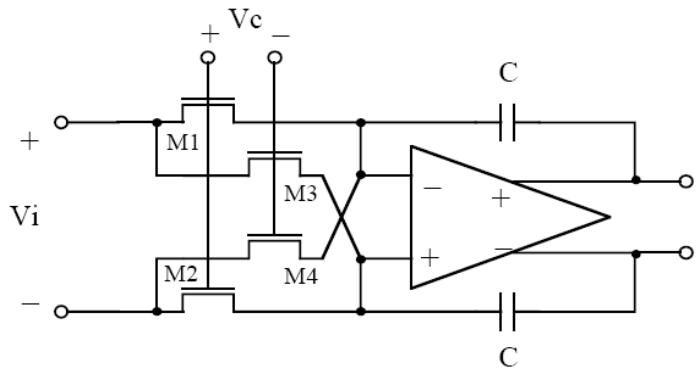


Figure 1.10 MOSFET-C filter

Several nonlinearity cancellation technologies can be used in order to improve the high linearity. Considering all the MOS transistors work in triode region, this configuration has a counterpart of Op Amp RC filter.

The advantage of this structure over its counterpart is that tuning of the resistors is possible through the gate voltages of the transistors and hence tuning of the filter frequency. As a result, the drawback from the Op Amp RC filters can be avoided in some degree. However, a large tuning range also requires a large Voltage range, which may not be easy at low supply voltages. Moreover, MOSFETs have a limited frequency range of operation.

1.2.4 The Transconductance-Capacitor Filter (Gm-C or OTA-C Filter)

Gm-C filter is one of the most important continuous time filters. And there are

several advantages in using the Gm-C filters as compared to some other counterparts such as Op Amp RC Filters.

A. Gm-C filter has much higher frequency ranged. The highest frequency can be made to hundreds of MHz.
B. Gm-C filter can be fabricated in the same semiconductor chip with the digital signal processing circuits. As a result, a hybrid signal processing system can be truly produced on one integrated system, which greatly reduces the cost and size as well as increases the reliability of the hardware.
C. A Gm-C filter is tunable simply by changing the DC bias current, which in turn changes gm. This advantage is hard to realize for other kinds of the filters.

The workhorse of the Gm-C filter is the Operational Transconductance Amplifier (OTA). Generally speaking, OTA is a linear Voltage Control Current Source. Recently, the OTA is used more and more widely in both linear and nonlinear applications. There are two kinds of OTA: the bipolar junction OTA and the CMOS OTA. Compared to the BJT one, the CMOS OTA has a lower gain and narrower tuning range. However, it has high input impedance and low power dissipation, which leads it easy to be fabricated with other parts of the circuits to a fully CMOS integration system.

1.3 The significance of the research of this thesis

In this thesis, based on the research of the linear technology, adaptive technology and low power technology, a cross coupled fully differential OTA is designed whose

linear range is between -0.3V and 0.3V. This OTA is employed in the BandPass filter which plays a key role in the charge sensitive system. The small signal at the input of the system can be detected through the charge sensitive amplifier as well as the BandPass filter. The significance of the thesis is the integration of the three technologies in the same component and it is a good implementation of CMOS technology in signal detection area.

2. Technology of Linearity, Low Power and Adaptive

In these two decades, the Operational Transconductance Amplifier (OTA) has been developed fully under the contribution of a large number of analog designers. As one of the most important components in analog integrated circuits, OTA has been widely used in filter design, ADC and DAC. Thousands of people devote themselves to improving the performance of it, during which several novel technologies are invented. Between these ones, the linearity technology, low power technology and adaptive technology are very significant.

2.1 Linearity Technology

Basically, the modern technology of the linearity includes three main subjects, the nonlinearity cancelation, the float gate and the bulk driven technology. In the following, several different configurations of the circuits are presented as the samples.

2.1.1 Nonlinearity Cancellation

In the following, a number of topologies are introduced. Some of them also employs the weak inversion transistors which help them to achieve the low power goal.

A. In figure 2.1 [41], a linear OTA is presented. The transconductance, gm, defined as Iout/(Vin+-Vin-), is proportional to the bias current, Ibias, which has an exponential dependence on the gate voltage for an MOS transistor operating in the subthreshold region. It is a single-stage amplifier with a dominant pole set by its transconductance

and the load capacitance. It has a linear range of approximately 150 mV at room temperature with differential pairs of conventional configuration. When the OTA is connected as a follower, the distortion is minimal, but in other configurations, such as in high-dc, second-order filters, the nonlinear transconductance may present some stability problems.

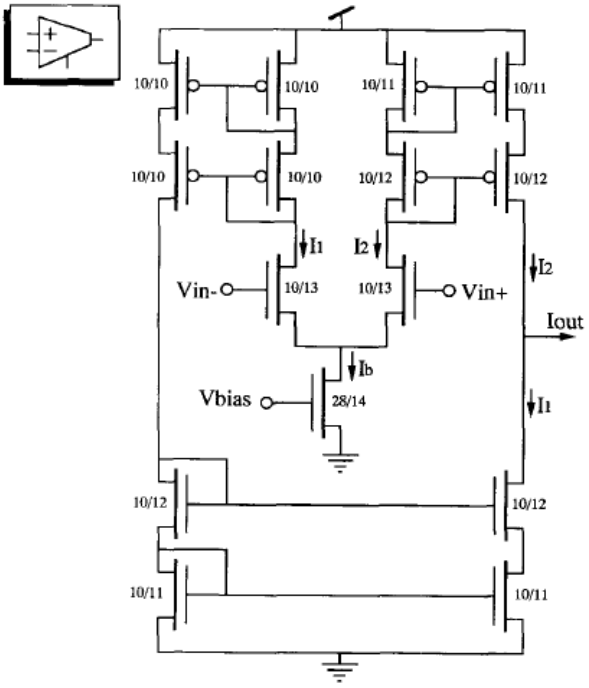


Figure 2.1 linear OTA1

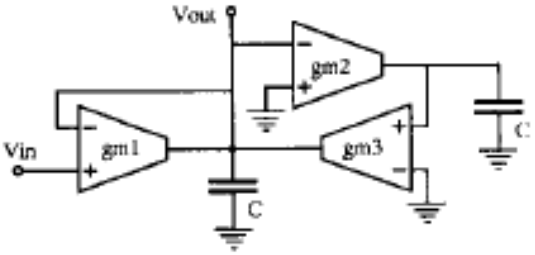


Figure 2.2 Second-order Gm-C BandPass filter

The BandPass characteristic is expressed in (2.1)

$$H_{BP}(s) = \frac{\frac{\omega_0}{Q_3} s}{s^2 + \frac{\omega_0}{Q3} s + \omega_0^2} \tag{2.1}$$

B. A linear OTA is presented in figure 2.3[3][10], in this OTA, the input differential

pair is in the weak inversion with diode-connected transistors loads, and current mirrors to provide either a source or sink current to the integrating capacitance.

Any mismatch in the input differential pair or current mirrors will give a mismatch in the transconductor output currents. Since the output is high impedance this difference in the current flowing through the n and the p devices can cause a large variation of the operating point at the output. So a Common Mode Control Circuit is needed (figure2.4). The double differential pair in the following senses this effect.

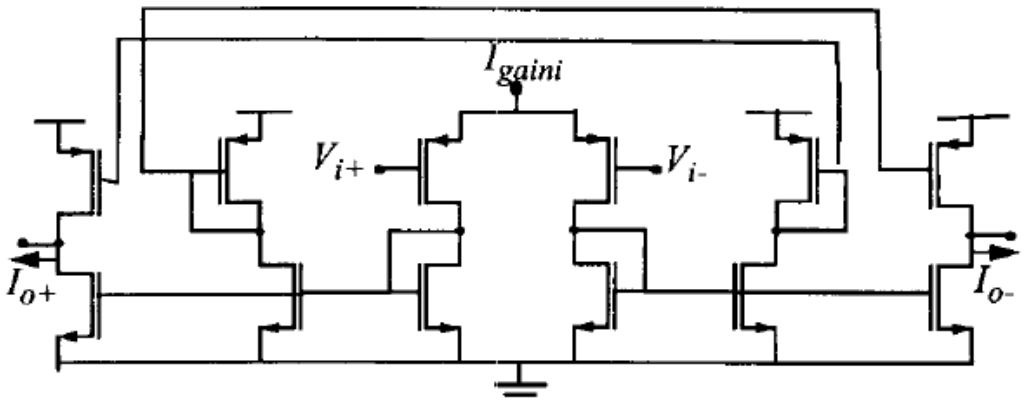


Figure 2.3 linear OTA2

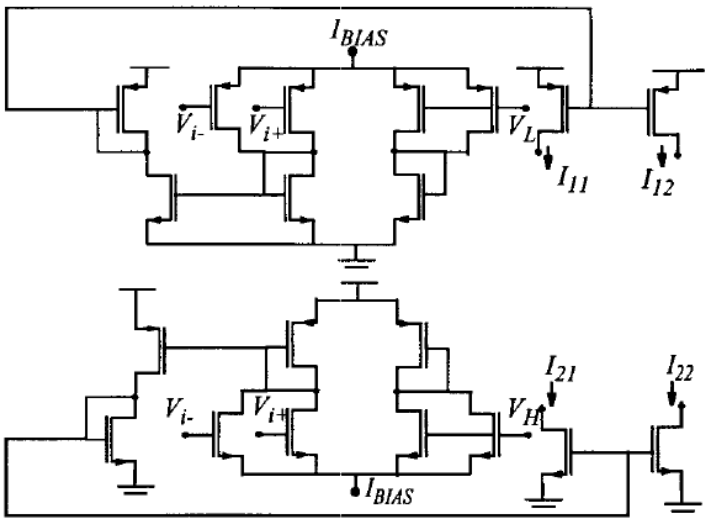


Figure 2.4 The Common Mode Control Circuit of OTA2

C． In figure 2.5[7], a linear OTA is presented. In order to minimize the harmonic distortion components, the OTA is based on a triode biased transistor, MR, with

saturation voltage of 0.25 V. The drain current of MR is divided by MM, M1 and MN; transistor MM is designed wider than M1 and MN. Therefore, most of the ac current flows to ground through transistors MM

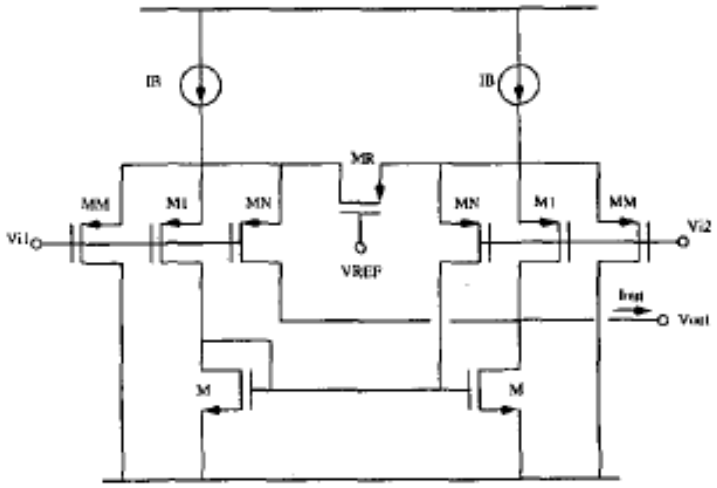


Figure 2.5 linear OTA3

D. In figure 2.6[12], a linear OTA is presented. Transistors M1and Ml', biased by current sources M3 and M3', form the input differential pair, the transfer characteristic of which is linearized by the voltage-controlled degenerating "resistors" M2 and M2'. The common-mode output voltage is stabilized by M5 and M5', which operate in the triode region.

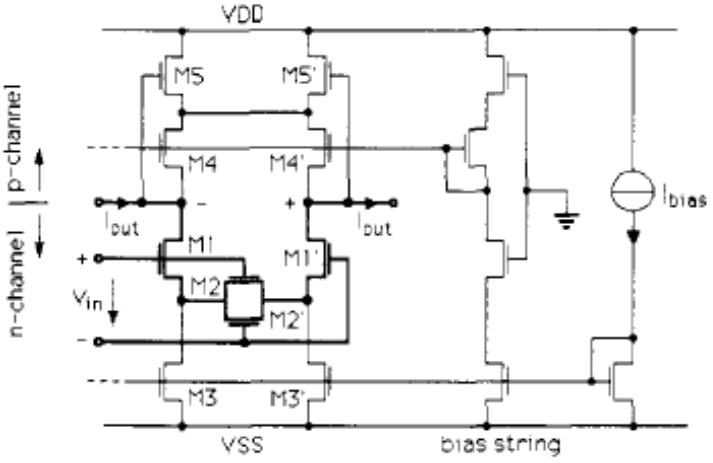


Figure2.6 linear OTA4

E. In figure 2.7[19], the technique uses three MOS transistors Ml-M2-M3 operating in their linear regions. The large signal transconductance Gm of the integrator can be tuned by the control voltages Vcl and Vc2 at the gates of the three transistors. By choosing W/L(M2,M3) =2WJL(Ml), it can be calculated that the Gm is linearly proportional to the differential control voltage as given by:

$$Gm = \frac{1}{R}\left(\frac{1}{2} + \frac{V_{cd}}{V_{cm} - V_T - V_A}\right) \tag{2.2}$$

where Vcm = (Vcl+Vc2)/2, Vcd = Vc1-Vc2 represents the common-mode and differential control voltage, respectively, VT is the threshold voltage and V, is the dc bias voltage at the node A.

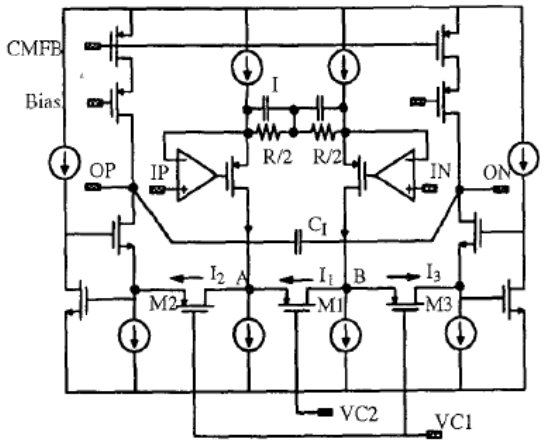


Figure 2.7 linear OTA5

F. In figure 2.8 and figure 2.9 [23], in order to achieve a very small transconductance, a chain of gm-l/gm stages were cascaded. In the design of the integrator, each g, stage was realized by a simple CMOS OTA with PMOS inputs and each l/gm stage by a diode-connected NMOS transistor, all stages biased to operate in weak inversion. A total of three g, and two l/gm, stages were cascaded. The input transistors are to be kept in weak inversion in figure 2.8.

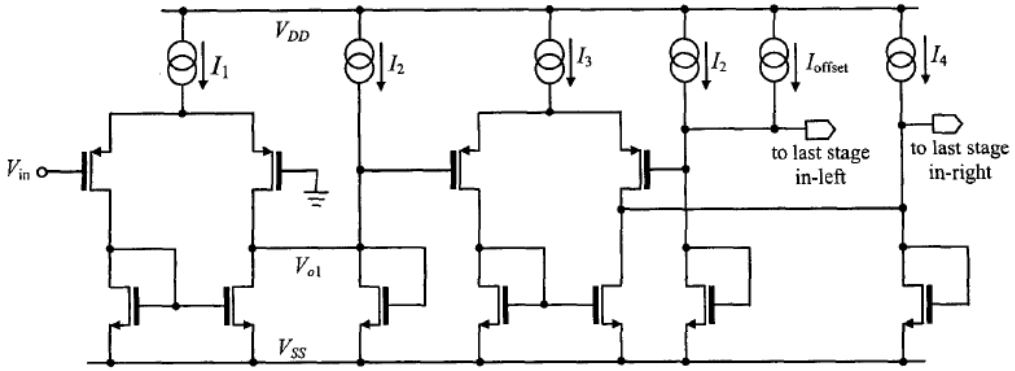


Figure 2.8 linear OTA6, the first four stages of the gm-1/gm chain

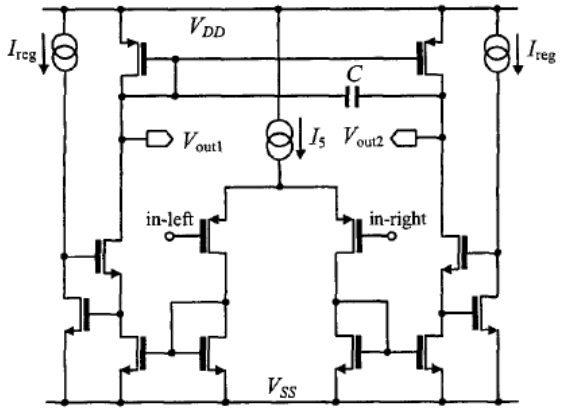


Figure 2.9 Linear OTA6, the last stage of the gm-1/gm chain

Some other topologies of the linear OTA can be found in the following publications:[4], [6], [13], [16], [22], [28],[29], [31], [32], [34], [35], [37], [40], [42], [43], [45] and [69].

2.1.2 Floating Gate Technology

The floating gate transistor is a kind of transistor that is commonly used for non-volatile storage such as flash, EPROM and EEPROM memory. Floating-gate transistors are almost always floating-gate MOSFETs. Floating-gate MOSFETs are useful because of their ability to store an electrical charge for extended periods of time even without a connection to a power supply. Floating-gate MOSFETs are composed of a normal MOSFET and one or more capacitors used to couple control

voltages to the floating gate. Oxide surrounds the floating gate entirely, so charge trapped on the floating gate remains there. The charge stored on the floating gate can be modified by applying voltages to the source, drain, body and control gate terminals (since we have Vfg=Ccg/CT*Vcg+Cs/CT*Vs+Cd/CT*Vd+Cb/CT*Vb) such that the fields result in phenomena like Fowler-Nordheim tunneling and hot carrier injection. Floating Gate Technology is also used as an important part of the linearity technology while sometimes it is combined with weak inversion techniques.

A. In figure2.10 [5], the FGMOS OTA is presented and the Gm-C filter (figure2.11) is shown as well as its performance. This case is a good application of the FGMOS OTA in the linearity technology.

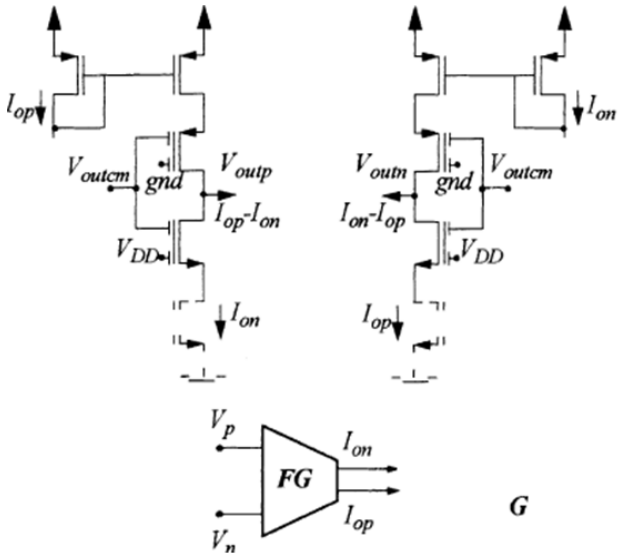


Figure 2.10 FGMOS OTA1

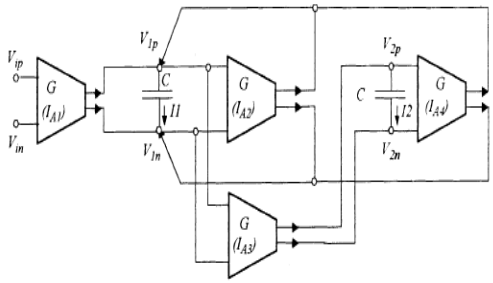


Figure2.11 FGMOS Gm-C filter

Maximal THD (Vpp<1V@200Hz, Q=1,HLP(0)=1,f0=900Hz)	<-40dB
IM3 (Vpp1=Vpp2<0.5V@200Hz, Q=1,HLP(0)=1,f0=900Hz)	<-40dB

Table 2.1 Performance of the FGMOS OTA in linearity

B. In figure 2.12[21], FGMOS technology is used as well as the nonlinearity cancellation technology.

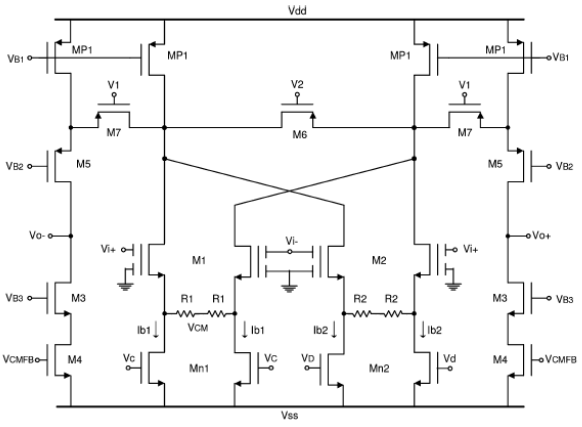


Figure2.12 FGMOS OTA2

In [21], it is seen that the Gm-C filter consisting of this kind of OTA also has good linearity. Another kind of structure of the FGMOS OTA is shown in [33].

2.1.3. Bulk Driven Technology

As the development of CMOS techniques, more and more methods are under the experiments to pursue the high performance of the semiconductor circuits. Bulk Driven technology, which is called body driven too, is invented. In this technology, the input voltage will be biased on the bulk terminal, which is different from the traditional topology. And from the previous research, this technology also makes contribution to the linearity improvement.

In figure2.13 [11], a bulk driven OTA is presented and its Gm-C filter is shown in Figure2.14

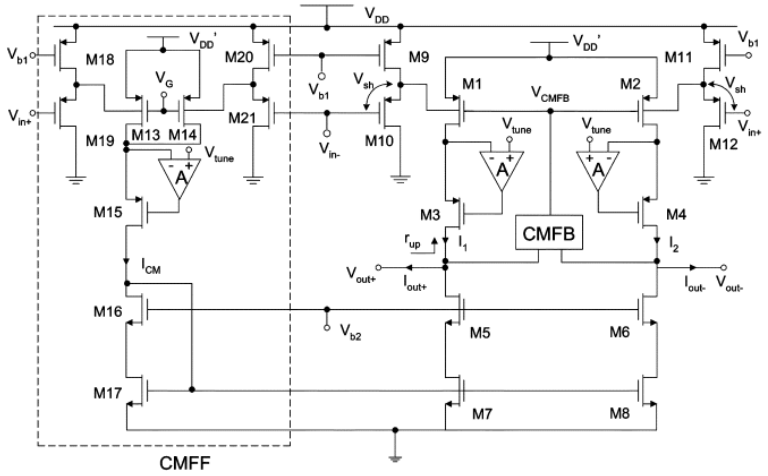


Figure 2.13 Bulk Driven OTA

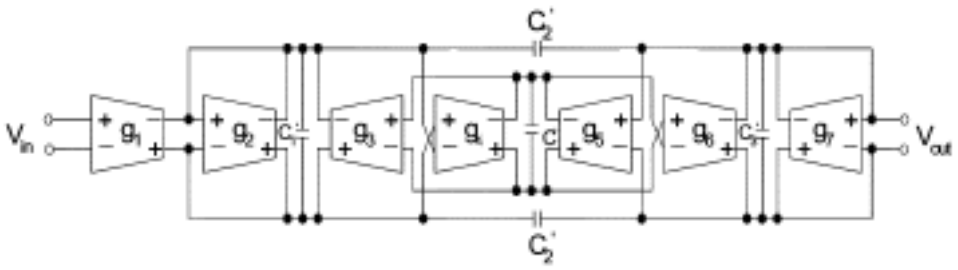


Figure2.14 Third-order Elliptic LowPass OTA-C Filter using Bulk Driven OTA

The performance of the third-order Elliptic LowPass OTA-C Filter is that -45dB @800mVpp, which means that its linearity is good.

A similar application can be found in [44].

2.2 Low Power Technology--Analog Design in Weak Inversion

2.2.1 Weak Inversion Theory

In the cases of analog circuits design, the hand calculation is always the first step and people use equation (2.3) as the approximation:

$$I_D = \frac{1}{2}\mu_n C_{OX}\frac{W}{L}(V_{GS}-V_{TH})^2 \qquad (2.3)$$

This equation provides a convenient model of MOSFET in saturation region. However, when the gate-voltage (V_{GS}) of MOSFET is less than the threshold voltage (V_T), the ideal model assumes that the current in the gate and source is zero. In some cases of analog circuit configuration, the transistors which are in the subthreshold region do not exist and this approximation works well. While in some other topology of circuit, the transistors in subthreshold region play a key role in the effect of the whole circuit. Facing this kind of situation, the models in weak inversion and moderate inversion are necessary considering these models will help people understand the principle of the MOSFET. At the same time, these models are important in hand calculation and CAD simulation.

The previous models have presented that the differences between subthreshold and above threshold operation is the way I_D changes as V_{GS} increases. In a weakly-inverted FET, the current increases exponentially. In a strongly-inverted FET, the current increases quadratically (square law). This can be understood by looking at a plot of I_D vs. V_{GS} in two ways: with a linear I_D axis and with a logarithmic I_D axis:

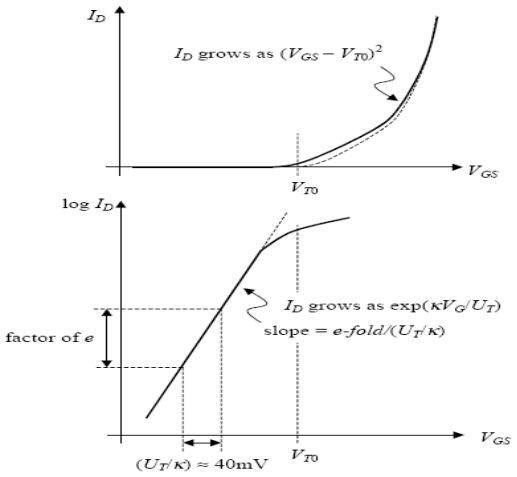


Figure2.15 I_D vs. V_{GS} in subthreshold and above threshold

Barron [101] gave an approximation expression for the weak inversion current. For an n-channel transistors, as

$$I_D = S\mu U_T^2 \left(\frac{1}{2} q\varepsilon_s n_i\right)^{1/2} e^{-(3\phi/2U_T)} \frac{e^{\psi_s/U_T}}{(\psi_s - U_T)^{1/2}} \cdot (e^{-(V_S/U_T)} - e^{-(V_D/U_T)}) \quad (2.4)$$

where S=geometrical shape factor of the transistor (effective width over effective length of the channel), μ =mobility of carriers in the channel, UT=kT/q, ε_s =permittivity of Si, n_i = intrinsic carrier concentration, $\phi = U_T ln(N_B / n_i)$ bulk Fermi potential, N_B =constant bulk impurity concentration, ψ_s = sur-face potential, constant along the channel in weak inversion, VS=source-to-substrate voltage, VD=drain-to-substrate voltage, V_G =gate-to-source voltage, I_D =drain current.

Vittoz [94] has developed the pertinent theory and his model in weak inversion is

$$I_D = \frac{W}{L} I_{D0} e^{V_G / nU_T} (e^{-(V_S/U_T)} - e^{-(V_D/U_T)}) \quad (2.5)$$

where I_{D0} is a characteristic current and n is a slope factor.

Based on this model, two different current references, an amplitude detector and a low-frequency BandPass amplifier are designed to verify the correctness of this model.

Similarly, in [95], the model provided is

$$I_D = I_0 \frac{W}{L} e^{kV_G/U_T} (e^{-(V_S/U_T)} - e^{-(V_D/U_T)}) \quad (2.6)$$

where kappa is 1/n or $1/\zeta$ (zeta). Moreover, in [95], a good, all-around approximation for kappa (unless another value is given) is

$$k = 0.7 \tag{2.7}$$

as a result,

$$\text{n}=\zeta = 1/k \cong 1.4 \tag{2.8}$$

In [100], the EKV model is introduced as one of the best models which combine both goals of transistor modeling: simulation by quantitative calculation on computer and highlighting properties to facilitate:

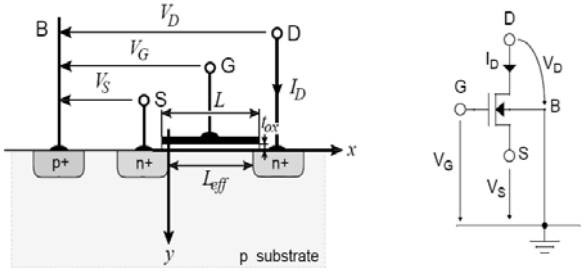


Figure 2.16 Bulk Reference of EKV Model

$$I_D = I_S \cdot [\ln(1 + \exp[\frac{k(V_G - V_{T0}) - V_S}{2U_T}])]^2 \tag{2.9}$$

where

$$I_S = \frac{2\mu C'_{OX} U_T^2}{K} \cdot \frac{W}{L} \tag{2.10}$$

An expression for transconductance gm valid in all regions of operation is given by

$$g_m = \frac{k I_D}{U_T} \cdot G(I_D) \tag{2.11}$$

where

$$G(I_D) = \frac{1 - e^{-\sqrt{I_D / I_S}}}{\sqrt{I_D / I_S}} \tag{2.12}$$

An important design parameter required in analog circuits is the current-to-transconductance ratio. In [97], based on EKV model, a universal

expression for MOS transistors is given as a powerful tool for circuit design since it allows designers to compute the available transconductance-to-current ratio in term of the inversion level if

$$\frac{I_F}{\phi_t \cdot g_{ms(d)}} = \frac{\sqrt{1 + i_{f(r)}} + 1}{2} \tag{2.13}$$

where

$$i_{f(r)} = \frac{I_{F(R)}}{I_S} = \frac{I(V_G, V_{S(D)})}{I_S} \tag{2.14}$$

In the discussion above, some parameters of the model can be learned. In [95] and [102], gm, kappa and n are studied in detail on their contribution in the model.

In figure2.18 [28] and figure2.19 [40], two configurations of the circuits are presented whose transistors all work in weak inversion, which are the good representation of the low power technology. At the same time, these configurations also have the good linearity in some particular range of the frequencies.

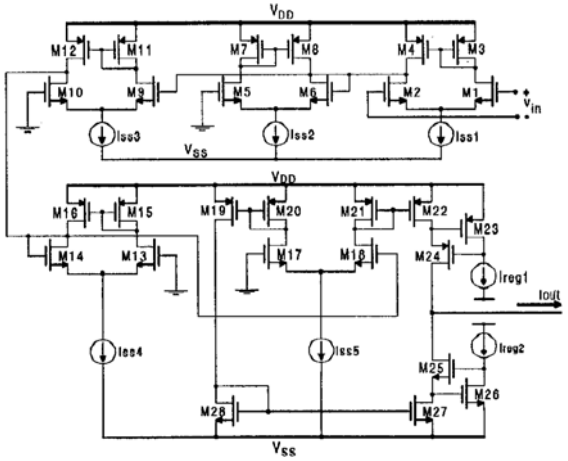


Figure2.17 The Weak Inversion OTA1

In figure 2.17, the power dissipation is in the nW level and its working frequency is very low. For instance, the LowPass Gm-C filter using this OTA can achieve the

cutoff frequency of 5Hz. As a result, this kind of configuration will play a key role in saving the power for the very low frequency circuits.

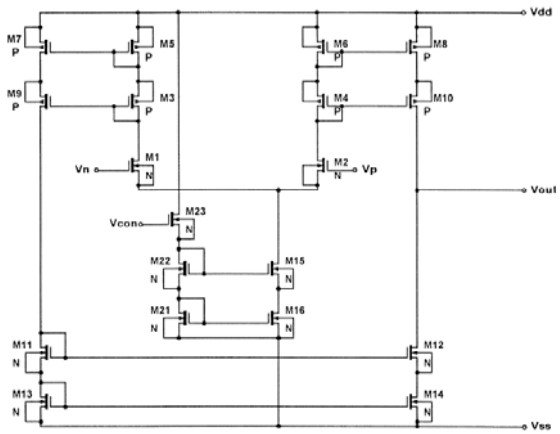


Figure2.18 The Weak Inversion OTA2

In figure 2.18, all of the transistors are operating in the subthreshold region and the OTA transconductance, Gm, is proportional to the biasing current, IB, in subthreshold operation and shows a different character than the operation in the strong inversion region, where Gm is proportional to $\sqrt{I_B}$ and given by

$$Gm = B\sqrt{2\mu C_{OX}(\frac{W}{L})I_B} \tag{2.15}$$

2.2.2 Design of a Common Source Amplifier

In this part of simulation, OrCAD Pspice is used in the schematics and simulations considering in the cases of analyzing the relationship between a parameter of the schematic and the gain of the circuit when the frequency of AC analysis is fixed, which is an advantage over Cadence Virtuoso.

In the following simulation, the Common Source Amplifier is chosen considering its wide application in many different complicated circuits. And the discussion of them is based on their ID-AV waveforms

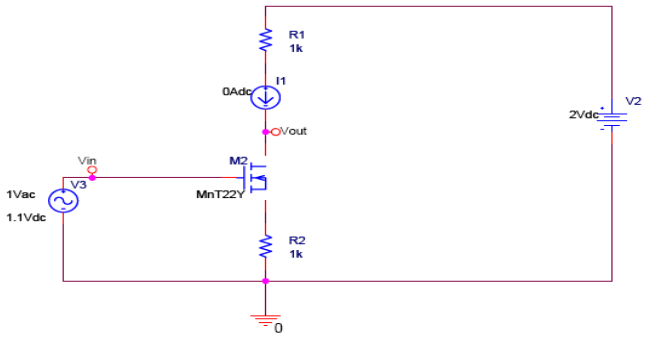


Figure2.19 Schematic of the Common-Source Amplifier

The analysis is based on the change of the drain current of the MOS transistor in the amplifier and its effect to the gain of it.

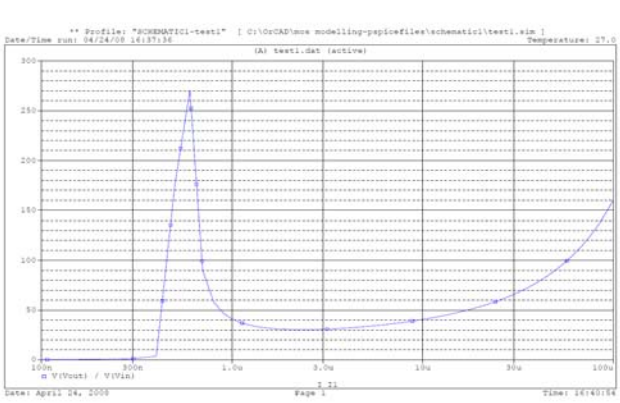


Figure 2.20 The waveform of the gain of this CS Amplifier

The waveform of Figue2.20 is based on the W/L=1.7/1.5 of the NMOS and the frequency is 1KHz. These two aspects can be analyzed:

A. The ratio of Width over Length of the MOS transistor

According to the small signal model of MOSFET, the W/L of the NMOS is proportional to the gain of the circuit. However, considering the restriction of the channel-length modulation and body effect, the actual model is much more complicated. As a result, based on the comparison of different width and length, 1.7/1.5 is chosen in order to get a relatively high gain of this CS Amplifier. Although

may be this value is not the one which can lead to the largest gain, it is useful because our focus on is the comparison of the gain in weak inversion and the rest part of the threshold region.

The horizon axel of figue2.20 is divided as 0.1uA, 0.3uA, 1uA, 3uA, 10uA, 30uA, 100uA. From it people can realize that the biggest gain appears in the region of moderate inversion and weak inversion. This result is meaningful because it will lead us to understand the advantage of weak inversion: maximum voltage gain, low device dissipation. For example, in some particular circuit configuration, people can use different currents to get the same gain of the amplifier. Just like the gain 100 in Figure2.20, the current can be chosen as 0.5uA or 70uA, the VDD is 2V. As a result, the power dissipation of the two choices is 1uW and 140uW. The advantage of the weak inversion far outweighs that of strong inversion.

B. The frequency of the circuit

The frequency of this configuration is 1KHz. In a certain range of the frequency, such as 10KHz and 50KHz, the gain of the circuit will not change a lot because these frequencies all belongs to a relative low range. However, if the frequency is in a much higher range, for example, 1GHz, the waveform will change a lot. As a result, the application of the weak inversion analog circuits works well in low frequency instead of high frequency. It is a short-cut of weak inversion. But in most situations in which the frequency is not the main domain of the requirement, the analog design of weak inversion plays a more and more important role.

2.2.3 Design of a basic Operational Amplifier

Operational Amplifier is one of the most popular circuits in analog field. In [98], the author presented an idea that the weak inversion can be applied in the first stage of the Op Amp. However, they did not simulate that. In this experiment, the gain of the Op Amp is simulated in a certain range of current and this idea is verified.

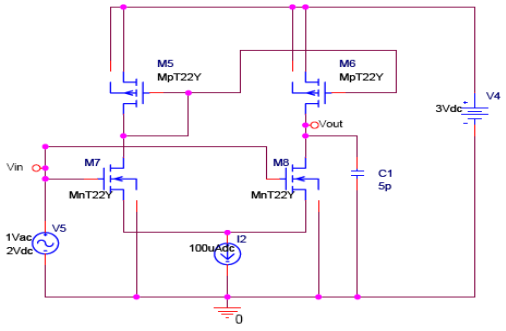


Figure2.21 Schematic of the Op Amp

As it mentioned above, the same gain can be obtained when the suitable current in weak inversion and strong inversion is chosen and the power dissipation of these two cases will be very different. Considering the wide use of Op Amp in A/D Converter, D/A Converter and Analog Filters, if the W/L can be chosen well, the reduction of the power dissipation will be obvious. As a result, the research of weak inversion is an important part of the analog low-power design procedure.

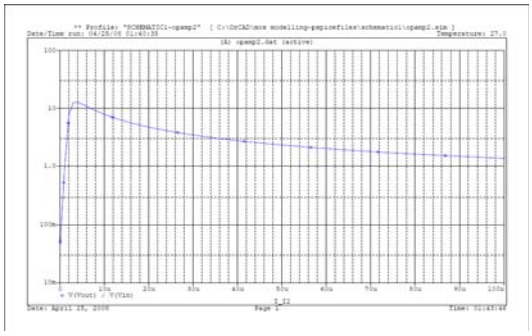


Figure2.22 The waveform of the gain of this Op Amp

2.3 Adaptive Technology

The adaptive technology is to use a bias voltage or current to revise the value of the frequency or the gain of the circuit. For example, an adaptive biasing amplifier adapts its biasing to be able to provide larger output currents.

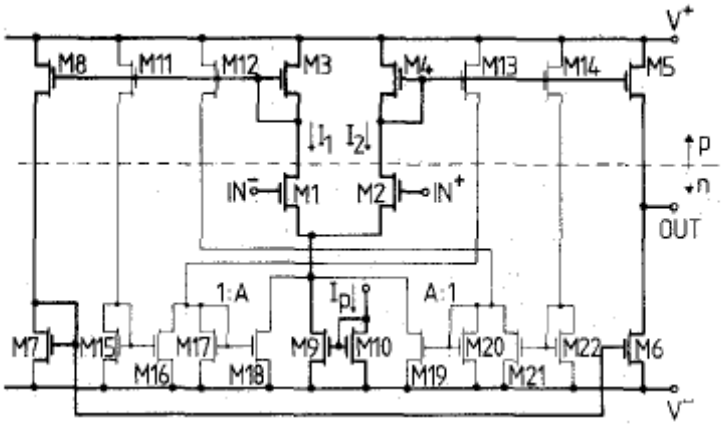


Figure 2.23 Adaptive Biasing Amplifier

The amplifier in figure2.23[76] is a symmetrical amplifier, which is single ended. Two times two current mirrors are added, i.e. with transistors M11/M12 and M13/M14. Without these transistors the maximum output current would be limited to BIP.

In order to increase this maximum current, biasing current Ip must be made larger for larger input voltages. This biasing current is adapted to the input signal level. This is why it is in parallel with two more current mirrors through transistors M18 and M19. The path can be followed to transistor M19. Transistor M19 forms a current mirror (with current factor A) with M20. This latter transistor takes the difference in current I1-I2, which are proportional to the currents in the input stage. The larger of these two currents wins. If I1 is larger than I2 then AI1 current is added to Ip, increasing the total biasing current of the first stage, and also increasing the maximum

output current.

If, however, I2 is larger than I1, then it is mirrored by M17/M18, also multiplied by A and also added to Ip.

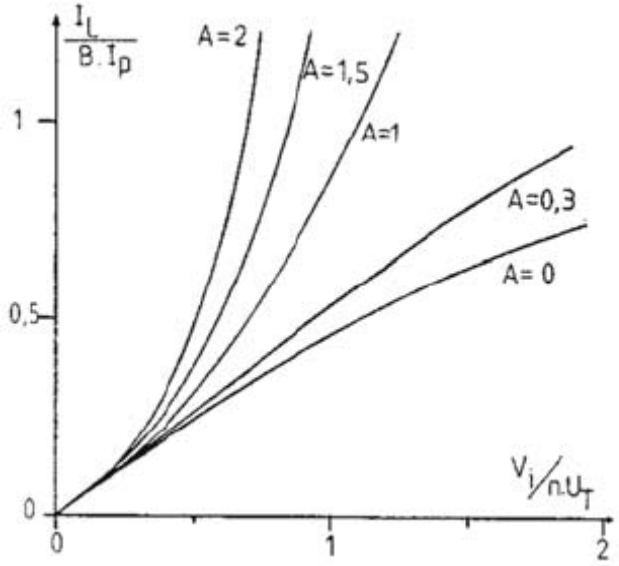


Figure 2.24 Transfer Curve of Adaptive Biasing Amplifier

For a current factor A equals to zero, no adaptive biasing takes place. The output current (normalized to Bip) is limited for larger input voltages (normalized to nUT or nkT/q.). For an increasing factor A, however, the expansion of the output current with the input voltage is more and more pronounced. A class-AB behavior is now obtained. Factor A cannot be increased to very large values, depending on matching. A practical limit is about 10. If cascodes are used however, the matching between all the current sources improves remarkably. Higher factors of A can then be tried.

A disadvantage of this amplifier is that transistors M11 – 14 are added on the node where the non-dominant pole is formed. They will therefore slow down the amplifier.

3. OTA Design

In the introduction part, the basic description of the OTA is presented.

The characteristic expression of the OTA is

$$Iout = Gm(V_{in+} - V_{in-}) \tag{3.1}$$

The differences between the OTA and the conventional Op Amp are:

A. Its output of a current contrasts to that of standard operational amplifier whose output is a voltage.

B. Except for its input stage (which is a simple two transistor differential amplifier), its internal circuitry is completely different. The OTA is constructed completely of transistors and diodes; it uses no resistors or capacitors.

C. It is usually used "open-loop"; without negative feedback in linear applications. This is possible because the magnitude of the resistance attached to its output controls its output voltage. Therefore a resistance can be chosen that keeps the output from going into saturation, even with high differential input voltages.

3.1 Basic OTA

3.1.1 The topology of the OTA

At the first stage of complicated OTA design, the basic configuration should be simulated and the result can be compared with the achievement of the ones with the linearity, low power and adaptive technology.

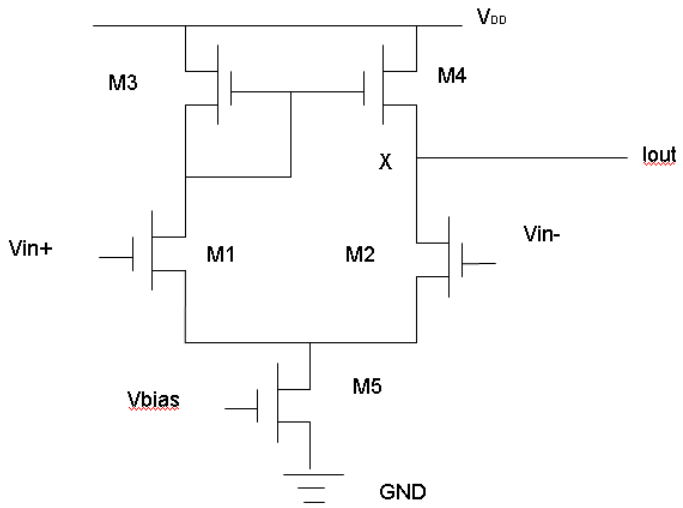


Figure 3.1 Basic OTA

In figure3.1, M1 and M2 are the input transistors and the specification of the OTA can be determined by the following equations

The transcinductance Gm=gm1=gm2, it is

$$Gm = \sqrt{2K_n' I_{D5} (\frac{W}{L})_1} \tag{3.2}$$

$$R_{OUT} = \frac{r_{o2}}{2} = \frac{V_A L_1}{I_{D5}} \tag{3.3}$$

where VA is the Early voltage.

As a result, the voltage gain Av is obtained by

$$A_V = GmR_{OUT} = V_A \sqrt{\frac{2K_n' W_1 L_1}{I_{D5}}} \tag{3.4}$$

The -3dB cut-off frequency (the dominant pole) is created on node X amd

$$f_d = \frac{1}{2\pi R_{OUT}(C_{nx} + C_L)} \tag{3.5}$$

where Cnx =CGD4+CDB4+CGD2+CDB2+CDS2+CDS4 and CL is the load capacitance.

The gain-bandwidth (GBW) is given by

$$GBW = A_V f_d = \frac{g_{m1}}{2\pi(C_{nx} + C_L)} \tag{3.6}$$

From (3.2) to (3.6), the transistors can be scaling and the OTA will work.

3.1.2 The Gm curve of the OTA

After operating the DC analysis of the difference of the input voltages versus the output current, the transconductance curve can be obtained

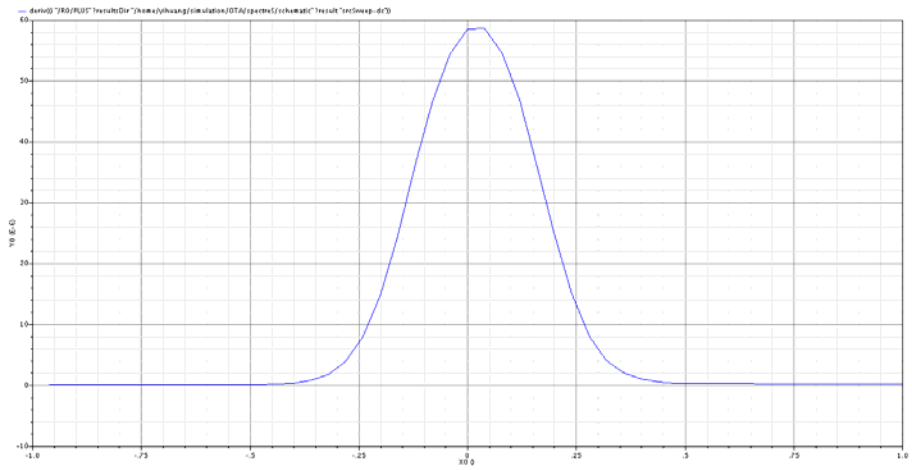


Figure 3.2 Transconductance curve of the basic OTA

From figure 3.2, it is known that this OTA only has the linearity in a very small range. If the range of the input signal is in a wider range, for example, in the Charge Sensitive System of this thesis, the input range will between -100mV and 100mV, this OTA will be impropriate considering the nonlinearity of it will cause some kinds of distortion. As a result, the linearity technology is needed for the suitable OTA which will be used in the Charge Sensitive System. At the same time, all the transistors in this OTA works in strong inversion, which call for the low power technology to save the dissipation.

3.2 Linear OTA Design

Based on the requirement of the linearity of the project and the nonlinearity, low power and adaptive technology available, a particular kind of the OTA is picked for this project. The prototype of this topology was first introduced by Coban /Allen in [70]. And Yang [6] revised the prototype using the two weak inversion transistors. As a result, this OTA has the characteristic of the linearity, low power and adaptive.

3.2.1 The topology of the OTA

The structure of the main part of the OTA is

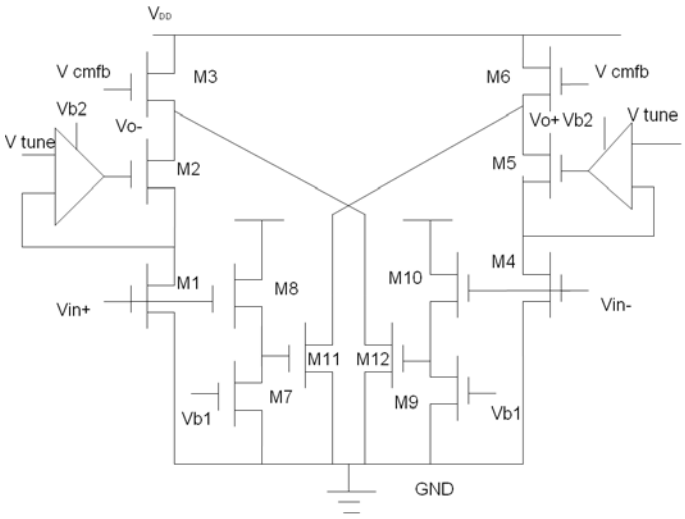


Figure3.3 The main stage of the proposed OTA

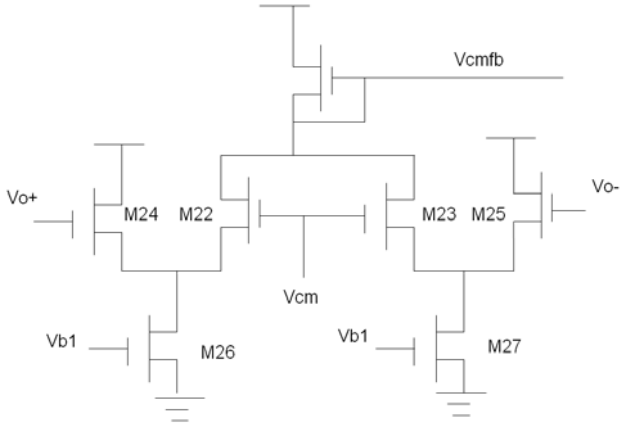


Figure3.4 The CMFB of the proposed OTA

Table 3.1 is the sizing of the transistors:

Name	Value	Name	Value
M1,4	3/6	M21	3/3
M2,5	3 /3	M16,20	60/3
M3,6	12/3	M22,23	3/3
M7 ,9	9/3	M24,25	60/3
M8,10	7.2/3	M26,27	3/3
M11,12	3/6	Vb1	0.846V
M13,17	4.5/3	Vb2	0.95V
M14,18	2.1/3	Vtune	0.2V
M15,19	3.45/3	Vcm	1.4V

Table 3.1 The sizing of the transistors

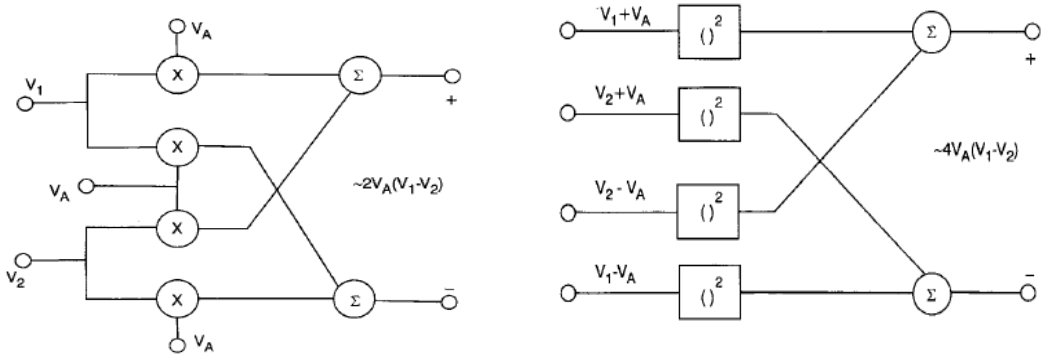
In this OTA, the input transistors M1 and M4 work in triode region as well as M11 and M12 work in the weak inversion. The cross coupled technology is used for the nonlinearity cancellation. And two shifters are used as the role of Op Amp to realize the adaptive technology. These sub-circuits will be presented in detail in the following.

3.2.2 Linearity of the proposed OTA

3.2.2.1 Cross-Coupled Topology

The most significant part of the OTA is the cross coupled structure, which makes a great contribution to the nonlinearity cancellation.

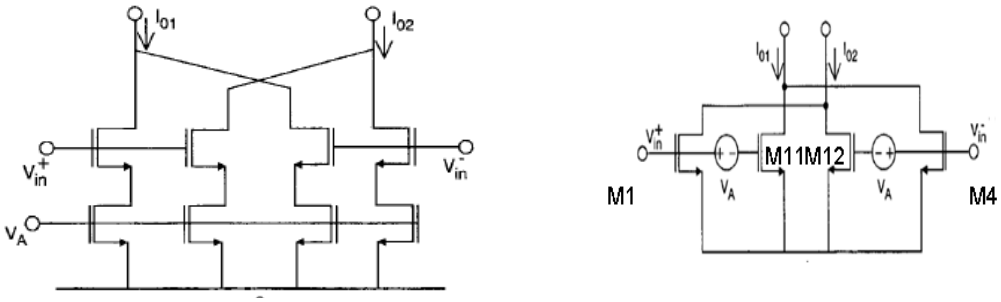
For cross coupled technology, the conceptual ideas are just like this



(a) (b)

Figure 3.5(a)Using single multipliers by a constant V_A (b)Using single-quadrant devices V1 = -V2

The detailed circuit configurations of Figure3.5 (a) and (b) are introduced in figure 3.6 (a) and (b). Considering in these circuits, the nonlinearities will be removed as only a linear relationship between the input voltage and the output current.



(a) (b)

Figure 3.6 (a) The single multipliers circuit (b)The single-quadrant circuit

In the proposed OTA, the structure of 3.6 (b) is utilized while M1,4 work in triode region and M11,12 work in weak inversion region. And the floating voltage sources in it are implemented by two simple source followers in order to fix the gate voltage of M11 and M12 less than the threshold voltage, which is the requirement of the weak inversion operation. The reason of using the transistors of triode region and weak inversion will be explained in the part of Harmonic Distortion (HD) analysis.

In [48]-[63], several different kinds of cross-coupled circuits are presented. Besides the cross coupled technology, the source degeneration method is also widely used for the nonlinearity cancellation.

3.2.2.2 The transconductance curve of the proposed OTA

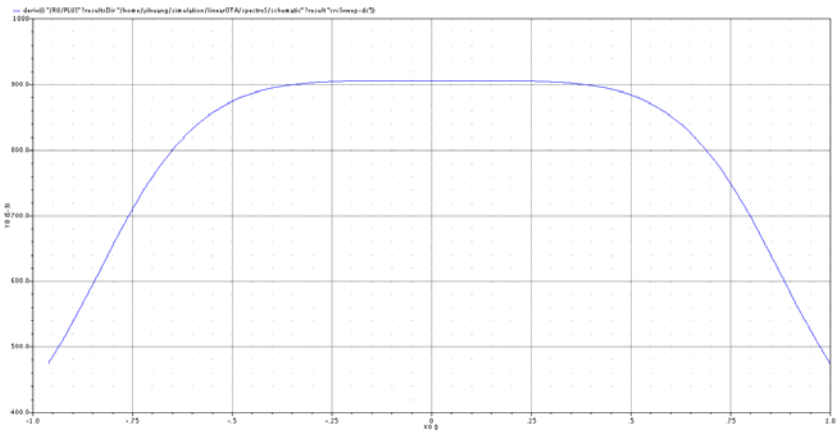


Figure 3.7 Transconductance Curve of the linear OTA

Compared to figure3.2, in the same input range, the linearity of the proposed OTA is much better than that of the basic OTA. In the Charge Sensitive System, the input range is between -100mV and 100mV, which is the linear range of the proposed OTA. This difference also represents the effect the nonlinearity cancellation.

3.2.2.3 Harmonic Distortion Analysis

When a sinusoidal signal of frequency w is applied to the input of the filter, the steady -state response at the output consists of not only the component at the fundamental frequency , but also the components at harmonic frequencies 2w, 3w, 4w……These higher order terms are referred to as harmonic distortion. HD

is an important criterion in judging the linearity of the OTA.

The total harmonic distortion (THD) is defined as

$$THD = \frac{\sqrt{V_{h2}^2 + V_{h3}^2 + V_{h4}^2 + \ldots}}{V_f} \times 100\% = 20\log_{10}\sqrt{\frac{V_{h2}^2 + V_{h3}^2 + V_{h4}^2 + \ldots}{V_f^2}} \quad (in \quad dB) \qquad (3.7)$$

where V_f is the amplitude of the components at w and V_{hk} is the amplitude of the component at the kth harmonic kw, k=2,3,4…

In [21], [24], [26], [27], [36], [38] and [46] several authors have done some research in the modeling of the harmonic distortion as well as reduce it by different methods. In the analysis of the harmonic distortion, the relationship between the input voltage and the output current should be described in power series. Because of the balanced structure of the transconducor, the output current can be expressed using only odd powers of the input voltage, where the fifth- and higher order terms are negligible compared to the third-order term in most practical cases. As a result, the relationship between the input and the output is

$$Iout = gm * Vin + h3 * V_{in}^3 + h5 * V_{in}^5 + \ldots \qquad (3.8)$$

In order to verify this relationship, the I-V curve of the OTA (figure3.8) is used in the curve fitting.

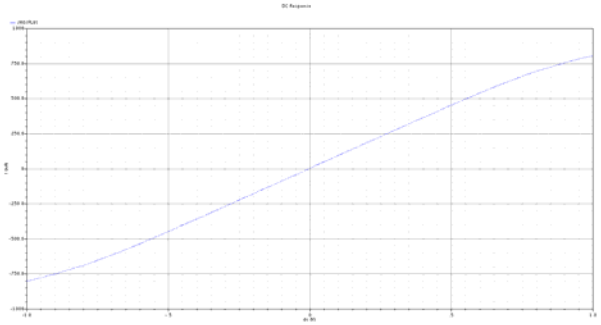


Figure 3.8 The I-V characteristic of the OTA

After using the curve fittling function in MATLAB, this relationship curve in the linear range (eg.-0.25V and 0.25V) can be written in fifth order

$$I_{OUT} = 10^{-6}((-2.64\times10^{-2})V^5 + 9.4\times10^{-3}V^3 + 0.8757V) \quad (3.9)$$

The equation (3.9) is the model of the proposed OTA and this model will be used in the SIMULINK modeling of the whole Charge Sensitive System, which will be introduced in the next chapter.

When the sinusoidal signal V=Acos(wt) is applied at the input, the output will become to

$$Iout = gm*Vin*\cos(wt) + h3*V_{in}^3*(\cos^3(wt)) + h5*V_{in}^5(\cos^5(wt)) + \ldots \quad (3.10)$$

If the terms above 3-order is neglected, one can define the third order harmonic measurement is

$$HD3 = \frac{Third \quad Harmonic}{Fundamental} = \frac{h3*V_{in}^3*\frac{1}{4}((\cos(3wt)) + 3\cos(wt))}{gm*V_{in}} \approx \frac{1}{4}\frac{h3}{gm}*V_{in}^2 \quad (3.11)$$

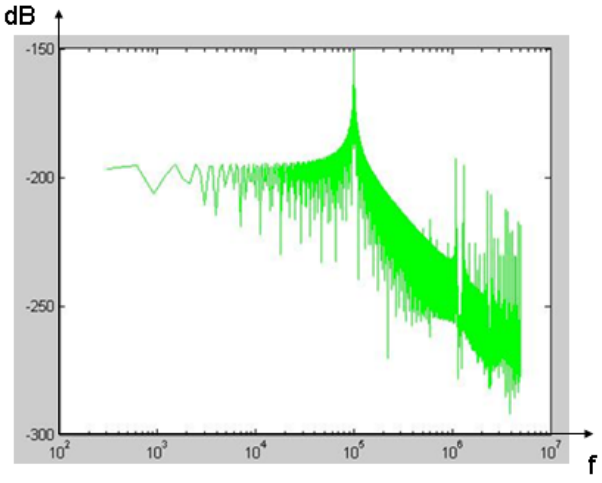


Figure 3.9 The Harmonic Distortion of the proposed OTA

In order to test the Harmonic Distortion of the proposed OTA, a sine signal is applied at the input terminal and the output current waveform is tested. The

HD versus frequency plot is in figure 3.9. It is known that in the frequency 100Hz to 900Hz, the THD is about 70dB. This specification will satisfy the requirement of the BandPass Filter in the Charge Sensitive System.

3.2.3 Low Power Characteristic of this OTA

The key components of the weak inversion technology in the structure of the proposed OTA are M11 and M12, the two transistors working in weak inversion.

In the real circuit, the current of M11 and M12 are in the nA level, which will save several hundred times of the power dissipation if these two transistors work in the saturation region. The Power of the whole OTA is about 400uW.

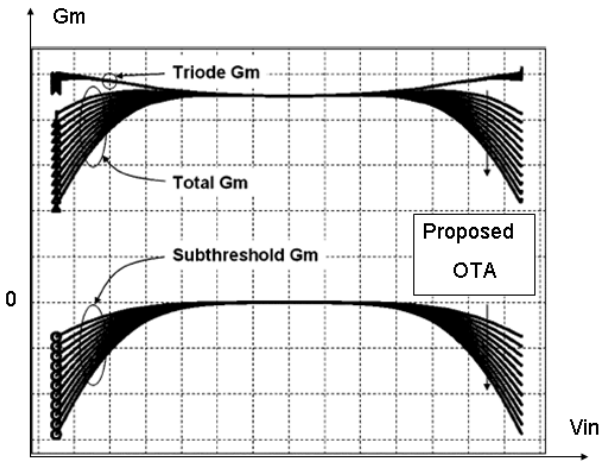


Figure 3.10 The Gm curve

At the same time, the parallel connection of the transistors in triode region and weak inversion will cancel the distortion term with a proper aspect ratio and can increase the linearity remarkably considering the fact that the third-order harmonic term of the triode and the weak inversion region devices have opposite signs. The transconductance of the triode region transistor, the

weak inversion transistor and their sum is presented in figure3.10.

3.2.4 Adaptive Characteristic of this OTA

In the proposed OTA circuit, the value of the transconductance can be revised by the outer voltage Vtune. Two Operational Amplifier or equivalent components are used in the circuit.

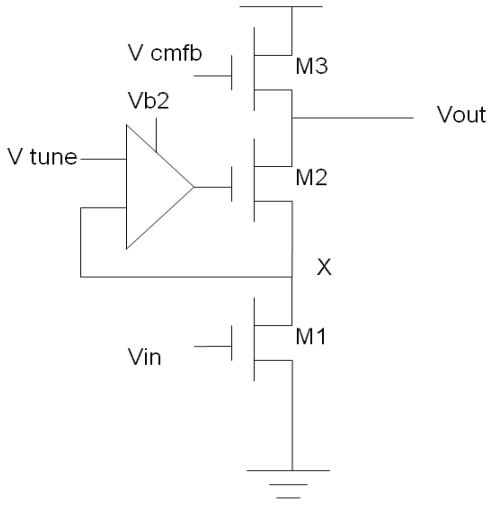


Figure 3.11 The tuning circuit

3.2.4.1 The effect of the Op Amp

In Figure 3.10, M3 works as the current source while M1 and M2 build a cascode circuit. The Operational Amplifier which is connected to M2 is used to enhance the output resistance.

$$Rout = \frac{Ag_{m2}}{g_{ds1}g_{ds2}} \tag{3.12}$$

The Op Amp can be replaced by some other configurations, for example, the MOS/BJT inverter or the shifter. In the proposed OTA, a shifter is used to take the place of Op Amp.

3.2.4.2 The shifter

In figure3.12, the shifter configuration is shown. The

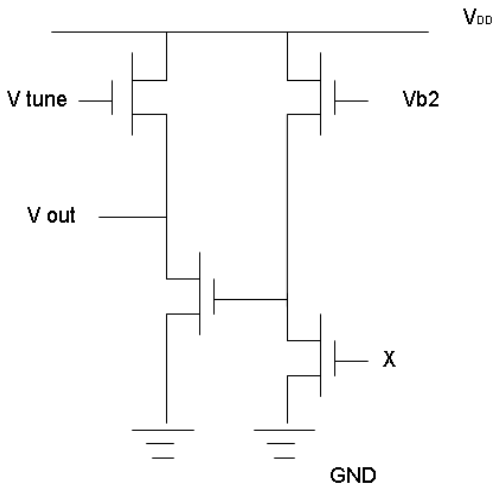


Figure 3.12 The shifter circuit

The realization of revising the transconductance value by changing that of Vtune comes from the working of the shifter. When the Vtune changes in a certain range, the four transistors work in saturation region. And the Vx is the drain source voltage of the input transistors M1 and M4, so when the Vx is different, the triode region transistors will provide the different values of their transconductance. Yielding that the total Gm of the whole OTA depends on the Gm value of the triode transistors and the weak inversion transistors, the total value will be changed as a consequence of the changing of Vtune.

3.2.4.3 Adaptive Characteristic

When the different voltage between the two input terminals is fixed at 100mV, which is in the linear range of the OTA, the DC analysis can be used to pursue the relationship between Vtune and Gm.

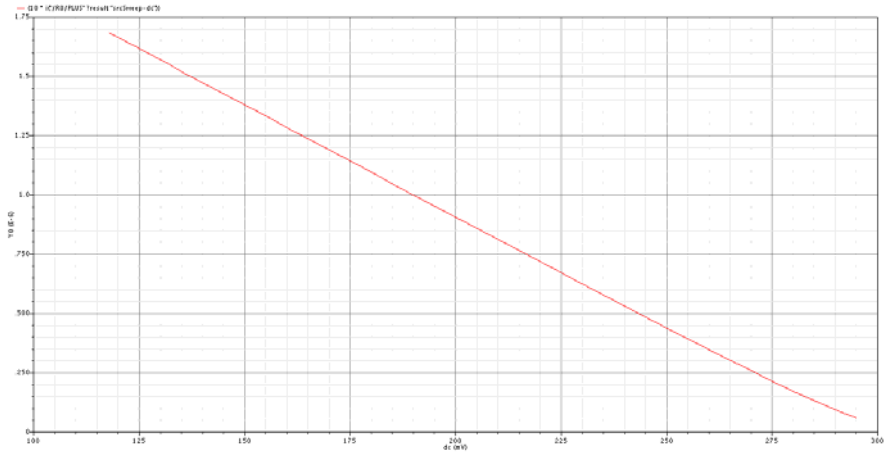


Figure 3.13 The adaptive characteristic of the proposed OTA

From figure3.13, people can see that when Vtune is between 0.118 and 0.295V, the value of the transconductance can be adjusted between 1.68uS and 0.08uS. The relationship is linear.

4. Charge Sensitive System

4.1 Overview of the System

The Charge Sensitive System includes two main parts. The first one is a Charge Sensitive Amplifier and the second one is the BandPass Gm-C filter. The goal of the whole system is to detect the value of the input signal, a very small one, by measuring the peak value of the output signal. The BandPass Filter should be designed properly in order to keep the relationship between the peak value of the output and input signal. Considering the output of the first part of the system, the output of Charge Sensitive Amplifier is proportional to the input signal, the testing between the output1 and output2 in figure 4.1 is also acceptable.

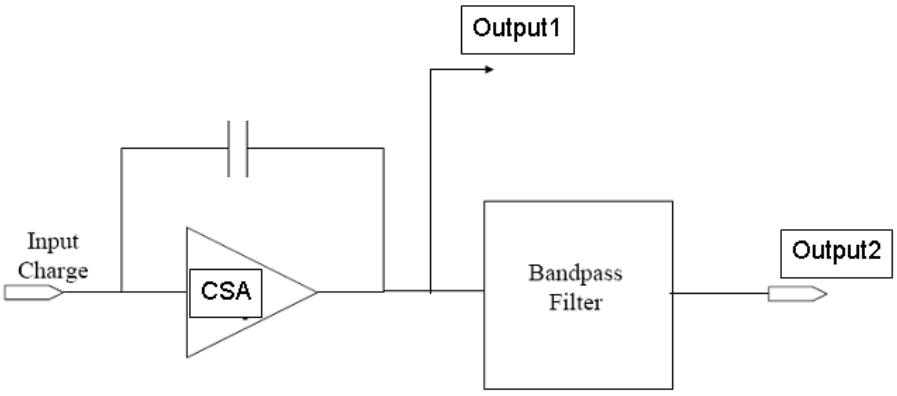


Figure 4.1 The Charge Sensitive System

Since in expression (3.9), the fifth-order model of the OTA is given, the simulation of some similar systems in MATLAB/SIMULINK can be used before the designing in CADENCE. The waveforms of the simulation will provide the criterion of verifying the performance of the filter design.

4.1.1 The SIMULINK Model of Charge Sensitive Amplifier

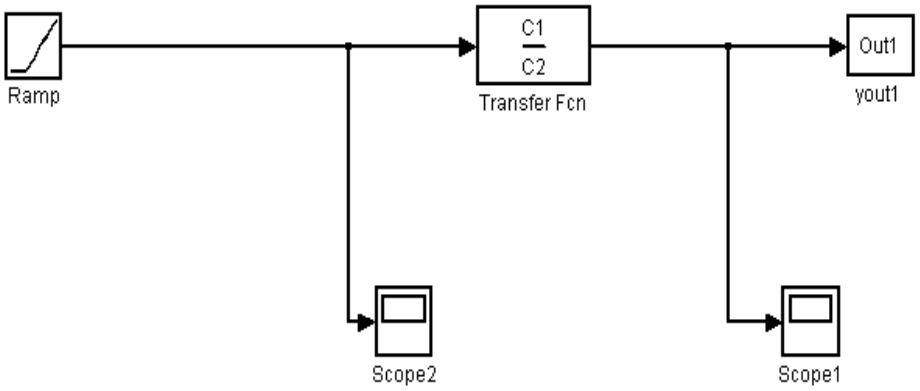


Figure 4.2 An approximation model of Charge Sensitive Amplifier

Figure 4.2 is an approximation of the Charge Sensitive Amplifier. C1 and C2 are two capacitors in it. C1 is connected in series with the amplifier while C2 is connected in parallel. There will also be a resistor which is in parallel with C2. And the input is a ramp with a fixed rising time and peak value. This SIMULINK model just represents the amplification effect.

4.1.2 The SIMULINK Model of BandPass Filter

The BandPass Filter consists of two subparts. One is the HighPass filter and the other one is LowPass filter. BandPass characteristic is achieved by connecting them in series. In SIMULINK model, f(u) is the OTA model which use equation (3.9) to define the relationship between the input voltage and the output current. Some capacitors are used in the BandPass Filter because of the Gm-C structure. The HighPass and LowPass filter can be described by two transfer functions H1(s) and H2(s), which will be introduced in detail in the circuit-level depiction.

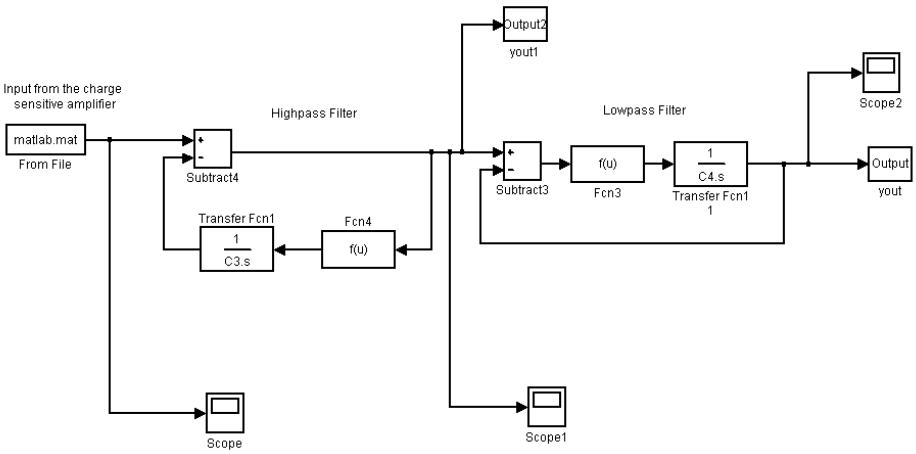


Figure 4.3 An approximation model of BandPass Filter

4.1.3 The simulation of SIMULINK Model

The simulation of the model consists of two parts. The first one is the transient waveform of the output of the Charge Sensitive Amplifier, the HighPass Filter and the LowPass Filter. The second one the linear relationship when the input signal is changed in a certain range.

4.1.3.1 The transient waveform of the system

When the peak value of the input signal is set to be 1uV, the output waveforms are displayed in figure4.4 to figure4.6. It is know that the output of the CSA, which is also the input of the BandPass filter, is a step signal. The output of the HighPass Filter is like a sawtooth signal while the final output, the output signal of the LowPass Filter is like a sinusoidal signal. The contribution of this SIMULINK simulation is just give people a blueprint of the signal in the circuit. The amplitude and some other information of these waveforms do not have to be corresponding to the simulation result of the CADENCE.

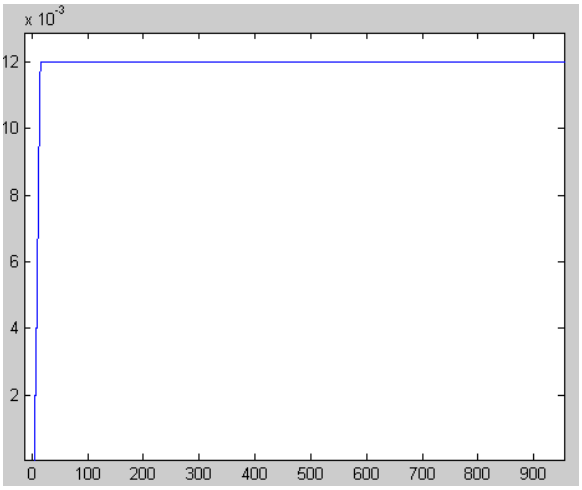


Figure4.4 The output of the Charge Sensitive Amplifier

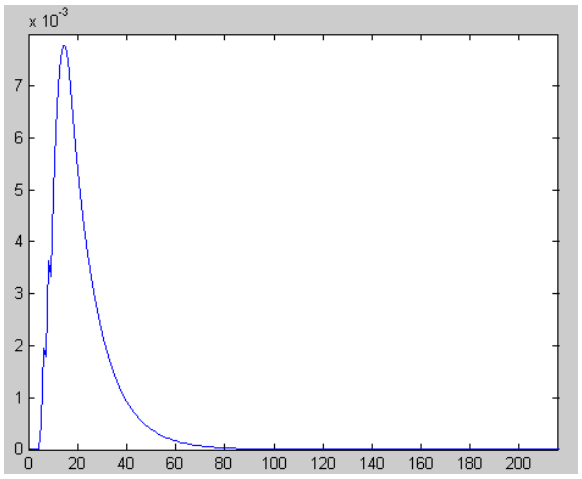


Figure4.5 The output of the HighPass Filter

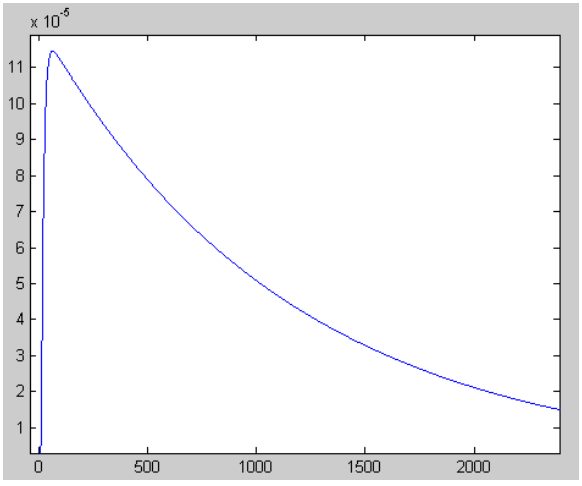


Figure4.6 The output of the LowPass Filter

4.1.3.2 The relationship between the input and output of the system

The linear relationship is shown between the input and output of the

BandPass filter. This relationship comes from the model of the OTA and the linear curve proves that the proposed OTA is good for the system.

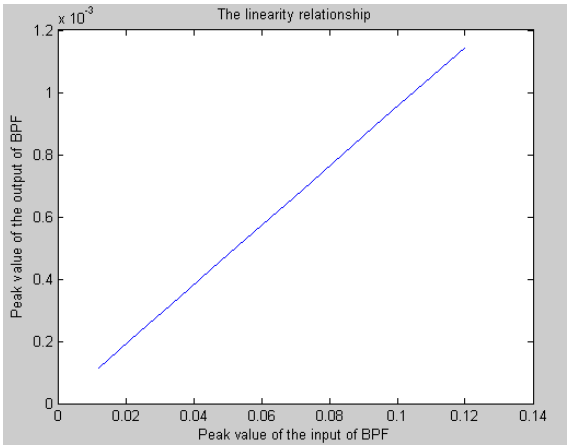


Figure4.7 The relationship between the input and output of the BandPass Filter

4.2 Charge Sensitive Amplifier

The effect of the charge sensitive amplifier is just to make sure the input signal, whatever the current signal or the voltage signal, can be amplified through C1,C2 and R1. The topology of the whole Charge Sensitive Amplifier is given in figure 4.8. The main structure is the foleded cascode circuit. C1 is 1pF and C2 is 100fF. And R1 is 200M Ohm.

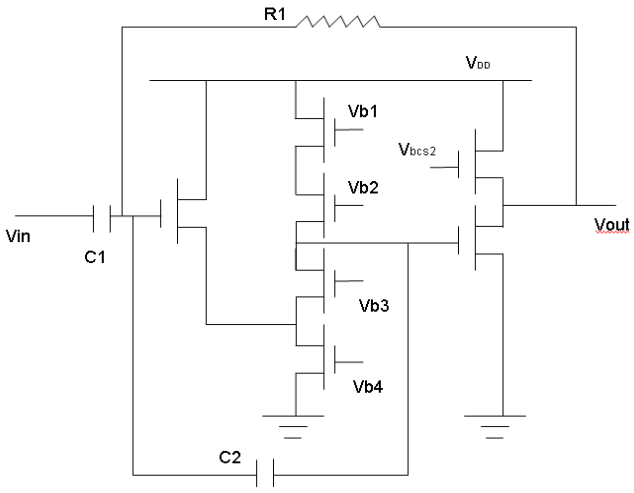


Figure4.8 The folded cascode CSA

Considering this is an one-input one-output amplifier, the folded cascode

topology is chosen because it has some advantages such as (1) the separate the ICMR and outputswing (2) high Gm without high power dissipation (3) low noise.

4.3 BandPass Filter

The BandPass Filter is made up of a HighPass Filter and a LowPass one. It is easy to explain that from the mathematical perspective.

The transfer function of the LowPass Filter is that

$$H_{LP}(s) = \frac{1}{s + \frac{Gm}{C}} \tag{4.1}$$

and the counterpart of HighPass Filter is

$$H_{HP}(s) = \frac{s}{s + \frac{Gm}{C}} \tag{4.2}$$

Hence the transfer function of the BandPass Filter is as expression (4.3) and its implementation in the actual circuit is the connection of the LowPass and HighPass Filter in series.

$$H_{BP}(s) = \frac{s}{(s + \frac{Gm}{C})} \bullet \frac{1}{(s + \frac{Gm}{C})} \tag{4.3}$$

The configurations of the Filter are so many that the designer should pick the proper one which is the most suitable for their project. The most popular structures are the Butterworth Filter, the Chebyshev Filter and the Elliptic Filter. Each of them has their own advantages and drawbacks. And according to the specification, the filters of the different orders can be implemented. In this thesis, both the HighPass and LowPass are the simplest first-order filters.

4.3.1 HighPass Filter and its Characteristic

For the single-ended OTA, the HighPass implementation is

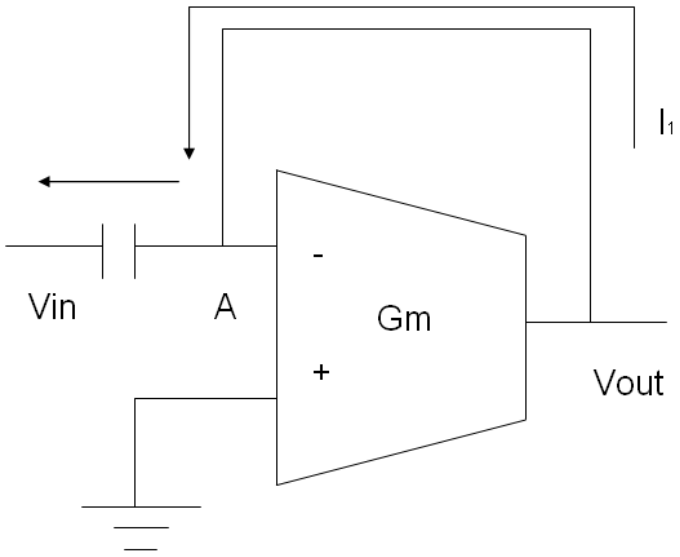


Figure 4.9 First-Order HighPass Filter for Single-ended OTA

At node A, the voltage is Vout. And there is a current from the output terminal to the node A. This current will go from A to the input terminal as well. Consequently, the equations are obtained in the calculation of the transfer function

$$\begin{cases} (0-Vout)*Gm = I_1 \\ \dfrac{(Vout-Vin)}{C_1 S} = I_1 \end{cases} \tag{4.4}$$

The transfer function (4.2) can be calculated from (4.4).

Similarly, the structure of the fully differential OTA's Gm-C Filter can be deduced from this idea.

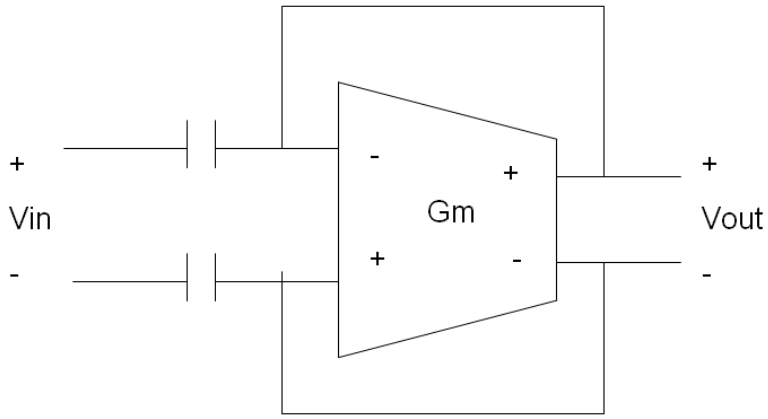


Figure 4.10 First-Order HighPass Filter for Fully-Differential OTA

When the values of the capacitors are 1pF, the HighPass AC Response is

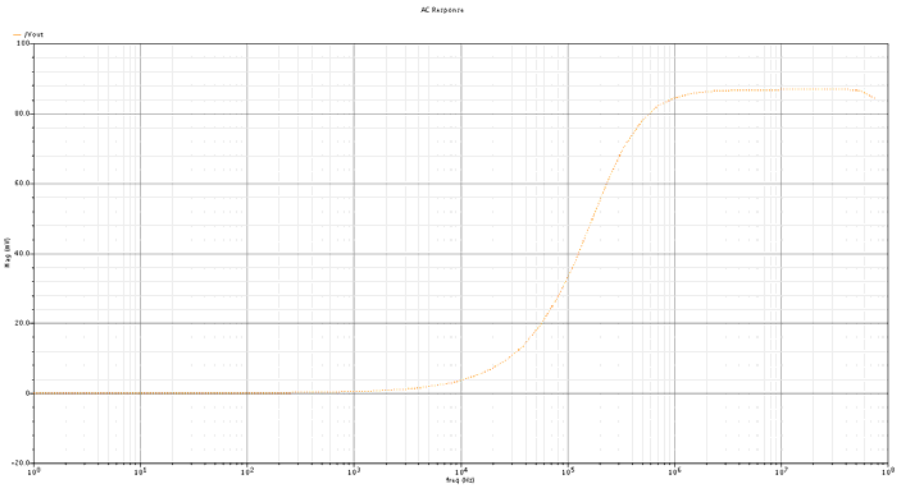


Figure 4.11 HighPass Characteristic

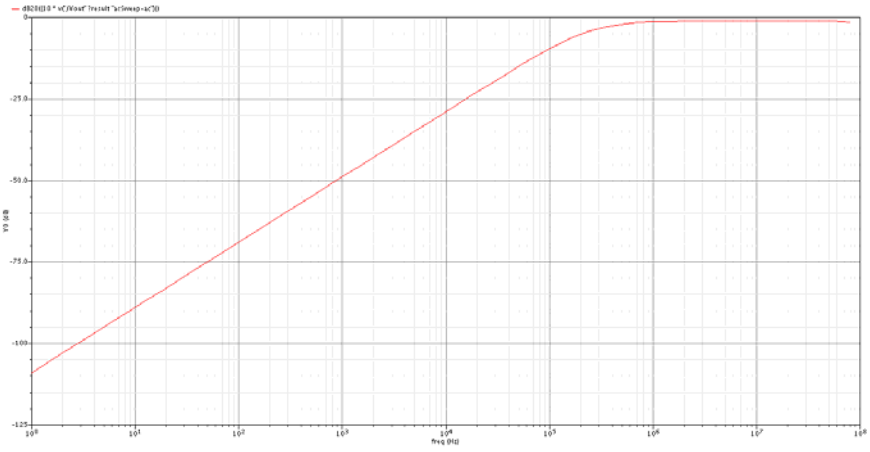


Figure 4.12 HighPass Characteristic (Y axis in dB)

4.3.2 LowPass Filter and its Characteristic

For the single-ended OTA, the LowPass implementation is

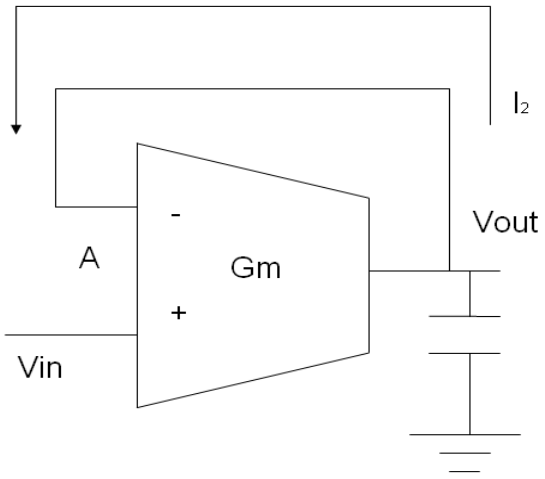


Figure4.13 First-Order LowPass Filter for Single-ended OTA

The derivation of the LowPass transfer function is

$$\begin{cases} (Vin - Vout) * Gm = I_2 \\ \dfrac{Vout}{C_2 S} = I_2 \end{cases} \tag{4.5}$$

From (4.5) the LowPass transfer function is

$$H(s) = \frac{G_m / C_2}{s + G_m / C_2} \tag{4.6}$$

Similarly, the fully differential OTA's LowPass Filter can be deduced.

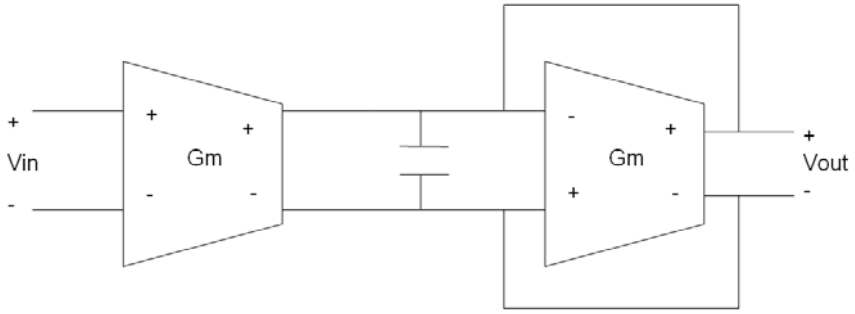


Figure4.14 First-Order LowPass Filter for Fully Diferential OTA

When the value of the capacitor is 1fF, the input is 100mV ac signal, the

AC Response curve is

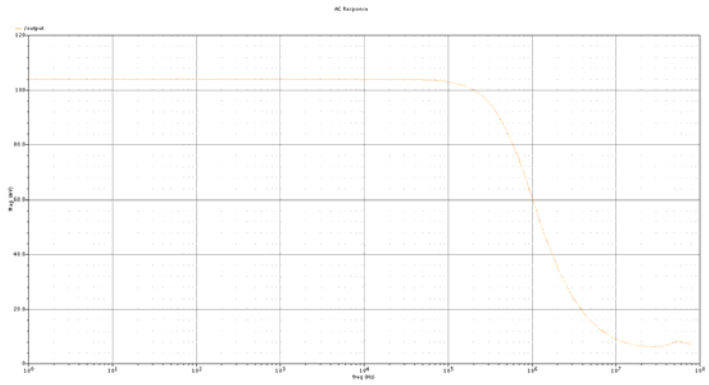


Figure 4.15 LowPass Characteristic

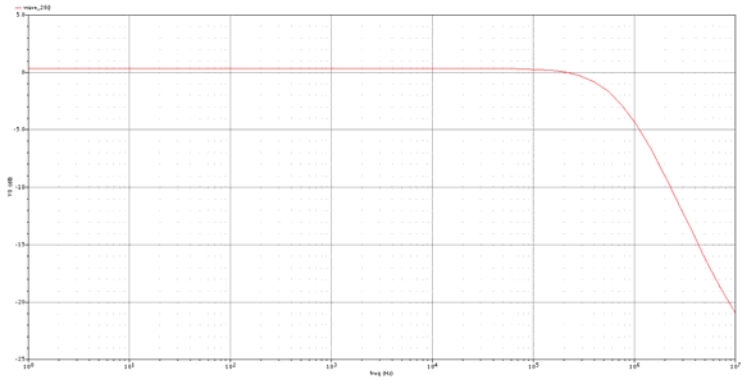


Figure 4.16 LowPass Characteristic (Y axis in dB)

4.3.3 BandPass Filter and its Characteristic

After connecting the LowPass and HighPass parts, the BandPass characteristic can be obtained when the input is 100mV ac signal.

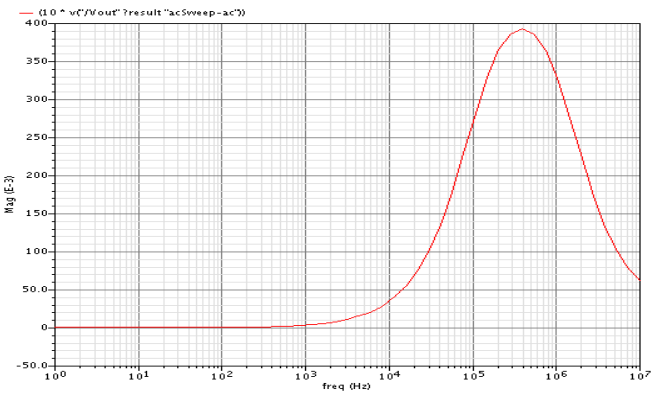


Figure 4.17 BandPass Characteristic

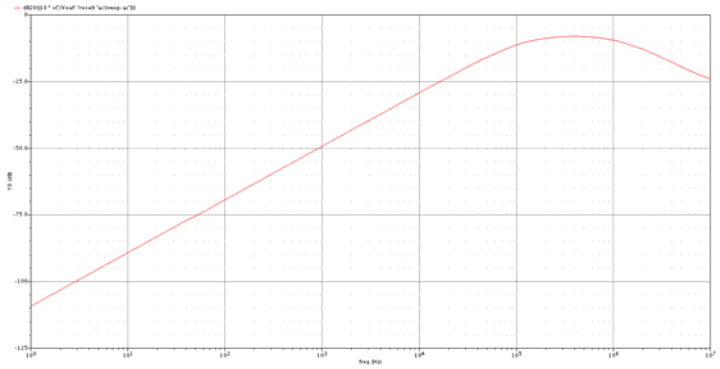


Figure 4.18 BandPass Characteristic (Y axis in dB)

4.4 Simulation of the whole system

After connecting the Charge Sensitive Amplifier and the BandPass Filter, a step signal is applied at the input. The initial amplitude is 50mV and after 20ns the signal decreases to 0. The falling time is 1ps. Assume the input is A, the output of the Charge Sensitive Amplifier is B, which is also the input of the BandPass Filter. The output of the HighPass Filter is C and the final output is D. Figure 4.19 shows the wave in these four terminals.

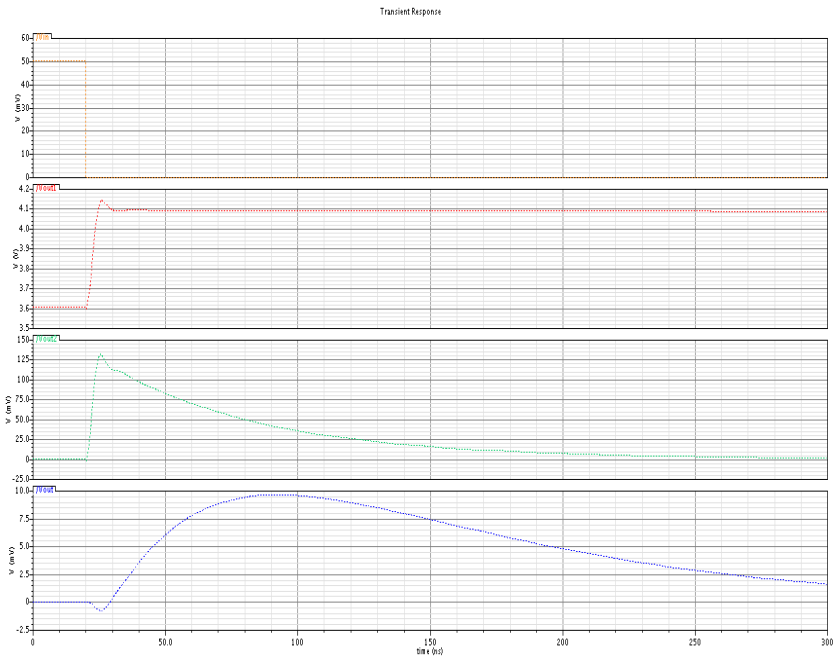


Figure 4.19 The waveform in nodes A, B, C and D

From figure4.19, the waveforms are similar to figure4.4 to figure 4.6, which means that the MATLAB simulation and CADENCE simulation are consistent. The waveform has been tested in different values of the input and the correctness has been verified. In conclusion, the BandPass filter design is successful.

5. Conclusion

In this thesis, a linear OTA combining the technology of nonlinearity cancellation, the low power and the adaptive is designed. Based on the research of these three kinds of technology, such as the analog design of weak inversion, the OTA has performed a good linearity in the range between -250mV and 250mV, which makes it qualify for the design of BandPass Filter. The BandPass filter is presented based on the fully differential OTA-C structure. It is connected to a Charge Sensitive Amplifier to build a Charge Sensitive System. The function of the system is to detect the small input signal by measuring the peak value of the output signal. The BandPass Filter is designed properly to fulfill the linear relationship between the input signal and the peak value of output signal. Simulations in MATLAB/SIMULINK and CADENCE have proved the correction of the design.

Reference

[1]C.-C. Hung, K. Halonen, V. Porra, and M. Ismail,"Low-Voltage, Micropower Weak-Inversion CMOS GM-C Filter," Proc. 3rd IEEE International Conference on Electronics, Circuits, and Systems (ICECS), pp.1178-1181, Rodos, Greece, Oct. 13-16, 1996.

[2] C.-C. Hung, K. Halonen, V. Porra, and M. Ismail, "Low-voltage CMOS GM-C filter with rail-to-rail common-mode voltage," in Proc. 39th Midwest Symposium on Circuits and Systems, Ames, Iowa, Aug. 1996.

[3] Rodriguez-Villegas E, Payne A J and Toumazou C 2002 A 290 nW, weak inversion, Gm-C biquad IEEE Int. Symp. on Circuits and Systems, 2002. ISCAS 2002 (26-29 May 2002) vol 2 pp II-221-II-224

[4] Hung C-C, Halonen K. “Micropower CMOS GM-C filters forspeech signal processing”. IEEE International Symposium on Circuit and Systems. 1997. p. 1972–4.

[5] Rodriguez-Villegas, E, Yufera, A, Rueda, A, A 1.25-V micropower G(m)-C filter based on FGMOS transistors operating in weak inversion, IEEE J SOLID-ST CIRC, 2004, Vol: 39, Pages: 100 - 111, ISSN: 0018-9200

[6] Sung-Hyun Yan, etc., “A Novel CMOS Operational Transconductance Amplifier Based on a Mobility Compensation Technique”, ” IEEE Trans. Circuits Syst. II, Expr. Briefs, vol. 52, no. 1, pp. 37–42,Jan. 2005.

[7] S.Solis -Bustos, J.Silva-Martinez, “A 4 Hz LowPass Continuous-Time Filter", IEEE International Conference on Electronics, Circuits and Systems

1998, Vol. 1, pp.169-172

[8] Masood-ul-Hasan, et al., “Second-order OTA-C Filters using a Single OTA ”, Proceedings of the 2005 European Conference on Circuit Theory and Design, 2005, Vol: 2, Pages:201-204

[9] Glinianowicz, J., Jakusz, J., Szczepanski, S. and Sun, Y., "A high-frequency two-input CMOS OTA for continuous-time filter applications," IEEE Proceedings: Circuits, Devices and Systems 147(1), pp. 13-18, 2000.

[10] Omeni, O, Rodriguez-Villegas, E, Toumazou, C, “A micropower CMOS continuous-time filter with on-chip automatic tuning”, IEEE T CIRCUITS-I, 2005, Vol: 52, Pages: 695 - 705, ISSN: 1057-7122

[11] X. Zhang and E. I. El-Masry, “A Novel CMOS OTA Based on Body -Driven MOSFETs and its Applications in OTA-C Filters,” IEEE Transactions on Circuits and Systems -I, Vol. 54, No. 6, June 2003, pp. 1204 – 1211.

[12] Krummenacher and Joehl,”A 4-MHz CMOS Continuous-Time Filter with On-Chip Automatic Tuning," IEEE Journal of Solid-State Circuits, 23(3):750-758, 1988

[13] C. Yoo, S.-W. Lee, and W. Kim, "A ± 1.5 V, 4-MHz CMOS continuous-time filter with a single-integrator based tuning." IEEE J. Solid-State Circuits, vol. 33, no. 1, 1998.

[14] E. Ibaragi, S. Nishioka, A. Hyogo, K. Sekine: A CMOS OTA free from second order effects with a high input resistance Gm control terminal. ISCAS (1) 2001: 300-303

[15] Koziel S, Schaumann R, Xiao H. Analysis and optimization of noise in continuous-time OTA-C filters. IEEE Transactions on Circuits and Systems I 2005; 52(6):1086–1094

[16] Peter M. VanPeteghem, et al.， “A Very-Linear CMOS Transconductance Stage for OTA-C Filters”, IEEE 1989 Custom Integrated Circuits Conference; pp. 25.3.1-25.3.4

[17] K.Su,”Analog Filters”,Kluwer Academic Publishers,2002

[18] R.Schaumann, M. Valkenburg, “Design of Analog Filter”, Oxford University Press, 2001

[19] Z. Y. Chang, et al, ”A Highly Linear CMOS Gm-C BandPass Filter for Video Applications", IEEE Custom Integrated Circuits Conf. 1996

[20] E. S. Sinencio and J. S. Martinez, ¡§CMOS transconductance amplifiers, architectures and active filters: A tutorial,¡¨ in IEE Proc. Circuits Devices Syst., vol. 147, pp. 3V12, Feb. 2000.

[21] J. Chen, E. Sanchez-Sinencio, and J. Silva-Martinez, "Frequency -Dependent Harmonic Distortion Analysis of a Linarized Cross-Coupled CMOS OTA and its Application to OTA-C Filters" IEEE Transaction on Circuits and Systems I: Regular Papers: Vol. 53, Issue:3 pp499-510, March 2006.

[22] A. Lewinski and J. Silva-Martinez, “OTA linearity enhancement technique for high frequency applications with IM3 below □65 dB,” IEEE Trans. Circuits Syst. II, Expr. Briefs, vol. 51, no. 10, pp. 542–548, Oct.2004.

[23] R. Rieger, A. Demosthenous, and J. Taylor, “Continuously tunable, very long time constant CMOS integrator for a neural recording implant,” in Proc. 29th European Solid-State Circuits Conf. (ESSCIR’03), Estoril, Portugal, pp. 441-444, Sep. 2003

[24] A. T. Behr, M. C. Schneider, S. N. Filho and C. G. Montoro, "Harmonic distortion caused by capacitors implemented with MOSFET gates." IEEE Journal of Solid-State Circuits 27, pp. 1470-1475, 1992.

[25] Zele, R. H. and Allstot, D. J., "Low-power CMOS continuous-time filters." IEEE Journal of Solid-State Circuits 31(2), pp. 157- 168, 1996.

[26] Z. Zhang, A. Celik, P. Sotiriadis, "State Space Harmonic Distortion Modeling in Weakly Nonlinear, Fully Balanced Gm-C Filters - A Modular Approach Resulting in Closed Form," IEEE Trans. Circuits Syst. I, Vol. 53, No. 1, Jan. 2006, pp. 48--59.

[27] Silva-Martinez et al, "A Large-signal very low-distortion transconductor for high frequency continuous-time filters," IEEE Journal of Solid-State Circuits vol. 26, No. 7 pp. 946-955, July. 1991

[28] U. Yodprasit, J. Ngarmnil, “Micropower transconductor for very-low frequency filters,” IEEE Asia-Pacific Conference on Circuits and Systems, 1998, p 5-8

[29] H. Voorman and H. Veenstra, “Tunable High-Frequency Gm-C Filters”, IEEE J. Solid-State Circuits, vo. 35, no. 8, pp.1097-1108, Aug. 2000.

[30] Ziyou Tan, “CMOS OTA Principles and its applications in Filters”,Master

Thesis, Hunan University, China, 2007

[31] S. Koziel and S. Szczepanski, "Design of highly linear tunable CMOS OTA for continuous-time filteres." IEEE Trans. Circuits and Systems-II, vol. 49, no. 2, pp. 110-122, 2002.

[32] Szczepanski, S. Wyszynski, A. and Schaumann, R., "Highly linear voltage-controlled CMOS transconductors." IEEE Trans. on Circuits and Systems I 40(4), April 1993.

[33] A.MOURABITEL G.LU P.PITTET, "Wide-Linear-Range subthreshold OTA for low-power, low-voltage and low-frequency applications", IEEE Transactions on Circuits and Systems I : Fundamental Theory and Application2005

[34] P. Wu, R. Schaumann, and S. Szczepanski, "A CMOS OTA with improved linearity based on current addition," Proc. IEEE Int. Symp. Circuits and Systems, (1990), 2296-2299.

[35] S.Solis Bustos, J.Silva, F.Maloberti, E.Sánchez Sinencio, "A 60dB Dynamic Range CMOS Sixth-Order 2.4Hz Low-Pass Filter for Medical Applications", TCAS-II, V.47, n°12, pp.1391--98, Dec.2000.

[36] R. van Langevelde and F.M. Klaassen, "Accurate Drain Conductance Modeling for Distortion Analysis in MOSFETs," IEDM Tech. Dig., pp.313 -317, 1997; ibid., Ph.D. Thesis, Univ. of Techn. Eindhoven, 1998.

[37] S. Szczepanski, J. Jakusz, and R. Schaumann, "A linear fully balanced CMOS OTA for VHF filtering applications." IEEE Transactions on Circuits

and System, vol. 44, no. 3, pp. 174- 187, 1997.

[38] F. Rezzi, A. Baschirotto, and R. Castello, "A 3V 12-55MHz BiCMOS pseudo-differential continuous-time filter." IEEE Trans. Circuits and Systems-II, CAS-42, pp. 896-903, Nov. 1995.

[39] P.G.Corbishley and E.Rodriguez-Villegas,"Design Tradeoffs in low-power low-voltage transconductors in weak inversion", IEEE Midwest Simposium on Circuit and Systems,2006

[40] G. Duzenli, Y. Kilic, H. Kuntman, and A. Atamam, "On the design of low-frequency filters using CMOS OTAs operating in the subthreshold region.",Microelectronics Journal, vol. 30, pp. 45-54, 1999

[41] W. Liu, A. Andreou, and M. Goldstein, "Voiced-speech representation by an analog silicon model of the auditory periphery." IEEE Transactions of Neural Networks 3(3), pp. 477-487, 1992.

[42] R. Harrison and C. Charles, "A low-power, low-noise CMOS amplifier for neural recording applications." IEEE J. Solid-State Circuit, vol. 38, pp. 958-965, June 2003.

[43] S.P. DeWeerth, G.N. Patel, and M.F. Simoni, "A variable linearrange subthreshold OTA." , Electronics Letters, vol. 33, no. 15, pp. 1309-1311, 1997.

[44] S. Chatterjee, Y. Tsividis, and P. Kinget, "0.5-V analog circuit techniques and their application in OTA and filter design," IEEE J. Solid-State Circuits, vol.40, no.12, pp.2373–2387, Dec. 2005.

[45] Antonio J. Lopez-Martin et al., “Low-Voltage Super Class AB CMOS

OTA Cells with Very High Slew Rate and Power Efficiency", IEEE Journal of Solid-State Circuits, vol. 40, No. 5, May 2005, pp. 1068-1077.

[46] A. Mohiedin, et al., "A fully balanced pseudo-differential OTA with common-mode feedforward and inherent common-mode feedback detector" IEEE Journal of Solid-State Circuits, vol. 38, no. 4, pp. 663–668, 2003

[47] P. Pankaj, J. Silva-Martinez, and X. Liu, "A CMOS 140mW 4th-Order Continuous-Time LowPass Filter Stabilized With a Class AB Common-Mode Feedback Operating at 550MHz" IEEE Transaction on Circuits and Systems I: Regular Papers: Vol. 53, Issue:4 pp811-820, April 2006.

[48] Nedungadi, A. and Viswanathan, T. R., "Design of linear CMOS transconductance element." IEEE Trans. Circuits and Systems, 31, pp. 891-894, October 1984.

[49] Ko-chi Kuo , A.Leuciuc, "A novel linear tunable MOS transconductor", Proceedings of the 43rd IEEE Midwest Symposium on Circuits and Systems, Volume: 1, On pages: 462-465 vol.1 2000.

[50] J. Silva-Martinez, M. Steyaert and W. Sansen, "A 10.7MHz 68dB SNR CMOS continuous-time filter with on-chip automatic tuning," IEEE J. Solid -State Circuits, vol. 27, no.12, pp. 1843-1853, December 1992.

[51] J. Silva-Martínez and J. Salcedo-Suner, "IC Voltage to Current Transducers with Very Small Transconductance", Analog Integrated Circuits and Signal Processing, vol. 13, pp. 285-293, July 1997.

[52] M. Steyaert, J. Crols, S. Gogaert, and W. Sansen, "Low-voltage analog

CMOS filter design", IEEE Int. Symp. Circuits Syst. 1993, vol.2, pp.1447-1450, May 1993.

[53] Y. Tsividis, Z. Czarnul, S. C. Fang, "MOS transconductors and integrators with high linearity." Electronics Letters 22(5), pp. 245-246, 1986

[54] SEEVINCK, E., and WASSENAAR, R F.: 'A versatile CMOS linear transconductor/square-law function circuit', IEEE J. Solid-state Circuits, 1987, 22, pp. 366377

[55] Z. Wang, "Novel linearization technique for implementing large-signal. MOS tunable transconductance," Electron. Lett., vol. 26, Jan. 1990.

[56] czarnul, z., and tsividis, y.: 'MOS tunable transconductor', ibid., 1986, 22, pp. 721-722

[57] FILHO, S.N., SCHNEIDER, M.C., and ROBERT, R.N.G.: 'New CMOS OTA for fully integrated continuous-time circuit applications', Electron. Lett., 1989, 25, (24), pp. 16741675

[58] SONG, B.S.: 'CMOS RF circuits for data communications applications', IEEE J. Solid-State Circuits, 1986, SC-21, pp. 310-317

[59] NAUTA, B.: 'CMOS VHF transconductance-C lowpass filter', Electron. Lett., 1990, 26, pp. 421422

[60] Z. Czarnul, "Modification of the Banu-Tsividis continuous-time integrator structure." IEEE Trans. Circuits Syst., vol. 33, pp. 714- 716, 1986.

[61] HAN, G., and SANCHEZ-SINENCIO, E.: 'CMOS transconductance multipliers: a tutorial', IEEE Trans. Circuits Syst. II, Analog Digit. Signul

Process., 1998, 45, pp. 155G1563

[62] PENNOCK, J.L.: 'CMOS triode transconductor for continuous-time active integrated filters', Electron. Lett., 1985, 21, pp. 817-818

[63] WANG, Z., and GUGGENBUHL, W.: 'A voltage-controllable linear MOS transconductor using bias offset technique', IEEE J. Solid-State Circuits, 1990, 25, pp. 315-317

[64] M. Banu, J. M. Khoury, and Y. Tsividis, "Fully differential operational amplifiers with accurate output balancing", IEEE Journal of Solid-State Circuits, Vol. 23, pp. 1410-1414, Dec. 1988.

[65] Prabir C. Maulik, L. Richard Carley, David J. Allstot, "Sizing of Cell -Level Analog Circuits Using Constrained Optimization Techniques", IEEE Journal of Solid-State Circuits, Vol. 28, pp.233-241, March 1993.

[66] Maria del Mar Hershenson, Stephen P. Boyd, Thomas H. Lee, "Optimal Design of a CMOS Op-amp via Geometric Programming", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 20, pp. 1-21, Jan. 2001.

[67] S. L. Wang, "Novel drain-biased transconductance building blocks for continuous-time active filters." Electron. Lett. 25, 100-101, 1989

[68] K. J. Lee, W. C. Wang, and K. S. Huang, "A current-mode testable design of operational transconductance amplifier-capacitor filters," IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process., vol. 46, no. 4, pp. 401-413, Apr. 1999

[69] Z. Wang and W.Guggenbuhl, “A voltage-controllable linear MOS transconductor using bias offset technique,” IEEE Journal of Solid-State Circuits, vol. 25, pp. 315-317, Feb. 1990

[70] A. Coban and P. Allen, Low-voltage CMOS transconductance cell based on parallel operation of triode and saturation transconductors, Electron. Lett. 30 (1994), pp. 1124–1126

[71] Michael Trakimas, Sameer R. Sonkusale: A 0.5V Bulk-Input Operational Transconductance Amplifier with Improved Common-Mode Feedback. ISCAS 2007: 2224-2227

[72] Pradip Mandal, V. Visvanathan, “CMOS Op-Amp Sizing Using a Geometric Programming Formulation”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 20, pp. 22-38, Jan. 2001.

[73] National Semiconductor, “A Basic Introduction to FiltersÐActive, Passive, and Switched-Capacitor”[Online]

[74] Mohieldin, E. Sánchez-Sinencio, and J. Silva-Martínez, “A Fully Balanced Pseudo-Differential OTA With Common-Mode Feedforward and Inherent Common-Mode Feedback Detector” , J.Solid-State Circuits, vol. 38, pp. 663-668, April2003.

[75] Haideh, Khorramabadi, et al., ”High-Frequency. CMOS Continuous-Time. Filters”. IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. SC-19, NO. 6, DECEMBER 1984. 939.

[76] Degrauwe, M. G., Rijmenants, J., Vittoz, E. A. and DeMan, H., "Adaptive

biasing CMOS amplifiers." IEEE Journal of Solid-State Circuits SC-17, pp. 522-528, 1982

[77] Un-Ku Moon,"LINEARITY IMPROVEMENT TECHNIQUE FOR CMOS CONTINUOUS-TIME FILTERS", Doctoral dissertation, University of Illinois at Urbana-Champaign, 1994

[78] Edgar Sanchez-Sinencio,"Common Mode Feed Back Techniques: A Tutorial", Texas A&M University(Online)

[79] Arun Ramachandran, "Nonlinearity and Noise Modeling of Operational Transconductance Amplifiers for Continuous Time Analog Filters", Master thesis, Texas A&M University, 2005

[80]Yuanyuan Fu, "Study on Fully-Integrated Current-mode Continuous-time Filter Based on OTA-C and its Layout", Master Thesis, Jilin University, China,2006

[81] Ying Long, "Study on Fully Integrated Continuous-time OTA-C Active Filters", Master Thesis, Hunan Normal University, China,2006

[82] Jialong Zhang,"Design of Active Analog Filter Based on Floating-gate Technology", Master thesis, Hunan University, China, 2005

[83] Cui Wang, "The Design and Study of Active filter based on the Amplifier Operator in the circuit", Master thesis, Nanjing University of Science and Technology, China,2006

[84] Wenxiao Shi, "The study of fully Integrated Current-mode Continuous -time Filter", Doctoral Dissertation, Jilin University, China, 2006

[85] C.C.Enz, F.Krumenacher, and E.A.Vittoz, “A Basic Property of MOS Transistor model valid in all regions of operation amd dedicated to low-voltage and low-current applications”, Analog Integrated Circuits Signal Process., Vol.8, pp83-114,1995

[86] K.Laker and W.Sansen,”Design of Analog Integrated Circuits and Systems”, McGraw-Hill International, 1994

[87]W.Sansen,” Analog Design Essentials”,Springer 2006

[88] Behzad Razavi, “Design of Analog CMOS Integrated Circuits”,McGraw -Hill International, Edition 2001

[89] P.R.Gray, P.J.Hurst, S.H.Lewis, and R.G.Meyer, Analysis and Design of Analog Integrated Circuits, 4th ed. New York: Wiley,2001

[90]P.E.Allen and D.R.Holberg, CMOS Analog Circuit Design, 2nd ed. New York: Oxford Univ. Press,2002

[91] D. A. Johns and K. Martin, "Analog Integrated Circuit Design", John Wiley & Sons, 1997.

[92] Y. Tsividis, “Integrated continuous-time filter design—An overview,”. IEEE J . Solid-State Circuits, vol. 29, no. 3, pp. 166–176, Mar. 1994.

[93] Geiger, R. L. and Sanchez-Sinencio, Edgar, "Active-Filter Design using Operational Transconductance Amplifiers: A Tutorial, " IEEE Circuits and Devices Magazine, Vol. 1, Number 2, pp. 20-32, March, 1985

[94] E. Vittoz, J. Fellrath, “CMOS analog circuits based on weak inversion operation”, IEEE J. Solid State Circuits, vol.12, pp.224, 1977

[95] R.R.Harrison,"The MOS Transistor in Weak Inversion", EE 5720/ University of Utah. [Online].

[96] J Madrenas et al., "A CMOS analog circuit for Gaussian functions", IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing. Vol.43, No. I, Jan.1996

[97]A.Cunha et al., "An MOS transistor model for analog circuit design", IEEE J.Solid-State Circuits, vol.33, pp.1510-1519, Oct. 1998

[98] D.J.Comer, D.T.Comer," Operation of analog MOS circuits in the weak or moderate inversion region", IEEE Transactions on Education,Volume 47, Issue 4, Nov. 2004 Page(s): 430 - 435

[99]R.Fried, C.Enz, "Nano-amp, active-bulk, weak-inversion analog circuits", Custom Integrated Circuits Conference, 1998. Proceedings of the IEEE 1998 Volume , Issue , 11-14 May 1998 Page(s):31 - 34

[100]C.C.Enz, F.Krumenacher, and E.A.Vittoz," A Basic Property of MOS Transistor model valid in all regions of operation amd dedicated to low-voltage and low-current applications", Analog Integrated Circuits Signal Process., Vol.8, pp83-114,1995

[101]M.B.Barron,"Low level currents in insulated gate field effect transistors", Solid-State Electron., vol.15, pp.293-302, Mar.1972

[102]Matthias Bucher et al, "The EKV MOSFET Model for Circuit Simulation", Swiss Federal Institute of Technology [Online]