Stony Brook University

Physically and Logically Reversible Superconducting Circuit

A Dissertation Presented

by

Jie Ren

to

The Graduate School

in Partial Fulfillment of the

Requirements

for the Degree of

Doctor of Philosophy

in

Physics

Stony Brook University

May 2011

Stony Brook University

The Graduate School

Jie Ren

We, the dissertation committee for the above candidate for the

Doctor of Philosophy degree, hereby recommend

acceptance of this dissertation.

Vasili Semenov – Dissertation Advisor
Research Professor, Department of Physics and Astronomy

Dmitri Averin – Chairperson of Defense
Professor, Department of Physics and Astronomy

Gene Sprouse
Professor, Department of Physics and Astronomy

Peter Shkolnikov
Deputy Director, Sensor CAT
Adjunct Professor, Department of Electrical and Computer Engineering

This dissertation is accepted by the Graduate School

Lawrence Martin
Dean of the Graduate School

Abstract of the Dissertation

Physically and Logically Reversible Superconducting Circuit

by

Jie Ren

Doctor of Philosophy

in Physics

Stony Brook University

2011

Prior to early this century, the semiconductor microprocessor can be scaled according to the Moore's law, basically doubling its performance in every 18 months. Only recently, the energy efficiency of semiconductor integrated circuits has become a concern than their computational capabilities since their power dissipation scales nonlinear with clock frequency. The specific energy dissipation per logic operation for a modern semiconductor computer is still over 6 orders of magnitude above the thermodynamic threshold k_BTln2. It has been known for a long time that this thermodynamic limit on the energy dissipation per logic operation can be overcome by physically and logically reversible circuits. Reversible circuits based on nSQUIDs (negative SQUIDs) or dc SQUIDs (superconducting quantum interference device) with negative mutual inductance between the arms of the SQUID loop, are introduced and investigated in this thesis.

First test reversible circuit contains one 8-stage shift register, cells that transfer the input data

to the outputs. Dynamic of this circuit illustrates unique properties which agree well with theoretical analysis. Based on the knowledge from the study of shift register, a new timing belt clocking scheme built upon the moving vortices along long Josephson junction (LJJ) is introduced and analyzed. The test circuits for this new scheme contain two 8-stage shift registers, one with direct and the other with inverted outputs. The energy dissipation per nSQUID gate per bit measured for these test circuits at 4 K temperature is already below the thermodynamic threshold. A family of logical gates based on the new timing belt and nSQUIDs shift register are continued to be developed and these gates are capable of fundamentally low energy dissipation and the ability to operate in both irreversible and reversible modes. Moreover, the extremely low energy dissipation in these circuits makes them a natural candidate to support circuitry working in quantum mode with unique advantages.

Table of Contents

List of Figures

Acknowledgements

I feel really honored and privileged to spend the past six years at Stony Brook University studying towards my doctoral degree. During this period, I received continuous help, support and encouragement from many people around me. This thesis would not be possible without them.

First and foremost, I own my deepest gratitude to **Professor Vasili K. Semenov**, a great advisor and mentor to me both academically and intellectually. His enthusiasm in science and engineering inspired me from the beginning of my graduate study. His continuous encouragement and guidance helped me in all the time of research and writing of this thesis.

Secondly, my sincere appreciation goes to many amazing collaborators that I have had the honor to work with on diverse exciting projects. I thank **Dr. Yuri Polyakov** for teaching me all the measurement equipments. His technical support helped me overcome many hurdles in several projects. I am truly grateful to Dr. Polyakov since I have benefited a great deal from working with him. I also thank **Professor Dmitri V. Averin** from SUNY at Stony Brook, **Dr. Stefano Poletto** from Karlsruhe Institute of Technology in Germany, and **Dr. Irina Kataeva** from Nagoya University in Japan for their helpful advice and discussion in various ways during my Ph. D study. I would also like to thank **Hypres Inc.** fabrication team for fabricating all the circuits I designed.

Thirdly, I extend my thanks to my colleagues in the Semenov Research Group, **Supradeep Narayana, Nathan Broggrern** and **Jie Yu**, all of whom have contributed so much to my studies and lives in their own way.

Last and most importantly, I would like to thank my family. My husband, **Xiaoping Liu**, is my ultimate support in every aspect of life. I simply could not achieve anything without him. I thank my parents and my brother for pushing me to be the best and for their unconditional support in every adventure that I choose to explore.

Chapter 1 Introduction

1.1. Superconducting and Josephson Junction (JJ)

Superconductivity was discovered by H. Kamerlingh Onnes in 1911 [1], just 3 years after he had the first liquefied helium. What he observed was that the electrical resistance of various metals such as mercury, lead and tin disappeared completely in a small temperature range near a critical temperature T_C, which is a characteristic of the material. For decades, many scientists were devoted in this field, and a remarkably complete and satisfactory theoretical picture of the classic superconductors merged in 1950s and 1960s. However, after the discovery of new class of high-temperature superconductors by Bednorz and Müller in 1986 [2], the subject was revitalized. This class of superconductors seems to obey the same general phenomenology as the classic superconductors, but with unknown basic microscopic mechanism so far.

Besides the perfect conductivity, the second hallmark of superconductor is perfect diamagnetism, found in 1973 by Meissner and Ochsenfeld [3]. This hallmark is also called Meissner effect. They found that not only a magnetic field is excluded from entering a superconductor, as might happen to perfect conductor, but also that a field in an originally normal sample is expelled as it is cooled through T_C. Actually, London equation [4] explains that the magnetic field in a superconductor decays exponentially from whatever value it possesses at the surface with a characteristic length called London penetration depth λ_L (typical value is 0.1 μm).

The formulation of these phenomenological theories was introduced by Londons [4] and by Ginzburg and Landau [5]. And eventually, Bardeen, Cooper and Schrieffer (BCS) created the well known microscopic BCS theory [6]. It was shown that even a weak attractive interaction between electron causes an instability of the ordinary Fermi-sea ground state of the electron gas with respect to the formation of bound pairs of electrons occupying states with equal and opposite momentum and spin, which are called Cooper pairs. These Cooper pairs have a spatial extension of order, which comprises the superconducting charge carriers anticipated in the phenomenological theories. The macroscopic variables (for example, current) depend on the phase of the wave function of Cooper pairs, which changes in a "quantum way" [5] under the action of an electromagnetic field. This quantum dependence leads not only to the two hallmarks mentioned above, but also to other unconventional effects like Josephson effect [7] and magnetic flux quantization [8, 9].

In a simple word, the magnetic flux quantization means the flux trapped in a 'hole' inside a superconductor is quantized in unit of Φ_0, where

$$\Phi_0 = \frac{h}{2e} \simeq 2.068 \times 10^{-15} V \cdot s. \tag{1.1}$$

Actually, this forms the basis of data encoding in RSFQ technology [10], which will be discussed later in this chapter.

Josephson effect [11] is the phenomenon of electric current tunneling across a Josephson junction (Figure 1.1), which is consisted of two weekly linked superconductors. The tunnel barriers between two superconducting electrodes can be a thin layer of insulator, a thin metal, a point contact or other kind of weak links. The basic equations govern the DC and AC Josephson

effects are shown in the followings:

$$I_S = I_C \sin\varphi, \tag{1.2}$$

$$V = \frac{\hbar}{2e}\frac{d\varphi}{dt}. \tag{1.3}$$

In the above equations, I_S and V are the supercurrent and voltage across the Josephson junction, φ is the gauge invariant phase difference of the phases of the macroscopic wave functions of the two superconducting electrodes, and I_C is the critical current of the Josephson junction.

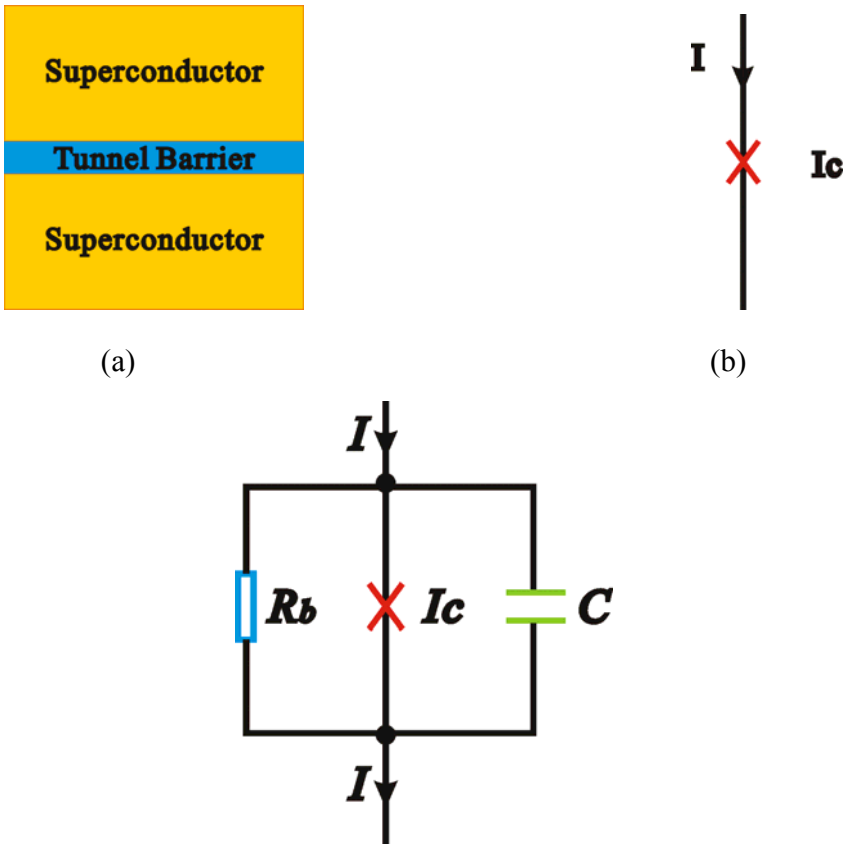


Figure 1.1. (a) Physical construction of a Josephson junction: two pieces of superconductors separated by a tunnel barrier, (b) circuit schematic for Josephson junction, (c) equivalent circuit of RCSJ model.

The DC Josephson effect (described by Eq. (1.2)) shows the tunneling of current through a

weak link without any applied voltage. The maximal current, limited by I_C, is a sinusoidal function of φ. The AC Josephson effect (described by Eq. (1.3)) illustrates the dependence of voltage of a Josephson junction on φ when the current through the junction is larger than critical current I_C. In case an average voltage V exists across the junction, which gives continuous oscillations of the phase φ with the angular frequency ω:

$$\omega = \dot{\varphi} = \frac{2e}{\hbar} V = \frac{2\pi}{\Phi_0} V. \tag{1.4}$$

Resistively and capacitively shunted junction (RCSJ) model is widely used in the analysis of Josephson junction dynamics, especially for that of weak links. RCSJ model can be claimed quantitatively valid in a narrow temperature range just below the critical temperature *Tc*, or for any type of Josephson junctions externally shunted by some circuit of small resistances and inductance. The equivalent circuit of RCSJ model is sketched in Figure 1.1(c), in which JJ is modeled by an ideal one described by Eq. (1.2), shunted by a resistor R_b and a capacitor C. The dynamics of JJ can be expressed by

$$I = I_C \sin\varphi + \frac{2\pi}{\Phi_0 R_b}\frac{d\varphi}{dt} + \frac{2\pi C}{\Phi_0}\frac{d^2\varphi}{dt^2}. \tag{1.5}$$

The dynamics of the phase difference φ is analogous to the motion of a point-like particle of mass ($\sim C$) and friction coefficient ($\sim 1/R_b$) moving on a tilted washboard potential. And here introduces a very important parameter of JJ, Stewart-McCumber parameter β_C:

$$\beta_C = \frac{2\pi}{\Phi_0} I_C R^2 C, \tag{1.6}$$

which is comparable with quality factor Q ($\sim \beta_C^{\frac{1}{2}}$) of the point-like particle damping system.

When $\beta_C \ll 1$, JJ is over-damped, which means that by reducing the bias current from above I_C, the particle gets trapped instantly in one of the minima of the washboard potential at $I = I_C$, i.e. resulting in non-hysteretic *I-V* characteristics. On the other hand, when $\beta_C \gg 1$, JJ stays in under-damped limit, Hence, the dc voltage stays finite even for $I < I_C$ until the current is reduced to 0. In contrast, when the current is increased from 0, junction stays in 0 voltage state until $I = I_C$.

The above parameters of the Josephson junction can be quite different depending on materials used and the way how the Josephson junction has been formed. The most common type is the Superconductor/Insulator/Superconductor (SIS) Nb/AlOx/Nb tunnel junctions. These junctions typically have $\beta_C \gg 1$. When the current exceeds the critical current, the junction transits into a resistive state with voltage equal to the gap voltage of the electrodes, $V = 2\Delta \approx 2.6$ mV. At a higher current the voltage scale is given by the so-called characteristic voltage, $V_C = I_C R_N$, for tunnel junctions which is about $V_C = \pi\Delta / 2e$.

The unique properties of superconductors lead to many applications, e.g., high-current transmission lines, high-sensitive magnetometer, or high-field magnets. Superconductors have already been used in MRI machines [12]. They have also been used in beam-steering magnets in particle accelerators [13], where the superconducting magnet coils produce a large and uniform magnetic field. SQUID [14, 15] magnetometer may be the most sensitive measurement device known to man. The schematic of SQUID is shown in Figure 1.2, The voltage (V) in this case is a function of the applied magnetic field and the period equal to Φ_0.

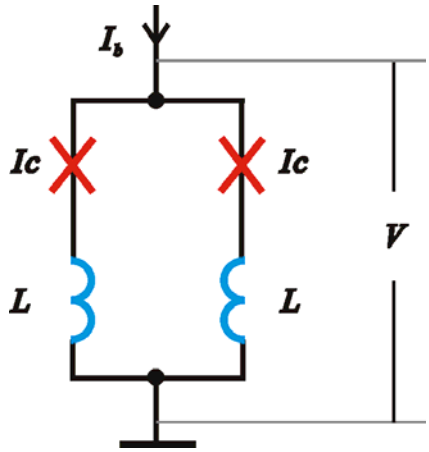


Figure 1.2. Schematic of a DC SQUID. Critical current of each JJ inside is I_C, and the loop inductance is $2L$. When the SQUID is biased by a current I_b, output voltage V is periodic to external magnetic field.

Also, the very low resistance, very high frequency operation and Josephson effect of the superconductors has lead to the rapid development of superconducting electronics. Niobium, with a critical temperature of around 9.2 K, is the mostly used superconducting material for superconducting electronics. In 1985, Rapid single flux quantum (RSFQ) technology [10] was introduced as a new approach to the existing Josephson junction digital computing system. In RSFQ the binary state is not presented by the DC voltage state of the gates but by magnetic flux quanta expressed in very short voltage pulses. In this thesis, we will focus on the application of using JJ as the basic element for the construction of a physically and logically reversible computing circuit.

1.2. Long Josephson Junction

Long Josephson junction (LJJ) is a kind of Josephson junction which has one or more dimensions longer than Josephson penetration depth λ_J (typical value is 10 μm). Compared with the (short) JJ, the phase difference in LJJ is a variable on both time and dimension scale.

Figure 1.3 shows the equivalent circuit of a one-dimension LJJ. In this equivalent circuit, the LJJ can be interpreted by a series of JJs connected in parallel by inductance L' and surface resistance R_S. In the figure, j_B is bias current, j_C is critical current, R is shunt resistance and C is capacitance of the JJ. A large variety of LJJs have been thoroughly investigated both theoretically and experimentally. The properties of continuous LJJs are described by the sine-Gordon equation traced back to 1870 [16, 17]:

$$\varphi_{xx} - \varphi_{tt} = \sin\varphi + \alpha\varphi_t - \beta\varphi_{xxt} - \eta, \tag{1.7}$$

where $\alpha = \dfrac{1}{RC\omega_p}$, $\beta = \dfrac{\omega_p L}{R_S}$, and $\eta = \dfrac{j_B}{j_C}$. In the above equation, time t is normalized to ω_p^{-1}, where $\omega_p = \sqrt{\dfrac{2\pi j_C}{\Phi_0 C}}$ is Josephson plasma frequency and x is normalized to Josephson penetration depth $\lambda_J = \sqrt{\dfrac{\Phi_0}{2\pi j_C \mu_0 (2\lambda_L + t_0)}}$.

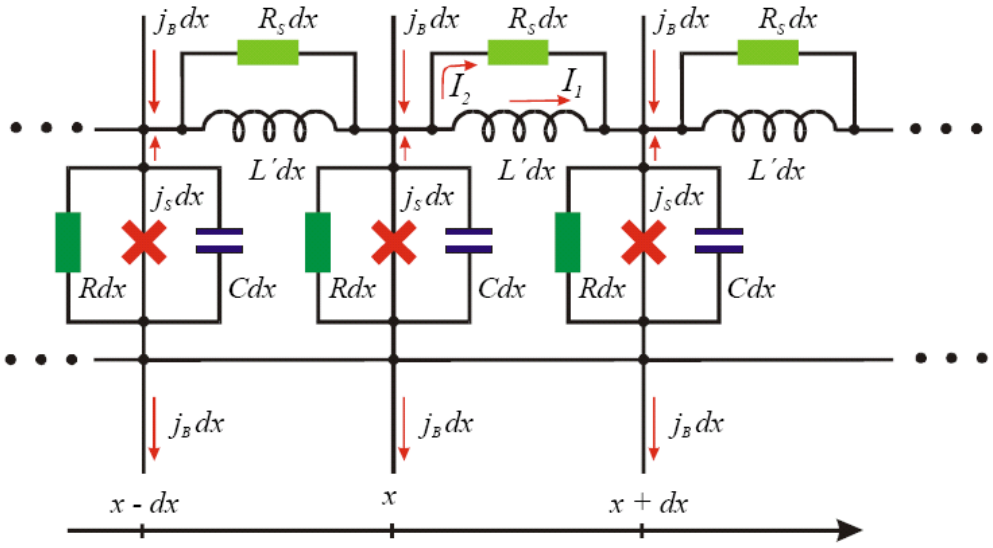


Figure 1.3. Equivalent circuit of a 1-D long Josephson junction. Notations are given per unit length along x. After Ustinov [18].

This equation is really unique because its solutions can be described as a combination of resting or freely moving vortices or solitons. In the physical language these vortices can be described as quasiparticles which are able to move along LJJs with arbitrary speeds and without any dissipation. More exactly, the speed of the nondissipative movement is limited by the Swihart speed $\overline{c}$, which is the "local" speed of electromagnetic waves in the device if the Josephson effect is not taken into account. $\overline{c}$ is defined as $\omega_p \cdot \lambda_J$.

1.3. Quantum Computing

Quantum-state engineering, i.e., active control over the coherent dynamics of suitable quantum-mechanical systems, has become a fascinating prospect of modern physics. Low-capacitance Josephson tunneling junctions offer a promising way to realize quantum bits (qubits) for quantum information processing. One of the motivations for quantum-state engineering with Josephson devices is their potential application as logic devices and for quantum computing. By exploiting the massive parallelism of the coherent evolution of superpositions of states, quantum computers could perform certain tasks that no classical computer could do in acceptable times [19]. At the most basic level, quantum computers are composed of quantum bits, or qubits, rather than the traditional bits that are the basic unit of digital computers. In contrast to the progress of developing advanced theoretical concepts of quantum computing, i.e. the ‘‘software’’, the development of physical realizations of qubits and gates, the ‘‘hardware’’, are far behind. The most up-to-date "quantum computer" can only have a few qubits [20-22], which is far from practical.

1.4. Reversible Computing

Modern supercomputers are highly scalable devices, of which the performance in principle could grow without limits. However, practical issues such as power dissipation set limits to the size and therefore to the performance of high-end supercomputers. Energy dissipation in the logic gates of modern supercomputers is still 6 orders of magnitude higher than their thermodynamic threshold [23]:

$$E_{th} = k_B T \ln 2, \tag{1.8}$$

which depends only on ambient temperature *T*. It can be easily proved if one realizes that the principal mechanism of the dynamic dissipation could be described as a charging/discharging of the parasitic gate capacitance. For a reasonable capacitance value *C* (~ 10 fF) and bias voltage *Vb* (~ 1V) the recharging energy ($E_C = C \cdot Vb^2/2$) is about $5 \cdot 10^{-15}$ J or about $1.7 \cdot 10^6$ times higher than the thermodynamic threshold that at room (300 K) temperature is $\sim 3 \cdot 10^{-21}$ J [24].

The following four paragraphs are based on text from V. Semenov [24]. Of course, when taking into account the number of single-bit logic operations associated with one floating point operation, it will help reducing the specific energy dissipation. However, by considering the facts that each floating point operation requires hundreds of single bit operations and that it is accompanied by a certain number of fixed point operations and by a reading/writing of data and result to/from memory, the energy dissipation per floating point operation can only be reduced to $3 \cdot 10^{-12}$ J, which is still way larger than the thermodynamic threshold.

Let us repeat similar estimations for specific energy dissipation for prospective superconductor RSFQ technology. The energy dissipation in its gates (in contrast with semiconductor

counterparts) could be easily scaled by proportional changing of critical currents of the Josephson junctions that serve as the building blocks of this technology. Such scaling down of the dissipated energy is limited only by an increasing error rate. The processes behind those thermally activated errors are well understood. To keep a sufficiently low energy rate the elevation of the dissipated energy over the threshold should be within 3 to 4 orders of magnitude. However, this estimation does not include the static energy dissipation in bias resistors that adds about 2 orders of magnitude and increases the total excess of dissipated energy over the thermodynamic threshold to 5 to 6 orders of magnitude. But this gain is completely offset by the low efficiency of state-of-the-art cryo-coolers that is still below 10% of the ideal (Carnot) cycle. As a result, a cryo-cooler for a prospective RSFQ high-end computer would dissipate roughly the same power as modern semiconductor supercomputers with similar performance.

Originally [25] it was supposed that Eq. (1.8) sets the fundamental limit on energy dissipated at any one-bit logic operation. However, an exception has been found: the threshold could be crossed if the logic gates are physically reversible devices and if special reversible algorithms are used. This is a highly important statement because it implies that all quantum algorithms must be reversible to prevent QCs [26] from overheating and immediate burning-out. Actually quantum mechanics prohibits any energy dissipation during the basic computational phase, and energy could and should be dissipated during error corrections, readout of the result and returning to its initial state. However these dissipation mechanisms deal with a small number of gates (qubits) and, as a result, they are able to provide very low additions for specific energy dissipation per a classical one-bit logic operation. The projected specific energy dissipation (i.e. the total energy

dissipated divided by the number of equivalent classical logic operations) should be many orders of magnitude below the thermodynamic threshold.

Unfortunately QCs are still years and even decades away from any practical devices. But more importantly this discussion gives a hint of a possibility to dramatically reduce the specific power dissipation in high-end computing systems. If the main commercial motivation behind QCs is the dramatically lower power dissipation, then reversible computers operating in classical mode could be a quick fix here. An investigation of such reversible computing circuits is the primary goal of this dissertation.

The following five paragraphs are after [27]. The general history of reversible computation was written by Bennett in 1988 [23, 28]. In fact this paper was reprinted by the journal again in 2000 [28] due to its importance and popularity. Let us reiterate some of Bennett's view points on the history of reversible computations. Bennett wrote that "⟨…⟩ the development of electronic digital computers had naturally raised the question of the ultimate thermodynamic cost of computation, especially since heat removal has always been a major engineering consideration in the design of computer ⟨…⟩ A major turning point in understanding the thermodynamics of computation took place when Landauer ⟨…⟩ was able to prove a lower bound of order kT for some data operations, but not for others. Specifically, he showed that "logically irreversible" operations – those that throw away information about the previous logical state of the computer – necessarily generate in the surroundings an amount of entropy equal to the information thrown away ⟨…⟩ A major step ⟨…⟩ [was] Edward Fredkin['s] ⟨…⟩ discovery of the billiard-ball model for computation ⟨…⟩".

In 1977 Likharev proposed that a reversible computer could be implemented using Josephson junction technology [29]. Two related but hard-to-find publications are dated 1976 [30] and 1974 [31] by Likharev. In 1982 more detailed estimations for ultimate energy dissipation within the suggested model for reversible computations were made [32]. But only at ASC-84 were the optimized parameters of the reversible gate (parametric quantron) revealed [33].

At that time a higher speed rather than lower energy dissipation was set to be the major optimization goal. As a result, RSFQ logic was suggested [10]. However, a new logic gate similar to parametric quantron was suggested by a strong Japanese research team. The gate received the new name Quantum Flux Parametron (QFP) and it was selected as a key component of a large multi-year project [34]. The energy dissipation of practical QFP gates was still far from the thermodynamic threshold (about $1,000\ k_B T$ according to the introduction in [34]) but theoretically it could approach and cross the threshold [35]. Much later parametric quantron was reinvented as INSQUID [36].

As discussed in the previous paragraph, it became clear that a minimization of energy dissipation is vitally important for some new applications, in particular, those related to quantum computation. As a result, circuits capable of operating in the reversible mode could be the ultimate winners of the race for prospective computation technologies. This is why reversible circuits was brought up again in the early 21^{th} century [37]. The main or even fatal drawback with known reversible gates was rather evident: multi-phase AC power supply. The drawback originated from large ($\sim 10^3 k_B T$) energy streams that should flow to and then back from any reversible gate at each clock cycle. Electrical losses in the AC power lines should definitely be

considered as part of the total energy dissipation and this means that in order to keep the losses per gate below the $k_B T$ level, the power line should recycle 99.9% of the applied energy or it should operate as a resonator with quality factor exceeding 10^3. This alone is an almost impossible task if the opposite sides of "the resonator" are at room and helium temperatures respectively, on wonder for the case when more similar power lines with identical resonant frequencies are needed.

In [37] it is pointed out that a DC biased Josephson junction is a natural and fundamentally accurate DC/AC converter which is able to AC bias reversible gates. Moreover, each converter is integrated with its gate. As a result, the new device operates as a DC biased reversible gate. The first DC biased reversible gate was suggested earlier [36] but the new nSQUID [37] is much more robust, its unique properties which will be reviewed and discussed in Chapter 2.

One important aspect of the nSQUID circuits is that they can be usefully operated in the classical mode [37]. In this capacity, they are positioned as the physically and logically reversible digital circuits [32, 38] with extremely low energy dissipation that can approach or even cross the psychologically important thermodynamic threshold of $k_B T \ln 2$ per logic operation. This energy dissipation is about 4 orders of magnitude smaller that the energy dissipation in RSFQ circuits.

The next part of this thesis is organized as followings. Shift register was chosen to be the first test reversible circuit based on nSQUID, and the first iteration of design without a return path will be discussed in Chapter 3. There, we miss the second key component of our circuitry is a Long Josephson Junction (LJJ). In Chapter 4 we will review its properties that are crucial for our

original “timing belt” clock scheme. Later in Chapter 5 and Chapter 6, a series of circular shift register, which demonstrate energy dissipation comparable to thermal dynamics threshold, and some other logical gates with return paths, will be discussed. Also, the nSQUID circuits can be used as the natural basis for implementation of the universal adiabatic quantum computation (UAQC) [39], and this application will be demonstrated in Chapter 7.

Chapter 2 Basic Properties of nSQUID

2.1. Introduction

The basic gate of reversible circuits: nSQUID, i.e., dc SQUID with negative mutual inductance between the arms of the SQUID loop, was introduced several years ago [37] and was further improved later [40]. Due to its importance, the most impressive properties of the nSQUID described in [37] and [40] will be reviewed in this chapter with some new analytical results.

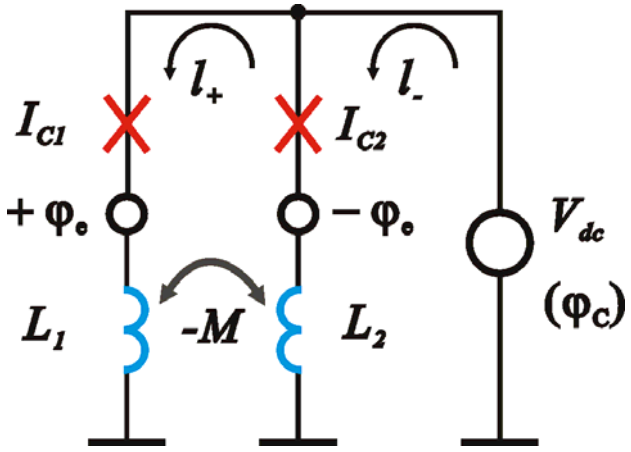


Figure 2.1. Schematic of an nSQUID biased with DC voltage source. $Ic_{1,2}$ are critical currents of two JJs. $L_{1,2}$ are inductances of two arms of the nSQUID. M is the absolute value of mutual inductance between L_1 and L_2 of the two arms. l_- and l_+ are dimensionless effective inductances corresponding to 'sum' and 'differential' mode of the system respectively, respectively. φ_e is magnetic flux applied externally to the nSQUID loop, while φ_c is clock phase applied by external DC voltage source.

As shown in Figure 2.1, the structure of the nSQUID is very similar to a conventional DC SQUID (Figure 1.2) but only differs from the DC SQUID by having a negative mutual inductance $-M$ between two parts of the SQUID loop inductances. This negative mutual inductance solves the conflicting need for the nSQUID system's two degrees of freedom. It

makes the system's effective inductance very different for the 'sum' and 'differential' modes of the system. The inductance of 'sum' mode is small enough to eliminate bi-stable state and thus quenches the dynamic property in this degree of freedom. On the other side, the large effective inductance corresponding to 'differential' mode enables a bi-stable energy profile to process computation [37, 39, 40].

The energy of the nSQUID in a symmetric case can be quantitatively analyzed. When $I_{C1} = I_{C2} = I_C$ and $L_1 = L_2 = L$, potential energy of the nSQUID can be expressed in terms of φ_+ and φ_- as:

$$\frac{U(\varphi_+, \varphi_-)}{\Phi_0 I_c / 2\pi} = \left(\frac{(\varphi_+ - \varphi_c)^2}{l_-} + \frac{(\varphi_- - \varphi_e)^2}{l_+} \right) - 2\cos\varphi_+ \cos\varphi_-, \tag{2.1}$$

where φ_e is magnetic flux applied externally to the nSQUID loop, φ_c is clock phase applied by external DC voltage source, φ_+ is the common phase of two JJs in the nSQUID as $\varphi_+ = \frac{\varphi_1 + \varphi_2}{2}$ and $\varphi_{1,2}$ are Josephson phase differences of two JJs, $\varphi_- = \frac{\varphi_1 - \varphi_2}{2}$ is the difference of phase drops cross two JJs, and $l_\pm = \frac{2\pi I_C L}{\Phi_0}(1 \pm m)$ are dimensionless effective inductances corresponding to 'differential' and 'sum' mode of the system respectively and $m = \frac{M}{L}$ is the ratio of the absolute value of the negative mutual inductance to half of the total inductance of the SQUID loop.

2.2. Dynamics of the "Common" Mode of nSQUID

The value of *m* is restricted by the nature limit of mutual coupling coefficient such that $m < 1$. When *m* is large (close to 1), l_- is much smaller than 1. The solution of φ_+ when the system is

in a stable state will follow the change of clock phase φ_C such that $\varphi_+ \approx \varphi_C$. This kind of relationship between φ_+ and φ_C is illustrated in a blue curve in Figure 2.2, which plots the φ_+ for minimal potential as a function of φ_C when external magnetic bias φ_e is 0. It is worthwhile to notice that this low effective inductance of the nSQUID for 'sum' mode is important only if the SQUID is used as part of a more complex composite circuit.

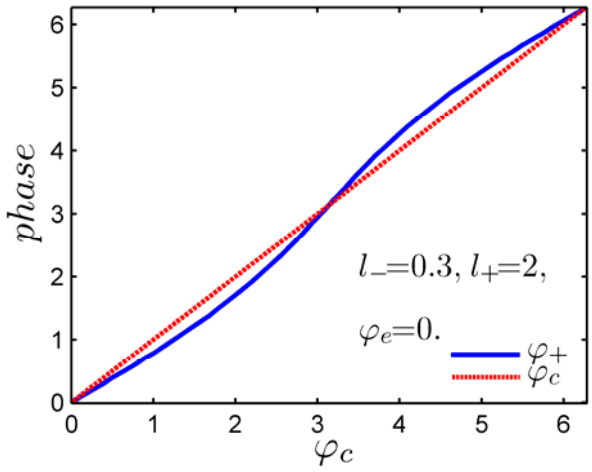


Figure 2.2. Relation between stable φ_+ and clock phase φ_c of nSQUID gate.

2.3. nSQUID with No External Magnetic Bias and the Error Rate

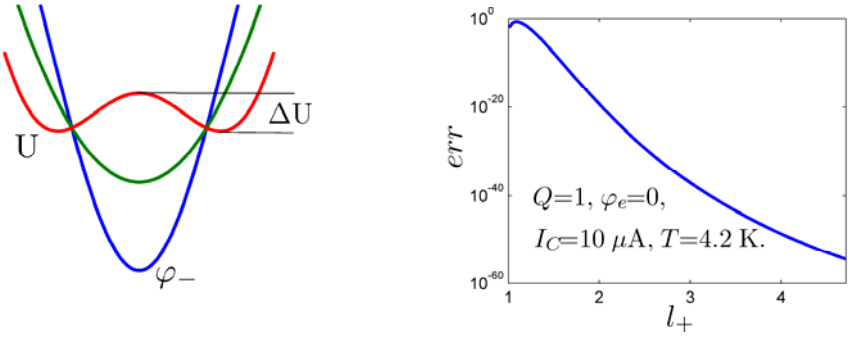
As shown in Figure 2.3(a) (or Figure 2.4(a)), in absence of external flux φ_e, system energy, *U*, is un-tilted (symmetric) and as the system enters into a bi-stable state from the mono-stable state, the probability of having a stabilized system is absolutely equal for either negative or positive φ_-. In this case it is impossible to carry out computation and thus it is usually called as 'incorrect' computation. However, this can be used as a random number generator. We anticipate the reversible implementation of its complementary operation as an erasure of a random number. Such a gate would be a good addition to the collection of primary gates (detail will be discussed

in Chapter 5). This is because random numbers play an important role in modern algorithms.

In this case we can also calculate the highest energy barrier ΔU between two states and therefore estimate the thermal excited noise. In classic mode, thermal noise of an oscillation system depends on temperature T and the analytic formula is [41]:

$$err = \frac{Q^{-1}}{\sqrt{\pi}}\left(\Delta U/k_B T\right)\exp\left(-\Delta U/k_B T\right) = \frac{Q^{-1}}{\sqrt{\pi}}\left(\frac{1}{2\pi}\frac{I_C}{I_T}\Delta u\right)\exp\left(-\frac{1}{2\pi}\frac{I_C}{I_T}\Delta u\right), \quad (2.2)$$

where $I_T = \frac{k_B T}{\Phi_0}$, $\Delta u = \frac{\Delta U}{\frac{\Phi_0 I_C}{2\pi}}$ is the dimensionless energy barrier of the double well potential as shown in Figure 2.3(a), and $Q = \beta_C^{\frac{1}{2}} = \omega_p RC$ is the quality factor of the oscillator system and $\omega_p = \sqrt{2eI_C/\hbar C}$.



(a) (b)

Figure 2.3. (a) Evolution of energy profile in absence of external magnetic flux. (b) Dependence of error rate on effective inductance l_+ at 4.2 K when I_C of JJs is 10 μA.

It is necessary to estimate the error rate at liquid Helium temperature 4.2 K, where the nSQUID operates. The typical I_C of JJs in the nSQUID is 10 μA. All the JJs in nSQUID is unshunted to avoid extra energy dissipation, i.e. $\beta_C >> 1$, and this helps to reduce the error rate. For simplicity, the error estimation is carried in the case of Q = 1. The result with l_+ from 1 to 3π/2 is shown in Figure 2.3(b). When l_+ is around 2.0, the error rate is about 10^{-20}, which is a

reasonable low error rate. As will be described in the following (Chapter 3), the translation of information between nSQUIDs requires direct coupling of nSQUIDs, which further reduces the error dramatically. Therefore, the calculation with nSQUIDs in principle can be very reliable.

2.4. Dynamics of the "Differential" Mode of nSQUID

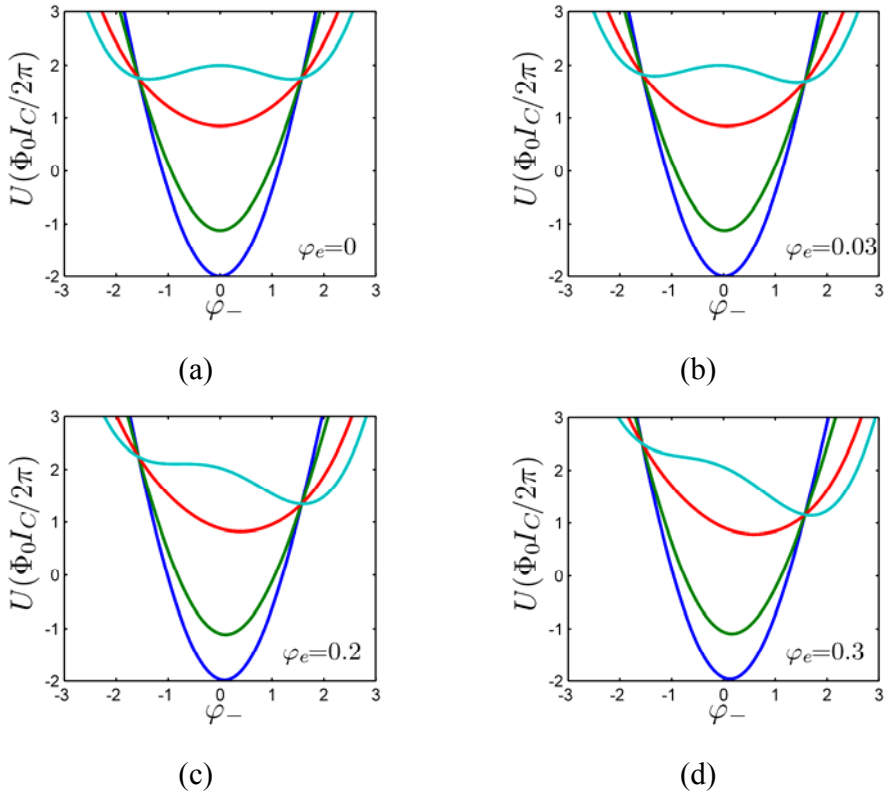


Figure 2.4. Evolution of energy profile as a function of φ_- with different external magnetic bias φ_e. The different colors represent different clock phases: blue, green, red and olive corresponding to $\varphi_C = 0$, $\pi/3$, $2\pi/3$ and π respectively.

Now let us move to the discussion of the effect of φ_-, the nSQUID will oscillate between mono-stable and bi-stable states with an increasing of clock phase φ_C. φ_- dependent dynamics of an individual nSQUID are demonstrated in Figure 2.3(a) and Figure 2.4(a)-(d). All plots are made for $m = 0.77$ and $l = 0.79$, under which conditions the nSQUID operates in an adiabatic regime. The same numbers are also the target parameters for the design and fabrication of the

circuits later on.

Externally applied flux in the loop φ_e will tilt the energy profile. Quantitative analysis of this dynamics shows that the range of parameters (*m* and *l*) for realizing correct adiabatic operation regime of the nSQUID strongly depends on φ_e. In case of Figure 2.4(b), when the bias is small, two minimums of the potential appears before it suppress into one global minimum. This means that there will occur an abrupt jump of φ_- when the system finally stabilizes into the global minimum, and this abrupt transition will dissipate energy. In this case, the range of properly operational parameters is extremely narrow.

This range will increase when φ_e increases as in Figure 2.4(c). The irreversibility is avoided since the second potential minimum is formed only after the system adiabatically changes its state following the evolution of the original minimum from the blue curve up to olive curve as shown in Figure 2.4(c). Although this regime of the nSQUID operation is quite satisfactory from the perspective of reversibility, a formation of the second potential minimum is not really necessary for the circuit operation. In fact, it imposes a constraint on the system parameters by creating a finite probability of error due to a possibility of thermal or quantum excitation of the system into this local potential minimum. In this respect, working in the regime of relatively large bias (i.e., strong inter-gate coupling in the multi-gate circuits) is more practical as shown in Figure 2.4(d). In this regime, the second potential minimum is not formed at all. In multi-gate circuits, this means that the gates are coupled sufficiently strongly, so that the errors become collective and can take place only by a simultaneous reversal of the states of many coupled nSQUIDs. This fact leads to the suppression of errors, and this strong-coupling regime is used in

design of multi-nSQUID circuits described in following chapters.

2.5. Layout of nSQUID

We have designed the nSQUID for two different technologies developed at HYPRES [42] and at NEC/ISTEC [43] respectively. The general evolution and optimization history is reviewed as followings. In 2002, the first version of the nSQUID was invented for 1000 A/cm^2 HYPRES technology, which is shown in Figure 2.5(a). Negative mutual coupling, the most striking new feature of the nSQUID, was realized by placing one layer of stripe inductance on top of each other. The opposite direction of current through each layer in an overlapping fashion increases the negative coupling factor. The ground plane was used to provide magnetic isolation between two cells as well as the return path for all bias currents. The hole of the ground plane under the overlapping of two layers of inductances reduces the screening effect, i.e., makes the negative coupling effect even stronger. This design configuration satisfies the requirements of strong negative mutual inductance. However, it is difficult to realize the direct magnetic coupling between adjacent nSQUIDs in order to transmit information. To satisfy this requirement, the next generation of the nSQUID (Figure 2.5(b)) was designed in 2003. In this version, the signal data which is saved as the magnetic field inside the nSQUID loop can be easily accessed by means of the two wires indicated as data line in the figure. The latest version of the nSQUID (Figure 2.5(c)) is based on the second revision of design but it further increases the effective inductance of the differential mode to boost the signal amplitude. Simultaneously, extra holes surrounding the inductances of nSQUIDs were placed to reduce the flux trapping inside the cell. The micrographic photo of the cell and the corresponding parameter values of HYPRES 30 A/cm^2

design technology are shown in Figure 2.5(c). Similar nSQUIDs designs were also fabricated with HYPRES 1000 A/cm^2 and NEC 350 A/cm^2 technologies.

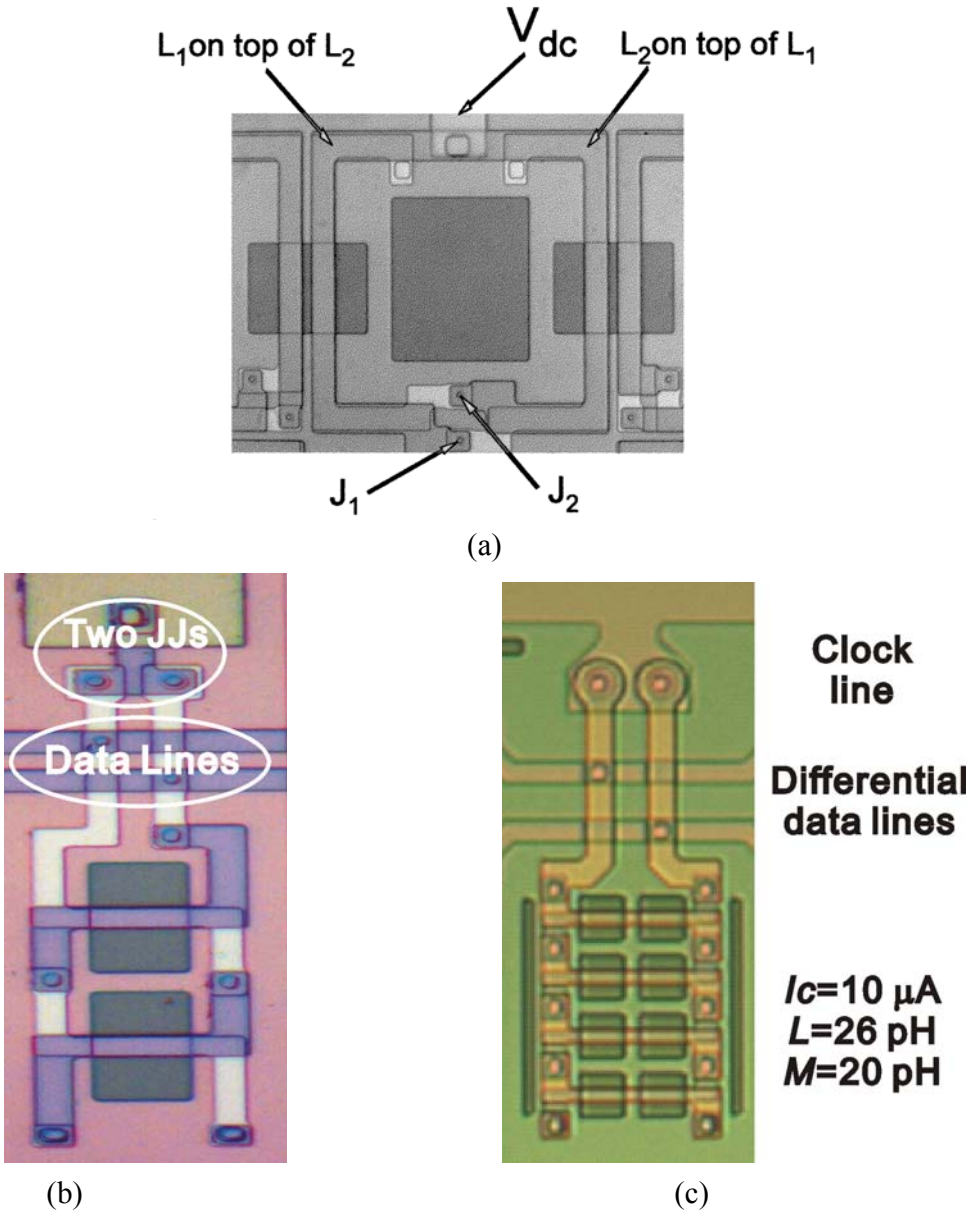


Figure 2.5. Micrographic photos of different versions of nSQUID designs fabricated in HYPRES. Figure (a) is after [37].

2.6. Conclusion

In this chapter, the properties of the basic gate, nSQUID, which is suitable for the experimental

demonstration of reversible information processing in Josephson-junction circuits, were reviewed. We presented theoretical analysis results and the layout design of an individual nSQUID. In the following chapters, we will discuss the progress of the reversible circuit based on this new suggested gate.

Chapter 3 Reversible Shift Register

3.1. Introduction

To develop a larger-scale nSQUIDs-based circuit, it is very important to make the design flow more "friendly" to conventional design techniques developed for semiconductor and RSFQ circuits.

As discussed in previous chapter, each nSQUID [37] is a 2-junction SQUID with a negative mutual inductance between its inductive arms. This negative mutual inductance resolves the two conflicting requirements for the two degrees of freedom of the system. In a common mode, which represents common dynamics of the two SQUID junctions, one would like to keep the low effective inductance ($\beta_l \sim 0.2$), and therefore, simple dynamics of this mode governed by the current bias of the junctions via the Clock line. For the differential mode, which represents the current circulating along the SQUID arms, one needs to provide a larger effective inductance ($\beta_l \sim 1.4$), so that there are two stable states in this degree of freedom.

A string of nSQUIDs (Figure 3.1) symbolically could be derived from a discrete model of the long JJ (Figure 1.3) by replacing each dot junction by a pair of dot junctions (Figure 3.1(a)). Such pairs of dot junctions work as a well known two-junction or DC SQUIDs. But nSQUID strings demonstrate unique properties.

The low ($\beta_l < 1$) inductance of the common mode of the string of nSQUIDs implies that the string support propagation of vortices along it. In plain words, the nSQUIDs string could be

packed with Josephson vortices that could propagate along the string almost the same way as in long JJs discussed earlier. (Let us assume that the critical current of each nSQUID and the critical current of each dot junction in Figure 3.1(b) are the same.) The properties of these vortices are similar to those of the vortices in long Josephson junctions.

However, the flux of Josephson vortex magnetically biases nSQUIDs and, in particular, at the center the value of this bias approximately corresponds to $\Phi_0/2$. At a properly selected loop inductance of the SQUID its energy profile has two "equal" minima that correspond to its two stable states and, as a result, the SQUID should fall into one of two possible states as shown on the top of Figure 3.1. In fact, closely located SQUIDs are magnetically coupled and, as a result, positive (or negative) energy minimum is the same for all SQUIDs within one Josephson vortex. In one word, each Josephson vortex carries on "its back" a magnetic domain and the direction of its magnetization could be used as a natural carrier of one bit of information.

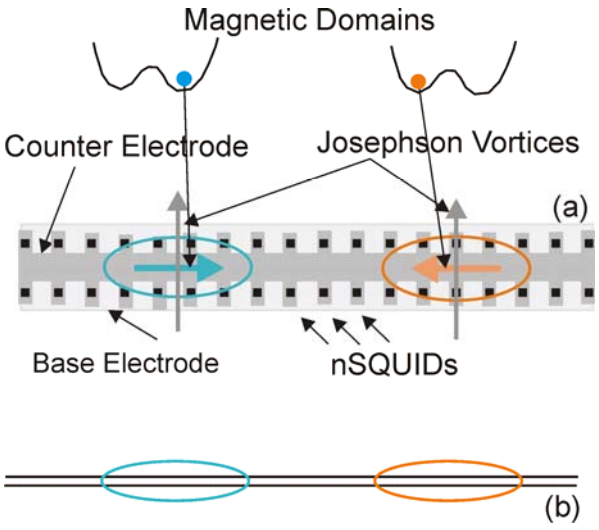


Figure 3.1. A simplified bird view of an nSQUID string (a) and its notation (b) (after [24]).

Magnetic domains (colored arrows in Figure 3.1(a)) are orthogonal to flux of Josephson

vortices (gray arrows). As a result, the magnetic interaction of these two objects is rather low. Moreover, the energy impact of this interaction does not depend on the magnetic domain direction. Figure 3.1(b) shows a generic notation for the nSQUID string. Color (light blue or pink) is used to indicate the direction of magnetic domains and therefore the carried binary data (logic "0" and "1").

3.2. Simple nSQUIDs Circuit with One Clock Line

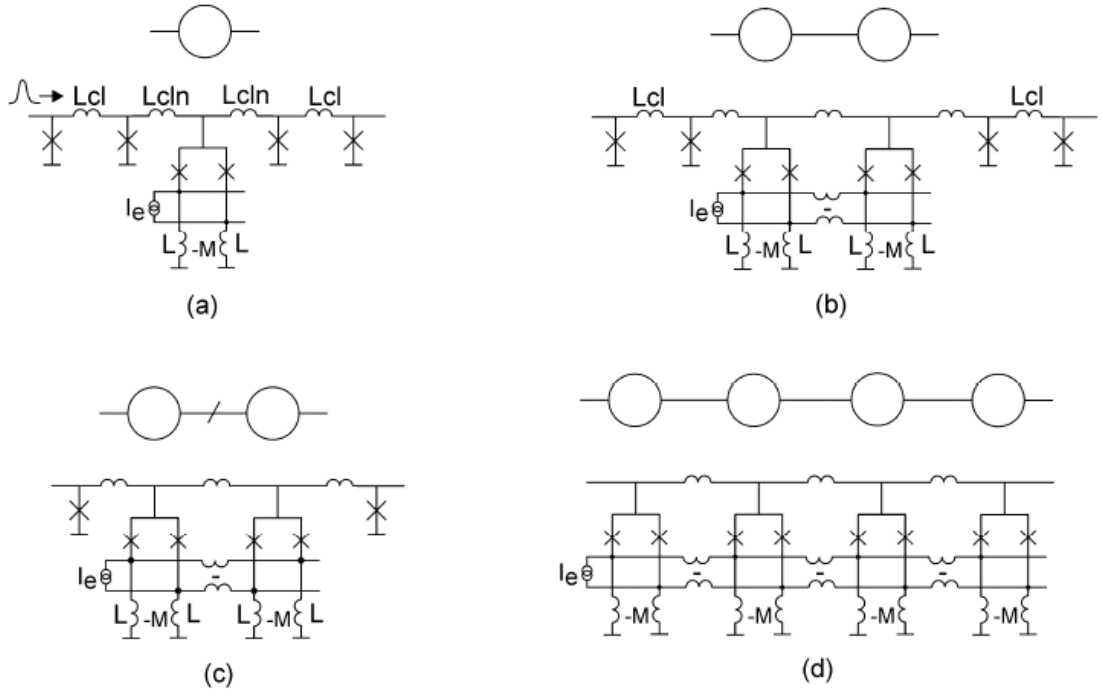


Figure 3.2. Simple nSQUID circuits with one clock line. All of them designed by substitutions of JJs in LJJ by nSQUIDs (after [24]).

Several simple but valuable reversible applications are shown in Figure 3.2, where nSQUIDs replace junctions in long JJs. We have already explained that for vortices moving along the long JJ nSQUID behaves as a single Josephson junction connected in series with a low inductance that can be neglected now at qualitative explanations. Of course we should provide

corresponding matching conditions between Josephson junctions and nSQUIDs, which will be discussed in details in Chapter 6.

When a vortex passes any point at the LJJ, it causes 2π increase of the clock phase or a Φ_0 increase of the clock flux at this point. During this flux increase, energy profiles shown in Figure 2.3 evolve as a closed cycle. In other words, moving Josephson vortices serve as native clock signals. Tilted energy profiles illustrate that the nSQUID is capable of amplifying weak external flux applied. For example, by applying current *Ie* in Figure 3.2(a), one would get the output of the differential flux corresponding to the lower minimum of energy profiles in Figure 2.3. Functionally nSQUIDs are similar to parametric quantrons introduced by Likharev et. al in 1985 [44]. But nSQUIDs could be efficiently clocked by other superconductor devices. This can be illustrated by the following examples. Figure 3.2(b) shows that the differential flux of one nSQUID could be used as an input signal for another nSQUID. In order for such a coupling not to destroy the operating dynamics of the nSQUIDs in the circuit, the connecting wires should have a negative mutual inductance. The required differential coupling is provided by these two connecting inductances and numerical simulations show that a negative coupling between these inductances makes circuits more robust against unavoidable fabrication spread of parameters. Figure 3.2(c) shows that a simple swapping of two wires inverts the sign of the transferred signal. (Note the positions of dots indicating wire connections.) This inversion (or NOT gate) does not contain any single Josephson junction! Finally Figure 3.2(d) shows a 4-stage shift register. It is important to note that the same sign of magnetization of neighbor cells could be physically interpreted as a magnetic domain moving synchronously on “the back” of the Josephson vortex.

Cells in this domain help each other: in other words, magnetizations of previous and the next cells tilt the energy profile of the analyzed cell toward its occupied state. This effect dramatically reduces thermally induced error rate. In fact, such errors could take place only at simultaneous large and unidirectional fluctuations of the differential fluxes in all nSQUIDs belonging to one magnetic domain. The probability of such events is exponentially lower in comparison with those of stand-alone nSQUIDs.

The shift register is one of the most widely accepted benchmarks used to certify new technologies. This kind of devices has already been well investigated experimentally with various technologies as we will discuss in the following. Here we demonstrate an nSQUID-based circuit with two 8-stage shift registers.

3.3. Comparison of RSFQ and nSQUID circuits

As mentioned in Chapter 1, nSQUID circuits dissipate dramatically less power than their RSFQ counterparts. To see this, one can look at the "primitive" RSFQ cell shown in Figure 3.3: two similar pieces of Josephson Transmission Lines (JTLs) that transfer the SFQ pulses (or vortices) which represent clock and data signals from JTL inputs to their outputs. Josephson junctions in JTLs are critically dumped by shunt resistors and relatively large bias currents I_b are applied to the junctions to compensate for the viscous friction between vortices and shunt resistors. The bias currents for many junctions are delivered via a single power line and are distributed between the junctions using the corresponding bias resistors R_b. In this case most of the energy is dissipated in the bias resistors rather than in the "active" circuitry. This drawback is practically unavoidable for two reasons. First, the required bias voltage V_b is too low to keep it

constant by means of semiconductor electronics. As a result, the constant current rather than voltage is supplied by the power source. The second factor is that the Josephson voltage-to-frequency relationship which implies that the average voltage across the JTL (shown as V_{jd} in Figure 3.3) fluctuates following the variable rate of flow of the data vortices. The distribution of the total bias current between the clock and data lines depends then on the data pattern. This parasitic effect is reduced to an acceptable level if the effective value of bias voltage is significantly higher than the variations of the voltage V_{jd}.

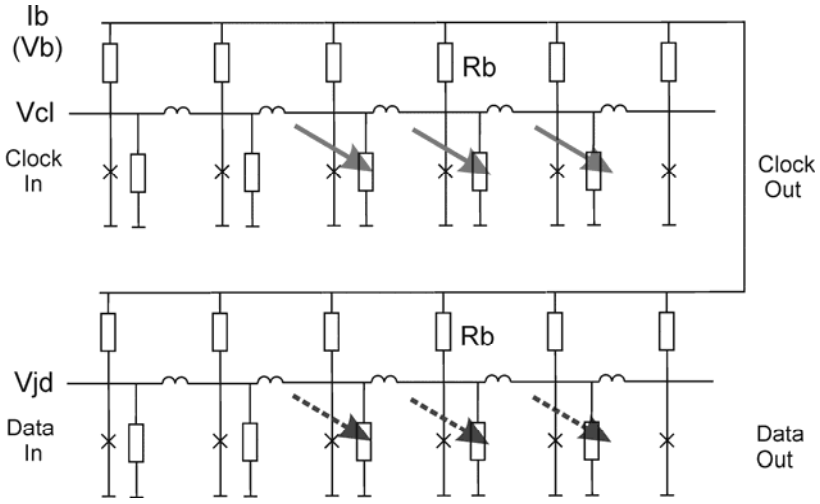


Figure 3.3. Data flow in clock lines of a typical RSFQ cell (after [39]). For discussion, see main text.

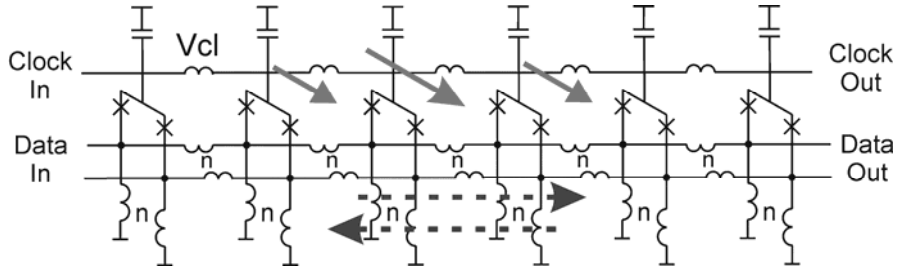


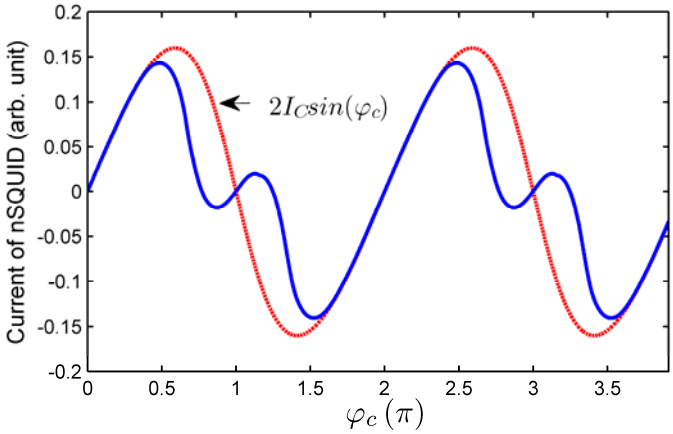
Figure 3.4. Data flow diagram in a string of nSQUIDs coupled through pairs of inductive strips with negative mutual inductance between them (after [39]).

As showed in Figure 3.2(d), the capacitively biased nSQUIDs can be arranged into a linear array of cells with strongly coupled differential (or signal) and common (or clock) modes (

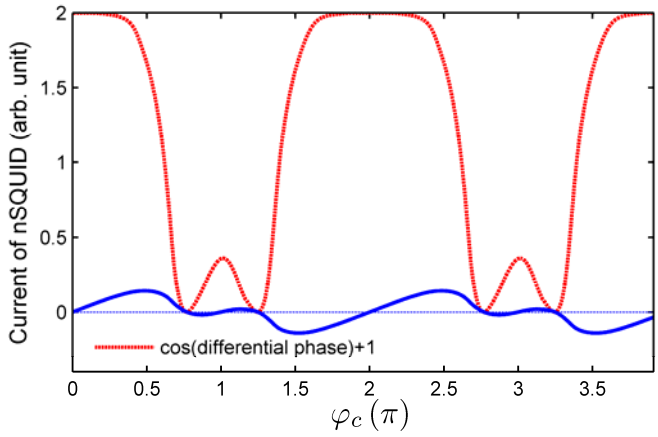
Figure 3.4). A signal interaction (for the differential nSQUID modes) is provided by the pairs of negatively coupled inductances. The synchronization of common modes of different nSQUIDs is provided by superconducting wires with small inductances. Due to coupling with external magnetic field the inductances provide necessary phase shift $d\varphi$ between oscillations of nSQUIDs energy profiles.

This kind of data presentation in the string of nSQUIDs has two advantages. First, the average voltage V_{cl} on the clock line is proportional to the frequency of the clock vortices and is independent of the data pattern. This independence of the data flow makes it possible to dramatically reduce the value of bias resistors and the bias voltage, if the biasing scheme shown in Figure 3.3 is used. However, as we will discuss later, the total bias current is so low that it can even be applied directly to the clock line. The second advantage is that the data domain is automatically "synchronized" with the clock vortex as mentioned in previous sections in this chapter, and the time jitter between the clock and the data is essentially suppressed. The practical consequence of this is that the critical currents of the Josephson junctions can be reduced. In addition to all this, the dynamics of the nSQUID string is quite simple. In fact, it is nothing more than a motion with constant speed of a clock vortex coupled with data domain. In this case, the shunt resistors can be completely eliminated, as one would expect for a reversible circuit.

3.4. Simulation of Dynamics of nSQUIDs Shift Register



(a)



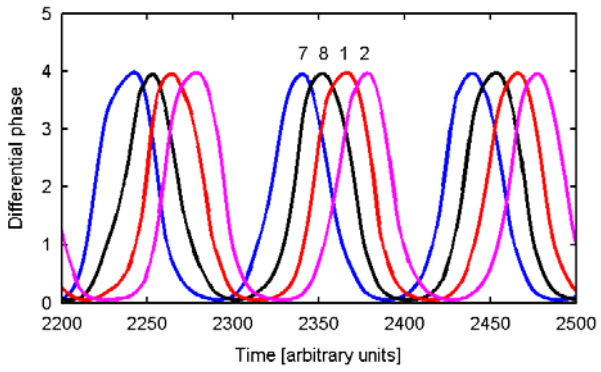
(b)

Figure 3.5. Total current of two JJs in one of nSQUIDs in a shift register with increasing clock phase φ_c. (a) Fitted the current by the formula of conventional DC SQUIDs with the same clock phase. (b) The unique property of nSQUID comes from the second dimension of degree: differential phase.

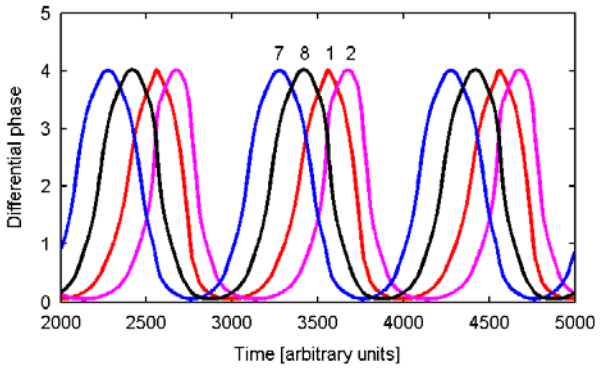
The dynamic of the circuit (in a classical mode) in Figure 3.4 is illustrated by the numerical simulations in the following two figures. The simulated shift register contains totally 8 nSQUIDs per one vortex connected in series and biased by a common DC voltage source. Figure 3.5 shows the influence of differential phase on the current of one nSQUID. Compared with conventional

DC SQUID, which has the current shown as dotted line in the upper plot, nSQUID shows unique property especially in the area near the center of vortex. From the bottom plot, the matched area between nSQUID and DC SQUID corresponds to the case when $\cos(\varphi_D)$ is equal to 1, where φ_D is the differential phase (mentioned also as $\varphi\_$), i.e. there is no loop current inside the nSQUID. The sum of currents through two JJs in one nSQUID is close to $I_C \sin(\varphi_C)\cos(\varphi\_)$.

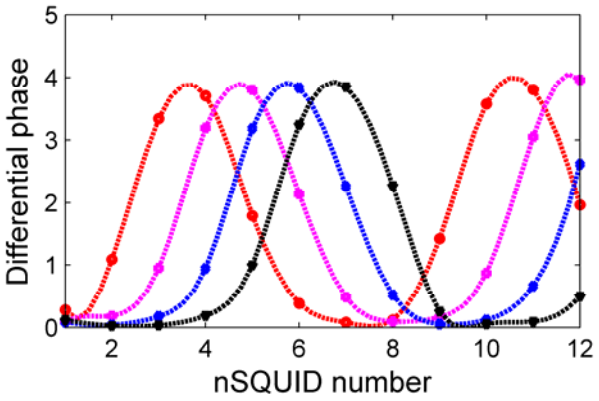
Figure 3.6 shows that each nSQUID oscillates between mono-stable and bi-stable states which can be represented by the low and high differential phases. (The positive signs of the phases in bi-stable mode are defined by boundary conditions.) For the simulation we selected clock phase shift $d\varphi = 2\pi/8 = \pi/4$ that provides the shift between oscillations in next nSQUIDs for 1/8 of their period. The propagation speed of the differential phase is strictly proportional to the DC voltage source as shown in the Figure 3.6(a) and (b). The DC bias voltages are 18 μV and 1.8 μV in simulation of plot (a) and (b) respectively. As expected, the period of the differential phase in (a) is exactly tenth of the period in plot (b). Plot (c) shows that the described complex process is, in fact, reduced to a trivial propagation of flux (or bi-stable) domain along the circuit. Due to the Josephson voltage to frequency relationship the propagation speed is also exactly proportional to the "clock" voltage. In classical mode the domain propagation can be described as a transfer of logic data along the circuit. At correct values of parameters the domain propagation is physically reversible and the energy dissipation associated with this process should be extremely low.



(a)



(b)



(c)

Figure 3.6. Dynamics of differential (signal) flux in the nSQUID array. (a) and (b) Evolution of signal over time in nSQUIDs 1, 2, 7 and 8; Waveform distortion of the first nSQUID is caused by the boundary conditions. The DC voltage in (a) is ten times of that in (b). (c) Snap shots of the signal in the first 12 cells at 4 different times. (The simulated array contains 24 nSQUIDs, space period for domains is 8 nSQUIDs.)

3.5. Energy Dissipation in nSQUID Shift Register

The Josephson voltage-to-frequency relationship implies that the measurement of the energy dissipated in an nSQUID circuit is reduced to the measurement of dc current *I* flowing through the circuit [40]. Indeed, the energy *E* dissipated during each logic operation can be obtained by multiplying the dissipated power

$$P = V \cdot I, \tag{3.1}$$

by the period *Δt* of the operation:

$$E = V \cdot I \cdot \Delta t. \tag{3.2}$$

Combined with the Josephson voltage-to-frequency relationship:

$$1/\Delta t = (1/\Phi_0) \cdot V, \tag{3.3}$$

this equation shows that the dissipation energy *E* is determined only by the current *I*:

$$E = \Phi_0 \cdot I. \tag{3.4}$$

As a result, comparison of the energy dissipation with its thermodynamic threshold $E_{th} = k_B T \ln 2$ is equivalent to the comparison of the dc current with the "threshold current"

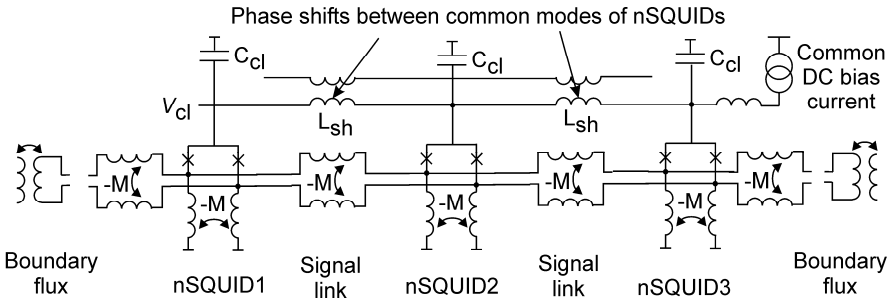
$$I_{th} = (\ln 2 / \Phi_0) \cdot k_B T. \tag{3.5}$$

At liquid helium temperature of 4.2 K, the threshold current is $I_{th} \cong 0.02\ \mu\text{A}$.

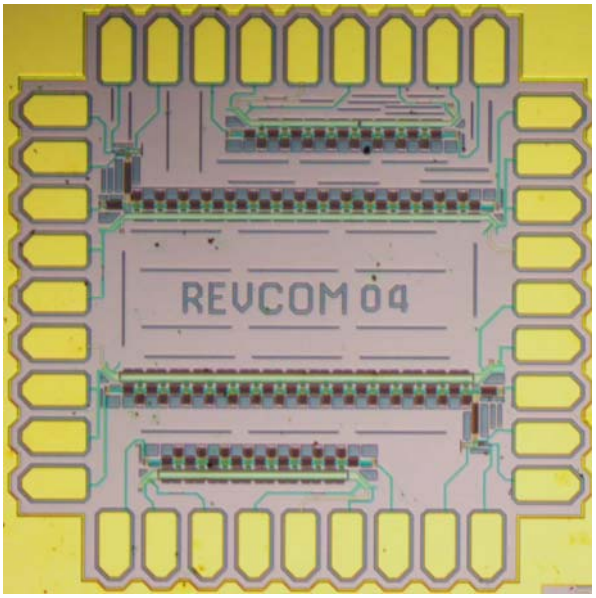
3.6. Design of Linear Shift Register

Our circuits (an example shown in Figure 3.7) usually have a high level of complexity. Such kind level of complexity means that the circuits can be fabricated only at the dedicated microelectronics facilities rather than university labs. In fact, our designs were optimized for fabrication at two of the best facilities specializing in superconductor circuits: HYPRES, Inc. and

ISTEC. Together, they cover a wide range of junction critical current densities: from 30 A/cm^2 (HYPRES), to 350 A/cm^2 (ISTEC) and 1000 A/cm^2 (HYPRES).



(a)



(b)

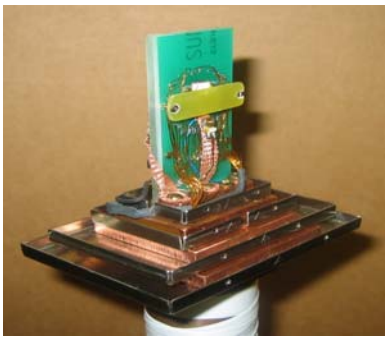
Figure 3.7. (a) Simplified structure and (b) micrographic photo of a 5 mm × 5 mm chip containing shift registers with galvanically coupled nSQUIDs. Eight and fifteen nSQUID registers have been submitted for fabrication at HYPRES. I_C of all JJs are the same and equal to 10 μA, L_{sh} = 2.4 pH and L_{sh} = 0.84 pH for the top two and bottom two shift registers respectively.

As the first step, several linear shift registers composed of different number of nSQUIDs in the array were designed, one of which is shown in Figure 3.7. The effective schematic of the shift register is plotted in Figure 3.7(a), where only 3 nSQUIDs are shown. To reduce the energy dissipation as much as possible, the imperfection effect coming from the edge of nSQUIDs

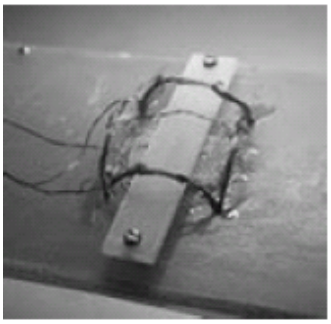
should be best avoided. This suggests that it is better to have more nSQUIDs in the array. Although there are only 3 nSQUIDs shown in Figure 3.7(a), we placed 8 and 15 cells in actual fabricated devices (a micrographic photo of a device with 8 cells is shown in Figure 3.7(b)). 8 is the minimal number of cells needed in the array which is proven to maintain good dynamics from the simulations of data translation, while 15 cells has reached the fabrication limit of 5 mm × 5 mm chip. These designed chips were fabricated in HYPRES using 30 A/cm^2 technology.

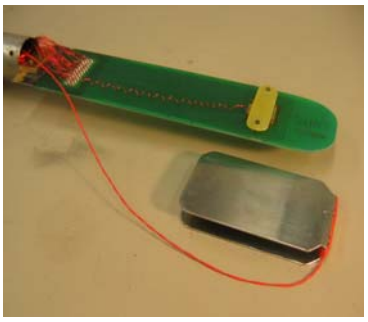
3.7. Experiment Setup

Two experimental setups were used for the measurement of our fabricated chips. One (Figure 3.8 (a)) is based on 0.5 W 2-stage close-cycle refrigerator "Coolpower 4.2GM" from Leybold Cryogenics. The other is the chip holder (Figure 3.8(b) and (c)) immersed in a commercial Helium Dewar (4.2 K). The Figure 3.8(b) shows the 3D Helmholtz coil arrangement for providing magnetic field during the experimentation in liquid Helium environment. Also, special chip holders (Figure 3.8(a) and (c)) were developed for testing superconducting circuits with 3D active shielding system for measurement in cryocooler and liquid Helium [45, 46]. In both setups, thermo cycling or "defluxing" procedure (the chip is heated above critical temperature to expel the frozen flux and then allowed to cool) was provided under OCTOPUX [47] control using off-chip heaters and thermometers. Additionally, the chip temperature was measured by the observation of the transition into the superconducting state of Niobium strips located on the chips but not involved in the operation of the investigated circuit.



(a)





(b) (c)

Figure 3.8. (a) Shield bases with the chip holder mounted on a second stage of a cryocooler. (b) 3D Helmholtz coil setup and (c) new probe with active shield technique for measurement in liquid Helium (after [45, 46]).

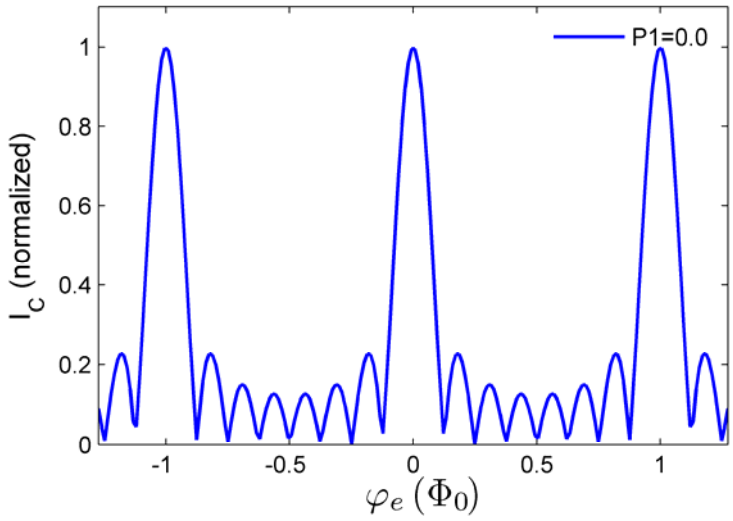
3.8. Analysis and Conclusion

If we temporarily neglect the new feature coming from nSQUID, the common mode dynamics of 8-nSQUID shift register is the same as that of a discrete long Josephon junction containing 8 JJs. The critical current of this long junction is calculated in Figure 3.9(a). The number of lobes of the critical current modulation in one period is equal to $N-1=7$, where N is number of JJs. Simulation results in Figure 3.6 correspond to the case when $\varphi_e = 0.25$, which means totally there is $2\Phi_0$ external magnetic flux applied into the shift register. As we have discussed, the new feature of nSQUIDs mainly comes from the extra degree of freedom corresponding to differential phase in nSQUID. Simulation results taken into account of this influence are

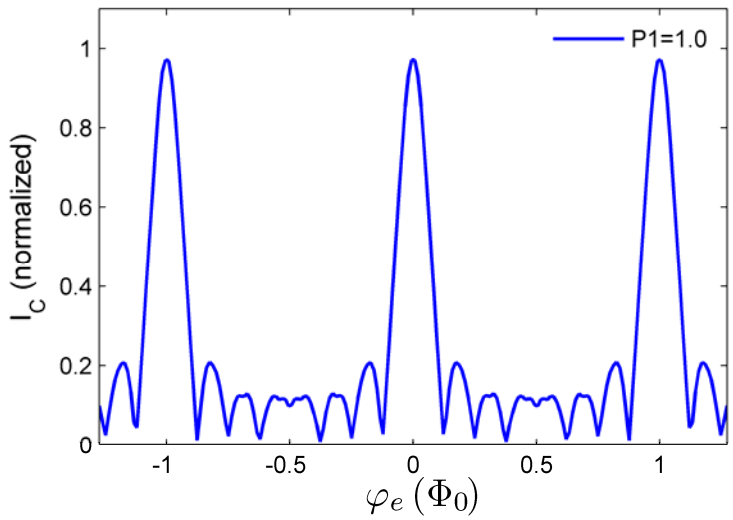
presented in Figure 3.9(b)-(d). In this model, current in nSQUID is set to be equal to $I_C \sin(\varphi_C)\cos(\varphi_D)$ as illustrated in the solid line of Figure 3.6(a), where φ_C and φ_D are in unit of $\Phi_0/2\pi$. The differential phase φ_D is also a function of φ_C, with their relationship shown as Figure 3.6(c). We simply set a parameter P1 which determines the maximum of φ_D in one period and make use of a simple pattern to describe the dynamics of φ_D as:

$$\varphi_D = P1 \cdot \left[\exp(-P2 \cdot Rem^2) + \exp(-P2 \cdot Rem1^2) \right], \quad (3.6)$$

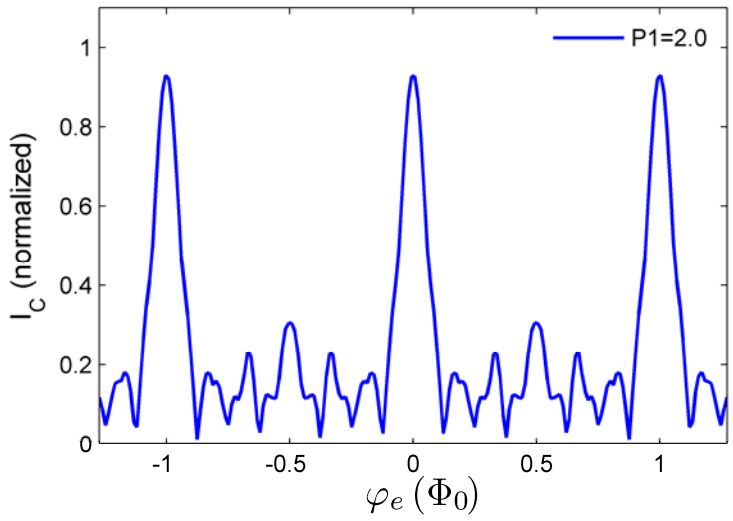
where P1 = 4.1 and P2 = 0.6 from the fitting of the result in Figure 3.6(c), and Rem and Rem1 are functions of φ_C as $Rem = rem(\varphi_C - \pi, 2\pi)$ and $Rem1 = Rem - 2\pi \cdot sign(Rem)$. Shown from (b) to (d) in Figure 3.9, the influence of the differential current of nSQUID increases as P1 is increasing from 1.0 to 4.0 while keeping P2 as a constant (0.6). As P1 increases, the maximal critical current decreases from 1.0, while the sub-minimal I_C (when φ_e is 0.5) gradually converts to a second maximal peak in one period. This feature can be explained by looking at the formula $I_C \sin(\varphi_C)\cos(\varphi_D)$, when φ_C is near π, difference phase places more role on totally current of nSQUID. When φ_e is 0.5, clock phase difference between two adjacent nSQUIDs is roughly close to π in unit $\Phi_0/2\pi$, where the current of all nSQUIDs becomes accumulated as a second maximum other than compensated each other. Simultaneously, the pattern of I_C becomes more irregular and complex.


P1=0.0
I_C (normalized)
$\varphi_e\,(\Phi_0)$
0
0.2
0.4
0.6
0.8
1
-1
-0.5
0
0.5
1

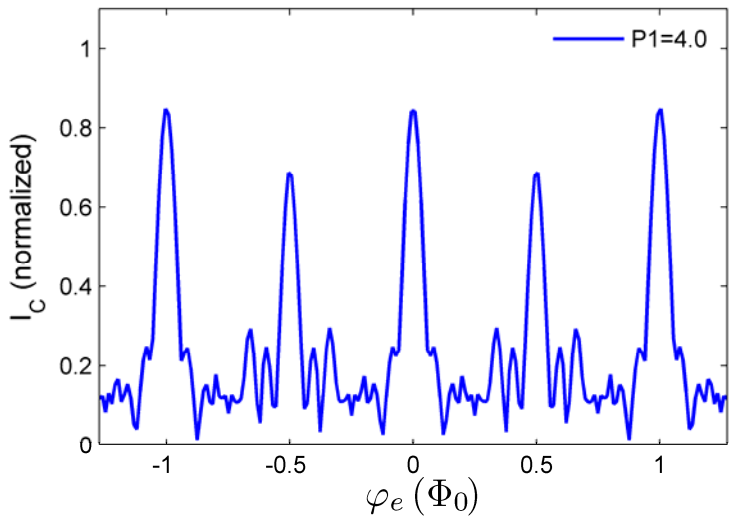
(a)


P1=1.0
I_C (normalized)
$\varphi_e\,(\Phi_0)$
0
0.2
0.4
0.6
0.8
1
-1
-0.5
0
0.5
1

(b)



(c)



(d)

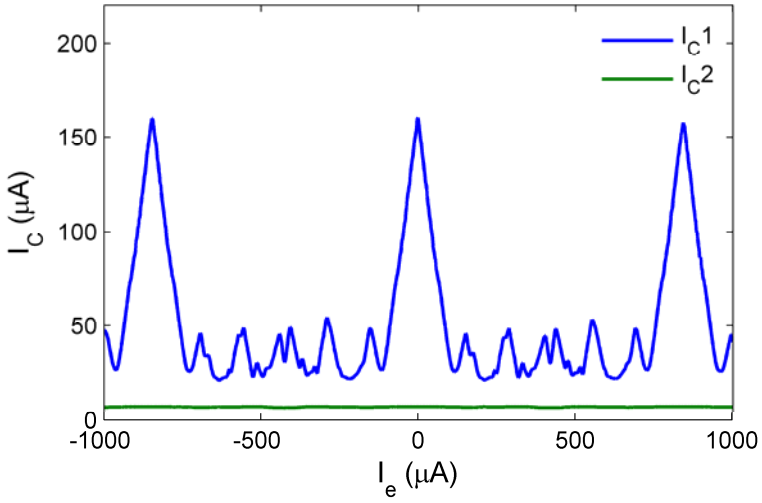
Figure 3.9. The evolution of critical current of the 8 nSQUIDs shift register with increasing differential flux in nSQUIDs. I_C is normalized by sum of critical currents of all nSQUIDs and φ_e, in unit of Φ_0, is the average external magnetic field induced into one nSQUID.

Measurement results of chip shown in Figure 3.7(b) at 4.2 K are presented in Figure 3.10. Figure 3.10(a) shows the modulation of the critical and return currents v.s. magnetic bias induced by applying a current (plotted along the horizontal axis of Figure 3.10(a)) that is inductively coupled to one segment of the shift register. The number of lobes is in agreement with the results

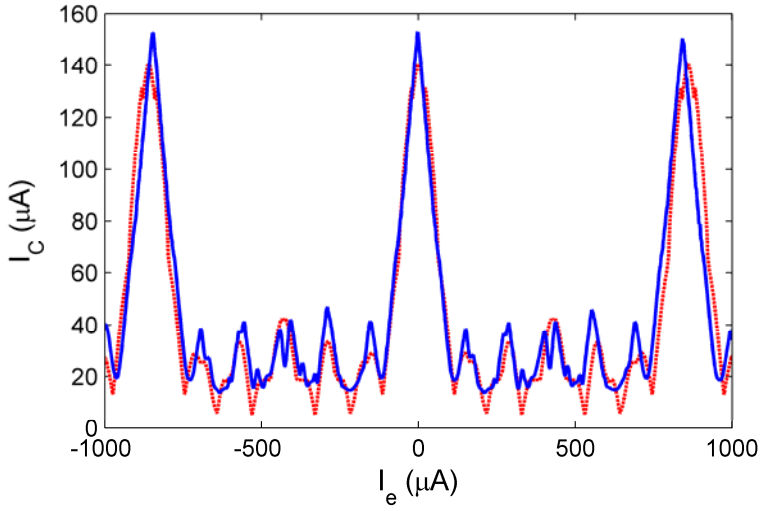
from the simple modeling shown in Figure 3.9(a). The main features of Figure 3.10(a) and Figure 3.9(a) agree, although the model used to obtain the result shown in Figure 3.9(a) does not take into account the inductance in the clock line or the unique property of the nSQUID coming from the differential dynamic (i.e. just simply treats nSQUIDs as JJs (the current in nSQUID is shown with the dotted line in Figure 3.6(a))). More accurate modeling results which include the effect of differential current and the clock line inductance (L_{sh}) on critical current are shown in Figure 3.10(c). The best fitted result, when setting the value of L_{sh} to 2.4 pH as designed and as well as measured, is shown in Figure 3.10(c). It matches very well with the experiment result when P1 is set to be 1.8. The slight derivation between simulation and experimental results, e.g. best fitted P1 is smaller than the simulated result, is basically related to parameter fluctuations (caused by, e.g., parasitic trapping of magnetic flux) in the real structure: noise in the regions of small critical currents and gradual suppression with bias of the current maxima.

The minimal of critical current is 15 μA, which is still much larger than the thermal dynamic threshold value at 4.2 K. Besides the parameter fluctuations mentioned above, the large critical current is also a result from the design flaws. First of all, the external magnetic filed was applied by an inductance coupled with the whole clock line inductance of shift register, this large area of coupling will introduce unexpected magnetic influence to the differential mode of nSQUIDs. Second, there is no return path for the moving vortex along the clock line. The waste of vortex results in an extra source of energy dissipation. Also, we were only able to extract the critical current instead of working current of the circuit, which should be definitely lower. In the following chapter, we will introduce the new timing mechanism based on long Josephson

junction (LJJ) for the return path of the shift register to eliminate one more energy dissipation source.



(a)



(b)

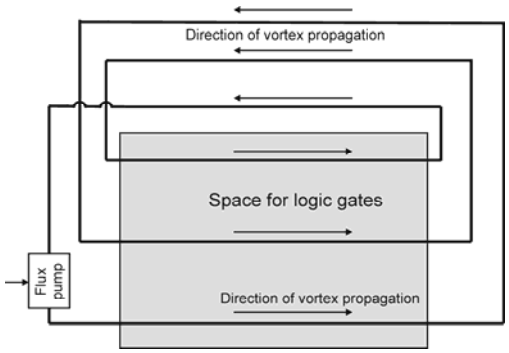
Figure 3.10. Measurements of the linear shift register at 4.2 K: (a) measured and (b) calculated dependence of the critical current on the magnetic bias. In (a), I_C1, I_C2 are the critical and return currents, respectively. For discussion, see main text.

Chapter 4 Long Josephson Junctions Serving as Timing Belt

4.1. Introduction

As we discussed in the end of Chapter 3, there is undesired energy dissipation if we do not recycle the vortex/vortices moving along the nSQUIDs shift register. Therefore, a return path should be introduced into to the design. Before we investigate the vortices in a closed loop of nSQUIDs circuit, let us first study the dynamic properties of them in the long Josephson junction (LJJ) since these two are very similar in many sides. Actually, the possibly nondissipative motion of a uniform train of vortices along ring LJJs described in Chapter 1 has already been utilized in some clock circuits that demonstrate outstanding timing stability [48]. Our circuits [27] utilize a similar motion but the implementation is quite different. This is because our primary optimization goal is to low the energy consumption rather than to achieve better clock stability. Besides, there is no size constrain for our circuit and it can take up the whole chip instead of being a compact device. Figure 4.1(a) illustrates a LJJ "timing belt". The light gray area marks the space to be occupied by logic gates. An incorporated vortex pump injects into the ring LJJ the required number of Josephson vortices. The timing of gates is provided by densely packed vortices that uniformly move along the belt (or ring). We show in Figure 4.1(b) a ribbon timing belt that can be found in many cars. Indeed their timing mechanisms are almost identical. In particular, each vortex acts as a tooth of the rubber belt. However, the translational symmetry of vortices in LJJ belts gives them a great advantage. Simply put, the vortices are absolutely

identical; they are not affected by wear and tear and distribution of currents in the belt before and after its rotation by any integer number of vortices are fundamentally identical.



(a)

(b)

Figure 4.1. Two functionally similar "timing belts". One (a) is built as a long ring Josephson junction (shown in a black curve) filled with vortices, while the other (b) is a rubber belt used in cars.

Of course the complete lack of dissipation is only a convenient idealization and we should control the impact of parasitic factors responsible for highly undesirable losses. In fact, we deal with discrete rather than continuous LJJs. Our LJJs can be described as microstrips made of two thin superconductor films sewn together by uniform stitches of equally distanced unshunted Josephson junctions (Figure 4.2(a)). As we mentioned earlier the vortices are densely packed in the LJJ and, as a result, the size of a squeezed vortex coincides with the vortex period a but is still much larger than the distance between the junctions d (nominally $a = 8.5 \times d$). Unfortunately the discreteness itself eliminates completely lossless solutions. More exactly, mathematical

solutions for discrete LJJs are a mixture of vortices carrying electromagnetic waves [49]. These waves actively interact and, in particular, resonate on discrete components [50]. Another feature to be aware of is "acoustic" vibrations of vortices that are similar to the vibrations of a chain of masses connected by springs (Figure 4.2(b)).

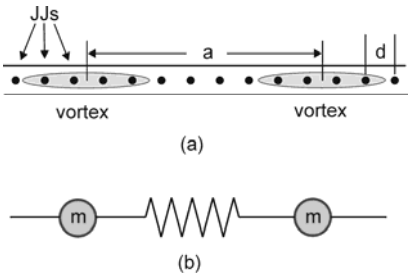


Figure 4.2. (a) Geometry and (b) mechanical model of the discrete LJJ (after [51]).

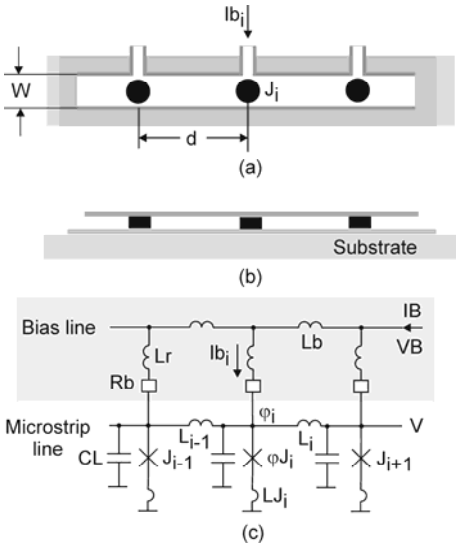
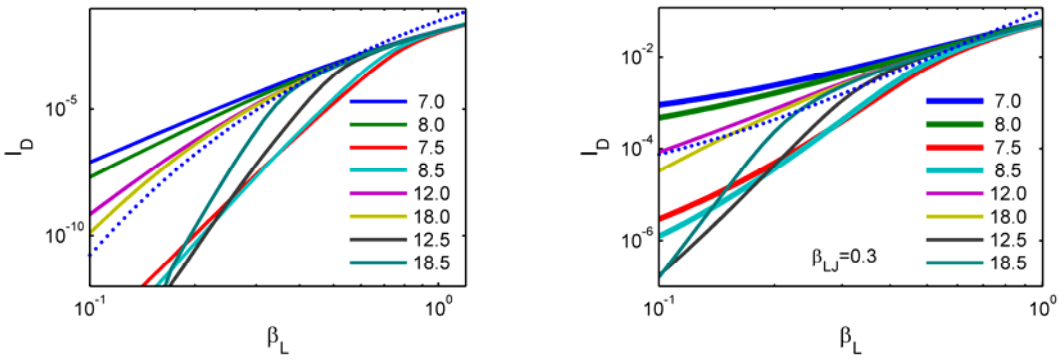


Figure 4.3. (a) & (b) Design and (c) equivalent circuit of LJJ. Basic parameters: d = 150 μm, W = 12.6 μm, Ic = 10 μA, L = 4.44 pH, CL = 378 fF, LJ = 8.18 pH, Rb = 0.77 Ohm.

Measurement of the energy dissipation in LJJ is in fact the same as measurement of energy dissipation of the nSQUID as in the Chapter 3. As we mentioned in earlier papers [39] it can be reduced to a direct measurement of DC bias current *I* according to Eq. (3.4). This same equation

also immediately gives the value of threshold current (per gate) that corresponds to the thermodynamic threshold current, e.g., about 0.02 μA at 4.2 K temperature.

4.2. Static Properties of LJJs



(a) (b)

Figure 4.4. Dependence of the critical current of LJJ normalized to total critical current of all junctions on β_L. Different lines correspond to different magnetic fields shown as the number of junctions per vortex period. Dependences are calculated for (a) vanishingly low inductance LJ and (b) for $\beta_{LJ} = 0.3$.

Continuous uniform LJJs with vortices at low voltages have quasi-linear volt-current characteristics (without any critical currents). As a result, this device with vanishingly low currents at voltages approaching zero easily passes the reversibility test. However, as mentioned earlier, the discreteness is able to undermine this unique advantage. Critical currents of discrete LJJs have been calculated in many literatures. However, we did not find accurate analytical expressions nor numerically calculated dependences of critical currents on dimensionless stage inductance β_L for an interesting range of vortex densities (Figure 4.4). Instead here we numerically calculated the depression of the LJJ critical current caused by vortices. We quantified the vortex density, nJJ, by the number of Josephson junctions per vortex period. The desired vortex density at current stage is between 8 and 9 junctions per vortex. However, in order

to show a broad picture we show the numerical results for an even wide range of vortex densities between 7.0 and 18.5 in Figure 4.4. Although a known technique dealing with the Peierls-Nabarro potential [49] could be used for calculations of critical current depression, we still could not find analytical results covering our range of parameters. This is especially true for our more favorable case of incommensurable number of junctions per vortex [52]. Instead we show (dashed line) the analytical result (at $A = 626$) derived for large separation between vortices [53] which has some similarity to our case here,

$$I_D = A\exp(-\pi^2/\sqrt{\beta_L}). \tag{4.1}$$

The left plot (Figure 4.4(a)) corresponds to a conventional LJJ with vanishingly low inductance LJ connected in series with Josephson junctions. The LJJ critical current depressed to about 10^{-3} of the value measured without Josephson vortices corresponds approximately to the threshold bias current per junction. Our target for the depression of the critical current is currently about 10^{-4}. Figure 4.4(a) shows that this level of depression corresponds to an easily achievable β_L ranging from 0.4 for nJJ = 8 to 0.6 for nJJ = 8.5. nSQUIDs are approximated by Josephson junctions connected in series with a relatively large ($\beta_{LJ} \cong 0.3$) inductance LJ. The right plot (Figure 4.4(b)) shows critical current depressions calculated for this β_{LJ}. In order to simplify our problem we searched for the best analytic approximation similar to Eq. (4.1) but with some effective inductance for the calculation of β_L which can be represented as

$$L_{eff} = L + \alpha LJ \tag{4.2}$$

The dashed line in Figure 4.4(b) corresponds to $\alpha = 0.96$. According to Figure 4.4(b) a

dimensionless inductance $\beta_L = 0.2$ at nJJ = 8.5 depresses the critical current 10,000 times.

4.3. Dynamic Properties of LJJs

Measuring the dynamic properties of LJJs is easier than simulating them. We designed several versions of ring LJJs that have been fabricated at HYPRES, Inc. [42]. The followings are measurement results of circuits fabricated with a custom process with 1 kA/cm^2 critical current density for Josephson junctions and with 2 Ohm sheet resistance for main resistive layer. The ring LJJ device contains 77 Josephson junctions as shown in Figure 4.5.

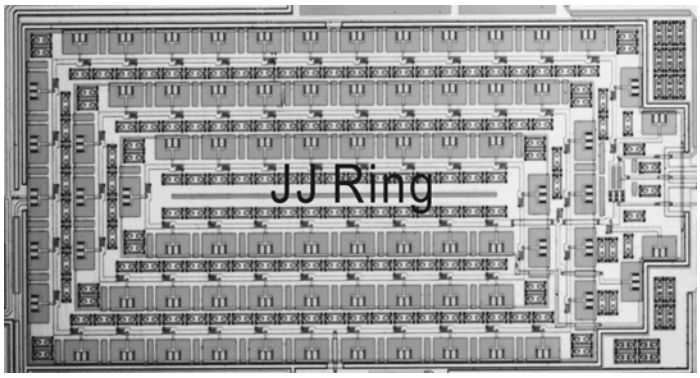


Figure 4.5. Microscopic photo of fragment of Integrated Circuit (IC) with ring LJJ.

We measured current-voltage (IV) curves at different numbers of vortices that could be changed using a built-in vortex pump. The effective circuit and micrographic photo of this vortex pump are shown in Figure 4.6. It is composed with three JJs in parallel with the same working mechanism as a conventional DC/SFQ converter [54]. The periodic current applied to IIN pad creates the vortices which are then injected into the JJs connected with the pump. This process is simulated by the software PSCAN and the simulation result is presented in Figure 4.6(c). In order to maintain the uniform property of the LJJ, we make the effective inductance of this

vortex injector the same as all the other clock line inductances in the LJJ. Experimentally, we have demonstrated that this vortex pump is capable of injecting 35 vortices into our LJJ circuit.

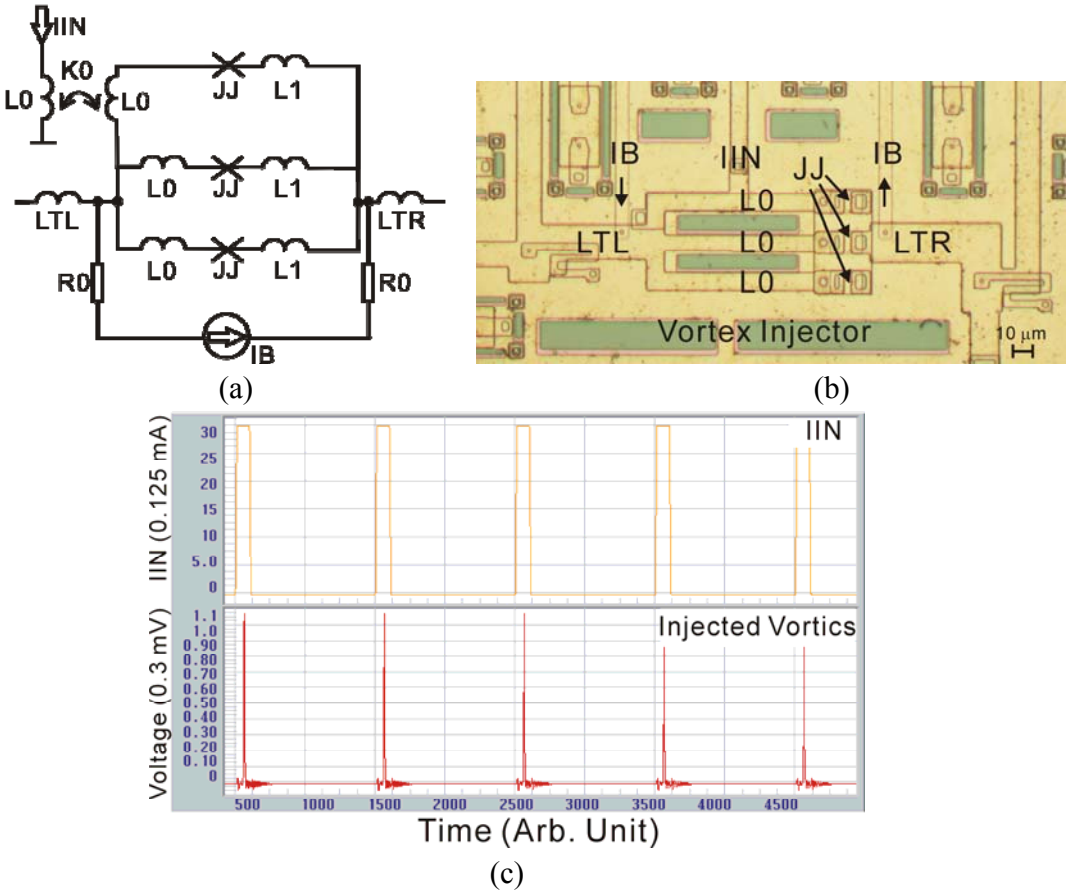
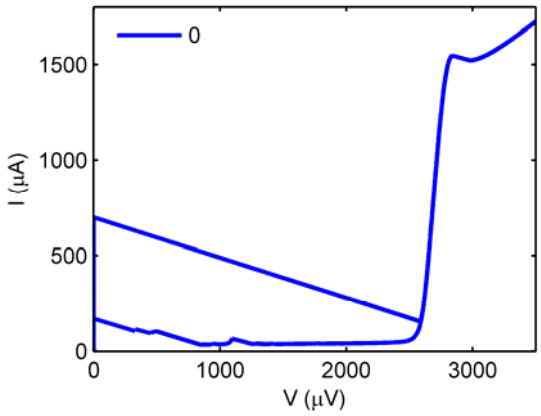
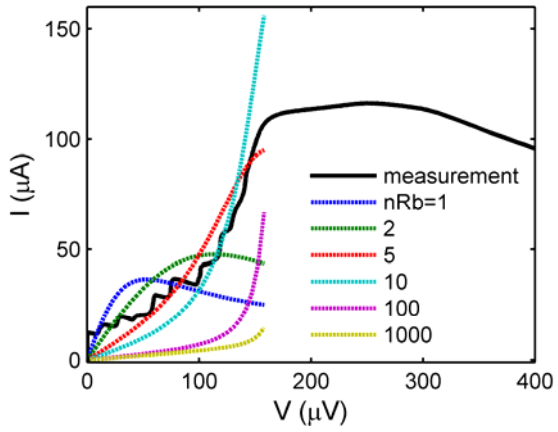


Figure 4.6. (a) Schematic and (b) micrographic photo of the build-in vortex injector (pump). L0 = 3.96 pH, I_C = 187.5 μA, β_C = 1.4, LTL = LTR = 2.64 pH. L1 is negligible, Mutual coupling K0/L0 = 0.3, effective inductance between left of LTL and right of LTR is equal to clock line inductance L (4.49 pH) of LJJ. (c) Simulation result of injecting vortices to JTL connected with the pump, 5 vortices are shown to be injected.

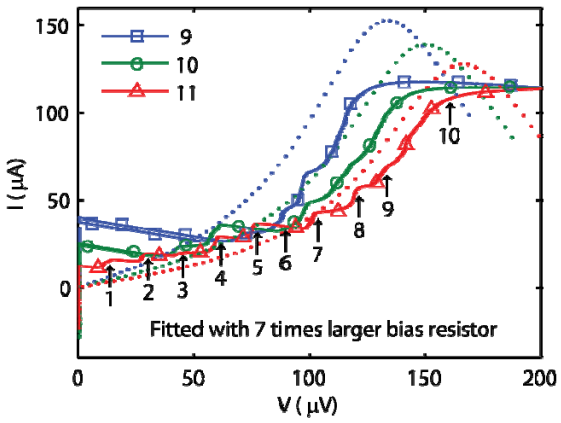
The IV curve without vortices (Figure 4.7(a)) is similar to those of a conventional tunnel junction with critical current about 0.7 mA. In general the IVs measured with injected vortices are rather messy. However, the part of IVs that corresponds to the operation condition of our circuit at low voltages and large numbers of vortices (Figure 4.7(b)) are quite simple and rather close to our expectations.



(a)



(b)



(c)

Figure 4.7. Voltage-current characteristics of the ring LJJ measured (a) at 0, (b) at 11 and (c) at 9, 10 and 11 injected vortices. Negative slopes are caused by a resistive bias current divider with 4.7 Ohm "load" resistance. Dashed lines in (b) and (c) are simulation results with model shown in Figure 4.8. nRd in (b) is the ratio between fitted and designed value of Rd. nRd is 7 for the simulation results in (c).

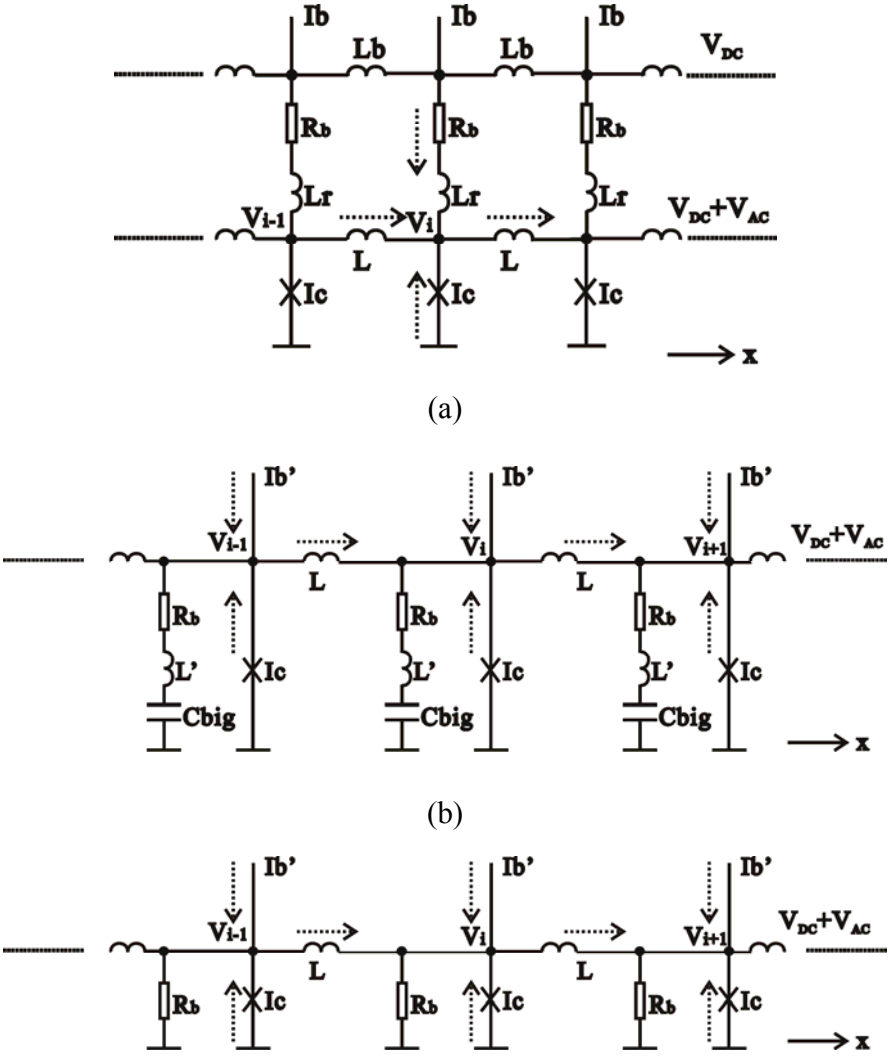


Figure 4.8. Demonstration of our model which includes bias resistor Rb into the simulation of critical current of LJJ. (a) Schematic of our LJJ circuit, which is almost the same as what is shown in Figure 4.3 but neglects only the inductance in series with each JJ. (b) and (c) present the approximation procedure that finally equates Rb to an extra shunt resistor of JJ. Dashed arrows show the direction of opposite currents of our model simulated using in-house software.

The most distinguishing feature of the curves in Figure 4.7(b) is the low (about 0.1 mA) heights of their turning points corresponding to vortices travelling at about Swihart speeds. Such low heights contradict simple theories assuming a uniform motion of the vortex grid with a constant speed. More exactly, peak heights in such theories (see, for example, [55]) should be

about as high as 0.7 mA corresponding to the cumulative critical current of all junctions in the ring.

The deviation between measurements and the theory predictions is caused solely by the biasing technique used in the experiments. This detail of this technique is shown in Figure 4.3(c) and can be approximated by another circuit as shown in Figure 4.8(a) because a low value bias resistor Rb acts similarly to subgap junction resistance. The correct heights of the peaks could be estimated in the frameworks of old theories [55]. Actually, the bias resistors are connected not with the ground plane but instead with a terminal having another voltage very close to the measured voltage V, which is a DC voltage shown as V_{DC} in Figure 4.8. If we neglect bias inductances Lr and Lb in Figure 4.8(b), the dynamic impacts of bias resistors could be taken into account by replacing subgap resistance with parallel connection of bias and real subgap resistances in Figure 4.8(c). Therefore, as the last step of our calculations we should subtract the nonexistent dc current flowing via bias resistor from the numerically obtained $I(V)$ (Ib' in Figure 4.8):

$$I(V) \to I(V) - V / Rb. \tag{4.3}$$

In Figure 4.7(b), the influence of increasing value of Rb, from 1 to 1000 times of real designed value of Rb (0.78 Ohm), is shown as dashed lines. When the ratio, nRb, between the simulated and designed Rb is 10, β_C of JJ is 1.22. As shown in the figure, when β_C is increasing, the position of the resonance peak of I-V curve shifts to a larger current value until it reaches the limit set by the maximal speed of vortices: Swihart speed. Simultaneously, the height of the peak is increasing due to the transition to the low-capacity JJ case [55]. The best fitting results (dashed

lines in Figure 4.7(c)) match reasonably well with the experimental data. However, the numerical values of bias resistors corresponding to the best fitting are about 7 times higher than their actual values. This mismatch is because of the negligence of inductances Lr and Lbt in the simulation, which in fact attenuate effectively ac currents in the circuit.

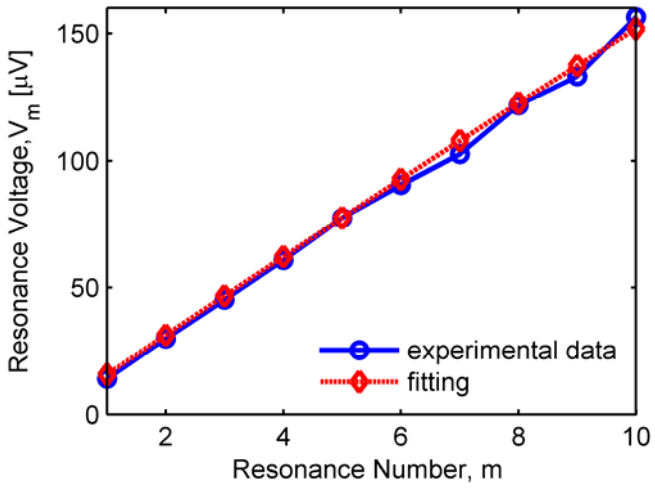


Figure 4.9. Comparison of measured resonance voltage with calculated ones using Eq. (4.4).

The numerical values of resonant voltages are in correspondence with the periodic motion of vortices along the ring with Swihart speed. Indeed, the voltage drop corresponding to the rotation of a single vortex along the ring with Swihart speed is about 15 μV. This voltage drop grows proportionally with the number of travelling vortices, and for resonances observed at 9, 10 and 11 vortices the corresponding voltage drops are expected at 135 μV, 150 μV and 165 μV. In addition, we see clearly "permanent" resonances at

$$Vm = \frac{\Phi_0}{\pi\sqrt{LC}} \sin\left(m\pi / N\right), \tag{4.4}$$

where L and C are the inductance and capacitance of a single stage, m is the resonance number and N = 77 is the number of stages in the ring. This formula is a simplified revision of several

different formulas that can be found in [56]. As shown in red curve of Figure 4.9, the calculated resonant voltages using this simple formula are in good agreement with the experimentally measured ones.

Another important observation is the more regular resonant structure with 11 vortices in the ring. It is because in this case there are an integer (seven) number of Josephson junctions per vortex period. The peculiarities mentioned here are discussed in detail, for example, in [52] and [56]. The peculiarities can serve as extremely valuable diagnostic tools. However, they are not important for circuit operation since at current state we plan first to operate our circuits at sufficiently slow clock frequencies. The lowest observed resonance corresponds to about 15 μV or about 7 GHz clock frequency.

The observed 10 μA to 20 μA critical current of the ring corresponds to 0.13 μA to 0.26 μA per stage. Although this number still exceeds the threshold, we are satisfied with the initial result because by testing this circuit we are able to indentify several parasitic factors. The first one to suspect would be a fabrication spread of critical currents. However, the fact that several chips from the same batch showed similar and consistent results does not support such suspicion. Next one would be flux trapping in the ground plane. This is connected to the fact that the measurement results are somehow different after each thermo-cycle. The last one would be several design irregularities existing in our circuit. I) Not all inductances L and LJ (see Figure 4.3) are identical. II) The vortex injector behaves differently than we expected. We assume that in a passive mode it could behave as a regular LJJ section, but the injector capacitance is 3 times larger than capacitances of regular sections. III) There are unaccounted capacitances of wires that

are needed to apply the bias current and to measure the voltage. IV) The greatest mistake is because of irregularities of the bias distribution scheme highlighted by light gray in Figure 4.3(c). Our idea was to make bias resistors as low as possible. The idea of low bias resistors by itself is not new, see for example [57]. But it is perfectly good for us because of purely periodic processes in biased junctions. V) Due to the dense vortices, the value of AC voltage component is lower than that for a stand-alone unshunted Josephson junction. As a result, we can assume that the value of bias resistance may approach zero. However, in this extreme case of "zero" bias resistors the inductances of the power distribution system (grey area in Figure 4.3(c)) become parts of the clock line. To reduce the impact of power distribution inductances we keep them large. Unfortunately, they are not large enough and we did not keep them equal.

4.4. Conclusion

In this chapter, the discrete long Josephson junction that matches our nSQUIDs shift register has been investigated. We theoretically analyze the static and dynamic properties of the LJJs, which are shown to have the low energy dissipation in a timing belt scheme. The measured results agree well with the theoretic prediction. In next chapter, we will discuss circular nSQUIDs shift register as a new test reversible circuit.

Chapter 5 Circular Shift Register

5.1. Introduction

From the measurement of the chip 'REVCOM04' discussed in Chapter 3, we realized several aspects of our circuit need to be improved or modified. Among them the most important one is to make shift registers in a loop to form a circulating path and to avoid the energy dissipation of moving vortex. In this chapter we will investigate the mechanism of such circular shift register.

In a string of nSQUIDs, we have eliminated the dissipation of energy in the shunt resistors and have reduced the bias voltage of LJJs to a nano-volt level. For this relatively short circuit, bias resistors have been completely eliminated. There is still, however, a considerable energy flow associated with the clock vortices themselves. To avoid energy dissipating coming from these vortices, they, together with their energy, can be "recycled", e.g., by connecting the clock lines of the two shift registers to form a circulating path or a ring as shown in Figure 5.1 [39]. In the simplest regime of operation, the ring contains only two vortices (N = 2 in Figure 5.1), one per each shift register, which propagate in opposite directions. Dynamics of the vortices in this structure is similar to the vortex motion in unshunted ring-shaped Josephson junctions. Ideally, such ring junctions have zero critical currents (i.e., any applied non-vanishing bias current leads to vortex motion), and the principal energy-dissipation channel for slowly moving vortices is the sub-gap junction leakage current, roughly proportional to the vortex speed.

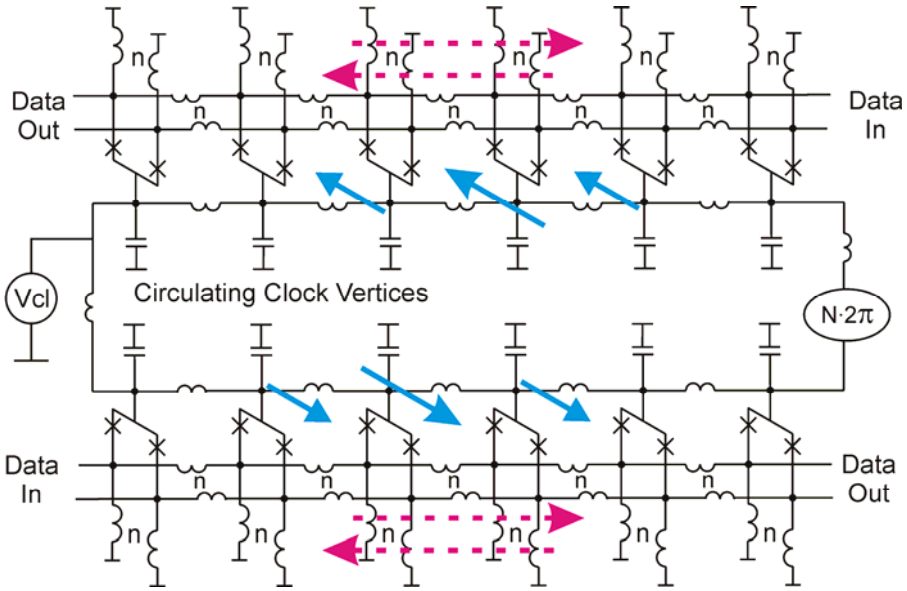


Figure 5.1. Equivalent circuit of the two shift registers with a common clock ring. Only 6 of 8 cells are shown.

Therefore, in an ideal regime, this model of vortex motion can be characterized as zero energy dissipation. However, any imperfections, e.g., the discrete structure of the junction or non-uniformity of the critical current density, immediately induce some finite critical current and additional dissipation mechanisms. In the regime of slowly moving vortices, the extra energy dissipation can be described in terms of variations of the speed of moving vortices. To suppress as strongly as possible these variations and therefore the variations of the voltage across the array, we need the source of the bias voltage *Vcl* to have minimum internal impedance. Such a voltage source has been tentatively implemented as a resistor with low resistance *Rv* (Figure 5.2). The required dc voltage *Vcl* is obtained by applying large current *Iv* to this resistor. Since only one such voltage source per circuit is needed, and its structure is independent of the circuit complexity, we treat it as external to the circuit and exclude the energy dissipation in the voltage source from our energy budget. Nevertheless, as one of the many measures to improve the circuit,

we plan to implement more advanced “capacitive” voltage source that would not dissipate energy.

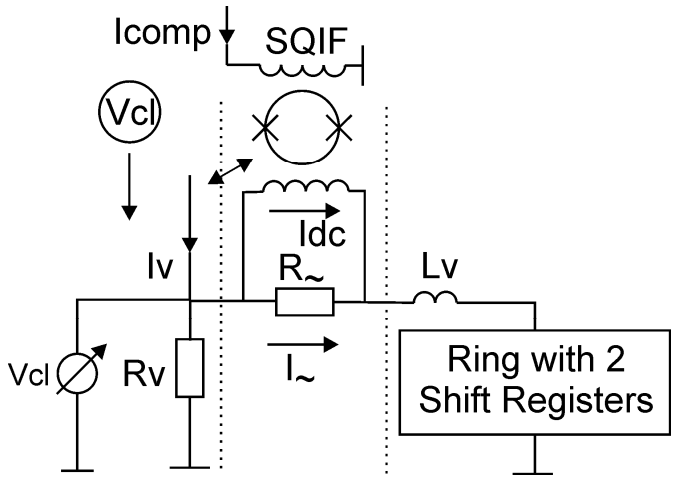
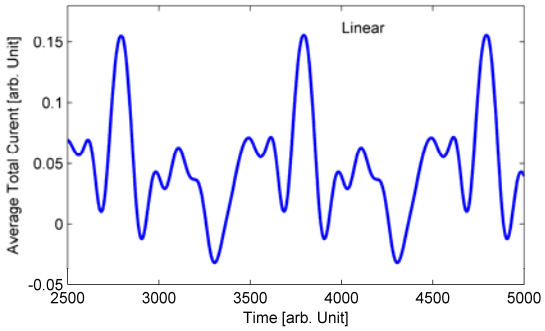


Figure 5.2. Diagram of the setup for measurement of the energy dissipation in the shift register structure shown in Figure 5.1. The bias current *Iv* flowing through the bias resistor *Rv* creates the voltage bias *Vcl* for the shift registers that is applied through the resistor $R_{\sim}$ shunting the inductance of the current-measuring part of the circuit at large frequencies. The current through the shift registers contains both the dc and ac parts *Idc* and $I_{\sim}$. The double-sided arrow indicates parasitic coupling between the bias current and the current-measuring SQIF. (For discussion of SQIF, please refer to Sec 5.3.1 in this chapter.)

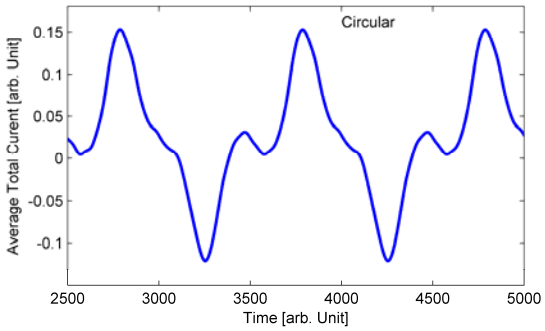
5.2. Simulation

Energy dissipation of circular shift register of nSQUIDs in Figure 5.1 was first analyzed by the numerical simulation tool PSCAN, which is developed to simulate superconducting circuit. From Eq. (3.4), the energy dissipation depends only on the working current of the circuit. For this reason, only the information of the working current is needed to access the energy dissipation and it is shown in Figure 5.3(b). Data in the figure is the averaged total current of the circuit over 100 arbitrary unit of time shown as x-axis. Figure 5.3(a) shows the same current but plotted for the circuit without return path (such as the circuit shown in Figure 3.7(a)) for comparison

purpose. Obviously, the pattern of the current is much more regular in circular shift register than that in linear shift register. At the same time, the current in Figure 5.3(b) is much more symmetric around the average total current. To get lower value of energy dissipation, we need to maintain smaller average current of the circuit. More regular and symmetric pattern of circuit current in the case of looped shift registers will give smaller average current and therefore lower energy dissipation of whole circuit.



(a)



(b)

Figure 5.3. Comparison of total working current of circuit between (a) convenrtional and (b) circular shift registers.

We have also simulated the actual time dependence of the current in the circuit of two shift registers (Figure 5.1) using the same tool PSCAN. Figure 5.4 presents the results of the simulation using parameters that are close to their experimental values. It shows that the

amplitude of current flowing in the individual nSQUIDs is quite large, about 10 μA, a number that is about 2 times larger than the critical current of a single Josephson junction. The current in different nSQUIDs, however, offset each other, so that the total current through the circuit does not scale with the number of nSQUIDs (Figure 5.4), and roughly has the same amplitude as the current in one nSQUID. Moreover, its average value is still much lower than its ac amplitude.

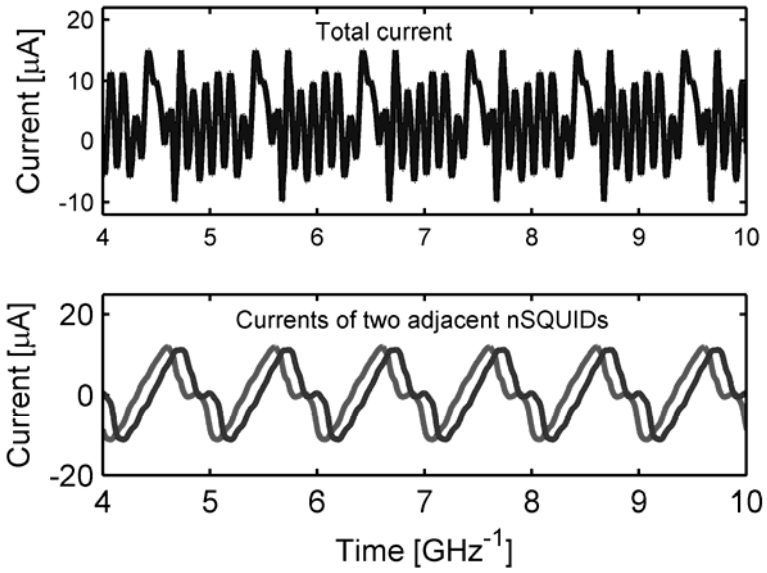


Figure 5.4. Numerically simulated behavior of the circuit shown in Figure 5.1.

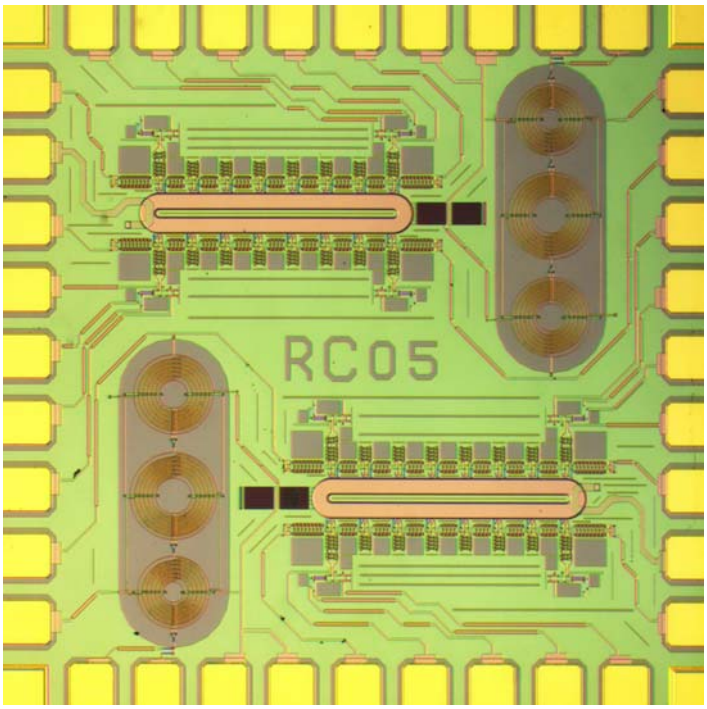
5.3. Optimization of Circuit for Minimal Energy Dissipation

In our measurement setup (Figure 5.2), the current is measured using a compensation technique, with a SQIF (for details, see, e.g., [58]) as the null detector. There are two limitations to such a measurement scheme. One is technical: a finite parasitic coupling between the bias current *Iv* and the SQIF. Another is more fundamental limitation, which is related to the non-vanishing ac component $I_{\sim}$ of the current through the measured shift register circuit. This component is created by the Josephson oscillations in the circuit which acquire finite critical

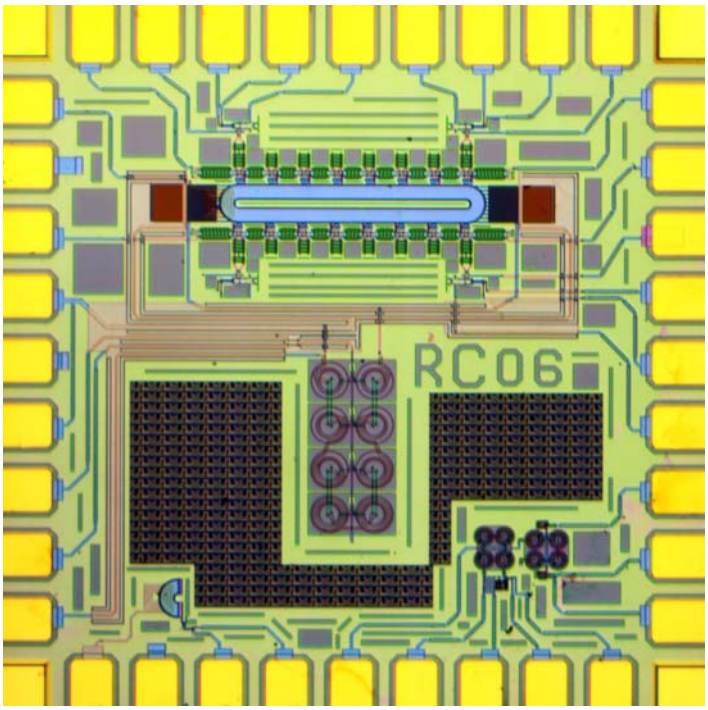
current *Ic* because of the discreteness of the structure and/or other possible imperfections. As usual, Josephson oscillations are characterized by, in general, complex relations between the power dissipation at different frequencies [59]. The limitation of our measurement setup is associated with the conversion of the zero frequency power to ac power at Josephson frequency $f = V_{cl} / \Phi_0$. Although this energy is dissipated physically in the resistor *Rv* of the voltage source, it is registered by the SQIF as correction I_f to the dc current *Idc* through the shift register circuit. In the relevant overdamped regime, where the circuit capacitance *C* can be neglected, I_f can be estimated by modeling the circuit as one Josephson junction with critical current *Ic*:

$$I_f = Iv - \sqrt{Iv^2 - Ic^2} \sim Ic \cdot (Ic / 2Iv). \tag{5.1}$$

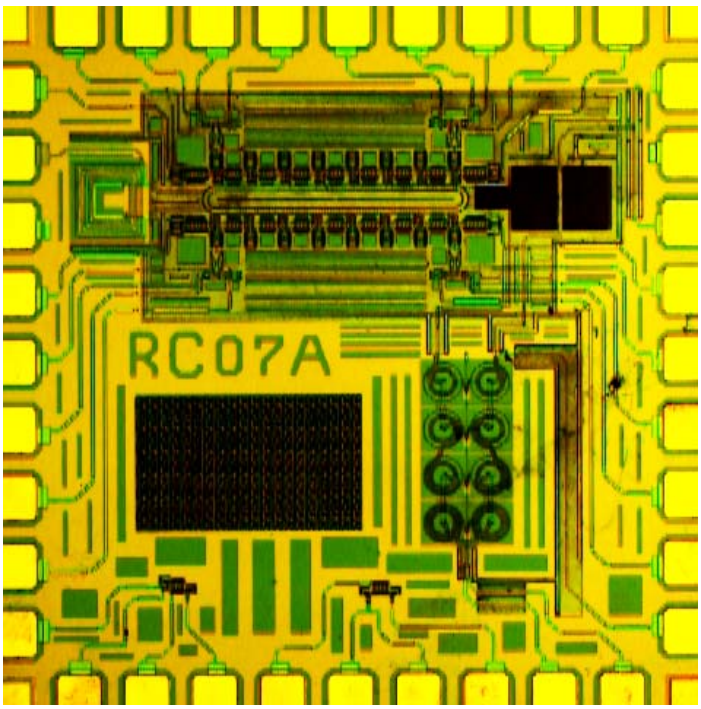
This above equation shows that this correction to the current decreases rapidly with increasing bias current *Iv*. The need to make I_f small, so that it does not preclude the measurement of energy dissipated in the circuit, was the main reason for making the resistance *Rv* in our circuit very low (0.0017 Ohm for chip RC06, RC07A and RC08, 0.0057 Ohm for chip RC05). Small *Rv* leads to large value of *Iv* at fixed bias voltage *Vcl* that determines the circuit operation frequency. As soon as there is no need to prove the low energy dissipation anymore, or a better measurement technique, e.g., based on a capacitive voltage source, is implemented, the resistance *Rv* can be dramatically increased.



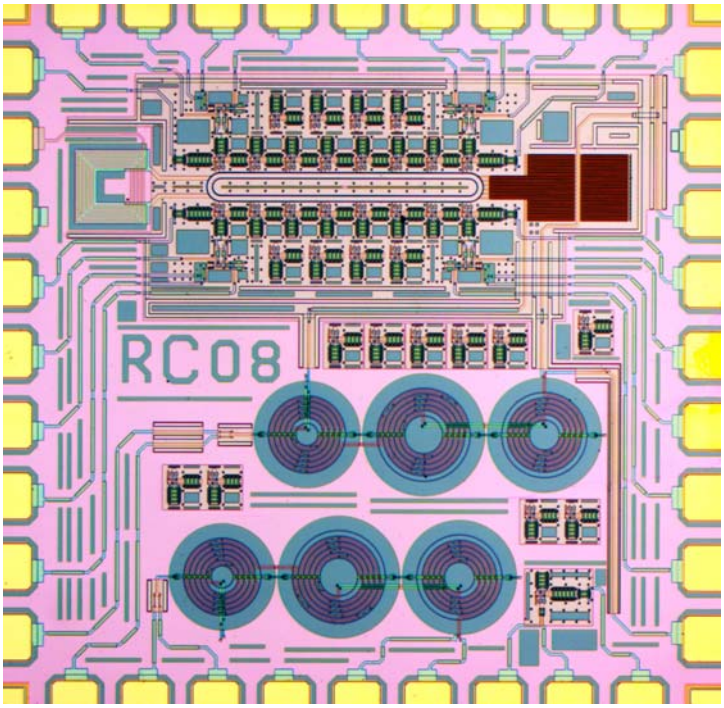
(a)



(b)



(c)



(d)

Figure 5.5. Layouts of four different versions of nSQUIDs circular shift registers.

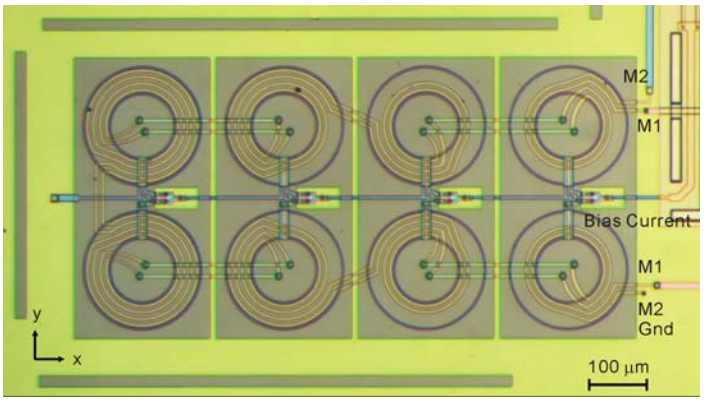
Because of the new characteristics of the reversible nSQUID circuits, we have gone through many iterations of development process to resolve design and (some of the) measurement problems. Figure 5.5 shows the micrographic photos of the four revisions of the circular shift registers. The fifth revision (RC05 in Figure 5.5(a)) showed the first sign of functional circuit and functional SQIF to track the working current of circuit. The sixth revision (RC06 in Figure 5.5(b)) of the shift register circuit showed an appropriate functionality, while the seventh (RC07A in Figure 5.5(c)) and eighth (RC08 in Figure 5.5(d)) revisions demonstrated a reasonable level of quantitative agreement with our numerical estimates.

5.3.1. SQIF

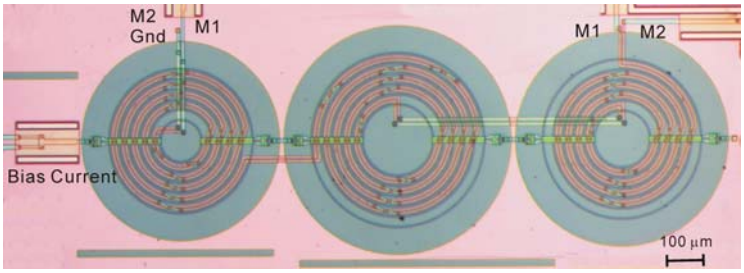
The working current of the tested circuit was measured by a compensation technique using superconducting quantum interference filter (SQIF) as the zero magnetic field sensor [60, 61]. SQIFs were proposed as high resolution magnetometers [62] or as broad band amplifiers [63] because of its unique properties and high transfer factor (gain). SQIF is an array of Josephson junctions (JJs) with a selected distribution of the loop areas, so that voltage modulation of the magnetic bias is a delta-like dip with the deepest point at zero magnetic field. The amplitude of the dip increases with the number of JJs loops connected in series. Based on the interferometer principle of all loops, SQIFs are expected to have an ultra-high sensitivity to the magnetic field, with a flux noise level of few $fT/\sqrt{Hz}$ [62]. The intrinsically high dynamic range and the linearity in the voltage output (in a certain region of the curve within the dip) represent the main advantages of using SQIFs.

There are two versions of SQIFs used in our circuit to measure current, which are shown in

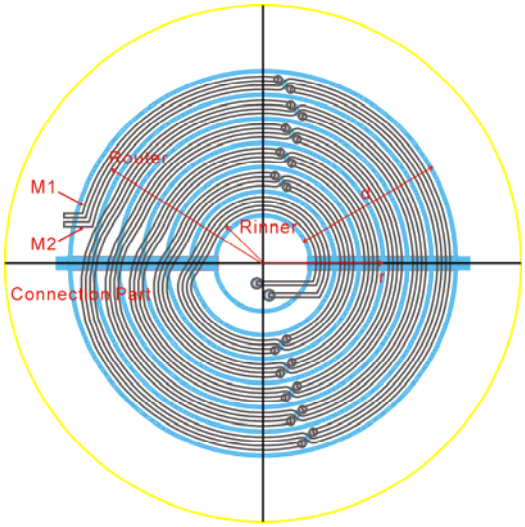
Figure 5.6(a) and (b) respectively. The one with four SQUIDs in series is used in chips RC06 and RC07A. The self inductance of every SQUID is composed of two coil inductances in series which are placed on right and left sides of JJs. These two coil inductances have opposite directions of rotation, which will cancel any frozen magnetic field in z direction (perpendicular to the chip plane). However, these two coil inductances will pick up the magnetic field in x direction (from the right coil to the left coil): the hole of the ground plan under the two coils will convert the x direction magnetic field to two opposite directions of magnetic field perpendicularly, and these will be detected by the SQIF. Besides, there is parasitic coupling of this version of SQIF sensor with high-current auxiliary circuitry, which also spoils the measurement result. The disturbance is shown in the unsymmetrical voltage modulation measurement in Figure 5.7(a).



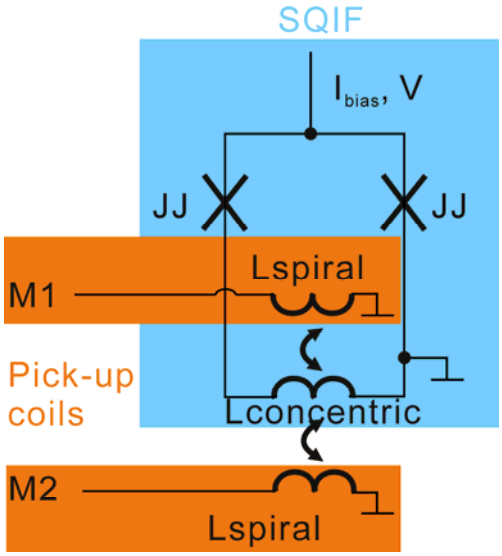
(a)



(b)



(c)



(d)

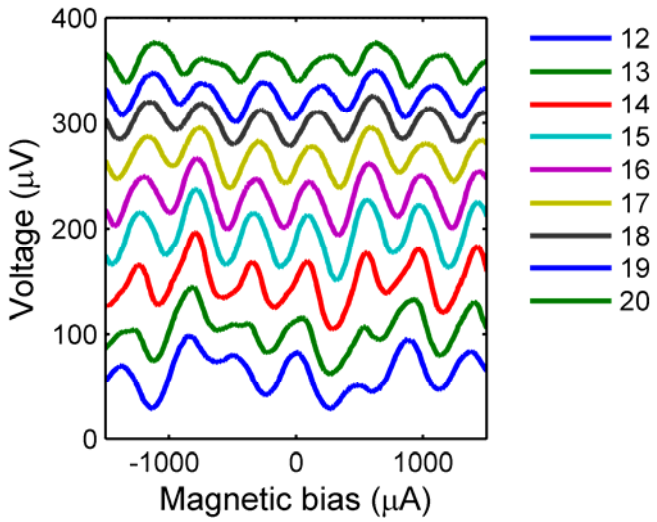
Figure 5.6. (a) and (b) Micrographic photos of SQIF with four (from chip RC06) and three JJs (from chip RC08) loops in series. The critical currents of the JJs in the SQIF are all identical: I_C = 10 μA, β_C = 0.6. (c) Layout of the two pick-up coils in the middle loop. The each turn of two coils intersected twice to make sure the total inductances are identical as much as possible. (d) Effective schematic which simplified the three JJs loop into one.

We prefer the SQIF containing three SQUIDs (Figure 5.6(b)), which is placed in chips RC05 and RC08. We have improved the design of the SQIF in RC08 compared to RC05 with some important optimizations. These SQIFs cover relatively large area of the chip and as a result they

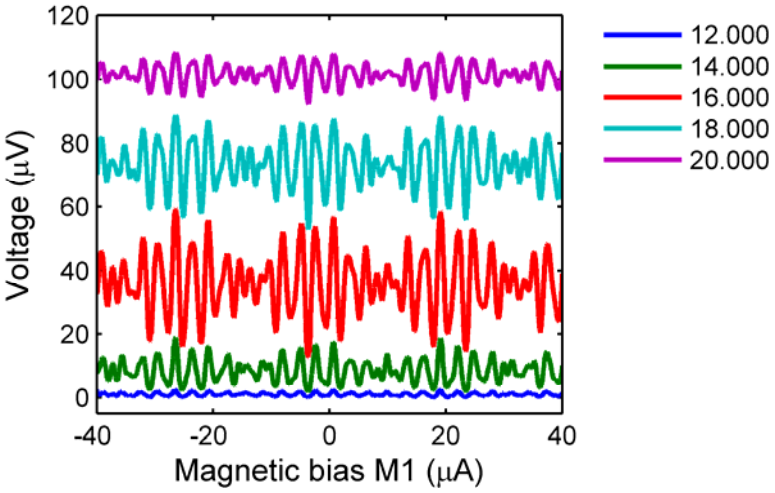
are very sensitive to external magnetic field. That is the reason why holes are always added to the ground plane under the SQIF. In order to avoid the influence of any small magnetic filed on the SQIF, in the RC08 revision, we made the holes on the ground plane in a circle shape under each circular coil and we added one JJ-like cell on the other side of coils in each SQUID. All these efforts are aimed to increase the symmetry of the circuit such that the current inside the SQIF will not introduce more disturbances to the measurement result. Also, extra metal layer of shield has been placed in the design after RC06 revision. We sacrificed one metal layer to increase the shielding against even small magnetic field distribution.

The SQIF implemented has two on-chip pick up coils for the compensation application (Figure 5.6(d)). The two pick up coils are designed identically to make sure they can completely compensate each other.

We start the investigation of the property of SQIF shown in Figure 5.6(b) by measuring the voltage vs. magnetic bias. The result is shown in Figure 5.7(b). The deepest dip is shifted from the zero magnetic bias because the flux trapping near the large area of SQIF. The modulation is symmetric to this dip; when bias current is 18 μA the dip falls into optimized case for detecting zero magnetic.



(a)



(b)

Figure 5.7. (a) Voltage modulation of SQIF shown in Figure 5.6(a). (b) Voltage modulation of SQIF shown in Figure 5.6(b). Legend is the bias current of SQIF in unit of μA. The shift of the deepest dip from the zero magnetic bias indicates the existence of external magnetic field, which most come from the flux trapping near to the SQIF.

The inductance of the pick up coils can be estimated based on Wheeler's formula [64]:

$$R_{mean} = (R_{inner} + R_{outer}) / 2, \tag{5.2}$$

$$\text{thickness} = R_{outer} - R_{inner}, \tag{5.3}$$

$$L_{spiral} = 3.93\times10^{-5}\cdot R_{mean}^{2}N^{2}/(8\cdot R_{mean}+11\cdot \text{thickness}), \quad (5.4)$$

where R_{inner} is the inner radius of the first loop of the coil in μm, R_{outer} is the outer radius of the last (outside) loop of the coil in μm, and L_{sipral} is the inductance of spiral coil in μH.

The inductance of the SQIF loop $L_{concentric}$ in μH can be calculated as:

$$L_{concentric} = \mu_0 r\left[\ln\left(8\cdot\frac{r}{d}\right)-0.5\right], \quad (5.5)$$

where $\mu_0 = 4\pi/10$ is the vacuum permeability, r is average radius in μm, and d is the thickness of the concentric coil in μm as shown in Figure 5.6(b).

The inductance of pick-up coil of the middle loop in the SQIF (Figure 5.6(a)) is the largest among the inductances of three loops. R_{outer} and R_{inner} are 224 μm and 108 μm. With N = 5, L_{spiral} is 9.86 nH. The inductance in the middle loop of JJs is 0.36 nH. The coupling coefficient of these two inductances is about 0.3, and therefore the mutual inductance between them equals to 0.56 pH. As shown in Figure 5.6(b), the magnetic bias difference between two closest adjacent dips ($\Delta I_{MagBias}$) is around 3.1 μA. This difference corresponds to the period of voltage modulation of the two JJs loop with the largest mutual inductance inside the SQIF. Therefore, the largest mutual inductance derived from the measurement is $\Phi_0/\Delta I_{MagBias} = 0.67$ pH. It matches well with the estimated value 0.56 pH.

The compensation technique is tested by tracking the modulation of SQIF on magnetic bias from one pick-up coil (M1) by applying different current trough the other pick-up coil (M2) as shown in Figure 5.8. Increasing current applied to M2 will shift the voltage modulation of SQIF to a lower magnetic bias of M1 as indicated by the dashed arrow in Figure 5.8. The amount of

magnetic bias shift of M1 equals approximately to the current change in M2. For example, the shift of dip or voltage modulation of magnetic bais (M1) is 3.99 mA when current applied to M2 changed by 4 mA. This observation confirms the validity of the compensation technique.

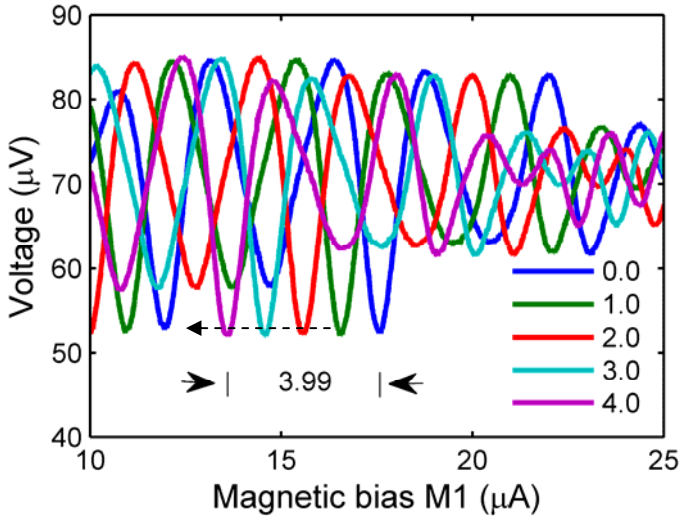
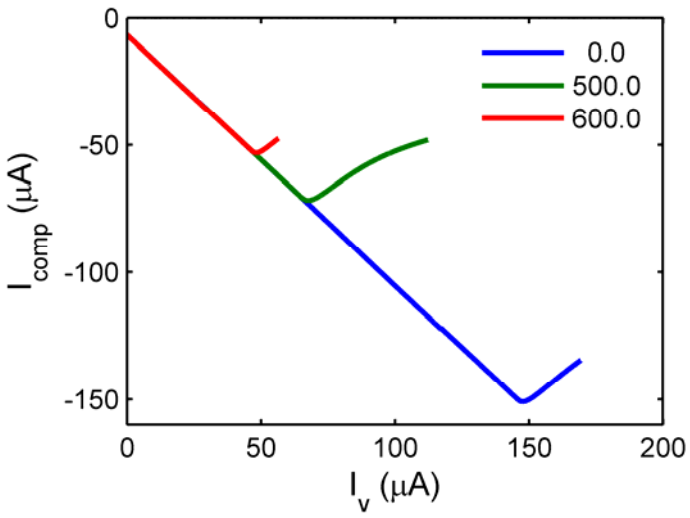
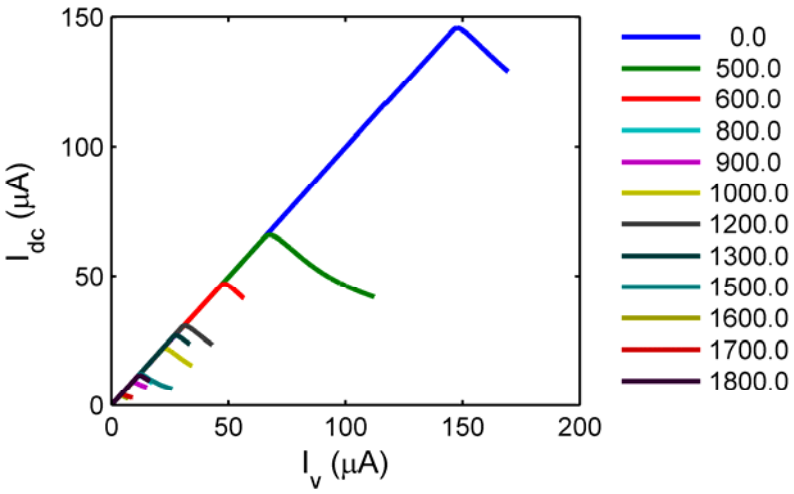


Figure 5.8. Working mechanism of SQIF for current measurement. Legends are magnetic bias applied by the other pick-up coil (M2) of the SQIF.

To measure the working current of the test circuit by SQIF as shown in Figure 5.2, we kept the voltage constant for the SQIF, with value corresponding to the deepest part of the dip by applying proper current I_{comp} through one pick-up coils to compensate the current I_{dc} through the other coil of SQIF. The measurement results, with different magnetic field applied into the shift registers or in other words with different critical current of the shift registers, are shown in Figure 5.9(a). Before the I_v reaches the critical current of the circuit, I_{dc} follows with I_v in magnitude since the JJs are in superconducting state. Using the data in this region we can obtain the accurate compensation ratio between two pick-up coils (I_{comp}/I_{dc}) of SQIF. Figure 5.9(b) shows the same plot but the y-axis I_{comp} is converted to show current through the circuit I_{dc}.



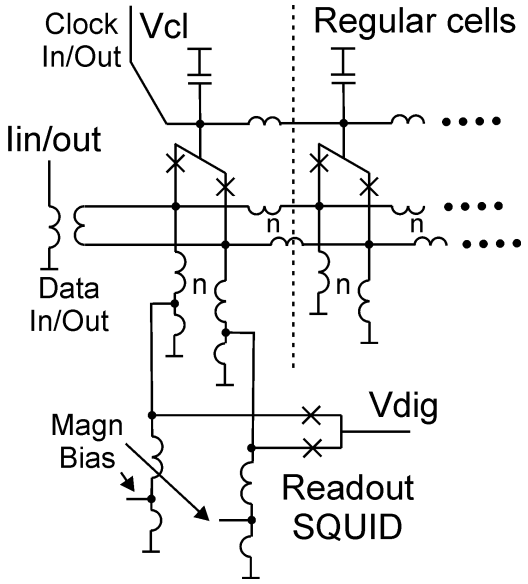
(a)



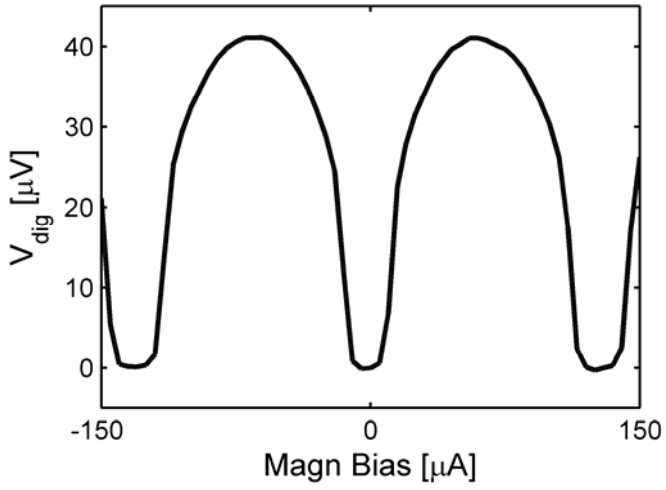
(b)

Figure 5.9. (a) I_{comp} v.s. I_v (Figure 5.2) while keeping voltage of SQIF unchanged for different magnetic bias applied to the clock line of shift registers. (b) Convert I_{comp} to I_{dc} (Figure 5.2) to obtain the measurement of working current of the circuit.

5.3.2. Readout SQUIDs



(a)

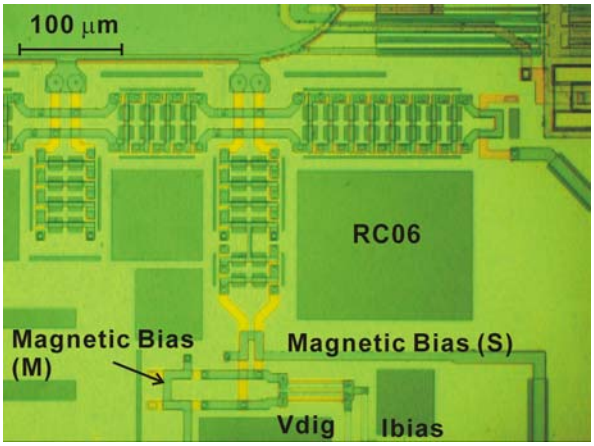


(b)

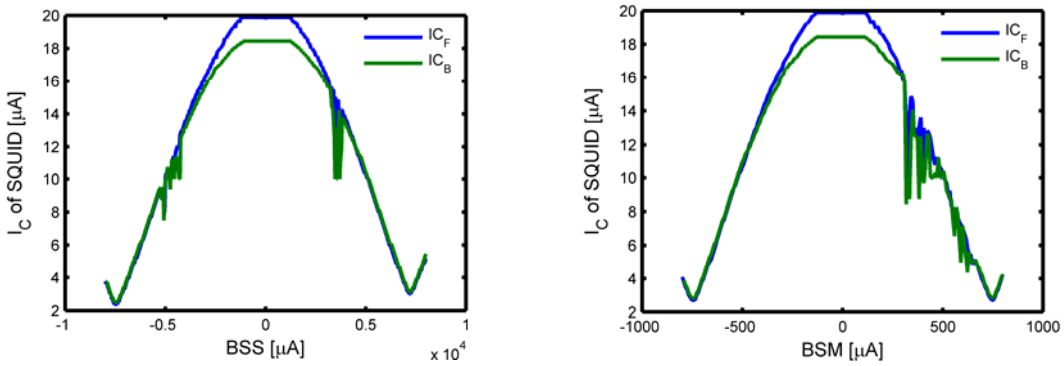
Figure 5.10. The universal read/write cell that terminates both ends of the two shift registers in our ring structure: (a) equivalent circuit and (b) measured output characteristics of the readout SQUID.

The data readout is performed by the SQUID shown in the lower part of the cell in Figure 5.10(a). This readout SQUID measures the differential magnetic flux representing logic data

stored in the corresponding nSQUID. The SQUID is only weakly coupled (the corresponding coupling coefficient is $k \sim 0.02$) to suppress their undesirable interaction. At the same time, this coupling is sufficient enough for measuring the flux state due to high sensitivity of the readout SQUID (see Figure 5.10(b)). To measure the readout or input of the shift register, we first need to apply proper external magnetic bias to make the voltage of SQUID stays in the largest slope range, e.g. around 20 μV as for the modulation shown in Figure 5.10(b).

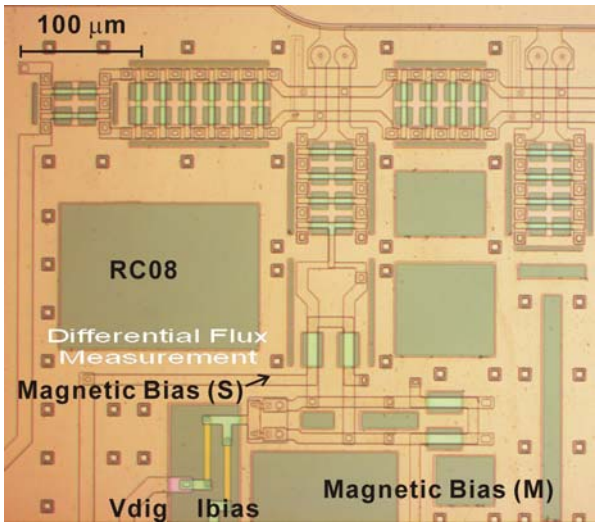


(a)

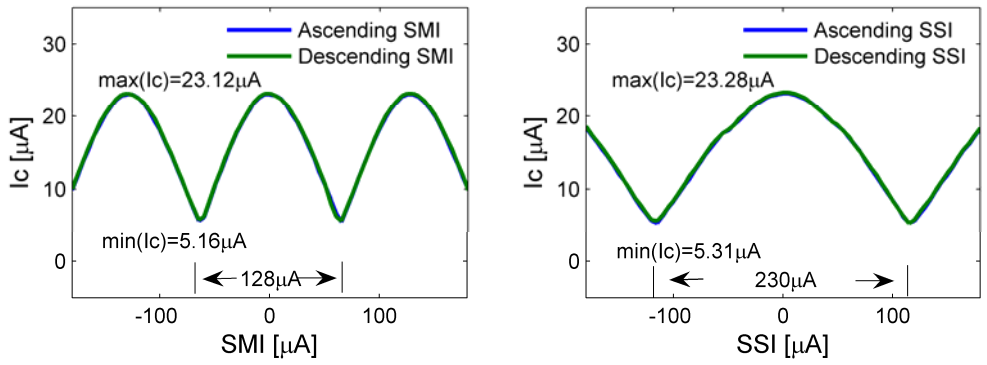


(b)

Figure 5.11. (a) Micrographic photo of readout SQUIDs in chips RC05 and RC06. (b) The dependence of critical current on the two channels of magnetic bias in the SQUIDs.



(a)



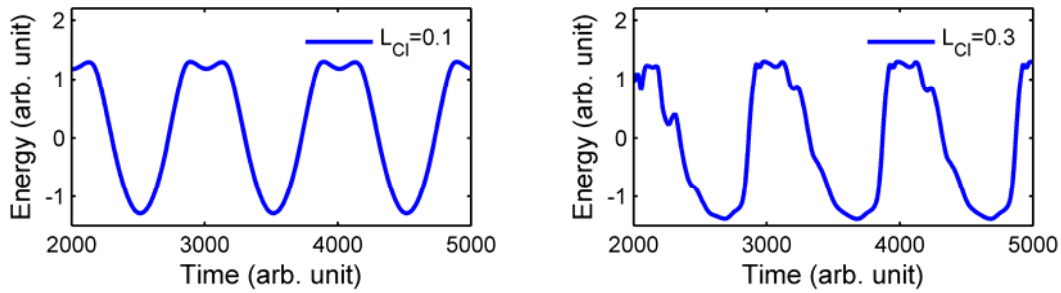
(b)

Figure 5.12. (a) Readout SQUIDs in chips RC07A and RC08. (b) The modulation of critical current of SQUIDs shown in (a).

There are two magnetic bias sources for the SQUIDs shown as M and S in Figure 5.11(a) and Figure 5.12(a). The measured modulation of critical current of SQUIDs for these two sources is shown in Figure 5.11(b) and Figure 5.12(b) respectively. The readout SQUIDs are the same for revision RC05 and RC06, and in the later revisions we make the two magnetic bias channels much more similar to make it easier to carry out compensation measurement. As shown in Figure 5.11, the period is 11.1 mA and 1.1 mA for channel S and M respectively. Since any high current may have influence on the current measurement with the sensitive SQIF, these two periods are

reduced to 230 μA and 128 μA in the SQUIDs shown in Figure 5.12. The reduction in periods is realized by adding extra holes in the ground plane under the magnetic bias wires of the transformer to increase the coupling effect. Simultaneously, moats of ground plane are placed close to SQUIDs in the later revision to avoid any flux trapping nearby. Moreover, the JJs in SQUIDs in Figure 5.12 are shunted with smaller resistor to reduce the oscillation in order for better voltage modulation, and therefore, for better measurement of readout.

5.3.3. Clock Line Inductance



(a) (b)

Figure 5.13. Simulation of the sensitivity of energy of 8-nSQUID shift register to the clock line inductance. The energy becomes much more irregular when clock line inductance is larger (b) compared to smaller L_{Cl} in (a). Inductance is unit of PSCAN simulation: 2.64 pH.

The value of clock line inductance L_{Cl} is a very important parameter for the shift register. As discussed in Chapter 4 on long Josephson junction, increasing clock line inductance will increase the energy dissipation. The simulation result shown in Figure 5.13(a) and (b) illustrates the fact that increasing L_{Cl} (form 0.1 to 0.3) spoils the regularity energy profile of the nSQUIDs shift register. Of course the need of small inductance will result in a larger area that the inductor has to occupy. The value of L_{Cl} in the first two chips shown in Figure 5.5 are chosen to be as small as 0.56 pH. The circular clock line inductor that occupies large chip area using two metal layers can

be easily recognized from the microscopic photo. However, after more careful analysis of LJJs shown in Section 4.2, L_{Cl} and LJ (inductance in series with JJ) influences the total critical current of the LJJs in a similar fashion. And LJ is already as large as 10.9 pH and this value can not be reduced (discussed in Chapter 2). Therefore, in the later versions (Figure 5.5(c) and (d)), we increased the value of the L_{Cl} to 1.69 pH. This clock line inductance still uses two metal layers and it makes crossing of wires impossible since the last wiring layer has been used as an extra magnetic shield (Section 5.3.5). Therefore in more complex circuit with longer nSQUIDs arrays, we prefer to increase the inductance a little more to free one wiring layer, which will be discussed in Chapter 6.

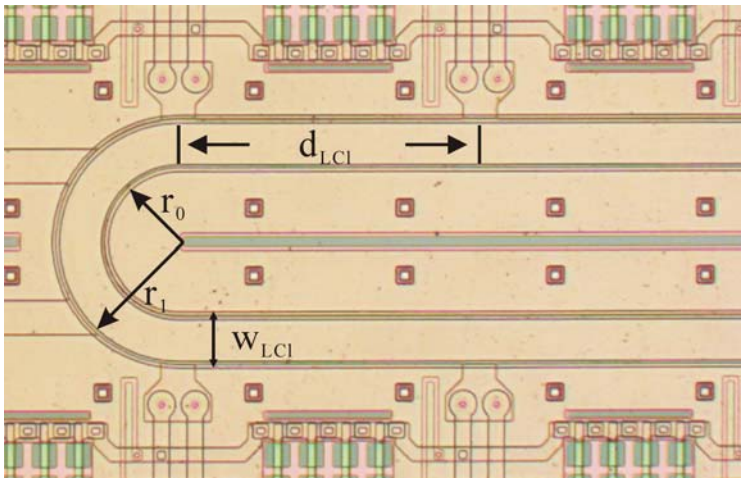


Figure 5.14. Micrographic photo of part of clock line inductor. This is the place where two shift registers are connected together.

From the view of long Josephson junction, L_{Cl} determines the penetration depth of the vortex (discussed in Chapter 1). In order to maintain a constant speed for the vortices moving along the shift register, it is very important to keep all clock line inductances (L_{Cl}) between adjacent nSQUIDs equal. For most of regular cells, we only need to keep their lengths d_{LCl} to be a

constant. The trick one is the semi-circle inductors which connect two shift registers together (Figure 5.14).

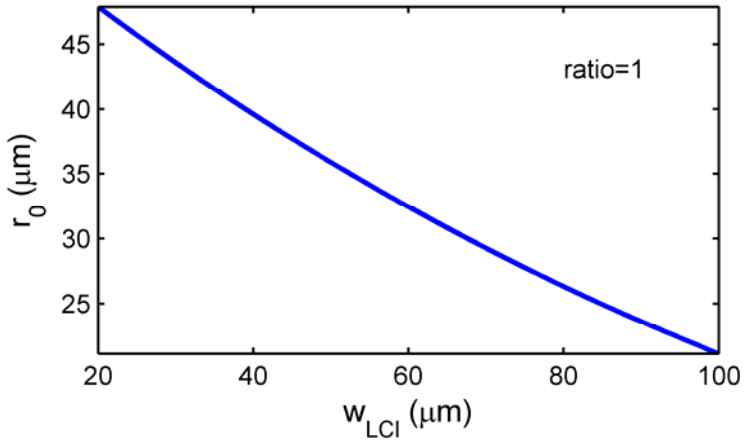


Figure 5.15. Dependence of inner radius r_0 on width of the inductance w_{LCl} in Figure 5.14 while keeping ratio of regular stripe and pi-turn circular inductances equaling to 1.

For the grounded inductor shown in this figure, the inductance of the pi-turn inductor is expressed as

$$L_{Turn} = \pi L_{\square} / \log(r_1 / r_0), \tag{5.6}$$

where $L_{\square}$ is the specific inductance, r_0 and r_1 are inner and outer radii of the pi-turn inductor.

The inductance of the stripe inductor with length d_{LCl} with the same width w_{LCl} is

$$L_{Cl} = L_{\square}(d_{LCl} / w_{LCl}), \tag{5.7}$$

where d_{LCl} is 180 μm for all the chips in Figure 5.5. Combined the above two equations, the relation between these two inductances can be expressed as:

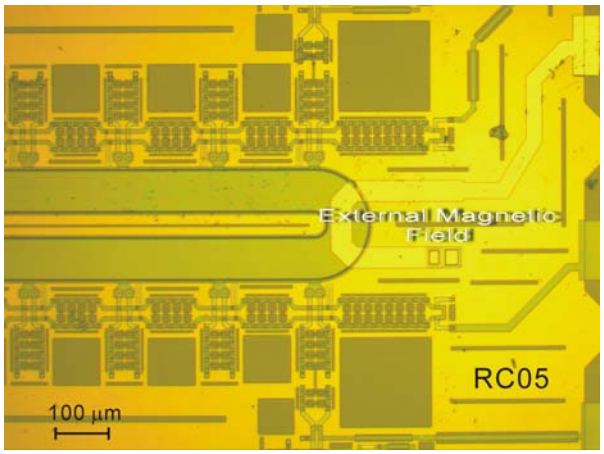
$$ratio = L_{TURN} / L_{Cl} = \frac{\pi}{N_{\square} \log(r_1 / r_0)}. \tag{5.8}$$

This ratio is set to be 1 for our circuit. The size of the circular inductor versus its width is plotted in Figure 5.15. Now with all the knowledge of the inductor, we are able to maintain the

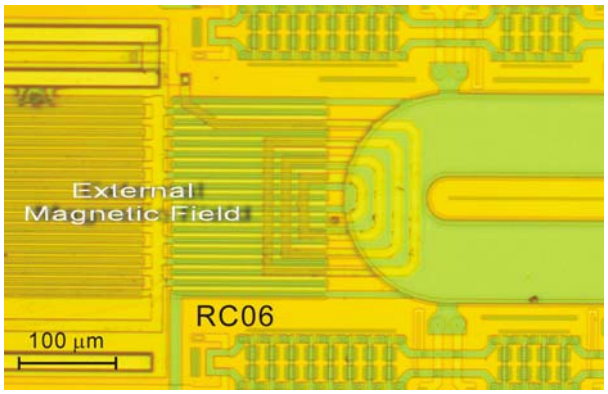
uniformity of the value of clock line inductances along the whole circular shift register.

5.3.4. Transformer for Injecting Vortex

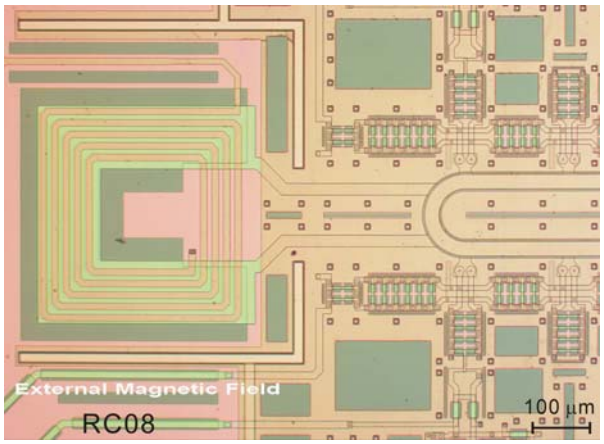
Another important fragment in the circuit is the transformer which applies the external field in the clock line of the circular shift register (Figure 5.16). Its function is to inject required number of vortices into the circuit to create certain clock phase shifts between nSQUIDs. The injected vortices will be the data carries and will reduce the total critical current of whole circuit. As for all on chip current sources, the current for injecting the vortices should not be large to influence the accuracy of SQIF. Current needed to apply $2\Phi_0$ magnetic field to two 8-nSQUIDs shift register was measured to be 21 mA for the transformer in Figure 5.16(a). This current is definitely too large. In the next revision shown in Figure 5.16(b), the required current was reduced to 5.6 mA. This current was further reduced to 1.7 mA in the design shown in Figure 5.16(c). The last revision not only reduced the amplitude of current, but also stayed much more isolated from the main circuit. This made the assembling work much easier and more importantly, reduced undesirable disturbance to the nSQUIDs circuit.



(a)



(b)



(c)

Figure 5.16. Evolution of the transformer to apply external magnetic field in the clock line of nSQUIDs circular. (a), (b) and (c) are transformers placed in chip RC05, RC06 and RC08 respectively. The transformer in chip RC07 is the same as in (c). From (a) to (c) the efficient of the phase source becomes larger, and meanwhile the transformer becomes more and more isolated from shift registers.

These transformers are good for applying small number of vortices into the nSQUID ring. Simultaneously, we can scan for critical current of circuit by varying the external magnetic bias to achieve the minimal point. However, for longer nSQUIDs arrays or circuits with more shift registers, it is not viable anymore because the increasing bias current. In that case, the RSFQ vortex injector mentioned in Chapter 4 is needed.

5.3.5. Extra Shield of Magnetic Field

As we discussed before, nSQUID circuits are very sensitive to external magnetic field. After testing the first revision of nSQUID circuits, mutual magnetic shielding was introduced to protect the cells (Figure 5.17(c)). As shown in Figure 5.17(a), typical circuits for quantum computing (QC) experiments contain two superconducting layers, while our first nSQUID circuit (Figure 5.5(a)) has an extra ground superconducting layer. In the later revisions of nSQUID cicuits (Figure 5.5(b), (c) and (d)), a fourth layer (most top layer) is connected with the ground metal to create mutual magnetic shielding for the cells inside. This mutual magnetic shield is critically important for our sensitive circuits and is proven to be necessary for much better measurement results.

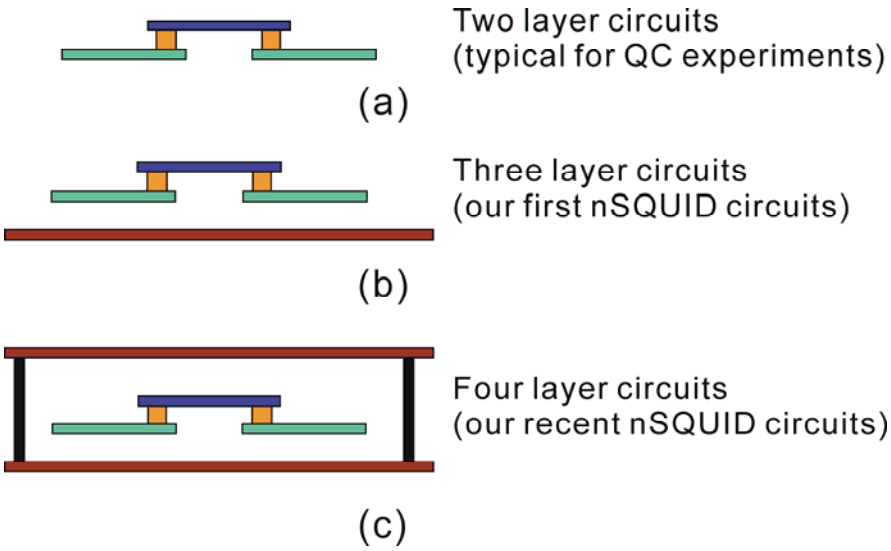
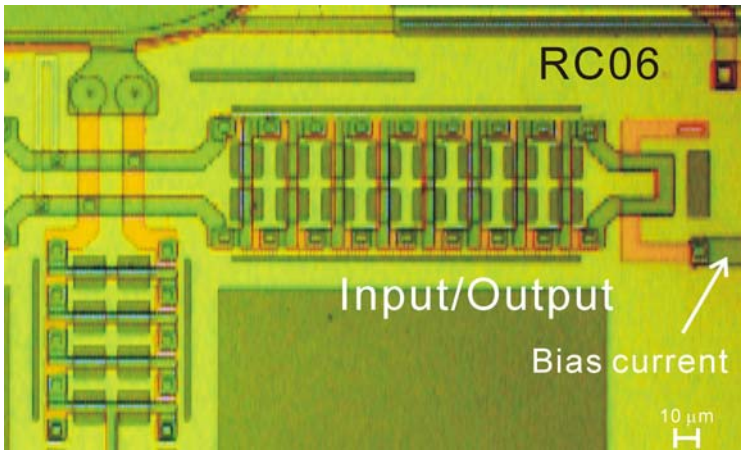


Figure 5.17. Illustration of mutual magnetic shield for our nSQUID circuits (c). Compared with conventional quantum computer circuit (a) and our first nSQUID circuits (b), four layer circuits (c) shows stronger magnetic shielding property.

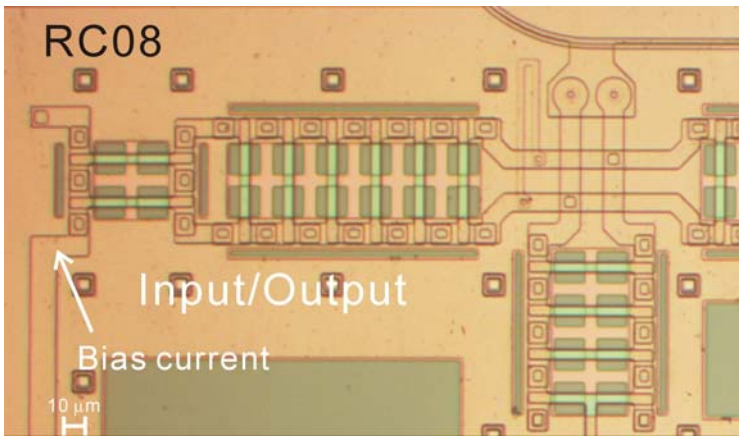
5.3.6. Input/Output Cell

Our general discussion of the vortex dynamics in the string of nSQUIDs is limited above to

regular, i.e., infinite long string. In the case of practical circuits, one needs to take into account that the string of nSQUIDs has finite length and it should be properly terminated. In order for the nSQUID string to act as a reversible computational device, the cells at the ends of the string should perform the functions of the data input/output, and in addition the data input/output these cells should not destroy the circuit's reversibility. A "geometric" aspect of this reversibility is that the direction of the data flow in the circuit should also be in principle easily reversible. It is appropriate then for the end cells to be able to perform both the input and the output functions (Figure 5.18).



(a)



(b)

Figure 5.18. Input/output for the nSQUID shift register in chip RC06 (a) and RC08 (b).

Input/output signal was applied to the shift register by the transformer as shown in Figure 5.18. In the later revision (Figure 5.18(b)), coupling of two inductors in the transformer was enhanced to reduce the bias current. Moreover, the value of the total of the input/output inductance was adjusted to make the differential flux of all nSQUIDs in the shift register more uniform. Simulations showed when the inductance of input/output cell is 1.5 times of the negative-coupled inductance between two nSQUIDs, the difference phases representing the signals become more identical along the nSQUID shift register.

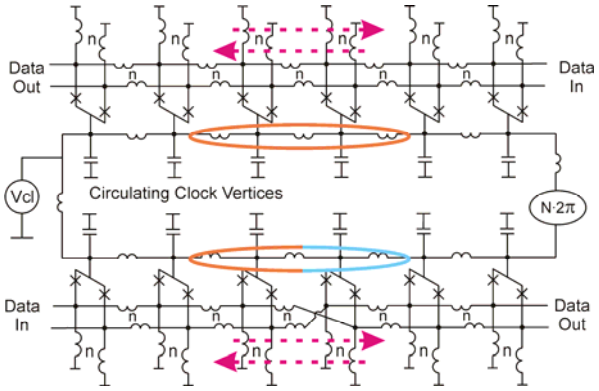
However, the ideal input/output should have the same time evolution pattern as how the signal looks like in each nSQUID along the shift register. The biggest challenge lies in the clock synchronization. Actually, we encounter the similar difficult for the readout cell. Later in Section 6.5, we will discuss possible design to implement the on-time input/output as well as signal measurement cell.

5.4. Main Measurement

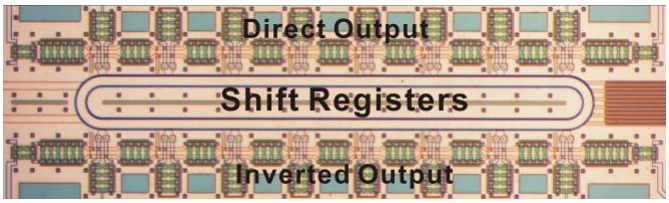
Full diagram of our setup for measuring the energy dissipation was shown in Figure 5.2. The data injection into the nSQUID strings is achieved by applying a differential dc magnetic bias created by the current *Iin* (Figure 5.10(a)). The nSQUID strings act as the shift register (Figure 5.1), i.e. the data are injected into the nSQUIDs at one end of the string, transported along it by the propagating vortex, and measured at its other end. As in Figure 5.19(a), a simple swapping of two wires inverts the sign of the transferred signal. Therefore, in chip RC08, we implemented a circular nSQUIDs circuit with one direct and one inverted output shift registers (Figure 5.19(b)).

Figure 5.20 shows typical measurement results which illustrate the digitization effect: at lower

analog input signal level, the output shows constant (digital) output corresponding to a negative differential state of the nSQUIDs (logical “0”), while at higher input signal, the differential state is positive (logical “1”). The overall process, viewed as “calculation”, is rather simple. It involves 3 primitive functions: writing bits of data into a shift register, propagating them by about 2 mm in distance, and reading them out. The novel feature of this calculation is extremely low energy dissipation, comparable to the basic thermodynamic scale of energy dissipation. In detail, Figure 5.20(a) shows the measurement result of chip RC07A (Figure 5.5), the circuit starts to operate at frequency 0.8 GHz, and it is fully operational up to 6.6 GHz. For the later revision of the circuit, the operation range of the circuit is improved to between 500 MHz to 7 GHz as illustrated in Figure 5.20(b).

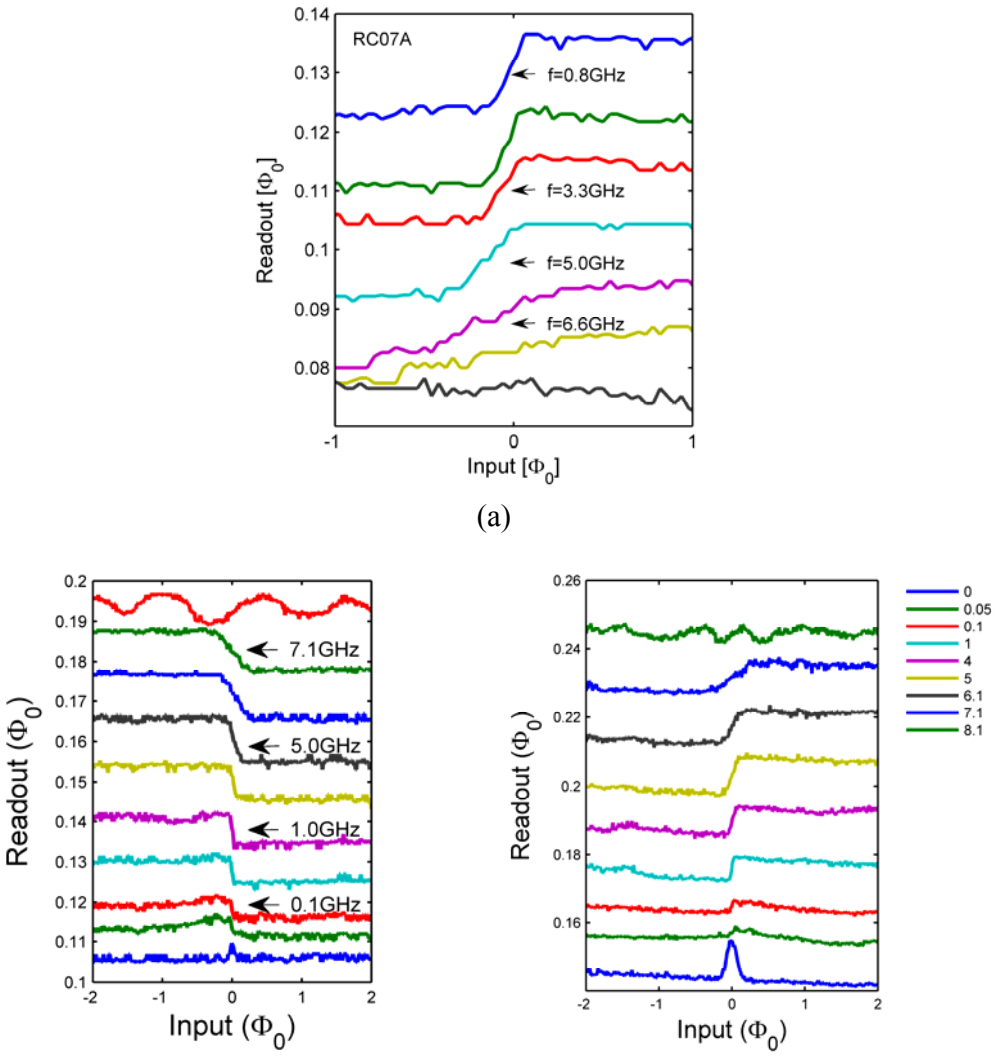


(a)



(b)

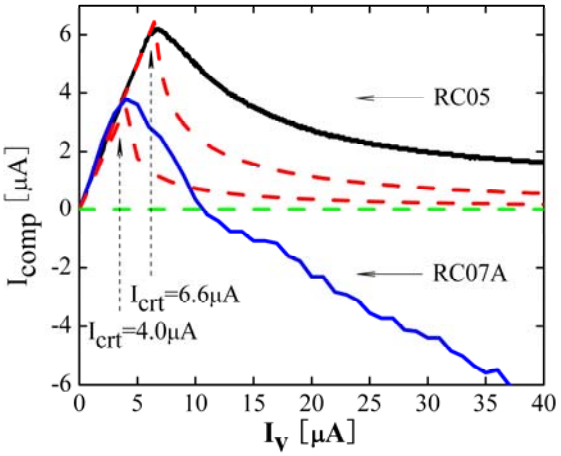
Figure 5.19. (a) Equivalent circuit, and (b) microphotograph of 2 shift registers with a common clock ring. Note that the lower register contains one inverting wire connection and therefore inverts the data. The length of one cell is 180 μm; the length of the ring is 1410 μm. Only 6 of 8 cells are shown in schematics (a).



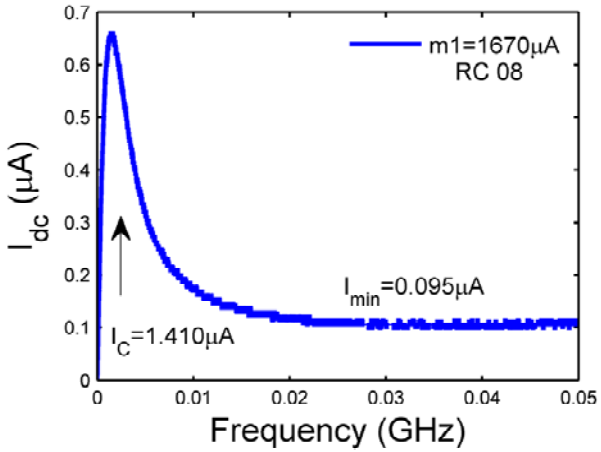
(a)

(b) (c)

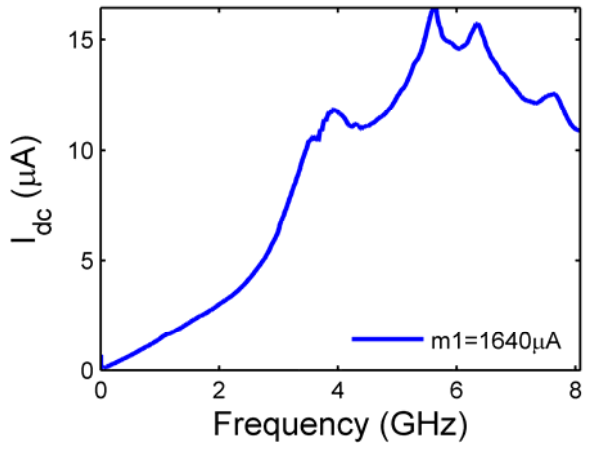
Figure 5.20. Digitization and propagation of the digitized data along the shift register. Analog input magnetic flux is created by current Iin, Digitized output is extracted at the other end of the register by the readout SQUID (for notations, see Figure 5.10a). (a) is the result from measurement of chip RC07A (wafer No. kl1107), and (b) and (c) are the result of direct and inverted shift register in chip RC08 (wafer No. kl1139).



(a)



(b)



(c)

Figure 5.21. Measured (solid lines) and estimated (dashed lines) energy dissipation in the nSQUID shift registers. The sample RC07 (wafer No. kl1107) is fabricated using 30A/cm^2 technology; RC05 (wafer No. kl1083) - with 1000A/cm^2 technology. For discussion, see text.

The measurement technique used to measure the energy dissipation in the shift registers was discussed above (see Figure 5.2 and related text). Figure 5.21 shows typical measured dependence of current I_{comp}, representing the dissipated energy, on the bias current I_v. Notice that when I_v is below the critical current of our circuit, all the bias current flows via the shift registers. However, once I_v crosses its critical value (4 and 6.6 μA for the two samples shown in Figure 5.21(a), and 1.41 μA for the sample shown in Figure 5.21(b)), current I_{dc} through the circuit as well as its corresponding I_{comp} decreases. In Figure 5.21(a), dashed lines illustrate this dependence using the simple model discussed earlier in Eq. (5.1). However, the fitting, especially for the sample RC07, is rather poor. The main reason for this is that the parasitic coupling between the bias current I_v and the measuring SQIF is too large in this sample. As a result, we can only roughly estimate the dissipated energy at that measurement.

With the improved design in the later revision (chip RC08), the energy dissipation can be measured accurately and the result is shown in Figure 5.21(b) and (c). The plot in Figure 5.21(c) shows variations of this current within the whole range of clock frequencies, while the plot in Figure 5.21(b) expands the range of frequencies when the bias current reaches its lowest values slightly below 0.1 μA. This is the current applied to two 8-stage shift registers or to 16 nSQUIDs. If we consider that each register is a logic gate consuming 0.05 μA of bias current then the energy dissipation is only 2.5 times higher than its thermodynamic threshold. But each nSQUID could be treated as a gate such that it consumes only 0.007 μA of current or dissipates less than one third of the threshold energy per logic operation. These figures here are close to our expectations for this particular circuit.

The major dissipation sources are the sub-gap resistances of the unshunted Josephson junctions in nSQUIDs and the resistors (74 Ohm) between two arms of nSQUID for damping purpose. Using the total critical current of junctions in one shift register (about 0.08 mA) and the sub-gap voltage (about 70 mV) reported by HYPRES the cumulative sub-gap resistance of the shift register is estimated to be about 875 Ohm. The current via this resistance is proportional to the applied voltage or equivalently the operation frequency given in Figure 5.20. This current in fact remains below the thermodynamic threshold current I_{th} in the whole frequency range of the normal operation of the shift registers in Figure 5.20. As to the differential resistors between two arms of nSQUID, we can reduce their energy dissipation by further increasing their value or removing them from cells where we do not need to readout the data.

As discussed in Section 5.3 in this chapter, another source of the energy dissipation is the "detection" of the Josephson oscillations in the resistor R_v in the voltage source. The estimation in Eq. (5.1) shows that the equivalent current measure I_f for this energy dissipation equals the threshold I_{th} at frequency f close to 0.2 GHz and it decreases as $1/f$ with increasing frequency. These estimations mean that within the whole range of frequencies where our circuit is operational it should have energy dissipation below the thermodynamic threshold.

5.5. Conclusion

In this chapter, we exam the test circuits containing two 8-stage shift registers, one with direct and the other with inverted outputs. The energy dissipation per nSQUID gate per bit for the later revision of the circuit measured at 4.2 K temperature is already below the thermodynamic threshold. We are confident that we passed through the critical phase of the project.

Chapter 6 Logical Reversible Gate

6.1. Introduction

In this chapter, we will discuss the construction of logic gates using the string of nSQUIDs based on our knowledge on shift registers and the new clock scheme using LJJ studied in the previous chapters (Chapter 4 and Chapter 5). The discussion in this chapter is primarily based on the published paper [27] and unpublished data [24]. Before we start, we should discuss the details of the physical connections between LJJs and nSQUID strings. First, let us note that such connections should provide seamless passing of Josephson vortices. In other words, the circuit parameters should be optimized to provide equal energy and repulsive forces for Josephson and "colored" vortices. Second, as we discussed in Chapter 3, colored vortices, which carry data on their back, have another degree of freedom. Crossing the border between LJJ and nSQUID string has a strong impact on this degree. This impact could be described as a transition from a single-minimum (dash lines in Figure 6.1) to a double-minimum (bi-stable) (solid lines) energy profile. Un-tilted (symmetric) energy profile (Figure 6.1(a)) can be thought of a random number generator. And this LJJ-nSQUID string-LJJ connection could be a reversible operation because it has a trivial complementary operation: an erasure of a random number. The simplest cases for theoretical analysis are those of tilted energy profiles (Figure 6.1(b)-(d)). Note that the energy profile evolution naturally moves the system into a state corresponding to the deeper energy minimum of the double-minima. The right half of Figure 6.1(b) and (c) shows that the data could

be reversibly erased using properly tilted complementary transitions from the nSQUID string to LJJ. Such pairs of logically reversible operations have simple physical explanations: Resting dc magnets induce proper magnetizations of moving magnetic domains. Of course some energy should be dissipated to move the magnetized domains away from the magnets. But this energy is return to the system when the domain approaches to the other dc magnet and then disappears. Figure 6.1(d) shows highly undesirable case of irreversible operations when the sign of the erasing magnet is not consistent with the data.

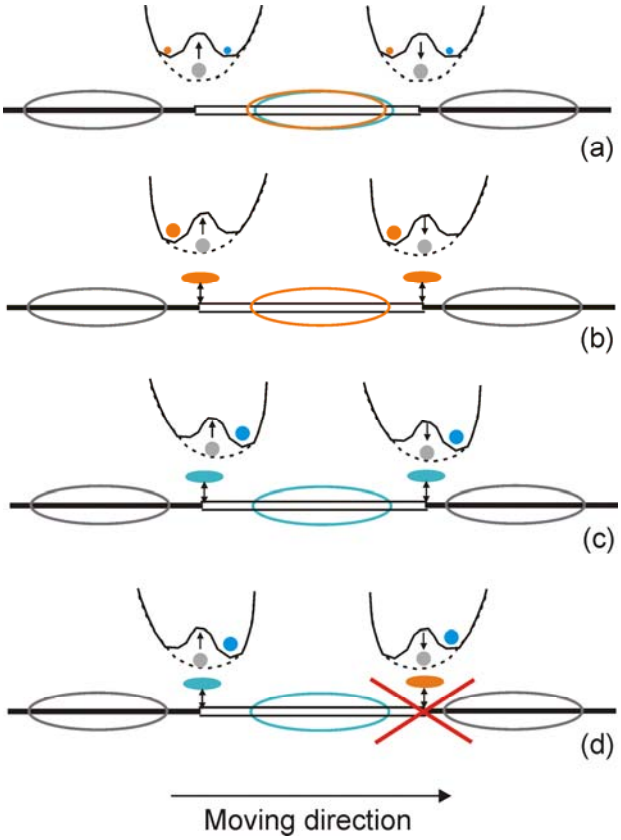


Figure 6.1. The entrance/exit of Josephson vortex into/from the nSQUID string corresponds to writing/deleting of binary information. (a) Transition of the long JJ mono-stable energy profile into a non-tilted bi-stable nSQUID profile leads to a random selection of one of two minima or writing a random bit. Transitions to the properly tilted bi-stable profiles lead to writing binary "0" (b) and "1" (c). (See text for details, after [24].)

It is important to note that the reversible operation should be a continuous and "slow" transition and several corresponding matching conditions should be maintained between Josephson junctions and nSQUIDs. First, all clock inductances should be equally valued. Second, the sum of two critical currents of nSQUID junctions should be equal to critical currents of one dot junction in the LJJs. In the third place, the inductor in series with JJ in LJJ should have the same value as the inductance of "common" mode in nSQUID. Besides, to make the transition "slow", it is better to have several nSQUIDs with inductance of "differential" mode increasing slowly to the desired value for the function gates.

6.2. Magnetic Coupling between nSQUIDs in Different Strings

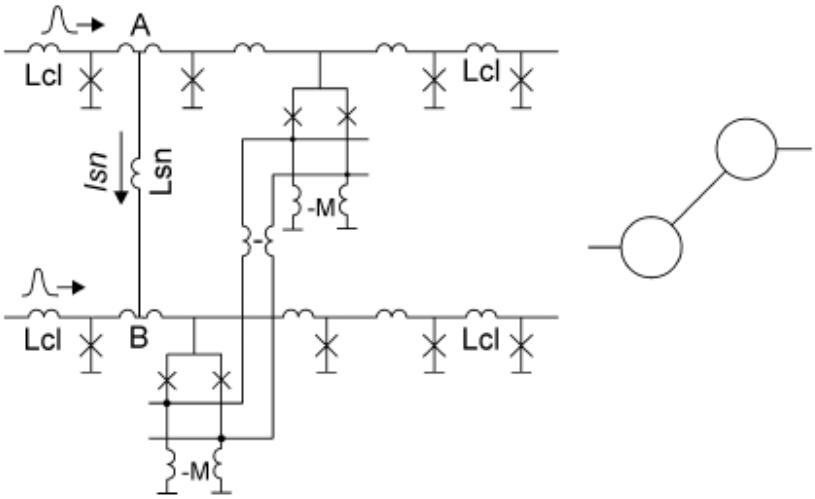


Figure 6.2. Transferring data between clock lines (schematics and notation, after [24]).

Next level of complexity lies in circuits with two clock lines (Figure 6.2) where synchronization of the propagation of clock vortices via the upper and lower clock lines has to be properly treated. One approach to solve this kind of synchronization issue is well known. As shown in Figure 6.2, the approach is that points A and B in the circuit need to be synchronized

by a superconductor inductor. Current *Isn* via inductor Lsn is proportional to the difference in fluxes flowing through points A and B: Current *Isn* produces Lorentz forces that slow down the vortex in one clock line and accelerate the vortex in the other line. Generally this mechanism is similar to Phase Lock Loop (PLL) mechanism [65] but, as we see, in superconductivity it can even work on dc current.

In Chapter 4 and Chapter 5, we have already shown that NOT gate does not contain any junctions and random bit generator could be treated as a primitive cell. Figure 6.3 illustrates how to copy bit A. The device consists of a longer (upper) and shorter (lower) string of nSQUIDs. A string of nSQUIDs is represented by a pair of lines in the figure. As we discussed earlier, at the entrance into the nSQUID string Josephson vortex should select a sign for its magnetic domain. Two nSQUIDs in upper and lower strings are magnetically coupled as it is indicated by the arrow shown on the left side of Figure 6.2. The upper nSQUID thus serves as a tilting magnet for the lower nSQUID that stimulates the selection of the "correct" sign. Correct operation of this device is possible only at mutually synchronized propagation of vortices in the strings. The slight deviation of the direction of the arrows (in Figure 6.3) away from the vertical (90 degree angle) direction indicates that the strongest tilting should be applied at the very beginning of the development of bi-stable energy profile to achieve optimum operation conditions. These condition are realized when the strongest central part of the upper vortex interacts with the front of the lower vortex. The right side of Figure 6.3 shows the complementary operation of reversible erasure of B. Note that this part of the circuit is symmetric and the description of the circuit would be practically unchanged if vortices would propagate from right to the left rather

than from left to the right.

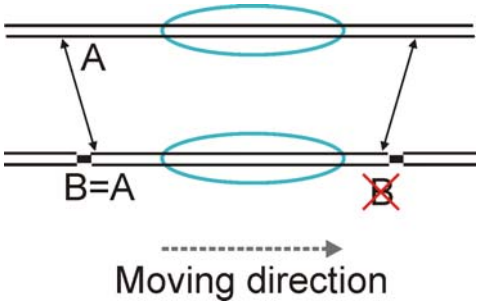


Figure 6.3. Copying and reversible erasure of information.

6.3. More Robust Gates

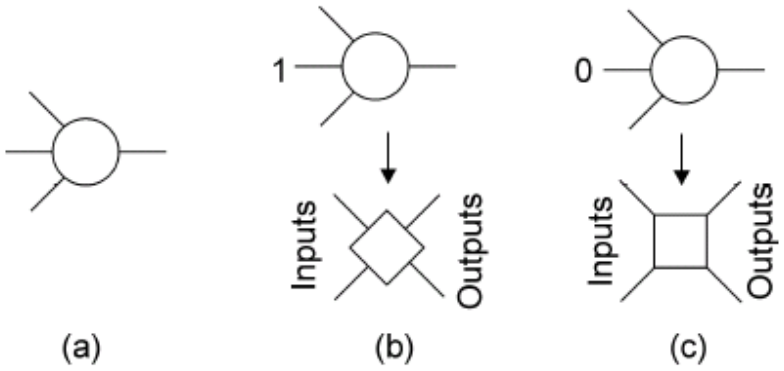


Figure 6.4. (a) Three-input majority gate; (b) and (c) 2-input OR and AND gates respectively derived from majority gate by applying permanent logic "1" and "0" to one of its inputs. Two output lines in (b) and (c) are shown to emphasize that irreversibility of OR and AND is achieved if they have an odd number of outputs (after [24]).

Gates with odd fan-in are more robust against irreversibility issues discussed in the previous paragraph. This is because odd number of signal inputs with same intensities but different signs cannot compensate each other. The basic 3-input gate (Figure 6.4(a)) executes majority function of 3 input signals with equal intensities. One of its inputs can be constantly loaded with a permanent source of positive or negative magnetic bias imitating input data. If the source is

positive it imitates logic “1” and the cell performs logic OR operation on the two remaining input signal ports (Figure 6.4(b)). Similarly, if one of inputs receives permanent logic “0” then the gate performs logic AND operation on the two other inputs.

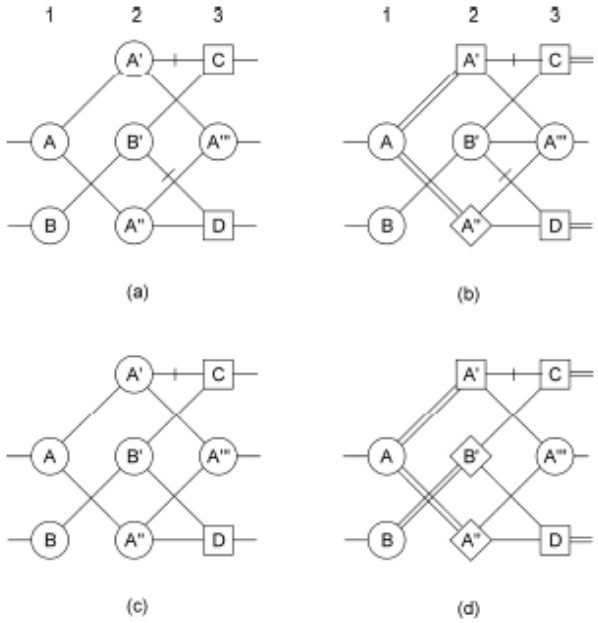


Figure 6.5. (a) & (c) Irreversible and (b) & (d) reversible implementations of K- (a) & (b) and K+ (c) & (d) cells (after [24]).

Various logic gates can be constructed using primitive cells shown in Figure 6.4. Two such cells can be used as parts of XOR gate. K-cell returns A at one of its outputs and performs two calculations:

$$C = \overline{A} \times B,\ D = A \times \overline{B}. \tag{6.1}$$

Its trivial (irreversible and redundant) implementation is shown in Figure 6.5(a). This implementation calculates variable C and D only in the third column, while the first column contains only input buffers and the second column makes two copies of input A: $A' = A$ and $A'' = A$.

Note that the logical reversibility is the mandatory requirement of the physical reversibility. In plain words, the reversibility means that input data could be reconstructed from the output results. It is straightforward to see that some of operations in our cell in Figure 6.5 are logically reversible. For example in Figure 6.5(b) A' could be restored from A''' and $\overline{C}$. It could be done, for example, if $A' = A''' + \overline{C} = A \cdot \left(A + \overline{B} \right) = A.$ This two-input operation is OR function and thus its execution requires an OR gate (Figure 6.4(b)). However, as we mentioned earlier the OR gate contains a dc magnet imitating effect of logical "1" on one input. This magnet can completely compensate one input signal and, as a result, OR gate cannot perform function *A'= A*. This is because OR gate should have two inputs with only one input *A'*. However, in our case two identical input signals are created by coping them from the same source. This fact is emphasized by drawing two lines connecting *A* and *A'* in Figure 6.5(b). Of course a real implementation would contain only one coupling component. But the correct operation is performed only if the strength of this coupling is two times higher than those for regular couplings. Other revisions in Figure 6.5(b) in comparison with Figure 6.5(a) have the same reasoning. For example, two-output AND gates (C and D) must have two outputs or one output with double strength (shown by dual lines) which is simply because AND should have two inputs and two output ports. Physically it means that in reversible logical gates neighbor cells help each other to build up magnetic domains. In other words, there are positive feedbacks between neighbor cells that dramatically reduce the probability of thermally induced errors.

Figure 6.5(c) and (d) show irreversible and reversible implementations of a K+ gate that returns A and calculates two functions:

$$C = \overline{A} \cdot B,\ D = A \cdot B. \tag{6.2}$$

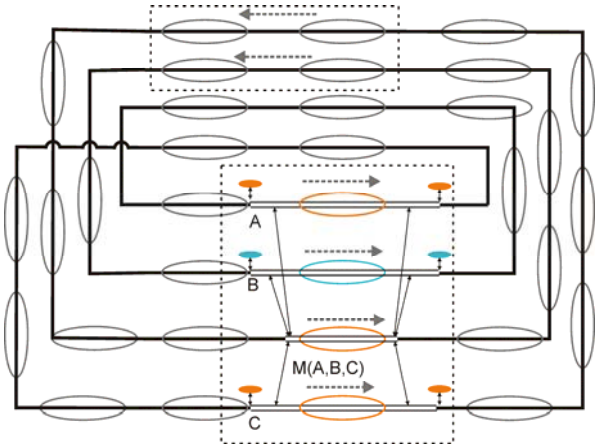
This gate is similar to K- gate and thus similar interpretation of how this gates works as K- gate applies here.

One of the challenging parts of the nSQUID design is the wiring. The currently available HYPRES fabrication process offers 4 superconductor wiring levels. However, we found that circuits operate much better if 2 of these layers (the lower and the upper) are used to build a superconductor shielding box and therefore can not be involved into the wiring. As a result, only two wiring levels are left which may only be sufficient for simple crossings of wires but can be insufficient for space-saving wiring solutions. It is anticipated that one extra wiring level would make a big difference while two extra levels would resolve all knowing wiring difficulties. We expect that the required extra wiring levels will be available in a foreseeable future as a result of natural progress of the fabrication technology.

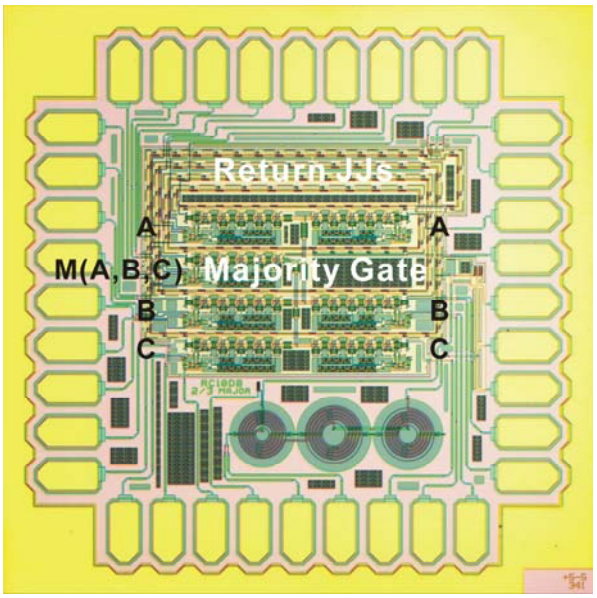
6.4. “Global” Synchronization of Gates

Figure 6.6 shows a structure of an integrated superconducting circuit that has been designed and fabricated. Its main part is a closed loop built upon LJJs and nSQUID strings. The loop is packed with Josephson and “colored” vortices that move along the loop with a constant speed. The movement is supported by a small uniformly distributed bias current (not shown in the Figure). The vortices are packed very densely and strong repulsive forces keep them equally distanced. Now we should recall that the vortices are “identical” quasi-particles and as a result, the shift of all vortices on one position returns the whole system into a very similar state and this means that the loop with vortices could serve as a global clock capable of operating without

clock skew.



(a)



(b)

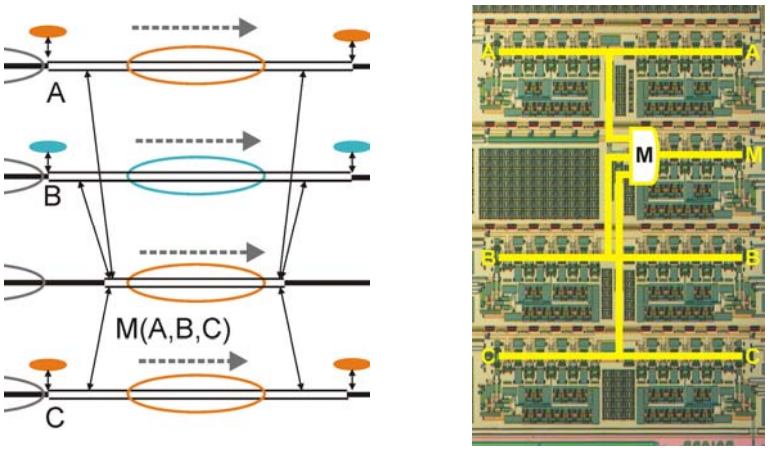
Figure 6.6. (a) Structure and timing of a reversible circuit. LJJs are shown in solid black lines, while nSQUID strings are shown in dual lines. Plain Josephson vortices are shows as gray ellipses, while those with magnetic domains are marked as pink (logic "0") and light blue (logic "1") ellipses. All vertices move along the closed loop (the timing belt) with constant speed. Strong repulsion between vertices keeps them equally distanced from each other. (b) Micrographic photo of fabricated circuit in (a). It is a 5 mm × 5 mm chip fabricated at HYPRES with critical density of 1 kA/cm^2.

Figure 6.6(b) shows a microscopic photo of the fabricated circuit. This circuit contains one 2/3 majority gate M and one gate that reversibly erases the result of majority operation. In addition,

it contains 3 cells that write input operands A, B and C as well as 3 reciprocal erasure cells that delete input data. All together this set contains 8 primary logic gates. As we mentioned in Section 3.6 of Chapter 3 we assigned about 8 nSQUIDs (16 Josephson junctions) per vortex period. The copying of data (see discussion of Figure 6.3) requires (or occupies) only a small fraction of the vortex period. This conclusion can be generalized to other operations as well. In physical terms the operation corresponds to applying strongest possible signal from one magnetic domain to the leading edge (or the growing point) of the other domain. Practically the center and the leading edge of the domain are separated about one quarter of the vortex period. In future we can add another quarter of period to provide a better isolation (spacing) between different logic operations to make up one half of the vortex period, which is a safe estimation for the geometrical length of any primary operation. The number of JJs per operation can be estimated as followings: 4 rows give us 64 JJs with 8 JJs per vortex period. Each string is involved into 2 to 4 logic operations and on average it corresponds to 3 operations per string. With one half of period per operation we have about 96 JJs per 8 operations or about 12 JJs per operation.

In the circuit shown in Figure 6.6(b), return path is composed of discrete JJs with critical current equal to that of nSQUID in logical gate. These JJs and nSQUIDs are basic cells in this circuit. There are totally 136 such basic cells with critical current as 25 μA. For each nSQUID, we maintain the l_+ and l_- the same as those in the chip RC08 (Figure 5.5(d)). The clock line inductance has been increased (4.44 pH) for the crossings of wires as shown in the figure. 17 vortices will be injected into the loop to maintain the desired requirement of 8 cells per vortex. As shown in Figure 6.7(a) and (b), the number of return JJs between two strings of nSQUIDs

was chosen carefully to keep the clock synthesized in data lines A, B and C but to make the clock in majority output line (M) one cell delayed compared to the above three data lines . This design helps the transmission of data through longer magnetic coupling inductance.



(a) (b)

Figure 6.7. Enlarged view of the logic block in Figure 6.6.

Figure 6.8 shows our proposed next prospective circuit that could be completely treated as a digital reversible integrated circuit. This circuit again looks like a timing belt but with the 13 junctions replaced by nSQUIDs. Positively and negatively magnetically shifted nSQUIDs performing OR and AND functions are shown as diamonds and squares respectively, while unbiased nSQUIDs used in the shift registers are shown as circles. Single and double lines indicate a weaker and two-time stronger data coupling between the gates. Crossed data lines mark the NOT function that is implemented by twisting straight signal wires shown in Figure 5.19(a). The operation E = XOR(A, B) is calculated in 3 steps: C = (NOT(A) AND B), D = (A AND NOT(B)), and E = (C OR D). The rest of the gates perform buffer functions and under certain circumstances could be omitted. “Timing belt” connections inside the XOR gate are

shown as wide grey lines. Ellipses are symbolic notations for timing vortices travelling along the belt.

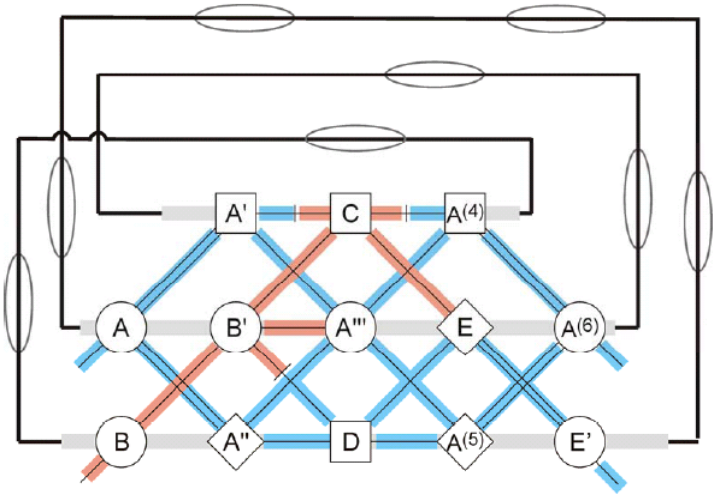


Figure 6.8. Structure and timing of a test circuit with the reversible XOR gate. LJJs clock lines are shown by solid black lines with gray ellipses showing moving Josephson vortices. Clock lines in nSQUID grid are shown in light grey, while nSQUID data paths are shown as pink – for logic "0" or blue – for logic "1". The data distribution shown here corresponds to input A = "1" and input B = "0". All vortices move along the closed loop (the timing belt) with constant speed. Strong repulsion between vortices keeps them equally distanced from each other.

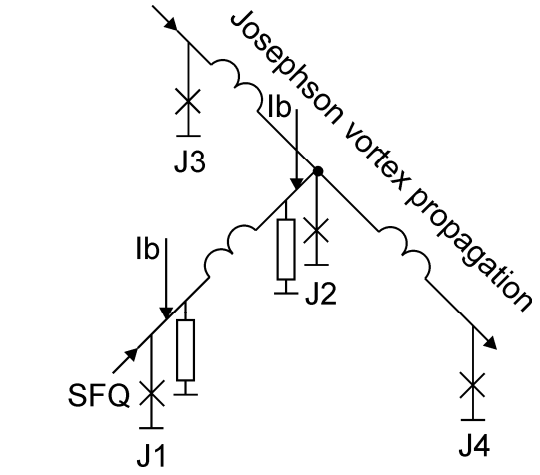
Most of the mentioned components above have already been tested with success and thus we do not expect major problems from these individual components. Here we would like to highlight the main advantage of the new timing scheme in comparison, for example, with multi-phase AC bias. AC microwaves unavoidably are attenuated and distorted while they are propagating along the chip. Moreover, attenuation and distortion could be data-pattern dependent. In contrast, the vortex timing belt is fundamentally accurate. It can be stopped and run again, and its states before and after a rotation by any integer number of vortex periods are fundamentally indistinguishable. In other senses, this is a rare example of a timing scheme potentially free of clock skews. As mentioned earlier the speed of the vortices in ring LJJs could be extremely

stable [48].

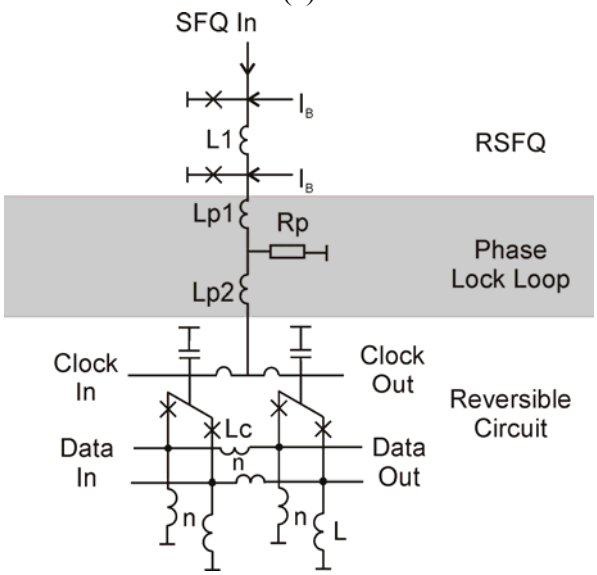
Finally, we would like to note that some reversible erasure of information could be eliminated from practical algorithms if space or hardware saving is more important than the reduction of energy dissipation. Note that we push toward fully reversible computation to reach more than 1,000,000 reduction in the energy dissipation against the best semiconductor technology. We can easily sacrifice some reversible features if less reduction in energy dissipation is still satisfactory. Moreover we can bear with the hybrid integration between conventional RSFQ logic and new nSQUID based gates.

6.5. Interface between RSFQ and nSQUID circuits

It is important to realize that there is no major obstacle in interfacing between RSFQ and nSQUID circuits. The only issue is that a typical, say, 50 μA bias current for an RSFQ circuit is more than thousand time larger than the already achieved bias current per a vortex in nSQUID circuits. Figure 6.9(a) shows a RSFQ turnstile for Josephson vortices. SFQ arm of the turnstile uses Josephson junctions with larger critical currents. These junctions are intentionally shunted to prevent a ballistic propagation of the vortices. And, as we just mentioned a relatively large bias current should be applied to compensate a strong vicious friction. Operation of the circuit is simple. Weak vortices travelling along the LJJ cannot pass the intentionally shunted junction J2. Each vortex injected via SFQ input performs two functions: it kills one vortex stopped by junction J2 and injects a new vortex into the LJJ. For any observer these two events correspond to a controlled passing of the stopped vortex via the turnstile.

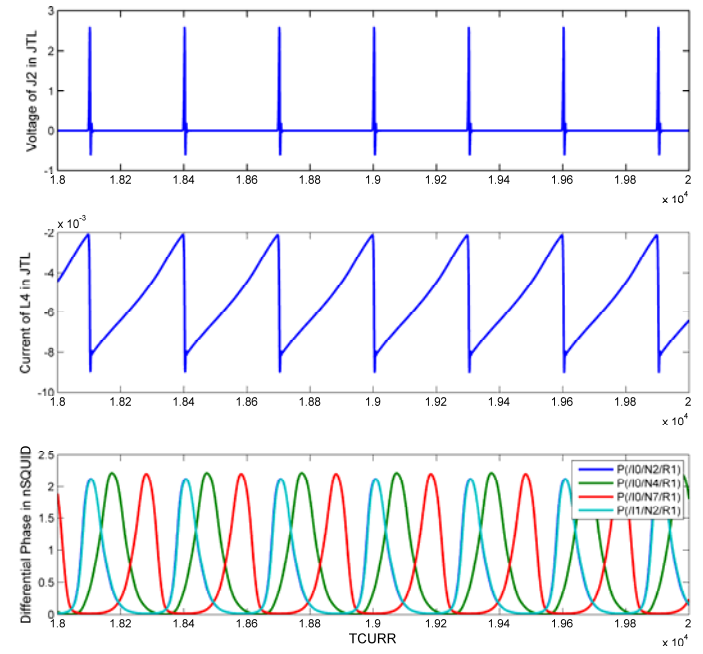


(a)

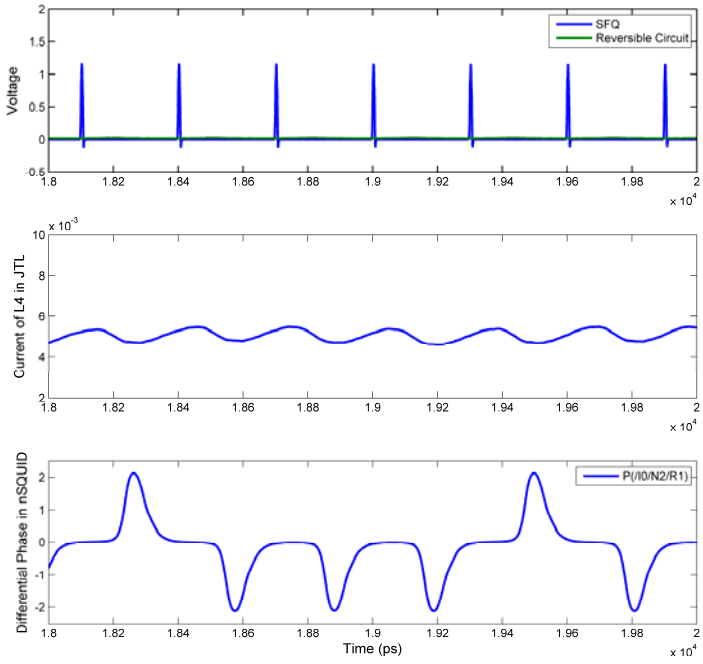


(b)

Figure 6.9. SFQ turnstile for (a) a discrete long Josephson junction and for (b) an nSQUIDs string.



(a)



(b)

Figure 6.10. (a) Simulation result when L4 in JTL is 2.64 nH, Ic of JJs in JTL is 87.5 μA, bias current is 87.5 μA, and the rest inductances in JTL are all 13.2 pH. Period of pulse input is 300 in arbitrary unit. x-axis "TCURR" is time in arbitrary unit. All phase is in unit of $\Phi_0/2\pi$. (b) Simulation of similar circuits to (a) but only grounding the inductance (Lp2 = 2.64 nH) by a resistor (Rp = 0.24 Ohm). The AC component of the total current of nSQUIDS ring is strongly suppressed as we expected.

Similar SFQ turnstile can be implemented with nSQUIDs string as shown in Figure 6.9(b). In this circuit, JTL, which replaces the DC voltage source made of small resistor in our previous designs discussed in Chapter 4 and Chapter 5, is placed to inject vortex into the ring nSQUIDs for the synchronization of clock in the ring. The advantage of this scheme is that it makes possible the synchronization of the readout of data transferred in the nSQUIDs ring with the clock.

In the simulation, the JJs ring contains 16 nSQUIDs with $2\Phi_0$ phase drop along the clock line. The JTL contains two JJs biased by a phase source and a DC bias current. Simulations from the first iteration give the following result shown in Figure 6.10. As in Figure 6.10(a), the period of data translation inside the ring is around 300 ps. The bottom subplot shows how signal is propagating along the string. The large inductance between JTL and nSQUID ring balances the bias current coming from bias of JTL and the energy dissipation of nSQUIDs ring. The current of the ring is AC current with reasonable low amplitude. AC current corresponds to extra energy dissipation. The sharp drops of the current correspond to moment when the pulse is injected into the nSQUIDs. Since the JJs in JTL is shunted with relative large resistor (βc is a little bit smaller than 1), the switching time is in pico-second range, which is too fast. So we can ground the large inductance by a resistor, which effectively behaves as extra shunt for the JJs. The resistor together with the inductor is a low path filter as a phase lock loop. The simulation result in Figure 6.10(b) shows that the signals keep propagating along the nSQUIDs string while the AC current of the circuit is suppressed approximately by a factor of 6. Note in this simulation, input signal to the first nSQUID has a random sign, which results in the positive and negative

propagation signal as shown in the Figure 6.10.

6.6. Conclusion and Discussion

In this chapter we have discussed more complex logical gates based on the shift register and timing belt we introduced in last two chapters. We show the successful construction of all the basic cells needed for any logical gate in a reversible mode. Especially, we demonstrate that an XOR gate containing only 13 nSQUIDs can be treated as a digital reversible integrated circuit. Finally we show that RSFQ circuit and the reversible circuit can be connected and integrated together seamlessly and that the RSFQ circuit is capable to serve as a new control circuit of clock vortices for the reversible circuit.

Let us return to the timing belt approach and discuss possible complications. The first potential complication is coming from design and fabrication imperfections. We have assumed that the timing loop is electrically uniform and the train of vortices moves freely. But the belt layout contains, for example, corners and especially self-crossings that could be implemented without disrupting the uniform requirement only if the wires of the crossing long JJs are fabricated in different superconductor layers. Our task has to take all non-uniformities into account when designing electrically uniform LJJs and nSQUID strings. The second issue is the excitation of unwanted vibration or phonon modes in the dense vortex grid used as the timing belt. Much stronger vibrations could be caused by interactions of vortices with energy bumps and holes. Fortunately, it is possible to actively synchronize the propagation of vortices by means of their intentional magnetic coupling as shown with an inductor Lsn in Figure 6.2. We anticipate that at a sufficiently strong coupling the vortices in different rows will move synchronously.

Chapter 7 Relation between Reversible nSQUID and Multi-qubit Circuits

7.1. Advantages of nSQUIDs in Quantum Computing

Besides the main goal of our nSQUID effort: to demonstrate reversible medium-scale computation in a classical regime, we also suggest it as an alternative approach to quantum computation (QC) with superconducting qubits. Results of this approach, which come from joint projects with Prof. Dmitri Averin in SUNY at Stony Brook and Dr. Stefano Poletto in Karlsruhe Institute of Technology, will be discussed in this chapter. This section is based on the published paper [39].

The major advantages of the nSQUID circuits in the QC context originate from the two circumstances. First, these circuits do not require controllable keys to switch on and off the interaction between the qubits. Such keys are critically important for other types of superconducting qubits in order to organize them into larger QC structures. Secondly, the quantum (qubits) and classical (support) parts of the nSQUID circuits can be naturally integrated into uniform structures that are actually scalable. Based on these points, we are confident that the nSQUID approach will overcome the initial skepticism and will be proven to be very useful for the further development of superconducting quantum circuits. In particular, as shown in this thesis, the nSQUID circuits can be used as the natural basis for implementation of the universal adiabatic quantum computation (UAQC). In this approach, the computations are performed within the ground state of the circuit Hamiltonian, while the energy gap between the ground and

excited states of the Hamiltonian can provide some degree of protection against decoherence.

There are several weaknesses of the ongoing QC projects. Currently QC circuits are associated with one or at maximum two passively coupled SQUIDs. In the past this coupling was via magnetic or capacitive coupling. Now researchers lean towards a resonant coupling, and main efforts are directed towards achieving long decoherence time. We think that the investigated QC circuits might be still too simple and the main research direction might not be as wide.

In fact, the absolute decoherence time means little if the temporal duration of logic operation can be varied. In other words, a more accurate parameter should be defined as how many logic operation could be executed for one decoherence time. Quantum operation with short duration will eliminate the requirement of long decoherence time.

The other important question involving QC is what will be the next step after the decoherence time can be extended onto a very long time scale, e.g., infinite. It would be natural to try to answer this kind of questions using the same Josephson junction technology and to try to search for other QC devices more complex than a SQUID.

Our nSQUID circuits can solve both mentioned tasks: we have suggested how to build complex quantum gates and as one of byproducts we have estimated and optimized the duration of quantum operations that could be as short as few hundred picoseconds. As a result we can conclude that the already demonstrated tens or hundreds nanoseconds decoherence time here would be sufficient for multi-qubit experiments.

These are also two more advantages in our approach, or more specifically in our fabrication choice. The fabrication line in HYPRES runs a compatible niobium process. Compared with the

most common “aluminum” process, it does allow the fabrication of multi-layer circuits. In addition, it allows hundreds thermo-cycles and a room temperature storage over one year period, which are not possible for “aluminum” circuits. As a result, much more complex circuits are enabled by the niobium process we use.

While other QC groups seem reluctant in pushing engineering activity to facilitate complex circuits, we have developed specific CAD tools and engineering techniques to design and to fabricate complex circuits with, say, more than hundred Josephson junctions. As a result, we think we have a unique competitive advantage.

Earlier our group introduced the “Flying Qubit Logic” (FQL) [40] that could be built using the nSQUID arrays. It has an important and probably unique advantage among the solid-state quits: the possibility to transfer quantum data along the circuit and, in this way, to bypass the problem of controllable keys. This feature is significant, since it addresses one of the main difficulties faced by the gate-model quantum computation: the need of precisely timing between the qubit-qubit interactions. Indeed, any two-qubit quantum logic operation can be viewed as a controlled rotation in the appropriate part of the Hilbert space. The rotation angle depends on the relevant interaction energy E of the two qubits and the time duration Δt of the operation:

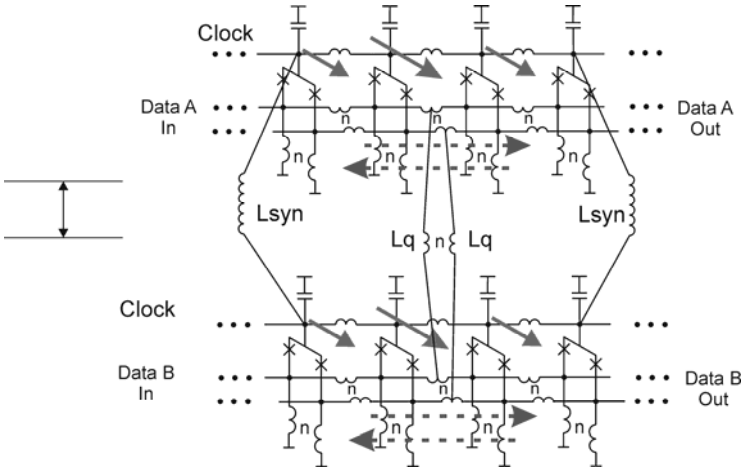
$$\vartheta = (2/\hbar) \cdot E \cdot \Delta t. \tag{7.1}$$

The main example of this is the controlled-NOT gate, which implements the rotation by $\vartheta = 180$ degrees, i.e. inversion of the state of the target qubit in the computational basis. To implement this rotation, one needs to switch the interaction on for precisely defined time interval such that

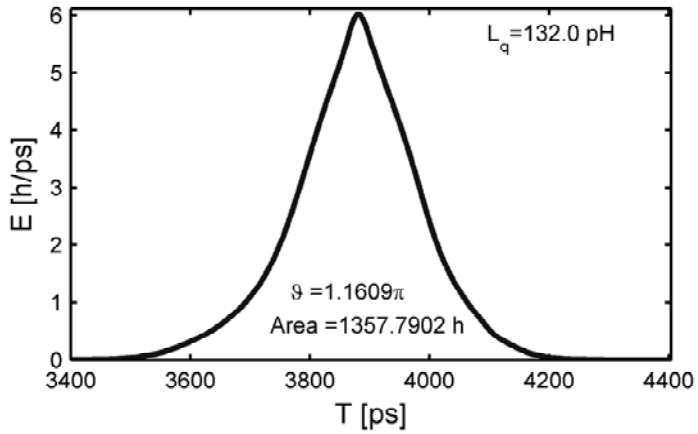
$$E \cdot \Delta t = h/4. \tag{7.2}$$

This equation gives the relation between the coupling energy and the time necessary to complete the quantum rotation. It illustrates the requirement of precise time-control of the qubit-qubit interaction that exists in the gate-model quantum computations. From practical perspective, the problem associated with the development of controllable keys capable of switching the interaction on and off with the required accuracy is no less difficult that the much more extensively discussed problem of making the qubit decoherence sufficiently weak.

The nSQUID circuits bypass this requirement of precise time control for the interaction by effectively replacing time evolution of the qubit states with propagation along the circuit. In the nSQUID arrays, the interaction of qubits necessary for the rotation and the resulting logic operation is provided by coupling of the two strings of nSQUIDs, e.g, as shown in Figure 7.1. Interaction energy E is estimated as $(\Phi_1 - \Phi_2)^2 / Lq$, where Φ_1 and Φ_2 are the differential fluxes in the first and the second nSQUID strings, which have rather limited ranges, say, from $0.1\Phi_0$ to $0.001\Phi_0$, while any desirable value of Lq can be implemented rather easily. Time of interaction T is inversely proportional to the speed of moving qubits. Of course, the realistic time dependence of the interaction will not have the rectangular profile, but it still can be presented as a pulse (Figure 7.1(b)), with only the total integral of this pulse over time relevant for the magnitude of the state rotation. The controlled-NOT gate used as an example above would require one nSQUID string to affect the junction critical current and therefore the tunnel splitting in the other nSQUID string through the coupling inductance.



(a)



(b)

Figure 7.1. A two-input quantum logic gate. (a) equivalent circuit and notation, (b) dependence of the interaction energy of the two moving qubits on time.

As usual, the controlled-NOT gate discussed above, combined with the similarly implemented rotations of individual qubits, is in principle all that is needed to build an arbitrary complex multi-qubit circuit of nSQUIDs. Figure 7.2 shows the sketch of the general structure of such a circuit, where the strings of nSQUIDs are shown by solid lines and the two-input gates are shown by the double-sided arrows. As with other type of qubits, this structure is also convenient for a simple set of initial experiments. Its main new feature would be the ability to "adjust" the

interaction parameters by changing the speed of flying qubits, e.g. by changing the voltage bias of the clock lines.

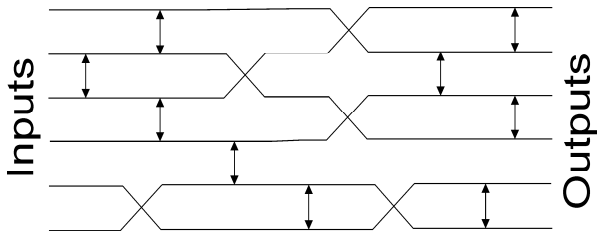


Figure 7.2. General structure of nSQUID network operating in quantum mode. Arrows represent gates shown in Figure 7.1.

The quantum operation of the nSQUID arrays described above assumes that the two modes of the nSQUIDs, “internal” differential mode and “external” common mode, exhibit different types of the dynamics. The differential mode which encodes the digital data is quantum coherent, and therefore, each internal state of the fluxon in the nSQUID string carries one qubit of quantum information. By contrast, the dynamics of the collective mode which is employed to transfer the fluxons along the array is classical, i.e. each fluxon is in definite position in the array and is driven along it by the voltage applied to the clock line. In principle, similarly to the fluxons in long Josephson junctions [67], the junction parameters for the nSQUIDs (most importantly, the area) can be chosen in such a way - see, e.g., [53], that the fluxons in nSQUID array propagate ballistically, and this ballistic propagation can be quantum coherent if the decoherence is sufficiently weak. An important feature of this regime is that the arrangement of several parallel nSQUID arrays with the structure of the type shown in Figure 7.2, realizes the general scheme of universal adiabatic quantum computation (UAQC).

UAQC [68], [69] is the approach to quantum computation which is equivalent to the more

standard gate-model quantum computation. Both historically and logically this scheme of quantum computation is closest to thermodynamically reversible classical algorithms. Its overall structure includes computational qubits and the clock register, and is represented by the "Feynman Hamiltonian" [70], [71]:

$$H = -\sum_{l} [U_l \otimes |l+1\rangle\langle l| + U_l^{+} \otimes |l\rangle\langle l+1|]. \tag{7.3}$$

Here U_l is the unitary transformation performed on the computational qubits at the *l*th step of the computation, and $|l\rangle$ are the states of the "clock" register, in which the qubits encode the transformation number *l* and therefore keep track of the ordering of U_l. In the nSQUID arrays, the role of the clock register is played by the common modes of the nSQUIDs in all strings of the array, while the computational qubits are represented by the fluxon differential modes.

When the common mode dynamics of the nSQUID is classical, i.e. when the circuit either realizes the classical reversible computation or FQL, the main purpose of the common modes of the nSQUIDs is to synchronize the fluxon dynamics in different strings (by appropriate inductive coupling between the strings) as needed for the operation of the different logic elements in the nSQUID structure in Figure 7.2. For all the couplings shown in Figure 7.2 to perform logic functions as described at the beginning of this Section, the fluxons in the two coupled lines should be traversing the interaction region during at the same time. This condition is satisfied most straightforwardly, if the fluxons in all nSQUID strings propagate together, as a common information-carrying wave. This type of the synchronized fluxon dynamics is needed regardless of whether the information is represented in this wave by classical or quantum–coherent states of the differential nSQUID modes, demonstrating deep similarity between the information

propagation patterns in the classical and quantum reversible computations.

In the UAQC regime, when the common mode dynamics is also quantum, it acquires additional purpose besides synchronization of the information propagation through the circuit. It ensures that while the wavefunction of the computational qubits encoded by the differential modes of the nSQUIDs within the propagating fluxons represents some meaningful computation, the overall state of the fluxons remains the ground state of the nSQUID array (Figure 7.2) as a quantum system. The main advantage of performing quantum computation in this way is the added degree of protection against decoherence offered by the energy gap Δ separating the ground from excited states of the array. At the minimum, such a gap makes it possible to meaningfully operate the circuit for a time scale much longer that the coherence time of individual qubits . An open problem of this approach is the fact that the energy gap Δ typically decreases rapidly with the size of the quantum algorithm. As one can see explicitly for the nSQUID realization of the UAQC approach, the gap Δ is produced physically by the quantization of ballistic motion of a massive object, synchronized wave of fluxons in coupled nSQUID strings which are moving ballistically along the array. It is obviously quite a challenging task to make the size-quantization gap associated with this motion sufficiently large. Still, protecting quantum states with the energy gap maybe the best approach to solving the decoherence problem in future large-scale quantum computation.

7.2. Progress toward SFQ control of nSQUID qubits

Figure 7.3 and Figure 7.4 show a possible evolution of the lower (gradiometric) qubit that allows an SFQ control. The following two pages are based on unpublished data [66]. This kind

of qubit is very similar to the tunable flux qubit investigated in [72, 73]. SFQ control has a great advantage because unshunted Josephson junctions isolate the qubit from the noisy room temperature electronics. The following steps have been made. First, a narrow superconductor ground strip shown by grey color (layer M0 in HYPRES notation) is placed below the junctions and one point of the qubit is connected with the ground plane. Next, two Josephson junctions (J3 and J4) are added. Finally, these two junctions are incorporated into Josephson Transmission Lines (or long Josephson junctions).

The circuit operates as following:

- The first (Start) vortex passes the JTL and creates about 2π phase drop on all its junctions. However, because of differential nature of the circuit only about a half of this phase drop is applied to the qubit junctions. In other words, two transformers with negative coupling operate as a phase divider. As a result, the qubit is its bi-stable state.
- The second (Stop) vortex passes the qubit with a controlled time delay. And it causes a similar 2π phase drop on all junctions of the second JTL. As a result, a complete 2π phase drop is applied to qubit junctions. But, fortunately for us 2π phase drop is equivalent to 0 drop. And the qubit again in its mono-stable (resonator) state.

All these mean that the qubit-like circuit is controlled by SFQ pulses. More exactly, SFQ pulses control the energy profile. If the circuit is symmetric then the profile variations are deep. If the circuit is asymmetric (with one transformer's inductance larger than the other one) then profile variations could be rather small.

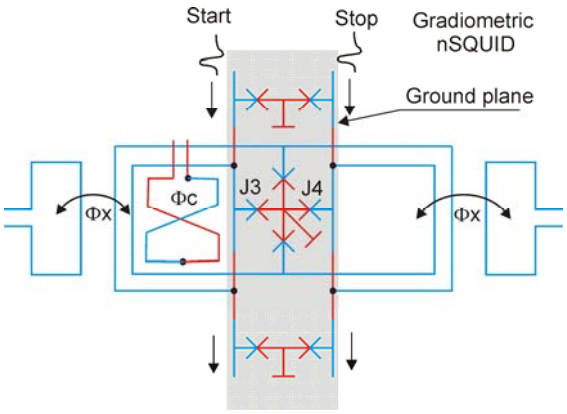


Figure 7.3. The first iteration for SFQ control of the nSQUID. Transformers with negative couplings look like two-turn coils. Φ_C could be applied via a differential coil.

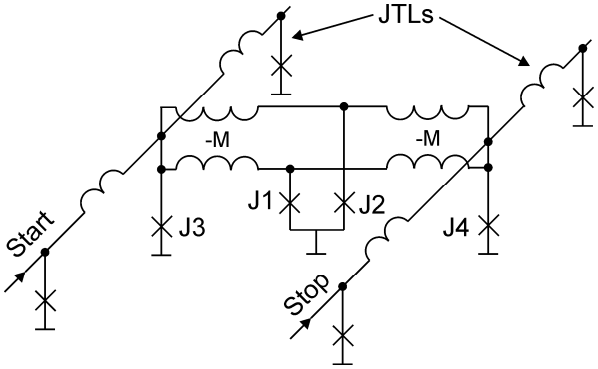
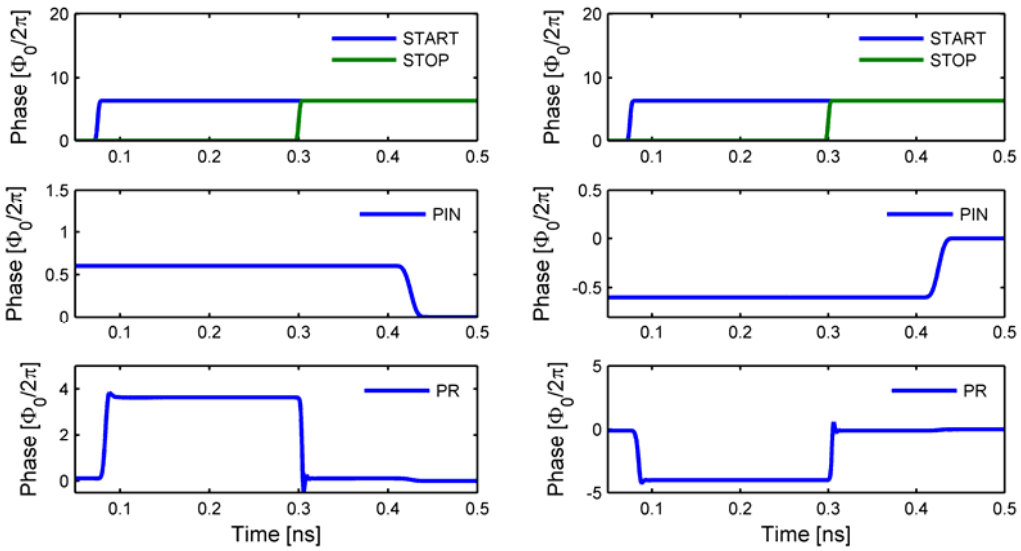


Figure 7.4. A schematic notation of the circuit in Figure 7.3. It is supposed that critical currents of J3 and J4 are much larger than those of J1 and J2.

The circuit shown in Figure 7.4 is simulated in PSCAN and proved to operate as expected. Critical currents of junctions J3 and J4 are both 62.5 μA, which are much larger than those of junctions J1 and J2 (5 μA).

After the first vortex (START) passing the JTL, the qubit will be in bi-stable state. After the 'STOP' vortex passes the JTL, qubit will return to mono-stable (resonator) state. The simulation result of this process is shown in Figure 7.5. PIN is the external magnetic field applied to the qubit loop; it changes the symmetry of the qubit. PR is the differential phase in the qubit loop.

When qubit is in bi-stable state, sign of PR indicates which state qubit stays in. As shown in Figure 7.5, after the 'START' vortex passes by, qubit stays in positive (negative) state while PIN is positive (negative) as in Figure 7.5(a) (Figure 7.5 (b)). After the 'STOP' vortex, in both cases qubit will return to mono-stable state.



(a) (b)

Figure 7.5. Simulation of how 'START' and 'STOP' vortices control the qubit.

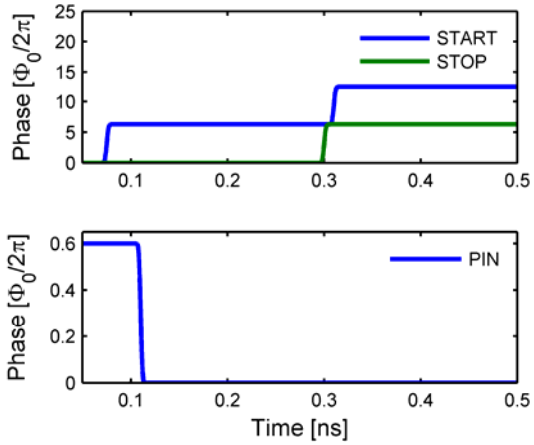


Figure 7.6. Input signals for simulation of circuit in Figure 7.4 with two 'START' vortices.

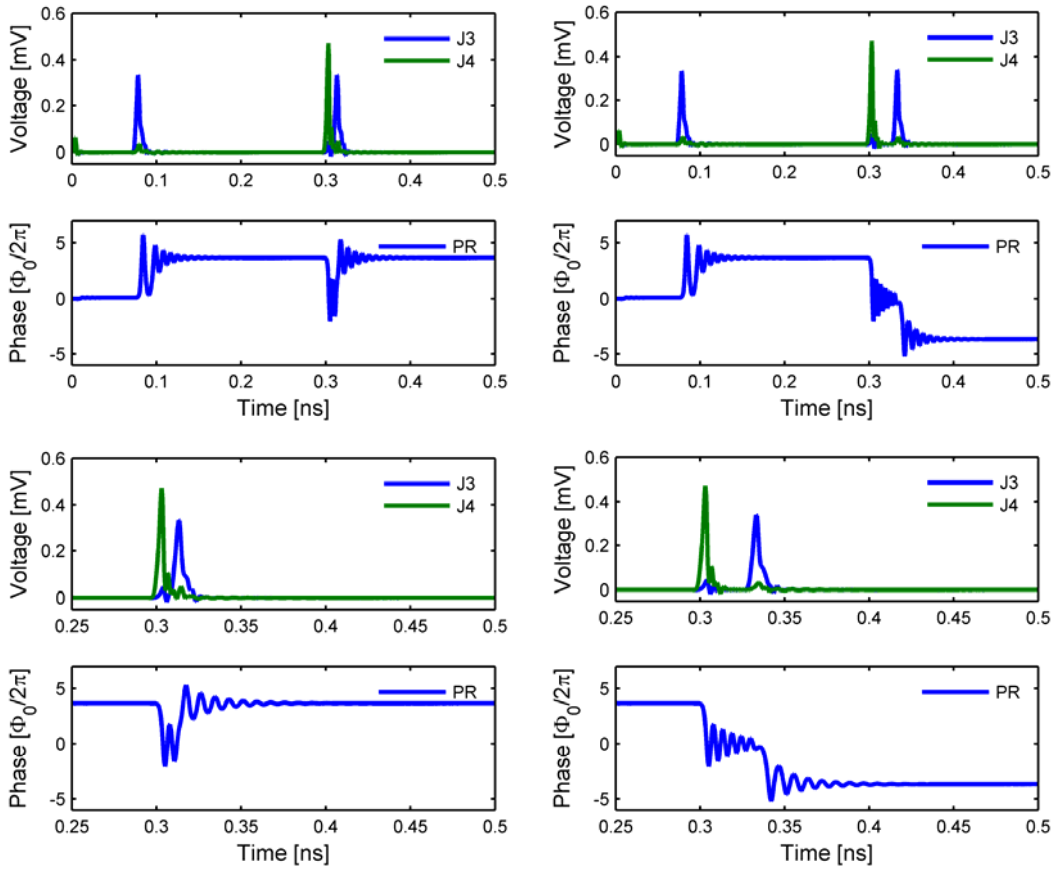


Figure 7.7. Simulation result of two different time interval between 1st STOP (shown as the pulse V of J4) and 2nd START vortex (shown as the second pulse).

If a second 'START' vortex passes the JTL immediately after the 'STOP' vortex, by controlling the time interval between them, we can obtain different states while the qubit is in bi-stable state again. The input signal of this process is shown in Figure 7.6. And the result is shown in Figure 7.7. The time intervals are 0.01 ns in Figure 7.7(a) and 0.03 ns in Figure 7.7(b) respectively. After the first 'START' vortex passing by, qubit stays in positive state in Figure 7.7(a) and (b), because PIN is positive as in bottom of Figure 7.6. After the second 'START' vortex, qubit stays in different states (positive in Figure 7.7(a) and negative in Figure 7.7(b)) resulting from the different time intervals in two cases.

Note currently a controllable delay generator between the Start and Stop pulses is not integrated into the circuit. Instead it is controlled by an external room-temperature pulse generator. Its raising edge activates Start pulse, while its descending edge activates Stop pulse.

7.3. Conclusion

In this chapter, we have discussed the advantages of the nSQUID circuits in the quantum computing (QC), which include the ability to transfer the quantum data along the chip, to bypass the requirement of controllable keys in the QC, and to form complex multi-qubit circuits. In the full quantum regime, the nSQUID arrays can be used directly to construct the scheme of universal adiabatic quantum computation. Conventional SFQ is shown as a good switch of the nSQUID qubit, which will make our UAQC more controllable.

Chapter 8 Conclusion

Superconductor electronics has been competing with semiconductor electronics for decades. The first superconductor 50 μs speed record was established in 1954, and in 1999 it reached 1.3 ps (or more exactly up to 770 GHz operating frequency for a T flip-flop [74]). Ironically the same author involved in the superconductor electronics [74] also participated in a semiconductor electronics work reporting record (100 GHz) speed demonstrated with SiGe T flip-flop [75]. From the speed perspective, it seems that the superconductor has won the race. Its success in speed is significant for some applications such as satellite communications [76]. However, the clock rate of modern high-end computing systems is "artificially" reduced because it has become less of a concern than other technical and economic requirements. For example, nowadays the main stream is to run these computing systems energy efficiently. Unfortunately some advantages of conventional RSFQ superconductor circuitry in lowering the specific energy dissipation are partly offset by poor cooling efficiency and other complications related with the low operation temperature, and thus the energy efficiency in this case is largely undermined.

This thesis has shown an approach to tackle the energy efficiency issue using superconductor circuitry. In short, a functional reversible superconducting circuit that can work with ultra low energy dissipation has been developed during the span of my PhD study. In the thesis work, I have gone through the whole design, simulation, fabrication and testing phases and several iterations of them. In detail, we first investigated the dynamic properties of shift register, based

on the newly suggested basic gate, nSQUID. We showed that the critical current of the shift register possesses unique properties even though the circuit is very similar to simple discrete long Josephson junction. Theoretic analysis suggests that the source of the new features is coming from the extra dimension of freedom introduced by differential phase inside the nSQUID. Then, by borrowing some ideas from widely investigated long Josephson junction (LJJ), we invented a new mechanism for realizing reversible computing in superconducting circuit. The main idea in this case is to use the densely packed vortices as a timing belt to transit a signal inside the loop composed with nSQUIDs and LJJs. A new version of LJJs suitable for our approach to reversible circuit was analyzed using both theoretical and experimental approaches. The experimental result agrees reasonably with the simulation result, which suggests the validity of the theoretical model we used. Next, several layouts on different iterations containing reversible shift register with direct and inverted shift registers were investigated. In each successive layout, we eliminated the identified sources of energy dissipation from previous layout for the sake of approaching an operation with energy dissipation close to the thermodynamic threshold. In the latest layout, the circular shift registers, which work under a new mechanism recycling the vortices, was measured to be functional between 50 MHz and 7 GHz range. More importantly, the energy dissipation per nSQUID gate per bit measured at 4 K temperature was below the thermodynamic threshold. In addition, more complex logical gates built upon nSQUIDs, shift registers and timing belt were designed and discussed. We showed the successful construction of all the basic cells needed for any logical gate in a reversible mode. Also, we showed that RSFQ circuit and the reversible circuit can be connected and integrated

together seamlessly and that the RSFQ circuit is capable of serving as a new control circuit of clock vortices for the reversible circuit. Last but not the least, we discussed another important application of the nSQUID circuits, i.e. in the area of the quantum computing (QC). The advantages of using nSQUIDs for QC were discussed and explored by simulations. Also, conventional SFQ was shown to behave as a good switch for the nSQUID qubit to provide more controllability in quantum computer.

In short, our approach drastically diminishes all technical dissipation mechanisms to leave logical irreversibility as the main dissipation channel. The promised few $k_B T$ per irreversible operation is about 10^6 times less (if measured in $k_B T$ units) or about 10^8 less (if measured in absolute values) than the figures demonstrated by the state-of-the-art semiconductor technologies [77]. Such an impressive gain would not be easily wiped out by the cooling inefficiency. As a result, we do not anticipate any practical need to revise the current computer architectures to eliminate or even to reduce the number of irreversible operations in practical circuits. Moreover, the new SFL and RSFQ technologies including new ERSFQ/eSFQ families [77] are compatible and can be integrated on a single chip. Our next task is to demonstrate interfaces between SFL and eSFQ circuits. The hybrid SFL/eSFQ circuits would speed up the insertion and acceptance of new SFL technology. However, continuous work is needed to demonstrate several reversible circuits with energy dissipation below the thermodynamic threshold. These demonstrations would serve as solid proof that we indeed are able to reduce the cumulative impacts of all other dissipation mechanisms to a level below the thermodynamic threshold. Crossing any fundamental threshold is psychologically important because it allows us to see things differently.

For example, the impossibility of reversible computation is a statement that can be found in road maps and assessments. We would like to render this statement obsolete. In fact, we are not alone with our interest to reversible computing. We would like to mention a community of enthusiasts discussing reversible computing based on various technologies [78]. These technologies range from exotic to very exotic. However, we completely agree with the community that reversible circuits could serve as natural prototypes of prospective quantum computers.

References

[1] H. K. Onnes, "Further experiments with liquid helium D - On the change of the electrical resistance of pure metals at very low temperatures, etc V The disappearance of the resistance of mercury," *Proceedings of the Koninklijke Akademie Van Wetenschappen Te Amsterdam,* vol. 14, pp. 113-115, 1911.

[2] J. G. Bednorz and K. A. Muller, "Possible High-Tc Superconductivity in the Ba-La-Cu-O System," *Zeitschrift Fur Physik B-Condensed Matter,* vol. 64, pp. 189-193, 1986.

[3] W. Meissner and R. Ochsenfeld, "Ein neuer Effekt bei Eintritt der Supraleitfähigkeit," *Naturwissenschaften,* vol. 21, pp. 787-78, 1933.

[4] F. London and H. London, "The electromagnetic equations of the supraconductor," *Proceedings of the Royal Society of London Series a-Mathematical and Physical Sciences,* vol. 149, pp. 0071-0088, Mar 1935.

[5] V. L. Ginzburg and L. D. Landau, "On the theory of superconductivity," *Zh. Eksp. Teor. Fiz.,* p. 1064, 1950.

[6] J. Bardeen, L. N. Cooper, and J. R. Schrieffer, "Theory of Superconductivity," *Physical Review,* vol. 108, pp. 1175-1204, 1957.

[7] B. D. Josephson, "Possible New Effects in Superconductive Tunnelling," *Physics Letters,* vol. 1, pp. 251-253, 1962.

[8] B. S. Deaver and W. M. Fairbank, "Experimental Evidence for Quantized Flux in Superconducting Cylinders," *Physical Review Letters,* vol. 7, pp. 43-&, 1961.

[9] R. Doll and M. Nabauer, "Experimental Proof of Magnetic Flux Quantization in a Superconducting Ring," *Physical Review Letters,* vol. 7, pp. 51-&, 1961.

[10] K. K. Likharev, O. A. Mukhanov, and V. K. Semenov, "Resistive single flux quantum logic for the Josephson-junction technology," *in SQUID'85 Berlin, Germany,* pp. 1103–08, 1985.

[11] B. D. Josephson, "Discovery of Tunnelling Supercurrents," *Proceedings of the IEEE,* vol. 62, pp. 838-841, 1974.

[12] B. Dorri, E. T. Laskaris, and M. D. Ogle, "Compact MRI superconducting magnet," 5721723, Aug. 26, 1996, 1998.

[13] H. Padamsee and J. Knobloch, Eds., *Superconducting Accelerator Magnets*. World Scientific Pub Co Inc, 1996.

[14] R. C. Jaklevic, A. H. Silver, J. Lambe, and J. E. Mercereau, "Quantum Interference Effects in Josephson Tunneling," *Physical Review Letters,* vol. 12, pp. 159-&, 1964.

[15] J. Clarke and A. I. Braginski, Eds., *The SQUID handbook 1*. Wiley-Vch, 2004.

[16] A. Enneper, "Über asymptotische Linien," *Nachr. Königl. Gesellsch. d. Wiss. Göttingen,* p. 493, 1870.

[17] D. W. Mclaughlin and A. C. Scott, "Perturbation Analysis of Fluxon Dynamics," *Physical Review A,* vol. 18, pp. 1652-1680, 1978.

[18] Available:

http://www.pi.uni-karlsruhe.de/ustinov/group_hp/fluxon.physik.uni-erlangen.de/ustinov/seminars/ws_01_02/lecture.html

[19] A. Barenco, C. H. Bennett, R. Cleve, D. P. Divincenzo, N. Margolus, P. Shor, T. Sleator, J. A. Smolin, and H. Weinfurter, "Elementary Gates for Quantum Computation," *Physical Review A,* vol. 52, pp. 3457-3467, Nov 1995.

[20] J. Clarke and F. K. Wilhelm, "Superconducting quantum bits," *Nature,* vol. 453, pp. 1031-1042, Jun 19 2008.

[21] E. Knill, "PHYSICS Quantum computing," *Nature,* vol. 463, pp. 441-443, Jan 28 2010.

[22] T. D. Ladd, F. Jelezko, R. Laflamme, Y. Nakamura, C. Monroe, and J. L. O'Brien, "Quantum computers," *Nature,* vol. 464, pp. 45-53, Mar 4 2010.

[23] C. H. Bennett, "Notes on the History of Reversible Computation," *Ibm Journal of Research and Development,* vol. 32, pp. 16-23, Jan 1988.

[24] V. K. Semenov, "Unpublished Data," 2010.

[25] L. Szilard, "On the Decrease of Entropy in a Thermodynamic System by the Intervention of Intelligent Beings," *Behavioral Science,* vol. 9, pp. 301-310, 1964.

[26] A. M. Nielsen and L. I. Chuang, Eds., *Quantum Computation and Quantum Information*. Cambridge University Press, 2000.

[27] J. Ren and V. K. Semenov, "Progress with Physically and Logically Reversible Superconducting Digital Circuits," *IEEE Transactions on Applied Superconductivity,* accepted in 2010.

[28] C. H. Bennett, "Notes on the history of reversible computation (Reprinted from IBM Journal of Research and Development, vol 32, 1988)," *Ibm Journal of Research and Development,* vol. 44, pp. 270-277, Jan-Mar 2000.

[29] K. K. Likharev, "Dynamics of Some Single Flux Quantum Devices .1. Parametric Quantron," *IEEE Transactions on Magnetics,* vol. 13, pp. 242-244, 1977.

[30] K. K. Likharev, G. M. Lapir, and V. K. Semenov, "Properties of the superconducting loop closed with the Josephson junction with variable critical current," *Pis'ma v Zh. Techn. Fiz. [Sov. Tech Phys. Lett.],* vol. 2, pp. 809-14, Sept. 1976.

[31] G. M. Lapir, K. K. Likharev, and V. K. Semenov, "a switch," 539333, Dec. 11, 1974, Publ. Dec. 15, 1976.

[32] K. K. Likharev, "Classical and Quantum Limitations on Energy-Consumption in Computation," *International Journal of Theoretical Physics,* vol. 21, pp. 311-326, 1982.

[33] K. K. Likharev, S. V. Rylov, and V. K. Semenov, "Reversible conveyer computation in arrays of parametric quantrons," *IEEE Trans. on Magn.,* vol. 21, p. 947, 1985.

[34] W. Hioe and E. Goto, Eds., *Quantum Flux Parametron - A single Quantum Flux Superconducting Logic Device, Singapore*. World Scientific, 1991.

[35] K. Shizume, "Heat-Generation Required by Information Erasure," *Physical Review E,* vol. 52, pp. 3495-3499, Oct 1995.

[36] J. Clarke, T. L. Robertson, B. L. T. Plourde, A. García-Martinez, P. A. Reichardt, V. D. J. Harlingen, B. Chesca, R. Kleiner, Y. Makhlin, G. Schön, A. Shnirman, and F. K. Wilhelm, "Quiet Readout of Superconducting Flux States " *Physica Scripta,* vol. T102, pp. 173-77,

2002.
[37] V. K. Semenov, G. V. Danilov, and D. V. Averin, "Negative-inductance SQUID as the basic element of reversible Josephson-junction circuits," *IEEE Transactions on Applied Superconductivity,* vol. 13, pp. 938-943, 2003.
[38] R. Landauer, "Uncertainty Principle and Minimal Energy-Dissipation in the Computer," *International Journal of Theoretical Physics,* vol. 21, pp. 283-297, 1982.
[39] J. Ren, V. K. Semenov, Y. A. Polyakov, D. V. Averin, and J. S. Tsai, "Progress Towards Reversible Computing With nSQUID Arrays," *IEEE Transactions on Applied Superconductivity,* vol. 19, pp. 961-967, 2009.
[40] V. K. Semenov, G. V. Danilov, and D. V. Averin, "Classical and quantum operation modes of the reversible Josephson-junction logic circuits," *IEEE Transactions on Applied Superconductivity,* vol. 17, pp. 455-461, 2007.
[41] E. Benjacob, D. J. Bergman, B. J. Matkowsky, and Z. Schuss, "LIFETIME OF OSCILLATORY STEADY-STATES," *Physical Review A,* vol. 26, pp. 2805-2816, 1982.
[42] Available: http://www.hypres.com
[43] S. Nagasawa, Y. Hashimoto, H. Numata, and S. Tahara, "A 380 ps, 9.5 mW Josephson 4-Kbit RAM operated at a high bit yield," *IEEE Trans. on Appl. Superconductivity,* vol. 5, pp. 2447-2452 1995.
[44] K. K. Likharev, S. V. Rylov, and V. K. Semenov, "Reversible Conveyor Computation in Array of Parametric Quantrons," *IEEE Transactions on Magnetics,* vol. 21, pp. 947-950, 1985.
[45] Y. A. Polyakov, V. K. Semenov, and S. K. Tolpygo, "3D Active Demagnetization of Cold Magnetic Shields," *IEEE Transactions on Applied Superconductivity,* accepted in 2010.
[46] Y. A. Polyakov, "Unpublished Data," 2011.
[47] Available: http://pavel.physics.sunysb.edu/RSFQ/Research/octopus.html
[48] D. E. Kirichenko and I. V. Vernik, "High quality on-chip long annular Josephson junction clock source for digital superconducting electronics," *IEEE Transactions on Applied Superconductivity,* vol. 15, pp. 296-299, 2005.
[49] O. M. Braun and Y. S. Kivshar, "Nonlinear dynamics of the Frenkel-Kontorova model," *Physics Reports-Review Section of Physics Letters,* vol. 306, pp. 2-108, Dec 1998.
[50] M. V. Fistul, P. Caputo, and A. V. Ustinov, "Resonances in spatially modulated long Josephson junctions," *Physical Review B,* vol. 60, pp. 13152-13157, Nov 1 1999.
[51] A. L. Fetter and M. J. Stephen, "Fluctuations in a Josephson Junction," *Physical Review,* vol. 168, pp. 475-&, 1968.
[52] M. Cirillo, B. H. Larsen, A. V. Ustinov, V. Merlo, V. A. Oboznov, and R. Leoni, "On Magnetic-Flux Dynamics in 1d Arrays of Underdamped Josephson-Junctions," *Physics Letters A,* vol. 183, pp. 383-389, Dec 20 1993.
[53] D. V. Averin, K. Rabenstein, and V. K. Semenov, "Rapid ballistic readout for flux qubits," *Physical Review B,* vol. 73, 2006.
[54] Available: http://pavel.physics.sunysb.edu/RSFQ/Lib/AR/dcsfq.html
[55] V. K. Semenov, S. A. Vasenko, and K. K. Likharev, "Dynamics of the Long

Josephson-Junctions," *IEEE Transactions on Magnetics,* vol. 17, pp. 800-803, 1981.
[56] A. S. M. J. Pfeiffer, A. K. Feofanov, and A. V. Ustinov, "Vortices in Comb-arrays of submicron Josephson Junctions," to be published.
[57] N. Yoshikawa and Y. Kato, "Reduction of power consumption of RSFQ circuits by inductance-load biasing," *Superconductor Science & Technology,* vol. 12, pp. 918-920, Nov 1999.
[58] J. Beyer and D. Drung, "A SQUID series array dc current sensor," *Superconductor Science & Technology,* vol. 21, pp. -, Sep 2008.
[59] P. Russer, "General Energy Relations for Josephson Junctions," *Proceedings of the Institute of Electrical and Electronics Engineers,* vol. 59, pp. 282-&, 1971.
[60] J. Oppenlander, C. Haussler, and N. Schopohl, "Non-Phi(0)-periodic macroscopic quantum interference in one-dimensional parallel Josephson junction arrays with unconventional grating structure," *Physical Review B,* vol. 6302, pp. -, Jan 1 2001.
[61] C. Haussler, J. Oppenlander, and N. Schopohl, "Nonperiodic flux to voltage conversion of series arrays of dc superconducting quantum interference devices," *Journal of Applied Physics,* vol. 89, pp. 1875-1879, Feb 1 2001.
[62] J. Oppenlander, C. Haussler, T. Trauble, and N. Schopohl, "Highly sensitive magnetometers for absolute magnetic field measurements based on quantum interference filters," *Physica C-Superconductivity and Its Applications,* vol. 368, pp. 119-124, Mar 1 2002.
[63] V. K. Kornev, Soloviev, II, N. V. Klenov, and O. A. Mukhanov, "Development of SQIF-based output broad band amplifier," *IEEE Transactions on Applied Superconductivity,* vol. 17, pp. 569-572, 2007.
[64] Available: http://www.electroniq.net/electronic-tutorials/inductor-inductance-and-air-coil-inductance-formula.html
[65] D. Banerjee, Ed., *PLL Performance, Simulation and Design Handbook*. National Semiconductor, 2006.
[66] V. Semenov and J. Ren, "nSQUIDs with SFQ Control," *Unpublished,* 2009.
[67] A. Wallraff, A. Lukashenko, J. Lisenfeld, A. Kemp, M. V. Fistul, Y. Koval, A. V. Ustinov, "Quantum dynamics of a single vortex," *Nature,* vol. 425, pp. 155-158, Sep 11 2003.
[68] D. Aharonov, W. Van Dam, J. Kempe, Z. Landau, S. Lloyd, O. Regev, "Adiabatic quantum computation is equivalent to standard quantum computation," *Siam Journal on Computing,* vol. 37, pp. 166-194, 2007.
[69] A. Mizel, D. A. Lidar, M. Mitchell, "Simple proof of equivalence between adiabatic quantum computation and the circuit model," *Physical Review Letters,* vol. 99, pp. -, Aug 17 2007.
[70] S. Lloyd, "Robustness of adiabatic quantum computing," arXiv:0805.2757.
[71] M. H. S. Amin, C. J. S. Truncik, and D.V. Averin, "Role of the single qubit decoherence time in adiabatic quantum computation," arXiv: 0803.1196.
[72] F. Chiarello, P. Carelli, M. G. Castellano, C. Cosmelli, L. Gangemi, R. Leoni, S. Poletto,

D. Simeone, and G. Torrioli, "Superconducting tunable flux qubit with direct readout scheme," *Superconductor Science & Technology,* vol. 18, pp. 1370-1373, Oct 2005.

[73] S. Poletto, F. Chiarello, M. G. Castellano, J. Lisenfeld, A. Lukashenko, C. Cosmelli, G. Torrioli, P. Carelli, and A. V. Ustinov, "Coherent oscillations in a superconducting tunable flux qubit manipulated without microwaves," *New Journal of Physics,* vol. 11, pp. -, Jan 7 2009.

[74] W. Chen, A. V. Rylyakov, V. Patel, J. E. Lukens, and K. K. Likharev, "Rapid Single Flux Quantum T-flip flop operating up to 770 GHz," *IEEE Transactions on Applied Superconductivity,* vol. 9, pp. 3212-3215, Jun 1999.

[75] A. Rylyakov and T. Zwick, "96-GHz static frequency divider in SiGe bipolar technology," *IEEE Journal of Solid-State Circuits,* vol. 39, pp. 1712-1715, Oct 2004.

[76] O. A. Mukhanov, D. Kirichenko, I. V. Vernik, T. V. Filippov, A. Kirichenko, R. Webber, V. Dotsenko, A. Talalaevskii, J. C. Tang, A. Sahu, P. Shevchenko, R. Miller, S. B. Kaplan, S. Sarwana, and D. Gupta, "Superconductor digital-RF receiver systems," *IEICE Transactions on Electronics,* vol. E91C, pp. 306-317, 2008.

[77] O. A. Mukhanov, "Energy-efficient single flux quantum technology," *IEEE Trans. Appl. Supercond.,* vol. Submitted for publication, 2010.

[78] B. Hayes, "Reverse engineering," *American Scientist,* vol. 94, pp. 107-111, Mar-Apr 2006.