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Design of Low Noise and Low Power Front-end Readout Circuitry in Radiation Detector System

A Thesis Presented

By

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Abstract of the Thesis

Design of Low Noise and Low Power Front-end Readout Circuitry in Radiation Detector System

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This thesis presents a design methodology of a low-power and low-noise integrated front-end readout circuits for radiation detection. Since a charge sensitive amplifier (CSA) and a pulse shaper are essential circuit units in the low-power and low-noise front-end readout circuits, this thesis provides how to design the low power low noise CSA and the pulse shaper. The CSA can allow the electrons generated from the detector to integrate on a feedback capacitor of a CSA. The main function of a CSA is to amplify the input signal charge generated from the detector into the output voltage step signal. The input transistor optimization can significantly reduce the noise impact on the

whole system so it can help the front-end readout circuit increase the sensitivity in order to detect smaller electrons generated from the detector. The pulse shaper is a high order semi-Gaussian pulse shaping filter. The main function of the pulse shaper is to filter the output signal and noise from the CSA in order to maximize signal-to-noise ratio and obtain the lowest equivalent noise charge (ENC). In this thesis, the semi-Gaussian pulse shaper with ICON cells can achieve a longer time constant in order to minimize the noise in the circuitry.

To

My Parents and My Grandparents

For their continuous support, encouragement, and love

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1.0 Introduction

1.1. Radiation Detection System Overview:

Radiation detection is one of the important applications in the design of integrated microsystems. The radiation detection system usually integrates the detectors with the electronic interface and processing circuitry. The main function of the detector, also called a sensor, is to detect high energy radiation from the physical world and convert it into an electrical signal for further signal processing. The electronic interface and processing circuitry, also called front-end readout circuitry, should be placed close to the sensor array in order to efficiently process the electrical signal from the detector. The main function of the front-end readout circuitry is to capture the weak and short electrical pulse generated by the sensors, to perform analog signal processing, and to optimize the noise from the system before analog-to-digital conversion. The digital value can represent the number of electrons produced by the detector in case of an event and should be communicated to the digital processing units. The front-end readout circuitry can be shown by a common framework as shown in Figure1.1 and it usually contains charge sensitive amplifier (CSA), a pulse shaping filter, and analog-to-digital conversion units. Each of the circuit units is discussed below.

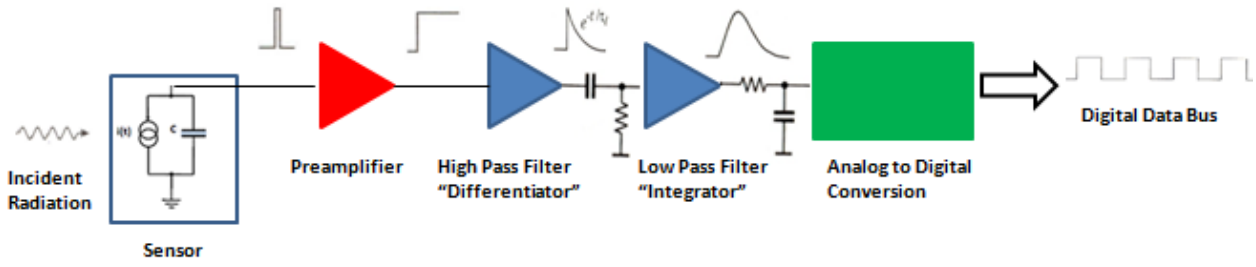

Figure 1.1 Proposed Readout System Block Diagram

1.1.1 Radiation Detector (Sensor):

The radiation detector (the sensor) can convert the radiation energy to an electrical signal. The energy is absorbed in a semiconductor, for example silicon, which produces mobile charge carriers – electron-hole pairs. An electric field applied to the sensor sweeps the charge carriers to electrodes, inducing an electrical current. The number of electron-hole pairs is proportional to the absorbed energy, so integrating the signal current can obtain the signal charge which is also proportional to the energy. The signal charge forms a short current pulse (of order nanoseconds or less) and the spatial extent of the charge cloud is small (of order microns) [1]. The processing

circuitry can measure the amplitude and the timing of the current pulse for each event. The current pulse is coupled to a low-noise charge amplifier and sent through a pulse shaper filter.

The detector can be modeled as a capacitor in parallel with a current source $i(t)$ in Figure1.2. The current source is represented as the electrical signal produced by the detector. The signal is a small current AC pulse, which has a time period in the nano-second range, on top of a constant DC leakage current. The constant DC leakage current is usually between 10pA to 100nA, which is dependent on the detector. The area of the AC pulse can represent the signal charge Q which is proportional to the number of electrons generated by the detector. The number of electrons is dependent on the detector and the energy of radiation source. The signal charge Q can vary from fractions of femtoCoulomb (fC) to several picoCoulomb (pC). We assume that the signal charge Q is collecting instantaneously:

$$i(t) = Q \times \delta(t), \text{ where } \delta(t) \text{ is the Dirac Delta Function.} \qquad (1.1)$$

The capacitance C as shown in Figure 1.2 represents the parasitic capacitance to the ground of the detector, and the value of the parasitic capacitance can vary from few femtoFarad (fF) to several nanoFarad (nF). For the pixel size of $1mm^2$, the capacitance C usually can be estimated to be $50pF$. Another important design parameter is the event rate, the frequency of the AC pulse. In our design, we are dealing with the low event rate so we expect that the period of the two consecutive AC pulses is $1000ms$. In order to avoid signal pile-up, the processing time of the circuitry should be kept within one tenth of the period of the two consecutive AC pulses.

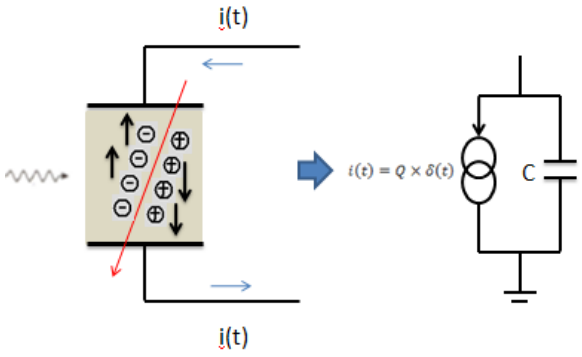

Figure 1.2 Sensor Model

1.1.2 Charge Sensitive Amplifier (CSA):

The sensor signal, the signal charge, can be quite small so the signal charge should be amplified. The signal charge from the detector can be pre-amplified in two ways: high input impedance amplifier and low input impedance amplifier as shown in Figure1.3. In both configurations, the network R provides the discharge of C or Cf after the measurement. However, in the low-impedance configuration, the feedback network R can provide stabilization of the sensing and output nodes of the amplifier. Therefore, we prefer to use a low input

impedance amplifier by implementing a charge sensitive amplifier (CSA). With the CSA, the input charge can be integrated on a small feedback capacitance Cf and a voltage step can be obtained at the output. Therefore, the primary function of the CSA is to convert the input charge signal into the output voltage signal.

The magnitude of the sensor signal is subject to statistical fluctuations, and electronic noise further smears the signal. Therefore, the sensor and preamplifier must be designed carefully to minimize electronic noise. A critical parameter is the total capacitance in parallel with the sensor capacitance and input capacitance of the amplifier. The signal-to-noise ratio increases with decreasing capacitance. The contribution of electronic noise also relies critically on the next stage, the pulse shaper [1]-[3].

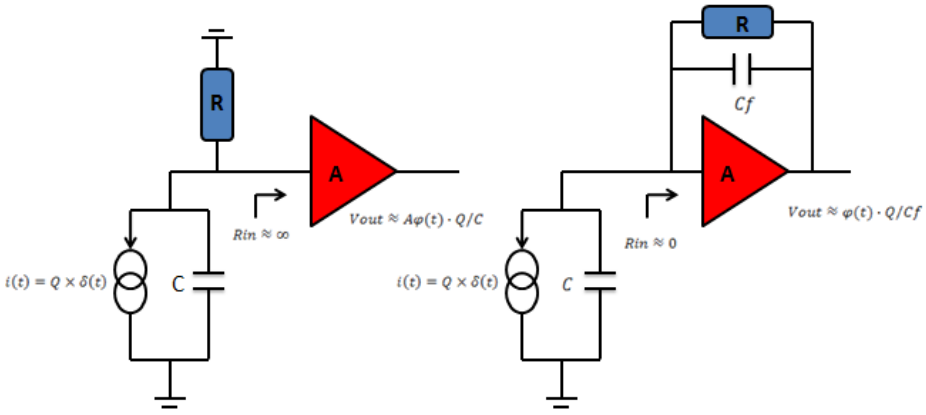

Figure 1.3 High Input Impedance Amplifier and Low Input Impedance Amplifier (CSA)

1.1.3 Pulse Shaper:

In a semiconductor detector system, the primary function of the pulse shaper is to maximize the signal-to-noise ratio. Although the signal pulses are considered as time-varying signals, the signal power is also distributed in frequency domain, derived by the pulse's Fourier transform. Since the frequency spectra of the noise and the signal is different, applying a pulse shaper after the CSA can improve the signal-to-noise ratio in order to filter the frequency response of the noise, while to tailor the frequency response to favor the signal. Since changing the frequency response also changes the time constant of the output pulse shape, that's why this function is called pulse shaping.

Figure1.1 shows how the pulse transformation can be accomplished. The preamplifier is configured as a CSA, which converts the AC current pulse from the sensor into a step voltage signal with a long decay time. A subsequent CR high-pass filter (a differentiator) introduces the desired decay time and a RC low pass filter (an integrator) limits the bandwidth and sets the rise time. Using multiple integrators in a more complex shaper can improve the pulse symmetry. This will be discussed in more details later. When designing a pulse shaper, it is necessary to set

proper the upper frequency bound which sets the rise time, and the lower frequency bound which determines the pulse duration. In addition, finding a balance between the conflicting requirements of reducing noise and increasing speed is necessary. Sometimes the speed is important, sometimes minimum noise is paramount, but usually a compromise between the two must be found [1]-[3].

In this thesis, we choose to use a semi-Gaussian shaper in our circuitry system, since many papers [4]-[9] have proven that a semi-Gaussian shaper generally gives the best noise performance. The output of the pulse shaper is a Gaussian shaped pulse with its peak amplitude proportional to the input charge Qin released by the detector. The peak of the pulse is captured by the subsequent peak detector and then sent through the analog-to-digital conversion units.

1.1.4 Analog-to-Digital Conversion:

The peak value of the output voltage from the pulse shaper should be sampled before it's sent to analog-to-digital converter. The peak detector can sample and capture the peak amplitude of the pulse at the output of the pulse shaper [10]-[13]. Once the peak amplitude of the pulse is sampled, it will be sent through to the analog-to-digital converter (ADC) and then we can get the digital output signals at the output of ADC for further digital signal processing.

1.2. Organization:

Chapter 2 describes theoretical background about signal/noise analysis and equivalent noise charge. Chapter 3 provides the design procedures of the CSA. Chapter 4 presents the design procedures of the pulse shaper. Chapter 5 summarizes the thesis and future work.

2.0 Theoretical Background

2.1 Signal Analysis:

The input signal charge generated from the detector can be represented as a Dirac current impulse, the integral of which is equal to the charge Q corresponding to one electron charge [14]. The output signal of the CSA is an exponentially rising step function with a rise time τs which is inversely proportional to the gain bandwidth of the amplifier and is proportional to the detector capacitance. In fact, the rise time τs can be designed to be as low as possible, several nanoseconds, by increasing the gain bandwidth of the amplifier so that the output signal of the CSA can be seen approximately as an ideal step signal with an amplitude Q/Cf. The output signal of the CSA was sent through the next stage, the pulse shaper. The transfer function $H(s)$ of the pulse shaper, a semi-Gaussian pulse shaper which consists of one RC differentiator and n RC integrators shown, is given by

$$H(s) = \left[\frac{s\tau}{1+s\tau}\right]\left[\frac{A}{1+s\tau}\right]^n \tag{2.1}$$

where τ is the time constant of the differentiator and integrators, and A is the DC gain of the integrator. The order n of the semi-Gaussian shaper is determined by the number of real coincident poles of the shaper. In the frequency domain, the signal at the output of the pulse shaper is the product of the transfer function $H(s)$ of the pulse shaper and the Laplace transform of the step signal Q/sCf. By taking the inverse Laplace transform of the product, the output signal in the time domain is given by

$$Vout(t) = \left(\frac{Q}{Cf}\right) \cdot h(t) = \int_{-\infty}^{+\infty} \left(\frac{Q}{sCf}\right) \cdot H(s) \cdot e^{-j2\pi ft} df = \frac{Q \cdot A^n \cdot n^n}{Cf \cdot n!} \cdot \left(\frac{t}{\tau p}\right)^n \cdot e^{-nt/\tau p} \tag{2.2}$$

where τp, called peaking time of the shaper, is defined by $\tau p = n \times \tau$. The voltage output at the pulse shaper has a semi-Gaussian pulse shape in the time domain. The peak amplitude at the peaking time τp can be easily obtained by taking the derivative of equation 2.2 so that the peak amplitude at the output of the pulse shaper as shown in Figure 2.1 is given by

$$Voutmaz = \left(\frac{Q}{Cf}\right) \cdot h(t_{max}) = \frac{Q \cdot A^n \cdot n^n}{Cf \cdot n! \cdot e^n} \tag{2.3}$$

The peak amplitude is proportional to the charge Q generated by the detector. Therefore, the energy of radiation can be determined by measuring the peak amplitude.

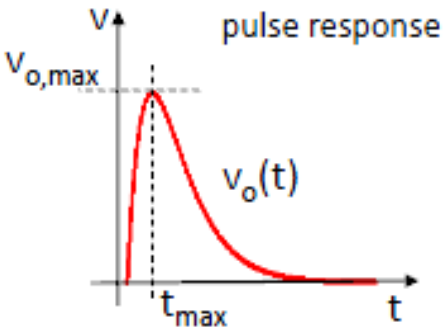

Figure 2.1 The Pulse Response at the Output of the Pulse Shaper

2.2 Noise Analysis:

2.2.1 Noise Power Spectral Density:

The power spectral density (PSD) shows how much power the signal carries at each frequency. More specifically, the PSD, $Sx(f)$, of a noise waveform $x(t)$ is defined as the average power carried by $x(t)$in an one-hertz bandwidth around f. In summary, the spectrum shows the power carried in a small bandwidth at each frequency, revealing how fast the waveform is expected to vary in the time domain [15].

Noise generators as shown in Figure 2.2 can be represented with their power spectral density, which is the distribution of average power in the frequency domain. The variance ${\sigma_n}^2$ of the noise with power spectral density $Sn(f)$ is given by

$$ {\sigma_n}^2 = \int_0^\infty Sn(f)df = \overline{S_n(t)^2} \tag{2.4} $$

Figure 2.2 Current and Voltage Noise Generators

which can be applied to voltage or current noise generators. In addition, if an input referred noise with spectrum $Sni(f)$ is applied to a linear time-invariant system with transfer function $H(f)$ as shown in Figure 2.3, the output noise spectrum $Sno(f)$ and the output variance ${\sigma_{no}}^2$ are given by

$$ {\sigma_{no}}^2 = \overline{S_{no}(t)^2} = \int_0^\infty Sno(f)df = \int_0^\infty Sni \cdot |H(f)|^2 df \tag{2.5} $$

Figure 2.3 Linear Time-Invariant System with Transfer Function $H(f)$

It agrees with our derivation that the spectrum of the signal or the noise should be shaped by the transfer function $H(f)$.

2.2.2 Thermal Noise:

Resistor Thermal Noise means that the random motion of electrons in a conductor introduces fluctuations in the voltage measured across the conductor even if the average current is zero. Thus, the spectrum of thermal noise is proportional to the absolute temperature. As shown in Fig.2.4, the thermal noise of a resistor R can be modeled by a series voltage source or parallel current source with the one-sided spectral density

$$Sv(f) = 4KTR \; ; Si(f) = \frac{Sv(f)}{R^2} = \frac{4KT}{R} \; , \; f \geq 0 \tag{2.6}$$

where $k = 1.38 \times 10^{-23} J/K$ is the Boltzmann constant; $T = 300K$is the absolute temperature; R is the resistive component of the device. Note that $Sv(f)$ is expressed in V^2/Hz.

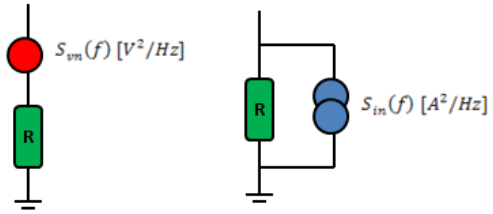

Figure 2.4 Series Voltage and Parallel Current Thermal Noise Generators with Noiseless Device

MOSFETs also exhibit thermal noise. The most significant source is the noise generated in the channel. It can be proven that for long-channel MOS devices operating in saturation, the channel noise can be modeled by a parallel current source connected between the drain and source terminals or by a series voltage source connected to the gate terminal as shown in Figure 2.5. Both models can be represented with their power spectral density as below.

$$Sv(f) = 4rKTgm \; ; Si(f) = \frac{Sv(f)}{gm^2} = \frac{4rKT}{gm} \; , \; f \geq 0 \tag{2.7}$$

where the coefficient r is derived to be equal to $2/3$ for long-channel transistors and which may need to be replaced by a large value for submicron MOSFETs; gm is the transconductance of MOSFET [15].

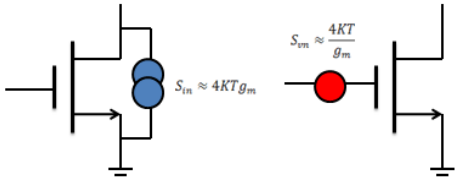

Figure 2.5 Series Voltage and Parallel Current Thermal Noise Generators with MOSFET

2.2.3 Flicker Noise ($1/f$ Noise):

The interface between the gate oxide and the silicon substrate in a MOSFET entails an interesting phenomenon. Since the silicon crystal reaches an end at this interface, many dangling bonds appear, giving rise to extra energy states. As charge carriers move at the interface, some are randomly trapped and later released by such energy states, introducing flicker noise in the drain current. The flicker noise is easily modeled as a voltage source in series with the gate and roughly given by

$$Sv(f) = {}^{K}/_{Cox \cdot WL \cdot f} \tag{2.8}$$

where k is a process-dependent constant on the order of $10^2 - 25^2(F)$. The noise spectral density associated with dangling bonds occurs at low frequency more often. For this reason, flicker noise is also called $1/f$ noise, which can be modeled in Figure 2.6. The inverse dependence of $1/f$ noise on WL suggests that to decrease $1/f$ noise, the device area must be increased. Therefore, it's not surprising to see devices having areas of several thousand square microns in low-noise applications [15].

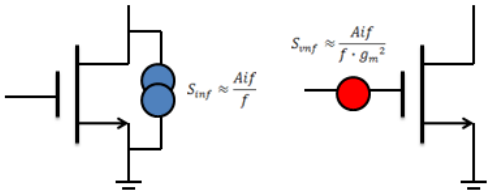

Figure 2.6 Series Voltage and Parallel Current $1/f$ Noise Generators with MOSFET

2.2.4 Shot Noise:

Shot noise in electronic circuits is due to the quantized nature of the electric charge. It consists of random fluctuations of the electric current in a DC current due to that current consisting of a flow of discrete electrons. The spectral noise density of shot noise is given as

$$Si(f) = 2qI \tag{2.9}$$

where I is the average DC current, and q is the electronic charge. Note that the criterion for shot noise is that carriers are injected independently of one another, as in semiconductor diodes. The shot noise of a reverse-biased diode can be modeled by a parallel current source as shown in Figure 2.7.

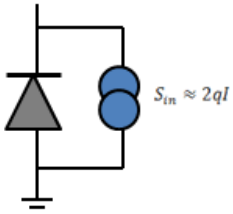

Figure 2.7 Parallel Current Shot Noise Generator with Reverse-Biased Diode

2.2.5 Noise Path:

The noise properties of a front-end readout circuitry can be represented by a series voltage noise generator and a parallel current noise generator at the input of the amplifier, as shown in Figure 2.8. C_D is represented as the detector capacitance. Rather than specifying the total noise over the full bandwidth, the magnitude of each noise source generator is described by its power spectral density. According to the generally accepted assumption, the total system noise is assumed to be dominated by the leakage current of the detector and the input MOS transistor of the CSA. Since the feedback resistor R of the CSA provides a white parallel noise source at the input node of the CSA, the feedback resistor R should be very large in order to make its noise contribution negligible. Therefore, we first ignore the noise contribution from the feedback resistor R in our noise analysis. The two equivalent noise sources are given by

$$Sv = Vn^2 = \frac{8}{3} \cdot KT \cdot \frac{1}{gm} + \frac{K_f}{Cox^2 \cdot WL \cdot f} \tag{2.10}$$

$$Si = In^2 = 2qI \tag{2.11}$$

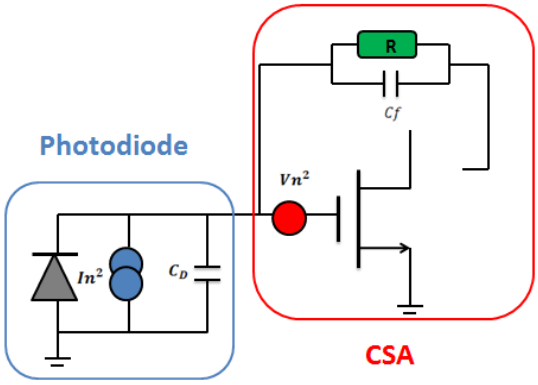

Figure 2.8 Noise Models for Detector System

where gm is the transconductance of the input transistor. The first term in equation 2.10 represents the channel thermal noise of the input MOS transistor. The second term in equation 2.10 represents the $1/f$ noise of the input MOS transistor, where Kf is the $1/f$ noise coefficient of the CMOS process used in [16] [17]. In addition to the input MOS transistor noise, the detector leakage current provides another noise component, which is shot noise. It generally can be expressed as equation 2.11, where I is the detector leakage current.

From the above two equations, the total noise power spectrum at the output of the CSA can be given by

$$Vn,out(s)^2 = \left(\frac{Cf+Cgs+Cgd+C_D}{Cf}\right)^2 \cdot Vn^2 + \left(\frac{1}{sCf}\right)^2 \cdot In^2 \quad (2.12)$$

The first term in equation 2.12 represents the thermal noise and $1/f$ noise from the input MOS transistor and the second term is the shot noise due to the detector leakage current. The total integrated rms noise at the output of the pulse shaper must be calculated first and then we can easily calculate the signal-to-noise ratio, which is that the amplitude of the signal divided by the total integrated rms noise, at the output of the pulse shaper. The transfer function $H(s)$ of a sem-Guassian pulse shaper consisting of one CR differentiator and n RC integrators is give by equation 2.1.

$$H(s) = \left[\frac{s\tau}{1+s\tau}\right]\left[\frac{A}{1+s\tau}\right]^n \quad (2.1)$$

The total noise power spectrum at the output of CSA is tailored by the transfer function $H(s)$ of the pulse shaper as shown in Figure 2.9. The total integrated rms noise at the output of the pulse shaper is then calculated as

$$\sigma_{n,tot}{}^2 = Vtot^2 = \int_0^\infty |Vo(j2\pi f)|^2 \cdot |H(j2\pi f)|^2 df$$

$$= \int_0^\infty Si \cdot |Htot(s)|^2 df + \int_0^\infty Sv \cdot \omega^2 \cdot Cin^2 \cdot |Htot(s)|^2 df \quad (2.13)$$

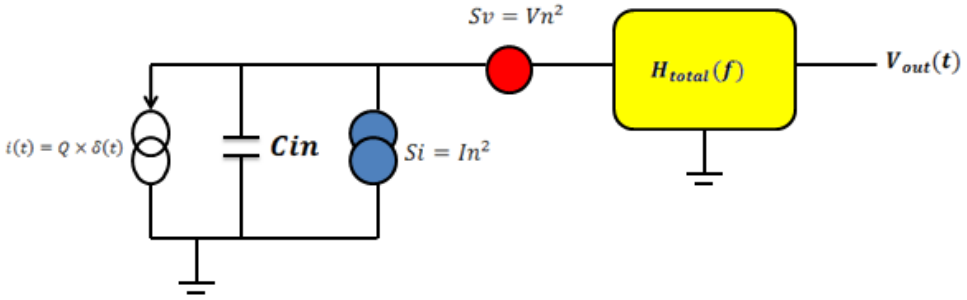

Figure 2.9 Simplified Noise Response for Detector System

where $Cin = Cf + Cgs + Cgd + C_D$ is equal to the sum of the capacitance; Cf is the feedback capacitance of the CSA, Cgs and Cgd is the capacitance of the input MOS transistor; C_D is the capacitance of the detector; $Htot(s)$ is the transfer function of the whole system; Si is the equivalent parallel current noise source from the shot noise of the detector leakage current, Sv is the equivalent series voltage noise source from thermal noise and $1/f$ noise of the input MOS transistor.

2.3 Equivalent Noise Charge (ENC):

In the detector readout system, the noise performance of the system is generally expressed as the equivalent noise charge (ENC). The ENC is defined as the charge that the detector has to release in order to yield a signal-to-noise ratio to one. In order words, the ratio of the total integrated rms noise at the output of the pulse shaper to the signal amplitude due to one electron charge Q represents the ENC [1] [14]. ENC can be given by

$$\frac{S}{N} = \frac{Vo_{max}}{\sigma_{n,tot}} = \frac{Q \cdot h_{max}}{\sqrt{\int_0^\infty Si \cdot |Htot(s)|^2 df + \int_0^\infty Sv \cdot \omega^2 \cdot Cin^2 \cdot |Htot(s)|^2 df}}$$

$$ENC = \frac{\sqrt{\int_0^\infty Si \cdot |Htot(s)|^2 df + \int_0^\infty Sv \cdot \omega^2 \cdot Cin^2 \cdot |Htot(s)|^2 df}}{h_{max}} = \sqrt{{ENC_{ws}}^2 + {ENC_{1/f}}^2 + {ENC_{wp}}^2} \quad (2.14)$$

where ENC is commonly expressed in fC or in rms electons; ENC_{ws}, $ENC_{1/f}$, and ENC_{wp} represent white series noise from the input MOS transistor, the $1/f$ series noise from the input MOS transistor, and the white parallel shot noise due to the detector leakage current. We try to design the front-end readout circuitry with the lowest possible ENC. Clearly, the ENC relies on the characteristics of the detector, the CSA, and the pulse shaper. Before designing the CSA and the pulse shaper, it is better to deal with each independent noise component separately.

2.3.1 ENC_{ws} Due to Channel Thermal Noise of Input MOS Transistor:

The thermal noise source originates from the channel resistance of the input MOS transistor. Dividing the integrated rms thermal noise to the signal amplitude due to one electron charge, the ENC_{ws} is given by

$$ENC_{ws} = \frac{8}{3} \cdot KT \cdot \frac{1}{gm} \cdot \frac{(Cg+Cf+C_D)^2 \cdot B(\frac{3}{2}, n-\frac{1}{2}) \cdot n}{q^2 \cdot 4\pi \cdot \tau} \cdot \left(\frac{n! \cdot e^{2n}}{n^{2n}}\right) = a_{ws} \cdot \frac{\gamma}{gm} \cdot (Cg + Cf + C_D)^2 \cdot \frac{1}{\tau} \quad (2.15)$$

where $B(x, y)$ is the beta-function; a_{ws} is the constant shaping factor that depends on the order of the pulse shaper; γ is the thermal noise coefficient that depends on the operation region of transistor; C_D is the summation of the detector parasitic capacitance; Cg is the input capacitance of the input MOS transistor; Cf is the feedback capacitance of the CSA. This is a general ENC_{ws} expression and is valid for most of detector systems by using semi-Gaussian pulse shapers with

n^{th} order. Obviously, the use of the pulse shaper with larger time constant τ can limit the thermal noise. In addition, the ENC_{ws} is proportional to the input capacitance and depends slightly on the order of the pulse shaper.

2.3.2 $ENC_{1/f}$ Due to 1/f Noise of Input MOS Transistor:

In the design of the detector readout system, a CMOS technology process provides $1/f$ noise, so the detector resolution is affected by $1/f$ noise significantly. The $1/f$ noise originated from the input MOS transistor. $ENC_{1/f}$ can be given by

$$ENC_{1/f} = \frac{K_f}{Cox^2 \cdot WL \cdot f} \cdot \frac{(Cg+Cf+C_D)^2}{Q^2 \cdot 2n} \cdot \left(\frac{n! \cdot e^{2n}}{n^{2n}}\right) = a_f \cdot Kf \cdot (Cg + Cf + C_D)^2 \qquad (2.16)$$

where a_f is the constant shaping factor that depend on the order of pulse shaper; Kf is $1/f$ noise coefficient of the input transistor. The equation 2.16 can show that $ENC_{1/f}$ strongly depends on the process parameters Kf, Cox, and the input MOS transistor dimension. In addition, $ENC_{1/f}$ is totally independent of the time constant τ of the pulse shaper and depends slightly on the order of the pulse shaper.

2.3.3 ENC_{wp} Due to Shot Noise of the Detector leakage current:

For the noise component $2qI$, due to the detector leakage current, ENC_{wp} can be expressed as

$$ENC_{wp} = 2qI \cdot \frac{\tau \cdot B(\frac{1}{2}, n+\frac{1}{2})}{q^2 \cdot 4\pi \cdot \tau} \cdot \left(\frac{n! \cdot e^{2n}}{n^{2n}}\right) = a_{wp} \cdot I \cdot \tau \qquad (2.17)$$

In contrast to ENC_{ws}, ENC_{wp} is proportional to the time constant τ of the pulse shaper. Furthermore, it depends on the characteristics of the shaper and is independent of the input transistor dimension.

In the following sections, we will discuss more details of ENC effect on the design parameters of the CSA and the pulse shaper. We want to design the lowest possible ENC in our front-end readout circuitry. The optimal input transistor characteristics of the CSA, the optimal peaking time of the pulse shaper, and the order of the pulse shaper will be designed in order to reach the minimum total ENC in our system.

3 The Design of the Charge Sensitive Amplifier

3.1 Charge Sensitive Amplifier Circuit Overview

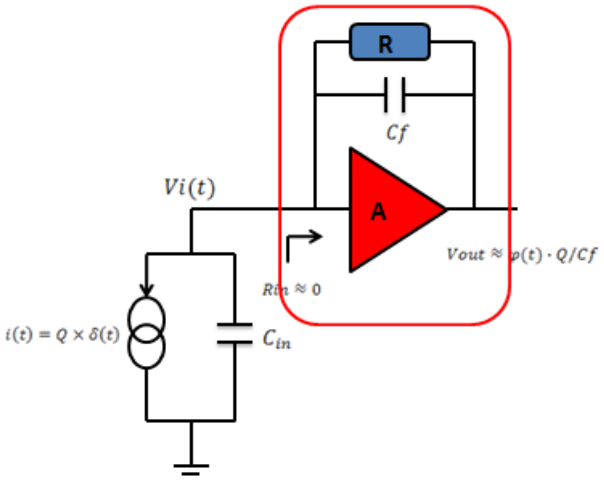

Figure 3.1 Charge Sensitive Amplifier (with the Detector).

Since the charge pulse released by the detector is too small to be processed, it has to be pre-amplified before any signal processing. The input pre-amplification can be performed by using a low input impedance charge sensitive amplifier (CSA). A basic structure of the CSA is shown in Figure 3.1. The CSA is composed of a voltage amplifier A, a feedback capacitor Cf, and a feedback network R. The charge Q released by the detector integrates into the feedback capacitor Cf. The main function of the CSA is to convert input current pulse into an output voltage signal [18]-[22]. If the CSA is assumed to be realized by an ideal voltage amplifier with infinite gain and bandwidth, the output of the CSA is very close to an ideal voltage step.

$$Vo(t) = \varphi(t) \cdot \frac{Q}{Cf}, \text{ where } \varphi(t) = 0 \; for \; t < 0; 1 \; for \; t > 0; \tag{3.1}$$

Due to the Miller effect, the input impedance of the CSA is very low so the current AC pulse mainly flows through the feedback capacitor Cf, as long as $Cl \ll Cf \cdot A_0$, where A_0 is the small signal gain of the voltage amplifier A. The CSA provides a virtual ground at the input node so the virtual ground at the input node stabilizes the potential of the sensor electrode and the operation of the input transistor.

The CSA requires an additional feedback network R for (i) discharging the feedback capacitor Cf after each event is processed; (ii) absorbing the DC leakage current of the detector; (iii) stabilizing the bias points at input and output nodes and the operation of the voltage amplifier A by providing necessary DC feedback.

3.2 Advance Cascade Amplifier Design

3.2.1 Advance Cascade Amplifier

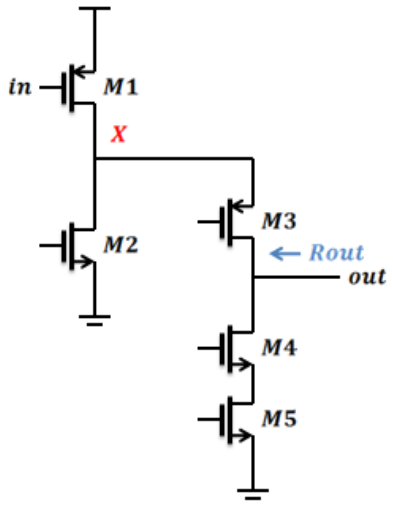

Figure 3.2 Advance Cascade Amplifier

In order to achieve a high voltage gain and wide bandwidth of the voltage amplifier, the voltage amplifier typically can be implemented by an advance cascade amplifier as shown in Figure 3.2. This configuration has several advantages. Since the cascade transistors, M3 and M4, boost the output resistance, the voltage gain of the amplifier is increased. In addition, the current of the output cascade transistors M3, M4, and M5 doesn't need to be the same as the drain current of the input transistor M1. Therefore, the input transistor M1 can operate at relatively high current to achieve high transconductance $gm1$, thus improving the voltage gain. On the other hand, the current of the output cascade transistors can be biased at relatively low current to increase the output resistance $Rout$, thus also increasing overall voltage gain. Usually, the current of the cascade stage is one tenth of the drain current of M1. Furthermore, using the input PMOS transistor instead of NMOS transistor provides lower $1/f$ noise which significantly affects the noise performance of the whole system. However, the note X adds a pole at relatively low frequency so there is a stability issue on the amplifier. It will be discussed more details later. Moreover, the output voltage range of the amplifier is also limited by the cascade configuration.

3.2.2 Input MOS Transistor Optimization

In a properly designed voltage amplifier, the dominant noise sources are only from the input transistor. The other noise sources (e.g. from the cascade, load, etc.) are made negligible. We will now focus our attention on the input transistor. The parameters that directly impact the resolution of the system are input transistor capacitances and the input equivalent noise sources.

MOSFET noise model:

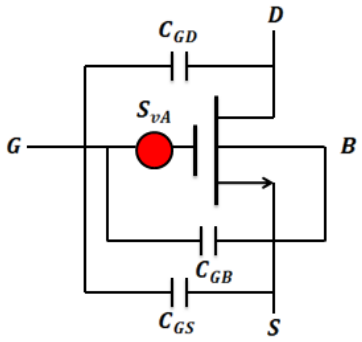

Figure 3.3 MOSFET Noise Model

Figure 3.3 shows the MOSFET noise model with series voltage noise source. Since the shot noise from the detector leakage current is only dependent on the detector and shaper characteristics instead of the design parameters of the CSA, we only should focus on the thermal noise and $1/f$ noise generated from the input transistor in the CSA. The series voltage noise S_{vA} of the thermal noise and of $1/f$ noise can be represented as

$$S_{vA} = \frac{S_{vf}}{f} + \gamma n \frac{4KT}{gm} = \frac{Kf}{Cox \cdot WL \cdot f} + \gamma n \frac{4KT}{g_{mW} \cdot W} \tag{3.2}$$

where n is the subthreshold slope coefficient; γ is the gamma coefficient from $\frac{1}{2}$ (weak inversion) to $\frac{2}{3}$ (strong inversion); Kf is the $1/f$ noise coefficient; Cox is the gate oxide capacitance per unit area; W is the width of the input transistor; L is the length of the input transistor; g_{mW} is g_m per unit W; i_{DW} is i_D per unit W; K is the Boltzman constant; and T is the absolute temperature. Then ENC_V can be expressed as

$$ENC_V{}^2 = \frac{A_{vw}}{\tau_p} \cdot \gamma n \cdot \frac{4KT}{gm} \cdot (Cs + Cg)^2 + 2\pi A_{vf} \cdot \frac{Kf}{Cox \cdot WL} \cdot (Cs + Cg)^2 \tag{3.3}$$

where Cs is the capacitance of the detector, and Cg is the input capacitance of the input transistor. The input transistor can operate in strong inversion, week inversion, and moderate inversion based on inversion coefficient IC. In these three different operation regions, the input transistor can have totally different noise impact on the system. Here, we discuss them separately.

a. Noise analysis in Strong Inversion Operation: (Vgs > Vth ; IC > 10)

The input transistor can work in the strong inversion if the $Vgs > Vth$ or we can determine the work region of the transistor by the inversion coefficient $IC = \frac{i_D}{i_S}$.

$$i_S = 2nV_T{}^2 \mu Cox \frac{W}{L} \rightarrow IC = \frac{i_D}{i_S} = \frac{i_{DW} \cdot L}{2 \cdot n \cdot V_T{}^2 \cdot \mu \cdot Cox} > 10 \tag{3.4}$$

where n is the subthreshold slope coefficient; i_{DW} is i_D per unit W; $W$is the width of the input transistor; L is the length of the input transistor; V_T is the thermal voltage; μ is the mobility of holes in a specific process; and Cox is the gate oxide capacitance per unit area. According to the first term of equation 3.3, we know that the thermal noise is inversely proportional to the transconductance gm. In order to get gm, the drain current i_D of the input transistor at the strong inversion is given by

$$i_D = \frac{1}{2n} \cdot \mu \cdot Cox \cdot \frac{W}{L} \cdot (V_{gs} - V_{th})^2 \tag{3.5}$$

where $V_{th}$is the threshold voltage; n is the subthreshold slope coefficient; μ is the mobility of holes in a specific process; Cox is the gate oxide capacitance per unit area; W is the width of the input transistor; L is the length of the input transistor; and V_{gs} is the gate-source voltage. Then gm can be obtained by

$$gm = g_{mW} \cdot W = W \cdot \sqrt{\frac{2\mu Cox \cdot i_{DW}}{n \cdot L}} \tag{3.6}$$

where g_{mW} is g_m per unit W; W is the width of the input transistor; L is the length of the input transistor; n is the subthreshold slop coefficient; μ is the mobility of holes in a specific process; Cox is gate oxide capacitance per unit area; i_{DW} is i_D per unit W. Furthermore, the input capacitance Cg of the input transistor can be expressed as

$$Cg = Cgs + Cgd + Cgb = Cox \cdot WL \tag{3.7}$$

where Cgs is the gate-source capacitance; Cgd is the gate-drain capacitance; Cgb is the gate-bulk capacitance; Cox is the gate oxide capacitance per unit area; W is the width of the input transistor; and L is the length of the input transistor. Therefore, by putting equation 3.6 and 3.7 into equation 3.2 and 3.3, the series voltage noise S_{vA} and ENC_V in strong inversion can be rewritten as

$$S_{vA} = \frac{Kf}{Cox \cdot WL \cdot f} + \gamma n^{\frac{3}{2}} \cdot \frac{4KT}{W \cdot \sqrt{i_{DW}}} \cdot \sqrt{\frac{L}{2\mu Cox}} \tag{3.8}$$

$$ENC_V{}^2 = 2\pi A_{vf} \cdot \frac{Kf}{Cox \cdot WL} \cdot (Cs + Cox \cdot WL)^2 + \frac{A_{vw}}{\tau_p} \cdot 4KT \cdot \gamma \cdot n^{\frac{3}{2}} \cdot \sqrt{\frac{L}{2\mu Cox \cdot i_{DW}}} \cdot \frac{(Cs+Cox \cdot WL)^2}{W} \tag{3.9}$$

From equation 3.9, the ENC_V can be minimized by properly designing the variables of W, L, τ_p, and i_{DW}. In order to minimize the ENC_V, the length of the input transistor can be selected as minimum length L_{min}, since the white noise term in strong inversion can be minimized. The value of i_{DW} is based on the power specification. The peaking time τ_p is determined by the design of the pulse shaper and is based on the event rate, the charge collection time, and the parallel shot noise from the leakage current of the detector. The transistor gatewidth W has a double effect. On the one hand, increasing the gatewidth Wreduces $1/f$ noise

due to increasing the gate area WL and also decreases the thermal noise due to increasing the $i_{DW} \cdot W$. On the other hand, the increase in the gatewidth W increases ENC_V due to enlarging the input capacitance $Cg = CoxWL$. As a result, an optimal gatewidth W_{opt} must be found for the minimum ENC_V. In our design, the noise and the power is our main concern, but there is trade-off between the power and the noise. In order to choose the proper gate size of the input transistor, we should see ENC_V in two conditions: without and within power constraints.

Without power constraint, $i_{DW} = i_{DWmax}$ at maximum Vgs-Vth, and the length of MOSFET in strong inversion can be selected as the minimum length L_{min} in order to minimize the thermal noise of the input transistor. The equation 3.9 can be rewritten as

$$ENC_V{}^2 = 2\pi A_{vf} \cdot \frac{Kf}{Cox \cdot WL_{min}} \cdot (Cs + Cox \cdot WL_{min})^2 + \frac{A_{vw}}{\tau_p} \cdot 4KT \cdot \gamma \cdot n^{\frac{3}{2}} \cdot \sqrt{\frac{L_{min}}{2\mu Cox \cdot i_{DWmax}}} \cdot \frac{(Cs+Cox \cdot WL_{min})^2}{W} \quad (3.10)$$

For a given i_{DWmax} in equation 3.10, both the white and $1/f$ series noise have a minimum for $= Cs\ (Capacitance\ Matching)\ or\ W = \frac{Cs}{C_{ox}L_{min}}$. The minimum ENC_V in strong inversion can be given by

$$ENC_{Vmin}{}^2 = 4Cs\left(\frac{A_{vw}}{\tau_p} \cdot 4KT \cdot \gamma \cdot n^{\frac{3}{2}} \cdot L_{min}{}^{\frac{3}{2}} \cdot \sqrt{\frac{Cox}{2\mu \cdot i_{DWmax}}} + 2\pi A_{vf} \cdot Kf(i_{DW}, L_{min})\right) \quad (3.11)$$

With Power constraint, if we impose a limit to the dissipated power and choose $i_D = i_{D0}$ according to our power budget, it increases the white series noise but has no impact on $1/f$ noise. The ENC_V can be rewritten as

$$ENC_V{}^2 = 2\pi A_{vf} \cdot \frac{Kf}{Cox \cdot WL_{min}} \cdot (Cs + Cox \cdot WL_{min})^2 + \frac{A_{vw}}{\tau_p} \cdot 4KT \cdot \gamma \cdot n^{\frac{3}{2}} \cdot \sqrt{\frac{L_{min}}{2\mu Cox \cdot i_{D0} \cdot W}} \cdot (Cs + Cox \cdot WL_{min})^2 \quad (3.12)$$

The $1/f$ series noise still has a minimum for $Cg = Cs\ (Capacitance\ Matching)\ or\ W = \frac{Cs}{C_{ox}L_{min}}$ while the white series noise has a minimum for $Cg = \frac{Cs}{3}\ or\ W = \frac{Cs}{3C_{ox}L_{min}}$ in strong inversion.

b. Noise analysis in Weak Inversion Operation: (Vgs < Vth or IC < 0.1)

For applications that have a very tight power budget, it's desirable to bias the transistor in weak inversion, $Vgs < Vth$. The work region of the transistor can also be determined by the inversion coefficient IC.

$$IC = \frac{i_{DW} \cdot L}{2 \cdot n \cdot V_T{}^2 \cdot \mu \cdot Cox} < 0.1 \quad (3.13)$$

where n is the subthreshold slope coefficient; i_{DW} is i_D per unit W; L is the length of the input transistor; V_T is the thermal voltage; μ is the mobility of holes in a specific process; and Cox is the gate oxide capacitance per unit area. According to the first term of equation 3.3, we know

that the thermal noise is inversely proportional to the transconductance gm. In order to get gm, the drain current i_D of the input transistor at the strong inversion is given by

$$i_D = \mu C_{ox} {V_T}^2 \frac{W}{L} e^{\frac{Vgs-Vth}{nV_T}} \tag{3.14}$$

where $V_{th}$is the threshold voltage; n is the subthreshold slope coefficient; μ is the mobility of holes in a specific process; Cox is the gate oxide capacitance per unit area; W is the width of the input transistor; L is the length of the input transistor; V_{gs} is the gate-source voltage; and $V_T$is the thermal voltage. Then gm can be obtained by

$$gm = g_{mW} \cdot W = W \cdot \frac{i_{DW}}{nV_T} \tag{3.15}$$

where g_{mW} is g_m per unit W; W is the width of the input transistor; n is the subthreshold slope coefficient; i_{DW} is i_D per unit W; and V_{th} is the threshold voltage. Furthermore, the input capacitance Cg of the input transistor can be expressed as

$$Cg = Cgs + Cgd + Cgb = Cox \cdot WL \tag{3.6}$$

where Cgs is the gate-source capacitance; Cgd is the gate-drain capacitance; Cgb is the gate-bulk capacitance; Cox is the gate oxide capacitance per unit area; W is the width of the input transistor; and L is the length of the input transistor. Therefore, by putting equation 3.15 and 3.6 into equation 3.2 and 3.3, the series voltage noise S_{vA} and ENC_V in weak inversion can be rewritten as

$$S_{vA} = \frac{Kf}{Cox \cdot WL \cdot f} + \gamma n^2 \cdot \frac{4KT \cdot V_T}{W \cdot i_{DW}} \tag{3.16}$$

$${ENC_V}^2 = 2\pi A_{vf} \cdot \frac{Kf}{Cox \cdot WL_{min}} \cdot (Cs + Cox \cdot WL_{min})^2 + \frac{A_{vw}}{\tau_p} \cdot 4KT\gamma n^2 V_T \cdot \frac{(Cs+Cox \cdot WL_{min})^2}{W \cdot i_{DW}} \tag{3.17}$$

With Power constraint, the input transistor operates in weak inversion because of the tight power budge. The $1/f$ noise still has a minimum for $Cg = Cs\ (Capacitance\ Matching)\ or\ W = \frac{Cs}{C_{ox}L_{min}}$ while the white series noise has a minimum for $W \to 0\ or\ Cg \cong 0$ in week inversion.

c. Noise analysis in Moderate Inversion Operation:

Most of the applications typically impose a limit of less than $\mathbf{1mW}$ per pixel. With these constraints, the input MOSFET operates in a region between strong and weak inversion, known as moderate inversion. In moderate inversion the white series has a minimum for $0 < Cg < \frac{Cs}{3}$. Depending on the relative weight of the 1/f noise contribution, which has a minimum for $Cg = Cs$, the overall minimum is achieved in $0 < Cg < Cs$. The optimization requires an

accurate model in the region of moderate inversion. First, the work region of the input transistor can be determined by the inversion coefficient IC.

$$0.1 < IC = \frac{i_{DW} \cdot L}{2 \cdot n \cdot {V_T}^2 \cdot \mu \cdot Cox} < 10 \tag{3.18}$$

where n is the subthreshold slope coefficient; i_{DW} is i_D per unit W; L is the length of the input transistor; V_T is the thermal voltage; μ is the mobility of holes in a specific process; and Cox is the gate oxide capacitance per unit area. According to the first term of equation 3.3, we know that the thermal noise is inversely proportional to the transconductance gm. g_{mW} is given by

$$gm = g_{mW} \cdot W = W \cdot \frac{i_{DW}}{nV_T} \cdot \frac{\sqrt{1+4 \cdot IC}-1}{2 \cdot IC} = \frac{W \cdot V_T \cdot \mu Cox}{L} \cdot \left(\sqrt{1 + 4 \cdot \frac{i_{DW} \cdot L}{2 \cdot n \cdot {V_T}^2 \cdot \mu \cdot Cox}} - 1 \right) \tag{3.19}$$

where g_{mW} is g_m per unit W; W is the width of the input transistor; n is the subthreshold slope coefficient; i_{DW} is i_D per unit W; L is the length of the input transistor; V_T is the thermal voltage; μ is the mobility of holes in a specific process; and Cox is the gate oxide capacitance per unit area. In addition, Gamma coefficient γ also can be determined by the inversion coefficient IC [29].

$$\gamma = \begin{cases} \frac{2}{3}, IC > 10 \; in \; strong \; inverstion \\ \frac{1}{2}, IC < 0.1 \; in \; weak \; inversion \\ r_{mod}, 0.1 < IC < 10 \; in \; moderate \; inversion \end{cases} \tag{3.20}$$

$$r_{mod} = \frac{1}{1+IC} \cdot \left(\frac{1}{2} + \frac{2}{3} \cdot IC \right) = \frac{1}{1+\frac{i_{DW} \cdot L}{2 \cdot n \cdot {V_T}^2 \cdot \mu \cdot Cox}} \cdot \left(\frac{1}{2} + \frac{2}{3} \cdot \frac{i_{DW} \cdot L}{2 \cdot n \cdot {V_T}^2 \cdot \mu \cdot Cox} \right) \tag{3.21}$$

In addition, in order to get more accurate modeling, the input capacitance Cg of the input transistor can be modeled in a more advanced approach as shown in Figure 3.4.

$$Cg = C_{ox} \cdot WL \rightarrow Cg \approx 2C_{ov}W + \frac{2}{3}C_{ox}WL \tag{3.22}$$

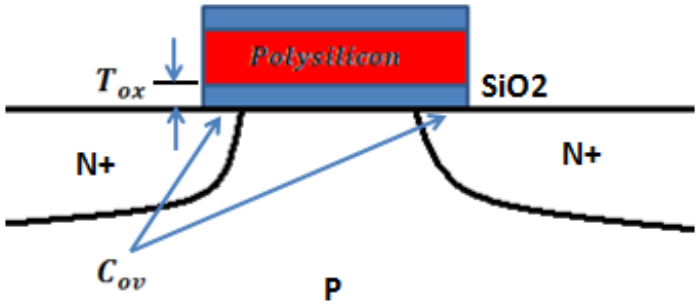

Figure 3.4 Drain-to-Source Overlap Capacitance

where Cov is the drain-to-source overlap capacitance per unit W; Cox is the gate oxide capacitance per unit area; W is the width of the input transistor; and L is the length of the input transistor. Thus, we can put equation 3.19, 3.21, and 3.22 into equation 3.3, and then ENC_V in moderate inversion can be rewritten as

$$ENC_V{}^2 = \left(\frac{A_{vw}}{\tau_p} \cdot r_{mod} \cdot n \cdot \frac{4KT}{gm_{mod}} + 2\pi A_{vf} \cdot \frac{Kf}{Cox \cdot WL_{min}}\right) \cdot \left(Cs + 2C_{ov}W + \frac{2}{3}C_{ox}WL_{min}\right)^2 \quad (3.23)$$

The equations for the optimization of the MOSFET in the moderate inversion are complex. Here, let's review the whole modeling and optimization in the moderate inversion from a more general point of view. We assume that the detector capacitance Cs is given and there is a power P_d constraint for the voltage amplifier. Imposing a constraint on power P_d means imposing a constraint on $i_D = i_{DW} \cdot W$, since $i_D = P_d/Vdd$. The constraint on the time constant τ is dependent on the event rate, the charge collection time, and the parallel shot noise. For given constraints, since the white noise can be minimized by increasing the peaking time $\tau_p = n \cdot \tau$, we assume that ENC_V is dominant by $1/f$ noise. Thus, the $1/f$ series noise has a minimum for $Cg = Cs\ (Capacitance\ Matching)\ or\ W_{opt} = \frac{Cs}{2C_{ov}W + \frac{2}{3}C_{ox}WL_{min}}$ in moderate inversion. In our design, the drain current i_D of the input transistor in the moderate inversion is designed to be 127uA and the optimum gatewidth W_{opt} is designed to be 16.8m. Since the input transistor provides a large power gain, the noise from the input transistor usually contributes more than 80% of the total voltage amplifier noise.

3.2.3 Gain & Bandwidth:

In order to compromise the power and the noise, the input MOSFET can operate in a moderate region. Once we know the power constraint P_D, the drain current of the input transistor can be obtained by $i_D = \frac{P_D}{Vdd}$. In addition, according to the above noise analysis in moderate inversion operation, the optimum width W_{opt} of the input transistor is chosen to be $\frac{Cs}{2C_{ov}W + \frac{2}{3}C_{ox}WL}$ due to capacitance matching, $Cg = Cs$. In addition, the current of the output cascade transistors M3, M4, and M5 doesn't need to be the same as the drain current of the input transistor M1. Therefore, the current of the output cascade transistors can be biased at relatively low current to increase the output resistance ro, thus also increasing overall voltage gain. Usually, the current of the cascade stage is one tenth of the drain current of M1. Therefore, according to above constraints, the transconductance g_{m1} of the input transistor has almost been fixed. If we want to enhance the amplifier gain $A \approx g_{m1} \cdot Rout$ as shown in Figure 3.5, the only thing we can do is to increase the output resistance $Rout$ roughly given by

$$Rout \approx [g_{m3}r_{o3}(r_{o1} \| r_{o2})] \| [g_{m4}r_{o4}r_{o5}] \quad (3.24)$$

Since $g_{m3}r_{o3}(r_{o1}\|r_{o2}) \ll g_{m4}r_{o4}r_{o5}$, $Rout$ is approximated by $g_{m3}r_{o3}(r_{o1}\|r_{o2})$. Therefore, we can try to increase g_{m3} by enlarging W_3 and increase r_{o1}, r_{o2}, r_{o3} by enlarging L_1, L_2, L_3 . Finally, the gain A can be achieved to $80dBm$. However, large W_1 and W_3 causes stability problem on the amplifier. We will discuss this issue later more details.

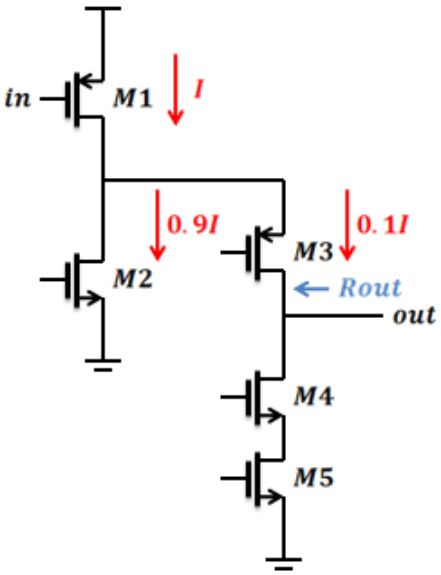

Figure 3.5 Advance Cascade Amplifier

3.2.4 Noise Contribution from Transistors:

Once the input transistor noise is optimized, the noise from other transistors must be minimized as well. Since the noise calculation is complex, we use approximate equations for the noise spectral densities here. First we compute the white noise from each transistor, and then $1/f$ noise as shown in Figure 3.6. First of all, the noise contribution from the cascading transistors $M3\ and\ M4$ is usually negligible [15]. Then, for the current source transistors $M2\ and\ M5$, white noise terms can be minimized by reducing $\gamma \cdot g_m$. Since the higher L reduces $\gamma \cdot g_m$, thus lowing white noise, the length of $M2\ and\ M5$ should be chosen as high as possible. For a given drain current, $M2\ and\ M5$ should operate in strong inversion as well. Next we try to minimize $1/f$ noise by increasing both $L\ and\ W$ of $M2\ and\ M5$ while maintaining a fixed W/L ratio in order to maintain the operating point of $M2\ and\ M5$. Finally, both white and $1/f$ noise in $M2\ and\ M5$ is minimized.

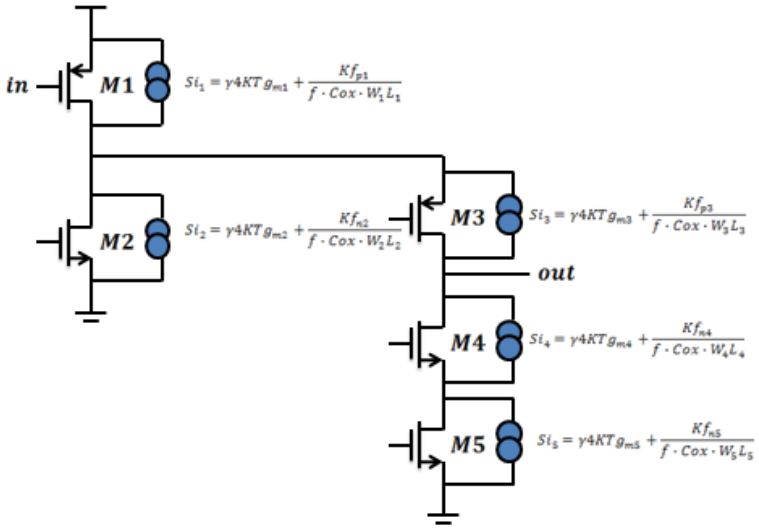

Figure 3.6 Advance Cascade Amplifier with white and $1/f$ noise generators

3.2.5 Adding a Buffer

In Figure 3.7, a source follower is used as a buffer to drive the output and to isolate the sensitive node from the large load capacitance.

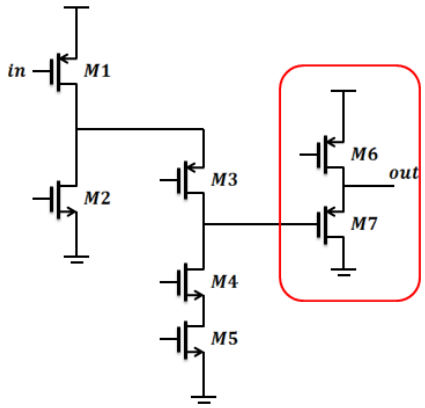

Figure 3.7 Adding a Source Follower, a Buffer

3.2.6 Stability:

Consider the circuit as shown in Figure 3.8. We identify five poles at the input node, the output node, node X, node Y, and node Z. In order to decrease the white noise of the load transistor M_5, L_5 is chosen as a large value and W_5 is chosen as a low value. Plus, the small-signal resistance at node Y is small. Therefore, the pole at node Y locates at relatively high frequency. Furthermore, since the output resistance of the buffer is usually small, the pole at the output node also lies at relatively high frequency, even with a moderate load capacitance C_L at the output node. In addition, since the small-signal resistance at node Z is higher than the small-

signal resistance at the other nodes, even with a moderate compensate capacitance C_X, the pole at node Z is usually the dominant pole in the amplifier. Furthermore, the total capacitance at node X is roughly equal to $Cgd1 + Cdb1 + Cgd2 + Cdb2 + Cgs3 + Csb3$. Since $W1\ and\ W3$ are usually large in our circuit in order to minimize the noise and to increase the gain, the capacitance at node X is quite large. It makes the pole at the node X be a first non-dominant pole and is close to the dominant pole at node Z, so the circuit easily becomes unstable. Thus, one way to solve unstable problem in the circuit is to increase the compensation capacitance C_X at node Z because larger compensation capacitance C_X moves the dominant pole at node Z close to the origin so that it makes the circuit more stable. However, the bandwidth becomes smaller and then the speed of the circuit is decreased. For our design, the chosen value of the compensation capacitance C_X is $2pF$ so the area of the compensation capacitance C_X is quite large in the circuit in order to make the circuit stable.

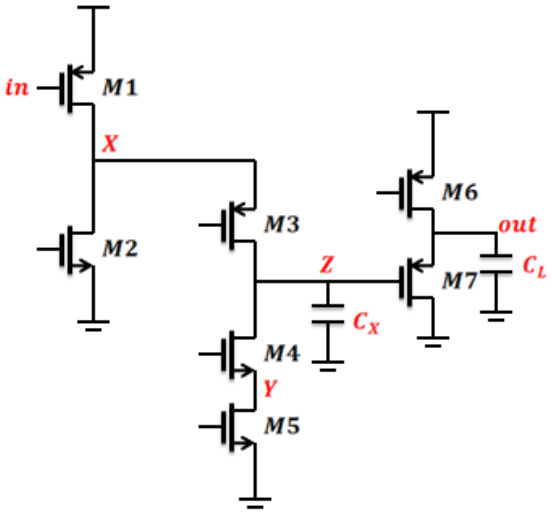

Figure 3.8 Cascade Amplifier with the Load Capacitance C_L

3.3 Reset Network

The reset network R provides the discharge of the feedback capacitor after the measurement. In the low impedance configuration R also provides stabilization of the sensing node and of the voltage amplifier. The reset network can be implemented by using a very large feedback resistor Rf as shown in Figure 3.9. Since the feedback resistor Rf provides a white parallel noise source at the input node of the CSA, the feedback resistor Rf should be very large in order to make its noise contribution negligible. The relationship between the noise from the feedback resistor Rf and the noise from the detector leakage current is shown as following

$$\frac{4KT}{Rf} << 2qI_{leak} \tag{3.25}$$

where K is the Boltzman constant; T is the absolute temperature; i_{leak} is the detect leakage current; and q is the electronic charge released by the detector. However, adding a large feedback resistor Rf has several disadvantages. First, Rf is too big to integrate on the chip due to limited area. Secondly, a large Rf creates a large voltage drop between the input and output nodes of the CSA. This large voltage drop would affect the work region of the transistors and the operation of the voltage amplifier. Third, a larger Rf makes the CSA has a longer time constant due to a larger $RfCf$ value. A Longer time constant leads to a longer discharge time so that the next pulse event would easily pile-up on the previous pulse event.

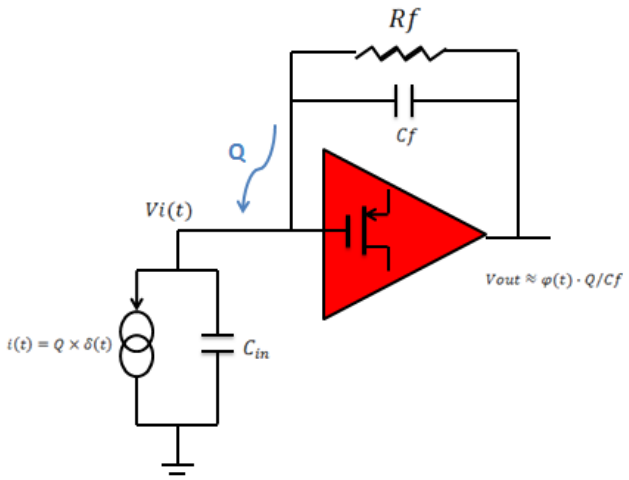

Figure 3.9 CSA with a Feedback Resistor Rf

An alternative is to use a single P channel MOFSFET biased in saturation as shown in Figure 3.10 [23][24]. The area of PMOS transistor is much smaller than the large feedback resistor Rf so it's easier to implement on the chip. The gate terminal of the transistor M_F is connected to a fixed biasing voltage. This biasing voltage should be chosen in order to make M_F in saturation (strong inversion) so that the PMOS transistor M_F in strong inversion has less noise contribution. The length of the transistor M_F should be selected very long, $\frac{L}{W} \gg 1$, so that the PMOS transistor M_F can easily operate in strong inversion by the given drain current. In addition, The PMOS transistor M_F can absorb the leakage current from the detector and provide the discharge of the feedback capacitor after the measurement. However, because of the nonlinear dependence of i_D and v_{gs}on M_F , the time dependence of the discharge of the output node doesn't show a simply exponential behavior, as in the case of the feedback resistor Rf. Therefore, a compensation circuit has to be used in order to minimize the non-linearity.

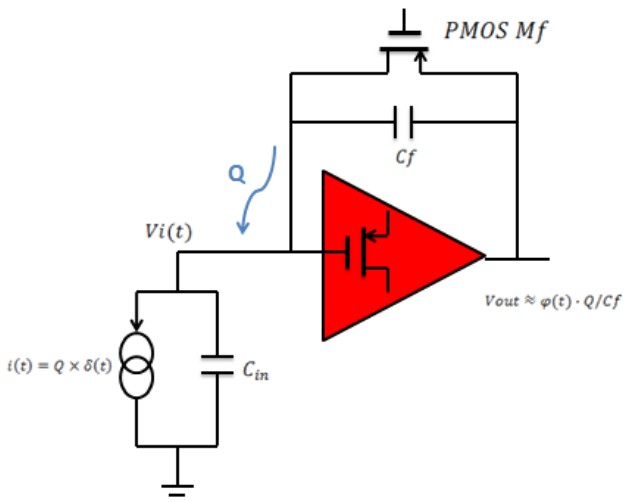

Figure 3.10 CSA with a Feedback PMOS Transistor

3.4 Compensation Circuit

The reset system with the compensation circuit is shown in Figure 3.11. The compensation is based on the use of a second PMOS transistor M_z in parallel to the second capacitor C_z. The source and the gate terminals of PMOS M_z are connected respectively to the source and the gate terminals of PMOS M_F. The drain terminal of PMOS M_z must be connected to the input of the pulse shaper in the next stage. In order to achieve the compensation, the length and width of PMOS M_z must respectively satisfy the conditions: $L_z = L_F and\ W_z = NW_F$, where N is the ratio of $\frac{C_z}{C_F}$. Therefore, the compensation circuit cancels the additional zero created by the feedback reset network. If these conditions are satisfied, the drain current of PMOS M_z is N times the drain current of PMOS M_F. And the charge Q_{out} produced by C_z is N times the charge Q_{in} generated from the detector, $Q_{out} = N \cdot Q_{in}$.

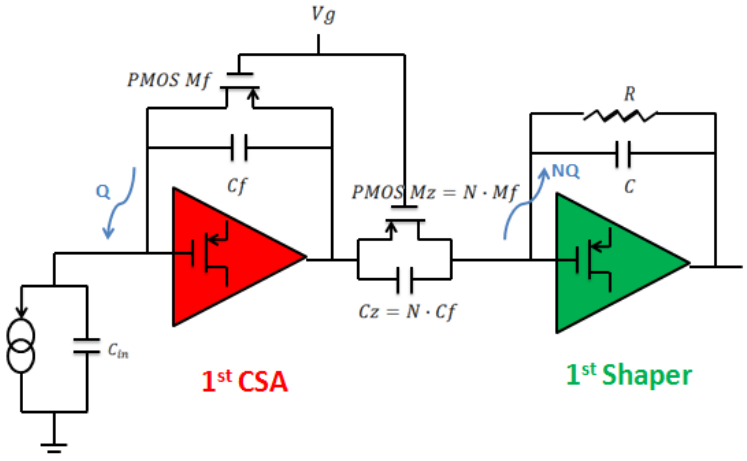

Figure 3.11 CSA with a Compensation Circuit

3.5 Two Stages of CSA

In Figure 3.12, a second CSA stage is added in order to the increase signal-to-noise ratio at the output of the pulse shaper. The compensation networks are composed by PMOS M_{Z1} parallel to C_{Z1} in the first stage and NMOS M_{Z2} parallel to C_{Z2} in the second stage. The source and the gate terminals of NMOS M_{Z2} are connected respectively to the source and the gate terminals of NMOS M_{f2}. The drain terminal of NMOS M_{Z2} must be connected to the input of the pulse shaper in the next stage. In order to achieve the compensation, the length and width of NMOS M_{Z2} must respectively satisfy the conditions: $L_{Z2} = L_{f2} and\ W_{Z2} = N_2 W_{f2}$, where N_2 is the ratio of $\frac{C_{Z2}}{C_{f2}}$. If these conditions are satisfied, the drain current of NMOS M_{Z2} is N_2 times the drain current of NMOS M_{f2}. Therefore, the drain current of NMOS M_{Z2} is $N_1 \cdot N_2$ times the drain current of PMOS M_{f1}. And the charge Q_{out} produced by C_{Z2} is N_2 times the charge Q_{in2} produced by C_{Z1}, $Q_{out} = N_2 \cdot Q_{in2}$. Therefore, the overall gain is $N_1 \cdot N_2 = \frac{Q_{out}}{Q_{in}}$. In our design, $N_1 = N_2 = 10$ so the overall gain is 100. The input charge released by the detector is amplified by 100 times.

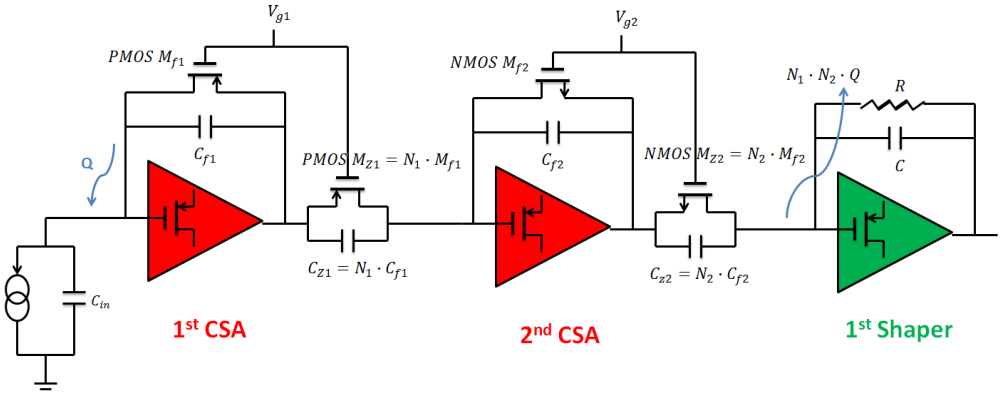

Figure 3.12 Two Stages CSA

3.6 The Simulation of CSA

The circuit is designed under AMI $0.6\mu m$ CMOS technology and the supply voltage is $3.3V$. This is simulated by using a Cadence Spectre simulator and BSIM3v3 transistor models.

3.6.1 AC Simulation of the Cascade Amplifier with the Buffer:

Figure 3.13 below shows the schematic of the cascade amplifier. Table 3.1 lists the size of each transistor and the capacitor values in the cascade amplifier. First, the power dissipation of the CSA is limited within $1mW$ so the current of the input PMOS transistor should be controlled at less than $300\mu A$. Therefore, we controlled our input transistor current at $127\mu A$ which is less than $300\mu A$ so that the total power dissipation can be minimized at $0.50787mW$

which is less than $1mW$. Furthermore, the input PMOS transistor is chosen to operate in the moderate inversion, $0.1 < IC < 10$, due to compromise the power and the noise. In the moderate inversion, the value of the input gate capacitance C_g should be chosen as less than the value of the detector parasitic capacitance C_S depending on the relative weight of $1/f$ series noise contribution and white series noise contribution. In our design, the optimum gatewidth size and the length size of the PMOS input transistor are chosen as $16.8m$ and $1.2u$ so that the value of the input gate capacitance C_g is about $22pF$, which is less than $50pF$ of the detector parasitic capacitance C_S. Since the size and the current of the input PMOS transistor have been fixed, the transconductance $g_m$of the input PMOS transistor has also been fixed. In addition, the buffer does not provide any additional voltage gain. Therefore, in order to enhance the voltage gain of the amplifier, we can try to increase the small signal resistance ro at node Z. The small signal resistance ro at node Z can be increased by increasing g_{m3}, r_{o1}, r_{o2}, and r_{o3}. Finally, the gain of the amplifier can reach 82.28 dBm as shown in Figure 3.16.

Figure 3.14 also shows the phase of the amplifier. Since the first non-dominant at node X is close to the dominant pole at node Z, it easily makes the amplifier unstable so we add a compensation capacitor C_X at node Z in order to stabilize the amplifier. The value of the compensation capacitor C_X is chosen as $2pF$ so that the phase margin can be achieved to $31.236°$.

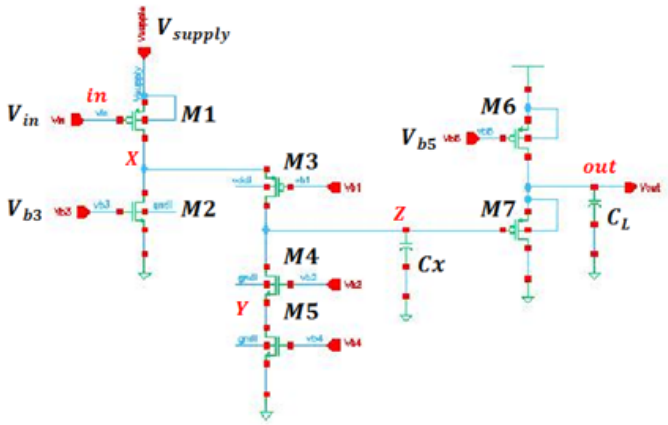

Figure 3.13 The Schematic of the Advanced Cascade Amplifier

W/L PMOS M1	16.8 m / 1.2 μ	V_{supply}	2.5 V
W/L NMOS M2	90 μ / 21 μ	V_{in}	1.65 V
W/L PMOS M3	130 μ / 1.2 μ	V_{b1}	1.2 V
W/L NMOS M4	90 μ / 0.6 μ	V_{b2}	1 V
W/L NMOS M5	30 μ / 12 μ	V_{b3}	1.4 V
W/L PMOS M6	24 μ / 2.4 μ	V_{b4}	0.9 V
W/L PMOS M7	60 μ / 0.6 μ	V_{b5}	2 V
C_X	2 pF	C_L	1 pF

Table 3.1 The Sizes of the Transistors, Capacitors, and Bias Voltage

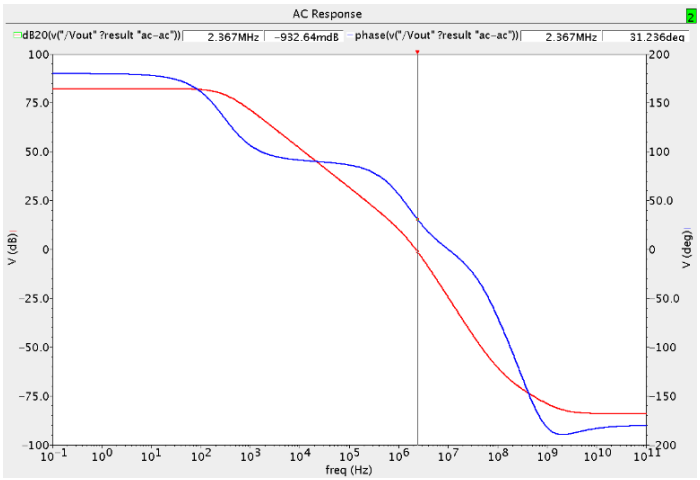

Figure 3.14 DC Gain and Phase of the Advanced Cascade Amplifier

3.6.2 Noise Simulation of the Cascade Amplifier with the Buffer:

Once the size of the input PMOS transistor is optimized, other transistors in the amplifier also need to be given proper values in order to minimize the noise. Figure 3.15 shows the noise simulation of the amplifier. The total output noise of the amplifier is calculated at $7.58215\mu V^2$.

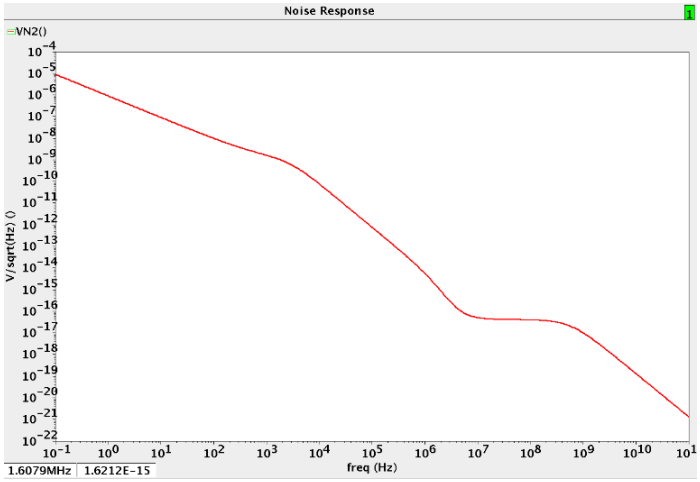

Figure 3.15 Noise Response of the Amplifier

3.6.3 Transient Simulation of 2 Stage CSA:

Figure 3.16 below shows the schematic of the 2 stages of the CSA. Table 3.2 lists the sizes of transistors, the values of capacitors, and the bias voltage in the 2 stage CSA. Adding one more stage of the CSA can improve the signal-to-noise ratio at the output of the pulse shaper. In addition, the compensation networks, composed of PMOS M_{Z1} parallel to C_1 in the first stage and NMOS M_{Z2} parallel to C_2 in the second stage, are used to improve the linearity problem

caused by the feedback transistors PMOS M_{f1} and NMOS M_{f2}. Moreover, the drain current of NMOS M_{Z2} is 100 times the drain current of PMOS M_{f1} and the output charge Q_{out} is 100 times the input charge Q_{in} generated by the detector. Therefore, the overall gain is $N_1 \cdot N_2 = 100$. Figure 3.17 shows the transient simulation of the 2 stages of the CSA by giving 625K input electrons which is about a $100fC$ input charge.

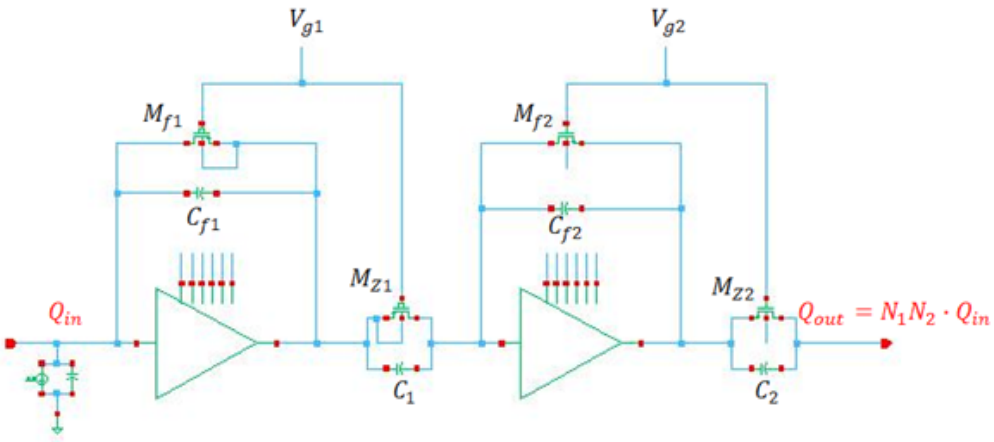

Figure 3.16 The Schematic of 2 Stages CSA

W/L PMOS M_{f1}	1.5 μ / 30 μ	W/L NMOS M_{f2}	1.8 μ / 60 μ
W/L PMOS M_{Z1}	15 μ / 30 μ	W/L NMOS M_{Z2}	18 μ / 60 μ
C_{f1}	$1pF$	C_{f2}	$1pF$
C_1	$10pF$	C_2	$10pF$
V_{g1}	0.8 V	V_{g2}	3.1 V
$N_1 = C_{f1}/C_1$	10	$N_2 = C_{f2}/C_2$	10

Table 3.2 The Sizes of the Transistors, Capacitors, and Bias Voltage

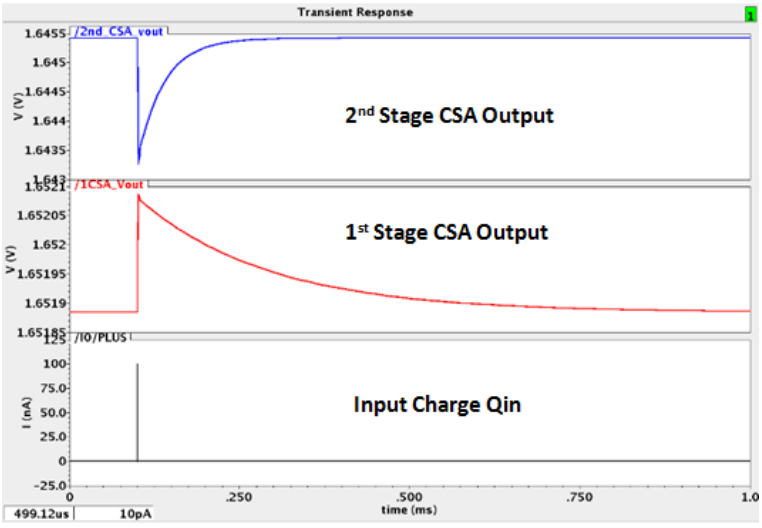

Figure 3.17 The Transient Simulation of 2 Stages CSA

3.6.4 Noise Simulation of 2 Stage CSA:

Figure 3.18 shows the noise response of the 2 stages of the CSA. The noise contribution from PMOS M_{Z1} and NMOS M_{Z2} in the compensation networks is negligible. Since the feedback transistor PMOS M_{f1} in the first stage and the feedback transistor NMOS M_{f2} in the second stage are biased at the strong inversion, the noise contribution from M_{f1} and M_{f2} can be minimized. Even though the feedback transistors M_{f1} and M_{f2} contribute some noise, the total output noise contribution from the input transistor of the amplifier is still dominant in the CSA. Therefore, the total output noise of the 2 stage CSA is calculated at $1.209393\mu V^2$ integrated from 0.1 to 100GHz.

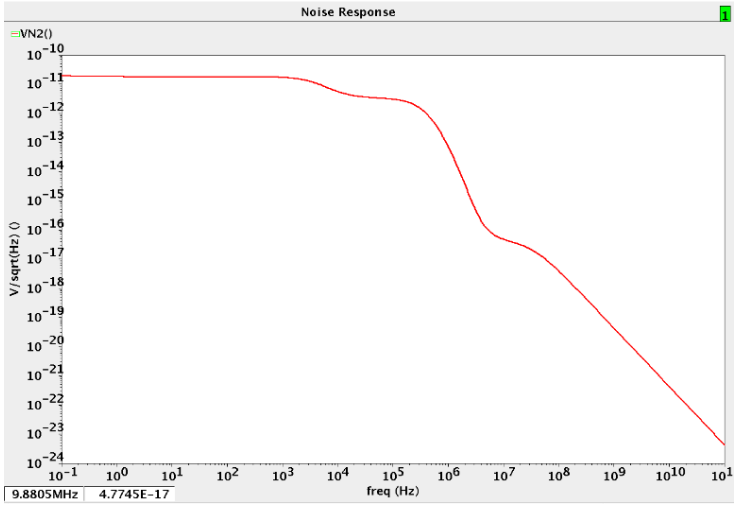

Figure 3.18 Noise Response of 2 Stages CSA

4 The Design of the Pulse Shaper

4.1 Semi-Gaussian Pulse Shaping Filter Overview

The primary function of the pulse shaper is to shape the output signal from the preamplifier in order to optimize the signal-to-noise ratio at the output of the shaper. In addition, the pulse shaper should operate properly at a high counting rate without degrading resolution. The most common pulse shaper employed in the radiation detector system is the semi-Gaussian pulse shaper achieved by one CR differentiator and n RC integrators [4]-[9]. A differentiator, a high-pass filter, sets the duration of the pulse by introducing a decay time constant τ, and an integrator, a low-pass filter, increases the rise time to limit the noise bandwidth. The transfer function of a semi-Gaussian pulse shaper is given by

$$H(s) = \left[\frac{s\tau}{1+s\tau}\right]\left[\frac{A}{1+s\tau}\right]^n \tag{4.1}$$

where τ is the time constant of the differentiator and integrators; A is the DC gain of the integrator; the order n of the semi-Gaussian shaper is determined by the number of real coincident poles. According to the noise analysis in the previous sections, the white noise ENC_{ws}, the $1/f$ noise $ENC_{1/f}$, and the shot noise $ENC_{wp}$are completely independent of the DC gain A of the integrators. Therefore, both the time constant τ and the order n of the semi-Gaussian shaper should be optimized in order to achieve the lowest ENC in the circuit. Before we start to design the pulse shaper, it's better to understand all design parameters first.

4.2 Pulse Shaper Design Parameters

4.2.1 The Order n of the Pulse Shaper:

The semi-Gaussian pulse shaper is composed of one CR differentiator and n RC integrators. The order n of the pulse shaper depends on the number of real coincident poles. Total ENC decreases as the order n of the pulse shaper increases since the output pulse signal gets more symmetrical and it approaches the Gaussian shape as shown in Figure 4.1. However, a higher order of the shaper, which is composed of more integrators, consumes more power and area in the circuit. Thus, we should determine the optimum order of the pulse shaper based on our power budget, the circuit area, and the total ENC requirement.

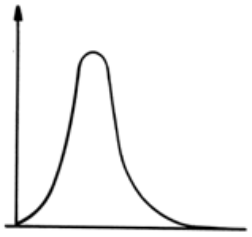

Figure 4.1 A Typical Gaussian Shaped Signal

According to our noise analysis in previous sections, we are mainly dealing with the equivalent white series noise ENC_{ws} due to the thermal noise of the input transistor, the equivalent $1/f$ series noise $ENC_{1/f}$ due to $1/f$ noise of the input transistor, and the equivalent white parallel noise ENC_{wp} due to the shot noise of the detector leakage current. Thus, the total ENC^2 can be given by

$$ENC^2 = \frac{\int_0^\infty Siw \cdot |H(f)|^2 df + \int_0^\infty (Svw + \frac{Svf}{f}) \cdot \omega^2 \cdot Cin^2 \cdot |H(f)|^2 df}{h_{max}{}^2} \tag{4.2}$$

$$h_{maz} = h(t_{max}) = \frac{V_O(t_{max})}{Q} \tag{4.3}$$

where Siw is the power spectral density of the shot noise due to the detector leakage current; $Svw\ and\ Svf$ are the power spectral density of the white noise and $1/f$ noise from the input transistor; f is the frequency of the signal; $C_{in} = C_s + C_f + C_A$ is the total input capacitance; $H(f)$is the transfer function of the whole system; h_{max} is the function of the whole system operating at t_{max}. First of all, we can consider the first case of an unfiltered charge amplifier as shown in Figure 4.2. The output voltage $Vout(t)$ and its Fourier transfer $Vout(f)$ can be given by

$$Vout(t) = Q \cdot h(t) = Q \cdot \frac{1}{C_f}\varphi(t), where\ \varphi(t) = 0\ for\ t < 0; 1\ for\ t \geq 0 \tag{4.4}$$

$$Vout(f) = Q \cdot H(f) = Q \cdot \frac{1}{j2\pi f \cdot C_f} \tag{4.5}$$

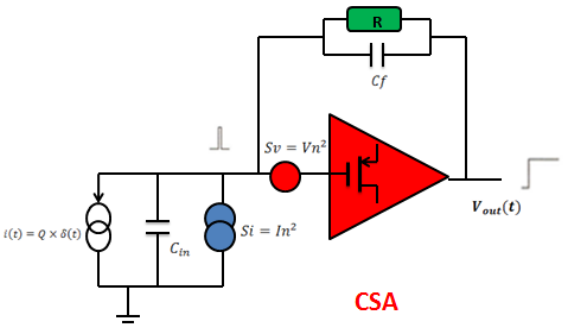

Figure 4.2 An Unfiltered Charge Amplifier

where Q is the input charge; C_f is the feedback capacitance of the CSA; $h(t)$ is the function of the whole system; $H(f)$ is the transfer function of the whole system. We can put $H(f)$ into equation 4.2 to get ENC^2 as below.

$$ENC^2 = \frac{\int_0^\infty Siw\cdot|H(f)|^2df+\int_0^\infty(Svw+\frac{Svf}{f})\cdot\omega^2\cdot Cin^2\cdot|H(f)|^2df}{h_{max}{}^2} = Siw\cdot\frac{1}{4\pi^2}\cdot\int_0^\infty\frac{1}{f^2}df + Svw\cdot Cin^2\cdot\int_0^\infty df +$$
$$Svf\cdot Cin^2\cdot\int_0^\infty\frac{1}{f}df = \infty+\infty+\infty,\ where\ H(f) = \frac{1}{j2\pi f\cdot C_f} \quad (4.6)$$

According to the above equation 4.6, the parallel white noise Siw, the series white noise Sv, and the series $1/f$ noise Svf become infinite. Thus, we consider to add a one real coincident pole shaper with the time constant τ after the CSA as shown in Figure 4.3. The output voltage $Vout(t)$ and its Fourier transfer $Vout(f)$ can be given by

$$Vout(t) = Q\cdot h(t) = Q\cdot H_0\cdot e^{\frac{-t}{\tau}}, where\ H_0 = h(t_{max}) \quad (4.7)$$

$$Vout(f) = Q\cdot H(f) = Q\cdot\frac{H_0\cdot\tau}{1+jw\tau}, where\ H_0 = h(t_{max}) \quad (4.8)$$

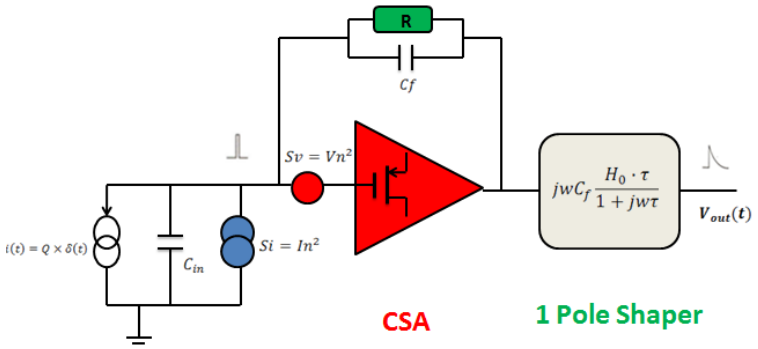

Figure 4.3 One Real Coincident Pole Shaper with Time Constant τ

where Q is the input charge; τ is the time constant; $h(t)$ is the function of the whole system; $h(t_{max})$ is the function of the whole system operating at t_{max}; $H(f)$ is the transfer function of the whole system. We can put $H(f)$ into equation 4.2 to get ENC^2 as below.

$$ENC^2 = \frac{\int_0^\infty Siw\cdot|H(f)|^2df+\int_0^\infty(Svw+\frac{Svf}{f})\cdot\omega^2\cdot Cin^2\cdot|H(f)|^2df}{h_{max}{}^2} = Siw\cdot\frac{\tau}{4} + Svw\cdot\frac{Cin^2}{2\pi\tau}\cdot\int_0^\infty\frac{x^2}{1+x^2}dx + Svf\cdot Cin^2\cdot$$
$$\int_0^\infty\frac{x}{1+x^2}dx = Si\cdot\frac{\tau}{4}+\infty+\infty,\ where\ H(f) = \frac{H_0\cdot\tau}{1+jw\tau} \quad (4.9)$$

According to the above equation 4.9, the parallel noise Siw contribution is proportional to the time constant τ of the pulse shaper but the series noise Svw and Svf contribution are still infinite. Thus, we consider to add a two real coincident poles shaper with the time constant τ after the CSA as shown in Figure 4.4. The output voltage $Vout(t)$ and its Fourier transfer $Vout(f)$ can be given by

$$Vout(t) = Q \cdot h(t) = Q \cdot H_0 \cdot \frac{t}{\tau} \cdot e^{\frac{-t}{\tau}}, where\ H_0 = e \cdot h(t_{max}) at\ t_{max} = \tau \quad (4.10)$$

$$Vout(f) = Q \cdot H(f) = Q \cdot \frac{H_0 \cdot \tau}{(1+jw\tau)^2},\ where\ H_0 = e \cdot h(t_{max}) at\ t_{max} = \tau \quad (4.11)$$

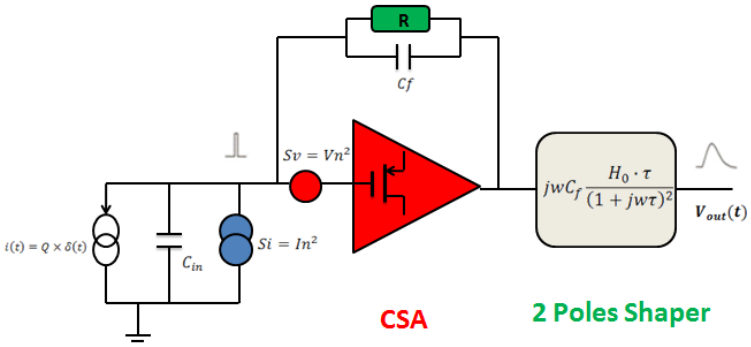

Figure 4.4 Two Real Coincident Poles Shaper with Time Constant τ

where Q is the input charge; τ is the time constant; $h(t)$ is the function of the whole system; $h(t_{max})$ is the function of the whole system operating at t_{max}; $H(f)$ is the transfer function of the whole system. We can put $H(f)$ into equation 4.2 to get ENC^2 as below.

$$ENC^2 = \frac{\int_0^\infty Siw \cdot |H(f)|^2 df + \int_0^\infty (Svw + \frac{Svf}{f}) \cdot \omega^2 \cdot Cin^2 \cdot |H(f)|^2 df}{h_{max}{}^2} = Siw \cdot \tau \cdot \frac{e^2}{8} + Svw \cdot \frac{Cin^2}{\tau} \cdot \frac{e^2}{8} + Svf \cdot Cin^2 \cdot \frac{e^2}{2} =$$

$$A_{iw} \cdot Si \cdot \tau + A_{vw} \cdot Sv \cdot \frac{Cin^2}{\tau} + A_{vf} \cdot Svf \cdot 2\pi \cdot Cin^2,\ where\ H(f) = \frac{H_0 \cdot \tau}{(1+jw\tau)^2} \quad (4.12)$$

where A_{iw} is the parallel white noise coefficient; A_{vw} is the series white noise coefficient; and A_{vf} is the series $1/f$ noise coefficient. According to the above equation 4.12, the parallel white noise Siw contribution is proportional to the time constant τ of the pulse shaper; the series white noise Svw contribution is proportional to the square of the input capacitance C_{in} and inversely proportional to the time constant τ; the series $1/f$ noise Svf contribution is proportional to the square of the input capacitance C_{in} and independent of the time constant τ. Therefore, in order to minimize the parallel noise and the series noise, the pulse shaper should be designed to be at least 2nd order of the shaper, composed of one CR differentiator and one RC integrator. Here, let's see whether ENC decreases or not if the order n of the shaper is increased. Thus, we consider to add a n real coincident poles shaper with the time constant τ after the CSA as shown in Figure 4.5 [29]. The output voltage $Vout(t)$ and its Fourier transfer $Vout(f)$ can be given by

$$Vout(t) = Q \cdot h(t) = Q \cdot \frac{H_0}{(n-1)!} \cdot \left(\frac{t}{\tau}\right)^{n-1} \cdot e^{\frac{-t}{\tau}}, where\ H_0 = e^{n-1} \cdot \frac{(n-1)!}{(n-1)^{n-1}} h(t_{max})\ at\ t_{max} = \tau \cdot (n-1) \quad (4.13)$$

$$Vout(f) = Q \cdot H(f) = Q \cdot \frac{H_0 \cdot \tau}{(1+jw\tau)^n},\ where\ H_0 = e^{n-1} \cdot \frac{(n-1)!}{(n-1)^{n-1}} h(t_{max})\ at\ t_{max} = \tau \cdot (n-1) \quad (4.14)$$

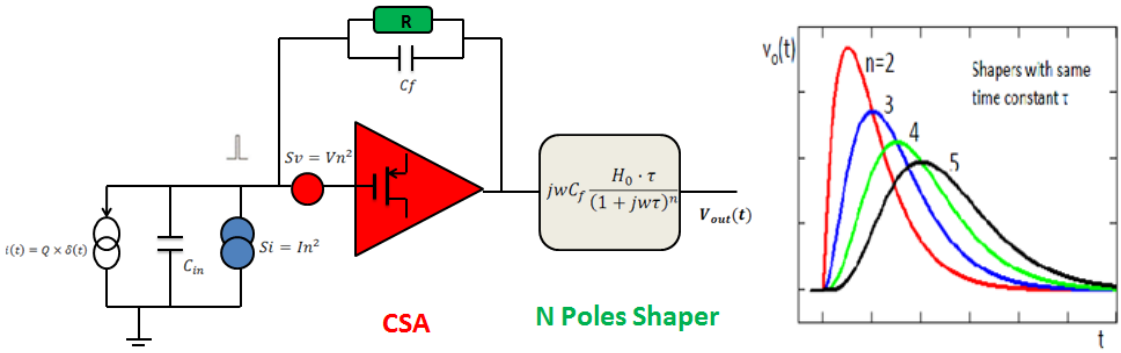

Figure 4.5 N Real Coincident Poles Shaper with Time Constant τ

Then, we can put $H(f)$ into equation 4.2 to get ENC^2 as below.

$$ENC^2 = \frac{\int_0^\infty Siw\cdot|H(f)|^2df+\int_0^\infty(Svw+\frac{Svf}{f})\cdot\omega^2\cdot Cin^2\cdot|H(f)|^2df}{h_{max}{}^2} = A_{iw}\cdot Si\cdot\tau + A_{vw}\cdot Sv\cdot\frac{Cin^2}{\tau} + A_{vf}\cdot Svf\cdot 2\pi\cdot Cin^2,\ where\ H(f) = \frac{H_0\cdot\tau}{(1+jw\tau)^n} \quad (4.15)$$

According to the above equation 4.15 and complex calculations, we made a Table 4.1 [29] as below and summarized the relationship between the order n of the pulse shaper and the coefficients $A_{iw}, A_{vw}, and\ A_{vf}$.

	n =2	n =3	n =4	n =5
A_{iw}	0.924	1.28	1.556	1.791
A_{vw}	0.924	0.425	0.311	0.256
A_{vf}	0.59	0.54	0.53	0.52

Table 4.1 Coefficients for ENC v.s. the Order n of the Shaper at Equal Time Constant τ

At the equal time constant τ, Table 4.1 shows that the parallel white noise coefficient A_{iw} increases with increasing n; the series white noise coefficient A_{vw} decreases with the increasing n; the series $1/f$ noise coefficient A_{vf} decreases slightly with the increasing n. Thus, the total ENC with the n real coincident poles shaper also can be shown in Figure 4.6 [29].

Figure 4.6 shows that ENC_{min} decreases as the order n of the shaper increases and the output pulse become more symmetric and flatter. However, ENC_{min} doesn't improve much when the order n of the shaper is above 5. Therefore, the order n of the shaper should be chosen between 2 and 5 according to our power budget and total ENC requirement. If we want to achieve lower ENC, we can choose to use the 5^{th} order shaper but it consumes more power and area. On the other hand, if the power is our first concern, we can choose to use the 2nd order shaper but get higher ENC.

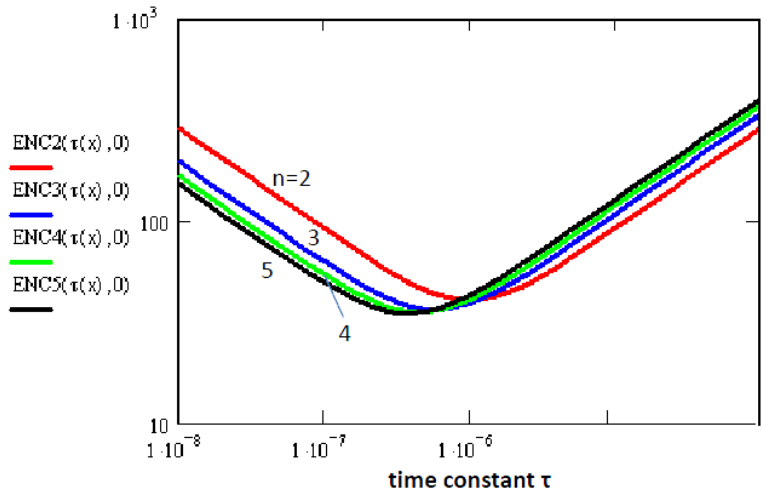

Figure 4.6 Total ENC with n Real Coincident Poles Shaper v.s. the Time Constant τ

4.2.2 Time Constant τ:

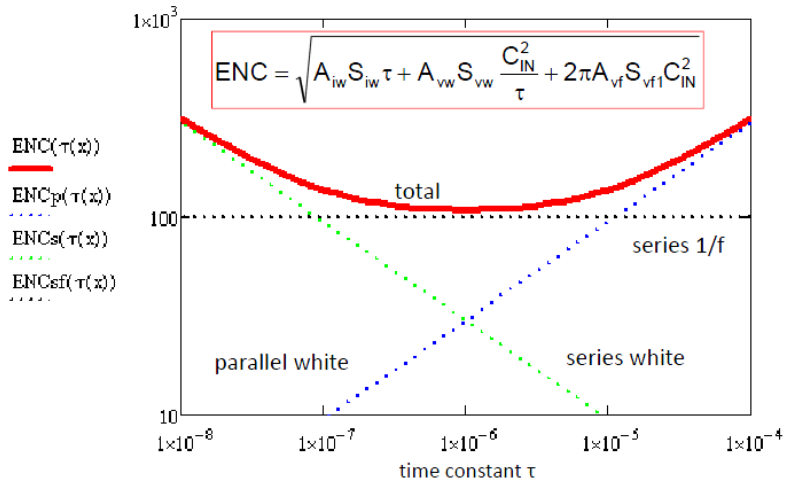

Figure 4.7 Total ENC v.s. Time Constant $\boldsymbol{\tau}$

The time constant $\boldsymbol{\tau}$ is one of the most important design parameters when we design the pulse shaper. The time constant $\boldsymbol{\tau}$ can be determined by the RC value of the differentiator and the integrator. Changing the time constant $\boldsymbol{\tau}$ of the shaper changes the noise bandwidth so it will affect the noise level, but it also affects the signal amplitude. Here, we design the pulse shaper with real coincident poles so that the time constant $\boldsymbol{\tau}$ of the CR differentiator and the RC integrators are equal. In Figure 4.7 [29], the parallel white noise Siw contribution is proportional to the time constant τ of the pulse shaper; the series white noise Svw contribution is inversely proportional to the time constant τ; the series $1/f$ noise Svf contribution is independent of the time constant τ. Therefore, the minimum ENC can be found when the ENC_{iw} and ENC_{vw} are equal at the optimum time constant τ_{opt}.

a. Peaking Time τ_p:

The shapers also can be defined as a more visible parameters, like the peaking time τ_p. The peaking time τ_p is defined as the time from 1% to 100% of the pulse amplitude as shown in Figure 4.8. The total ENC can be rescaled as function of the peaking time τ_p as follows:

$$ENC^2 = A_{iw}S_{iw}\tau_p\frac{\tau}{\tau_p} + A_{vw}S_{vw}\frac{Cin^2}{\tau_p}\frac{\tau_p}{\tau} + 2\pi A_{vf}S_{vf}Cin^2 = A_{iwp}S_{iw}\tau_p + A_{vwp}S_{vw}\frac{Cin^2}{\tau_p} + 2\pi A_{vf}S_{vf}Cin^2,\ where\ A_{iwp} = A_{iw}\frac{\tau}{\tau_p}\ and\ A_{vwp} = A_{vw}\frac{\tau_p}{\tau} \quad (4.16)$$

According to above equation 4.16, we made a Table 4.2 [29] to compare the performance of different order n of the shaper at the equal peaking time τ_p.

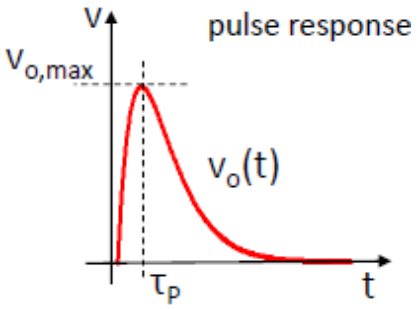

Figure 4.8 The $V_{out}(t)$ Pulse Response with the Peaking Time τ_p

	n =2	n =3	n =4	n =5
τ_p/τ	1	1.924	2.741	3.469
$A_{iwp} = A_{iw}\frac{\tau}{\tau_p}$	0.924	0.665	0.568	0.516
$A_{vwp} = A_{vw}\frac{\tau_p}{\tau}$	0.924	0.822	0.852	0.888
A_{vf}	0.59	0.54	0.53	0.52

Table 4.2 Coefficients for ENC v.s. the Order n of the Shaper at Equal Peaking Constant τ_p

At the equal peaking time τ_p, Table 4.2 shows that the parallel white noise coefficient A_{iwp} decreases with increasing n; the series white noise coefficient A_{vwp} is almost constant with the increasing n; the series $1/f$ noise coefficient A_{vf} slightly decreases with the increasing n. Thus, the total ENC and the $Vout(t)$ pulse with the n real coincident poles shaper at the same peaking time τ_p also can be shown in Figure 4.9 and 4.10 [29].

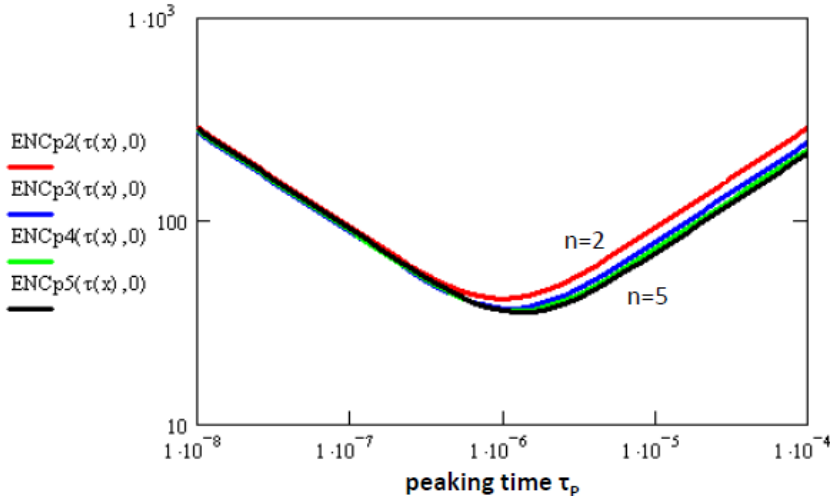

Figure 4.9 Total ENC with n Real Coincident Poles Shaper v.s. the Peaking Time τ_p

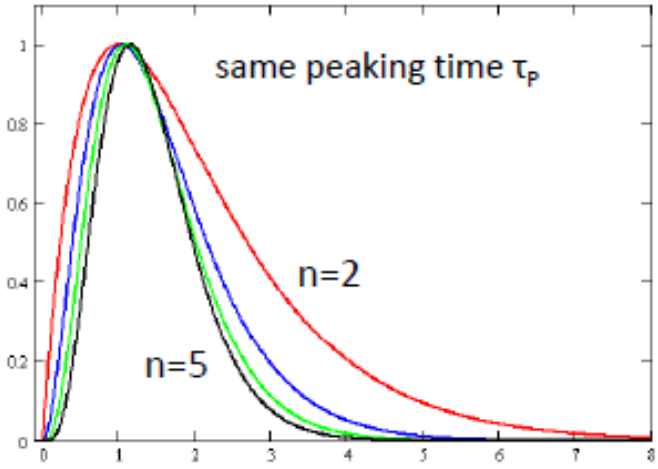

Figure 4.10 $Vout(t)$ Pulse Response with the Same Peaking Time τ_p v.s. the Order n of the Shaper

b. Pulse Width τ_w:

The shapers also can be defined as a more visible parameters, like the pulse width τ_w. The pulse width τ_w is defined as the measure at the two 1% of the full pulse amplitude. The total ENC can be rescaled as the function of the pulse width $\tau_w$as follows:

$$ENC^2 = A_{iw}S_{iw}\tau_w\frac{\tau}{\tau_w} + A_{vw}S_{vw}\frac{Cin^2}{\tau_w}\frac{\tau_w}{\tau} + 2\pi A_{vf}S_{vf}Cin^2 = A_{iww}S_{iw}\tau_w + A_{vww}S_{vw}\frac{Cin^2}{\tau_w} + 2\pi A_{vf}S_{vf}Cin^2,\ where\ A_{iww} = A_{iw}\frac{\tau}{\tau_w}\ and\ A_{vww} = A_{vw}\frac{\tau_w}{\tau} \quad (4.17)$$

According to above equation 4.17, we made a Table 4.3 [29] to compare the performance of different order n of the shaper at the equal pulse width τ_w.

	n =2	n =3	n =4	n =5
τ_w/τ	7.49	9.697	11.43	12.9
$A_{iww} = A_{iw}\frac{\tau}{\tau_w}$	0.123	1.132	1.136	1.39
$A_{vww} = A_{vw}\frac{\tau_w}{\tau}$	6.921	4.121	3.555	3.3
A_{vf}	0.59	0.54	0.53	0.52

Table 4.3 Coefficients for ENC v.s. the Order n of the Shaper at Equal Pulse Width τ_w

At the equal pulse width τ_w, Table 4.3 shows that the parallel white noise coefficient A_{iww} is almost constant with increasing n; the series white noise coefficient A_{vww} decreases with the increasing n; the series $1/f$ noise coefficient A_{vf} slightly decreases with the increasing n. Thus, the total ENC and the $Vout(t)$ pulse with the n real coincident poles shaper at the same pulse width τ_w also can be shown in Figure 4.11 and 4.12 [29].

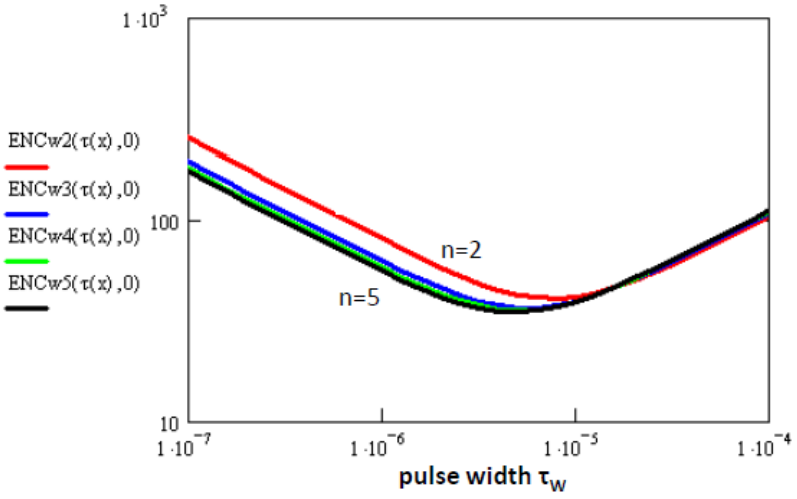

Figure 4.11 Total ENC with n Real Coincident Poles Shaper v.s. the Pulse Width τ_w

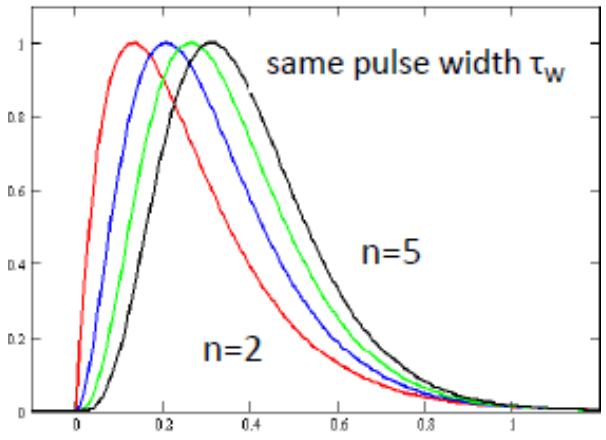

Figure 4.12 $Vout(t)$ Pulse Response with the Same Pulse Width τ_w v.s. the Order n of the Shaper

4.2.3 Design Constraints:

According to Figure 4.7, the minimum ENC can be found when the ENC_{iw} and ENC_{vw} are equal at the optimum time constant τ_{opt} or the optimum peaking time τ_p. For some applications that don't impose constraints on pulsing timing, we can design the pulse shaper with any selected value of time constant τ or peaking time τ_p in order to achieve minimum ENC. However, we still need to consider some design constraints on the pulse timing, event rate and charge collection time.

a. Event Rate:

The event rate is defined as the frequency of the continuing pulse events. If the event rate is high, the consecutive pulse events are coming very fast so that two consecutive pulses are very close and the period of the pulse event is very short. Therefore, if the event rate is high, the current pulse may be distorted by the previous one and the measurement is affected by an effort. The effect is called "pulse pile-up" as shown in Figure 4.13.

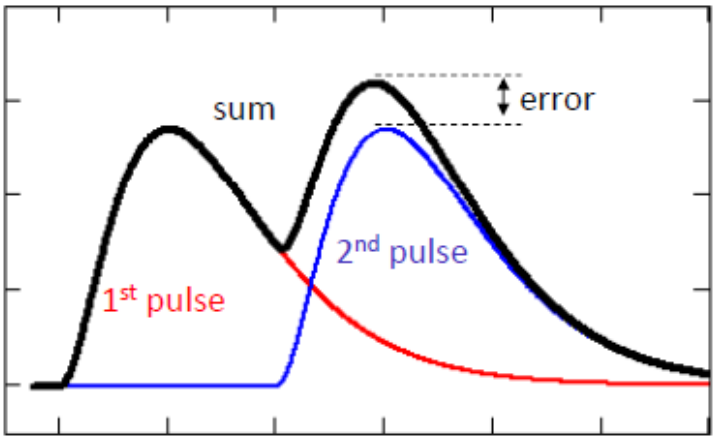

Figure 4.13 The Pulse Pile-up

The pulse pile-up can be reduced by decreasing the time constant τ of the shaper. As rule of thumb, the pulse width must be smaller than one tenth of the average period of the event.

$$\tau_w < \frac{1}{10R} \tag{4.18}$$

where R is the average rate of the events, $1/R$ is the average period of the event, τ_w is the pulse width. Luckily we are dealing with low event rates around $0.1K$ so that the average period of the event is about $10ms$ so that the pulse width τ_w should be controlled less than $1ms$ in order to avoid pulse pile-up. Therefore, for the 2^{nd} order of the pulse shaper, the time constant τ should be selected less than $133\mu s$. For the third order of the pulse shaper, the time constant τ should be selected less than $100\mu s$.

b. Charge Collection Time:

Figure 4.14 shows a sensor with two parallel planars. The current signal i_{sig} begins at the time of ionization and ends at the time when all electrons and holes have been collected by the electrodes. Therefore, the current signal i_{sig} has a charge collection time τ_c which depends on many factors. How quickly electrons and holes reach the electrodes of the detector is dependent on the electric field applied on the electrodes, the type of the sensor, the size of the sensor, and the distance between two parallel electrodes….etc. In general, the charge collection time τ_c should come from the specification of the sensor. When we design a pulse shaper and select the peak time τ_p of the shaper, as rule of thumb, the peak time τ_p must be selected as larger than 4 times the charge collection time τ_c, $\tau_p > 4\tau_c$.

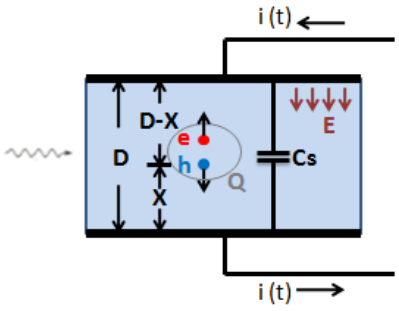

Figure 4.14 A Sensor with Two Parallel Planar Electrodes

4.3 The Design of the Semi-Gussian Pulse Shaper

4.3.1 The 2nd Order Pulse Shaper with Two Real Coincident Poles:

The primary job of the pulse shaper is to optimize the signal-to-noise ratio at the output of the shaper in order to get minimum ENC. First of all, we impose a limit of less than $1mW$ per pixel in our design so that we started to design the 2nd order shaper, composed of 1 CR differentiator and 1 RC integrator as shown in Figure 4.15, in our system. Furthermore, according to equation 4.19, we know that the parallel white noise Siw contribution is proportional to the time constant τ of the pulse shaper; the series white noise Svw contribution is inversely proportional to the time constant τ, and the series $1/f$ noise Svf contribution is independent of the time constant τ. The minimum ENC can be found when the ENC_{iw} and ENC_{vw} are equal at the optimum time constant τ_{opt}. Since our specific detector has a low leakage current about $10pA$ and the pulse event has fairly a low event rate about $0.1K$, the optimum time constant τ_{opt} can be large as $100us$. Therefore, we can choose RC values of the shaper as $100u$.

$$ENC = \sqrt{{ENC_{iw}}^2 + {ENC_{vw}}^2 + {ENC_{1/f}}^2} = \sqrt{A_{iw} \cdot Siw \cdot \tau + A_{vw} \cdot Svw \cdot \frac{Cin^2}{\tau} + A_{vf} \cdot Svf \cdot 2\pi \cdot Cin^2} \qquad (4.19)$$

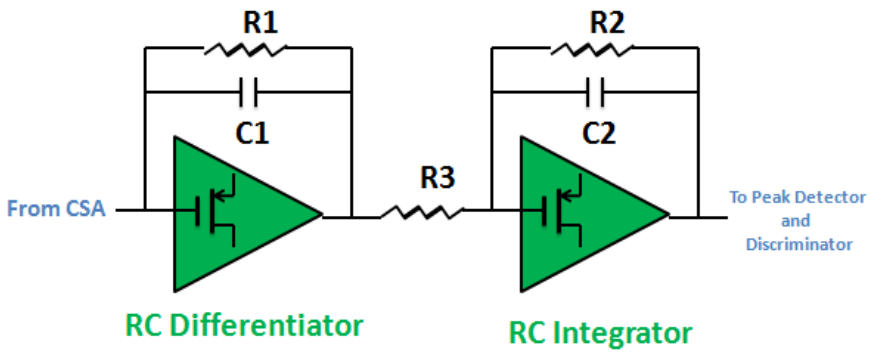

Figure 4.15 A 2nd Order Pulse Shaper with Two Real Coincident Poles

4.3.2 The nth Order Pulse Shaper with ICON Cells:

Due to constraints in technology and area, such a large resistor and capacitor as R and C of the pulse shaper cannot be implemented in our integrated circuit system. Thus, a structure with ICON cells has been selected to implement the pulse shaper in our system [25]-[28]. The principle of using ICON cells is to use a current mirror in order to de-magnify the current flowing in a resistor R so that the resistor R behaves as a resistor of higher value with respect to its real value. The ICON cell and the pulse shaper with the ICON cell can be shown in Figure 4.16 and 4.17as below.

In Figure 4.16, the voltage different between $Vx\ and\ Vy$ is converted into the current through the resistor R, in the hypothesis that the $1/gm$ input impedances of the common-gate NMOS and PMOS are negligible with respect to the resistor R. The current that flows into the ICON cell is then mirrored by the NMOS and PMOS mirror circuits. In addition, the ICON cell has the ability to absorb the leakage current and to accept current of either polarity. Because of the function of the current mirrors, the output current of the ICON cell is de-magnified by the factor $\alpha \cdot \beta$ so that the equivalent resistor Req becomes $\alpha\beta$ times the real value of the physical resistor R, $Req = \alpha\beta \cdot R$. Thus, the time constant of the shaper with ICON cells can be boosted by the factor $\alpha\beta$, $\tau = ReqC = \alpha\beta RC$, without consuming too much circuit area. In addition, the main advantage of the ICON cell is that the source voltage Vy of the common-gate PMOS and NMOS transistors is adjustable by changing the gate voltage of the common-gate PMOS and NMOS transistors. When no signal is applied from the resistor R and $Vy = Vx$, it's possible to have zero steady state current flowing through the resistor R and so flowing into the ICON cell. In this way, the biasing current of the transistors of the current mirrors can be chosen as low as possible in order to reduce the noise and the power of the ICON cell. In Figure 4.17, the output of the ICON cell can be connected to the next following stage. In this way, the pulse shaper can be cascaded in multiple stages to become a higher order pulse shaper. The stages of the shaper are dependent on the power budget, the circuit area, and ENC requirement [27].

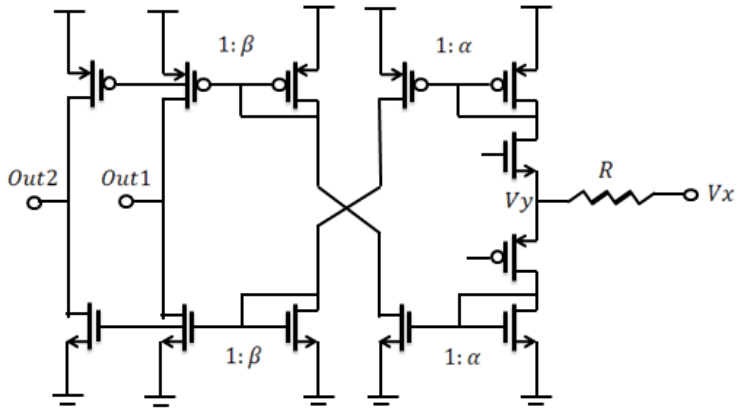

Figure 4.16: ICON Cell

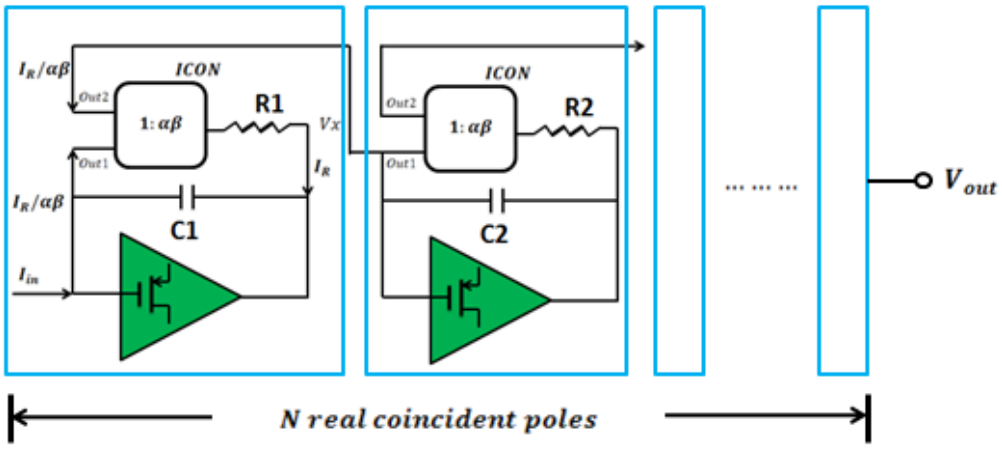

Figure 4.17: Nth Order Shaper with ICON Cells

4.4 The Simulation of Third Order Pulse Shaper with ICON Cells:

The circuit is designed under AMI $0.6\mu m$ CMOS technology and the supply voltage is $3.3V$. This is simulated by using a Cadence Spectre simulator and BSIM3v3 transistor models.

According to previous sections, the pulse shaper should possess at least 2 real coincident poles, otherwise the parallel noise Siw contribution or the series noise Svw and Svf contribution would become infinite. However, ENC_{min} does not improve significantly when the order n of the shaper is above 5. Therefore, in order to compromise ENC and the power, we chose to design third order pulse shaper with 3 real coincident poles as shown in Figure 4.18. It consists of one CR differentiator and two RC integrators. The ICON cells in the pulse shaper are used to increase the time constant τ without consuming much area in the circuit. The schematic of a single ICON cell is shown in Figure 4.19. Table 4.4 and 4.5 list the size of each transistor, the values of capacitors and resistors, and each bias voltage in the pulse shaper and ICON cells.

According to previous noise analysis, we know that the parallel noise Siw contribution from the detector leakage current is proportional to the time constant τ. However, the leakage current of the detector is usually small. In our design, we assume that the leakage current is $10pA$. Therefore, we can choose a longer time constant τ in order to minimize the series white noise Svw contribution which is inversely proportional to the time constant τ. The time constant τ of the third order pulse shaper is chosen as $100\mu s$ and the peaking time is $192.4\mu s$. Therefore, the $R_{eq}C$ value of the shaper is 100, $R_{eq}C = \alpha\beta \cdot RC = 100$. In Table 4.5, the resistor R is $100K\ ohm$ and the capacitor R is $10pF$ so that $\alpha\beta$ is chosen as 1000.

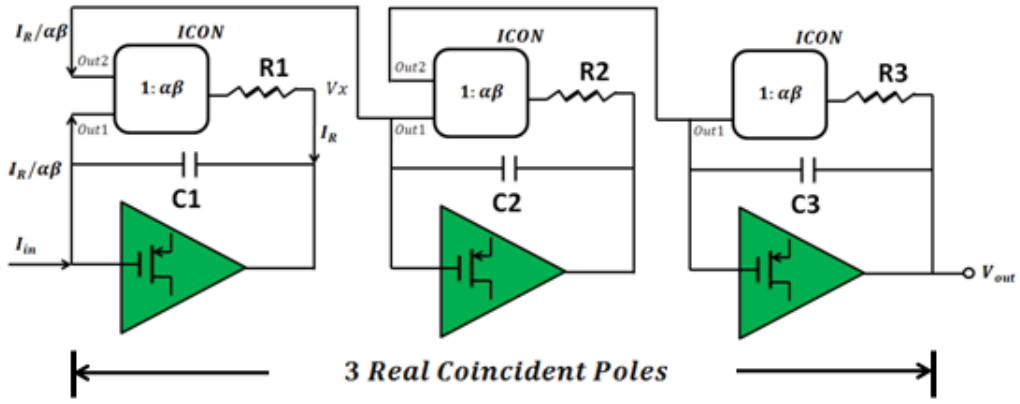

Figure 4.18 Third Order Shaper with ICON Cells

$R1$	$100K\ ohm$	$R3$	$100K\ ohm$
$C1$	$10pF$	$C3$	$10pF$
$R2$	$100K\ ohm$	α	10
$C2$	$10pF$	β	100

Table 4.4 The Values of Capacitors, Resistors, and Bias Voltageof the Shaper

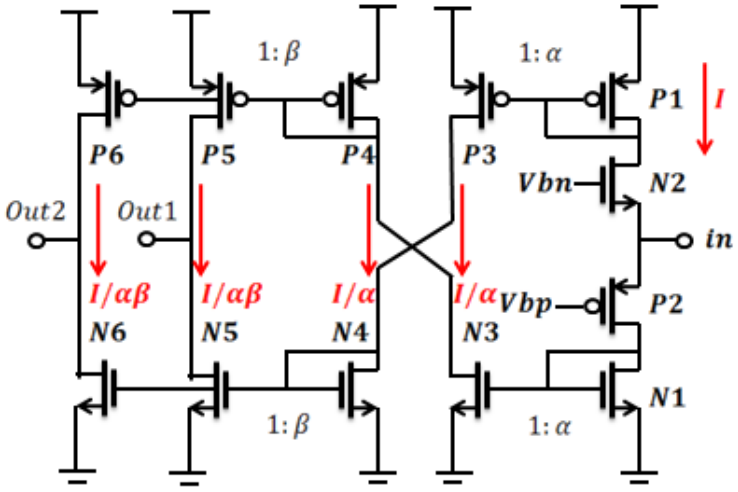

Figure 4.19 The Schematic of ICON Cell

(W/L)P1	15 μ / 12 μ	**(W/L)N1**	18 μ / 12 μ
(W/L)P2	3 μ / 0.6 μ	**(W/L)N2**	6 μ / 0.6 μ
(W/L)P3	1.5 μ / 1.2 μ	**(W/L)N3**	1.8 μ / 1.2 μ
(W/L)P4	150 μ / 12 μ	**(W/L)N4**	180 μ / 12 μ
(W/L)P5	1.5 μ / 0.6 μ	**(W/L)N5**	1.5 μ / 0.6 μ
(W/L)P6	1.5 μ / 0.6 μ	**(W/L)N6**	1.5 μ / 0.6 μ
Vbn	2.6V	**Vbp**	0.4V
I	400nA	**Power Consumption**	6 μW

Table 4.5 The Sizes of the Transistors and Bias Voltage of Each ICON Cell

4.4.1 AC Simulation of Third Order of Pulse Shaper with ICON Cells

Since the third order power shaper is composed of one CR differentiator (a high-pass filter) and two RC integrators (two low-pass filter), the function of the third order pulse shaper acts as a band-pass filter. Therefore, it can filter the low frequency and high frequency signals and noise. Figure 4.20 below shows the AC response of the pulse shaper.

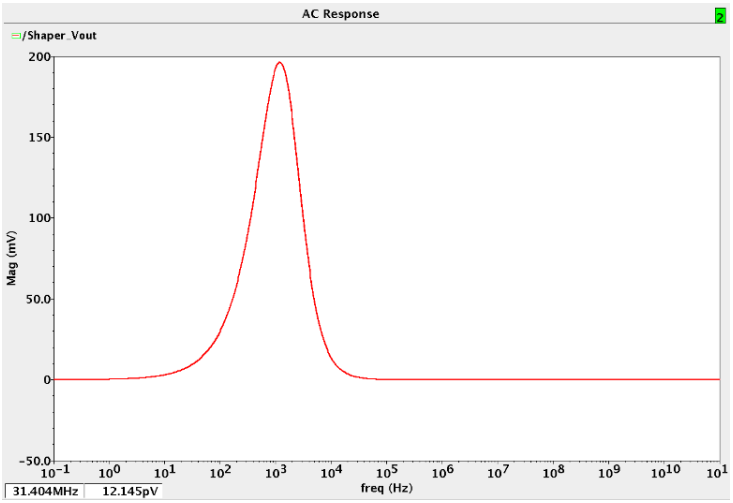

Figure 4.20 AC Response of Third Order Pulse Shaper

4.4.2 Noise Simulation of Third Order of Pulse Shaper with ICON Cells

Figure 4.21 shows the noise response of the third order pulse shaper. The noise from ICON cells becomes dominant in the shaper and contributes to about 70% of the total noise. Figure 4.18 also indicates that the $1/f$ noise from the transistors in ICON cells is dominant in the shaper. Therefore, increasing WL of the transistors of the ICON cells can reduce $1/f$ noise significantly but consume more circuit area. Finally, the total output noise of the shaper is calculated at $19.5135nV^2$ integrated from 0.1 to 100GHz.

Figure 4.22 shows a linearity plot of the third order pulse shaper. The X-axis is the input charge flowing into the shaper, and the Y-axis is the peak amplitude of the output pulse. Good linearity is achieved in our design.

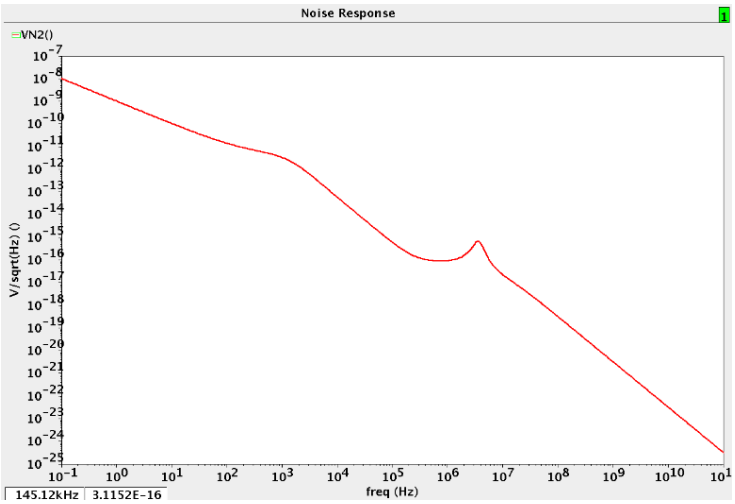

Figure 4.21 Noise Response of Third Order Pulse Shaper

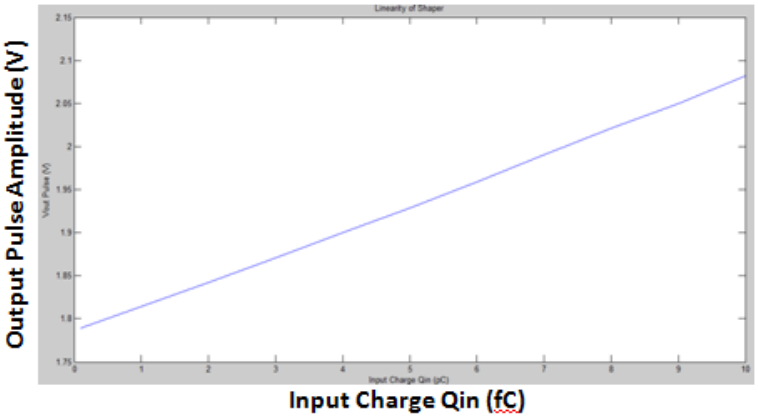

Figure 4.22 Linearity Plot of Third Order Pulse Shaper

4.5 The Simulation of CSA and Pulse Shaper:

Figure 4.23 below shows the schematic of the sensor, the 2 stage CSA, and the third order pulse shaper. The sensor is modeled as a current source in parallel with a parasitic capacitor $50pF$. The leakage current is assumed as $10pA$ and the pulse event rate is operating at $0.1KHz$. In addition, the 2 stages of the CSA provide an overall gain of $N_1 \cdot N_2 = 100$. Therefore the leakage current and the input charge from the detector are amplified by a factor of 100 at the output of the 2 stage CSA. Furthermore, the order of the shaper is chosen as 3 and the time constant τ of the shaper is given by $100\mu s$. The ICON cells in the pulse shaper are made of PMOS and NMOS mirror circuits in order to de-magnify the current flowing in a resistor R by a factor of 1000. Finally, we can obtain the Guassian shape voltage output at the output of the pulse shaper. Figure 4.24 shows the measured shaper outputs acquired over the entire dynamic range (0.1-100fC) with a peaking time 192.4 μs. Figure 4.25 also shows transient simulation of the CSA and the shaper for the different shaper outputs based on different input charges from

0.1fC to 100fC. Furthermore, Figure 4.26 shows a linearity plot of the 2 stages of the CSA and the third order pulse shaper. The X-axis is the input charge generated from the detector, and theY-axis is the peak amplitude of the output pulse. Good linearity is achieved in front-end readout circuitry.

Moreover, Figure 4.27 shows the noise response of the 2 stage CSA and the third order pulse shaper with ICON cells. The $1/f$ noise from the ICON cells is still dominant in the circuits. The total output noise at the output of the shaper is calculated at $25.433nV^2$ integrated from 0.1 to 100GHz. Figure 4.28 shows the output pulse for 2^{nd} to 5^{th} order of semi-Guassian pulse shaper. Figure 4.29 shows the output pulse for different time constant τ of the third order pulse shaper from $20\mu s\ to\ 100\mu s$. Finally, the total power dissipation is $1.518mW$. The maximum charge is $100fC$ and the minimum ENC is $0.1fC$ which represents 625 electrons released by the detector. Therefore, the dynamic range (DR) is 1000, DR = Maximum Charge / Minimum ENC.

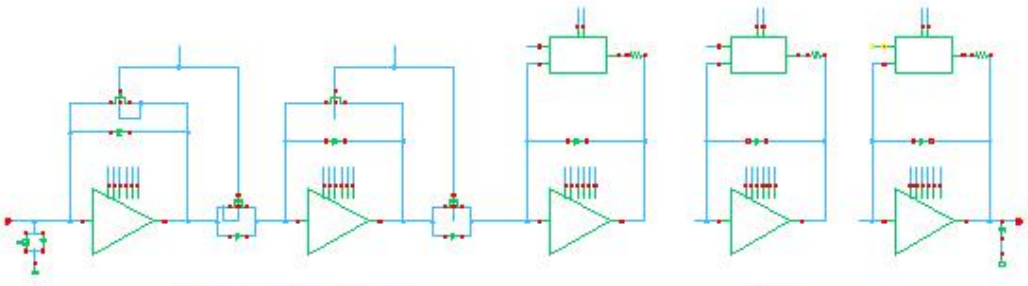

Figure 4.23 The Schematic of CSA and Pulse Shaper

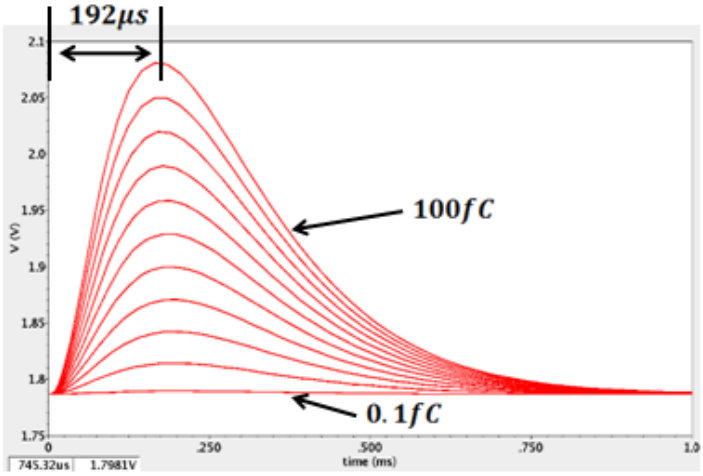

Figure 4.24 The Shaper Output Acquired over the Entire Dynamic Range (0.1-100fC)

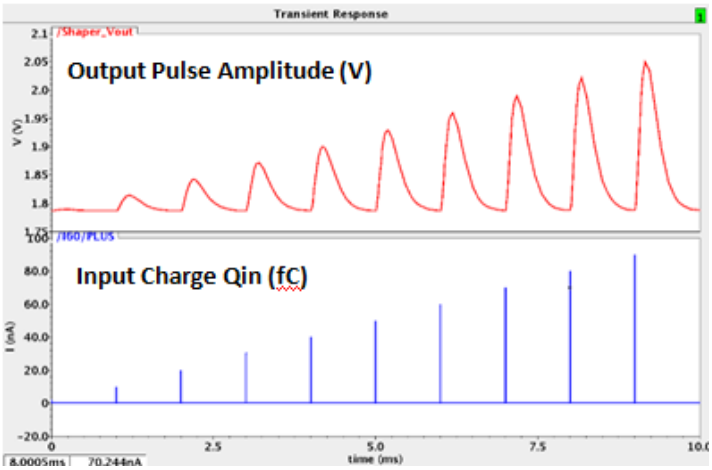

Figure 4.25 Input Charge Qin V.S. Output Pulse Amplitude

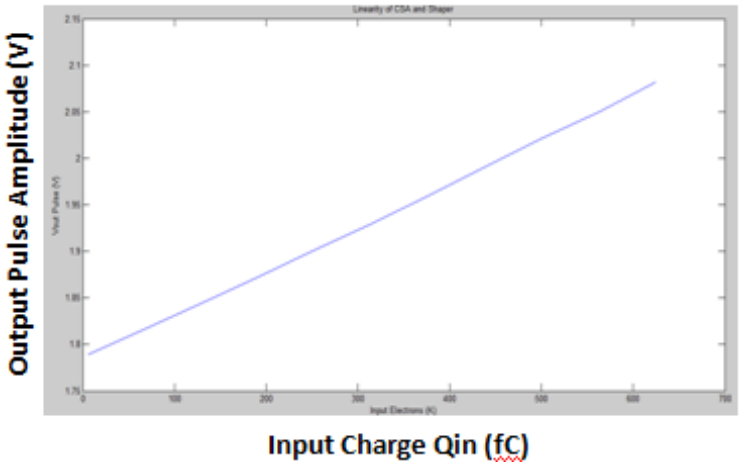

Figure 4.26 Linearity Plot of CSA and Pulse Shaper

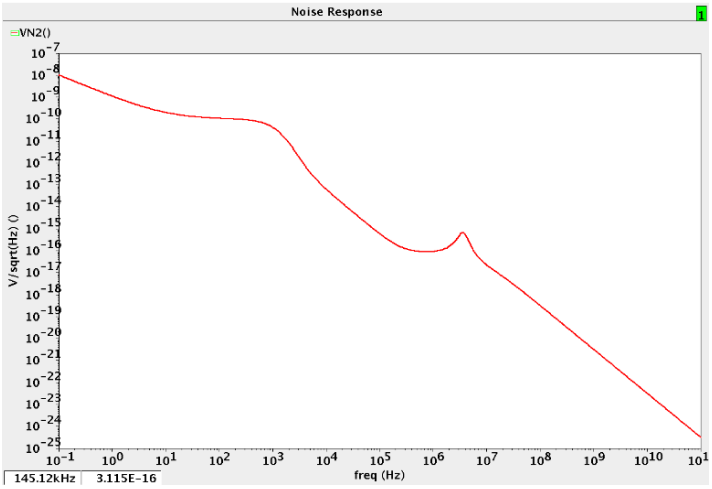

Figure 4.27 Noise Response of CSA and the Shaper

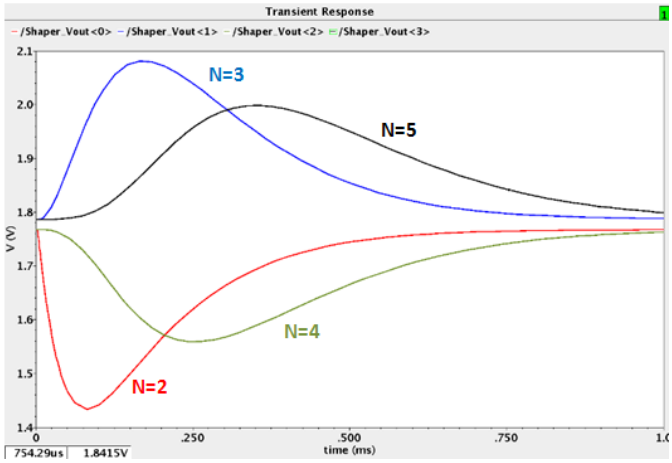

Figure 4.28 The Output Pulse for the 2nd to 5th order of Semi-Guassian Pulse Shaper

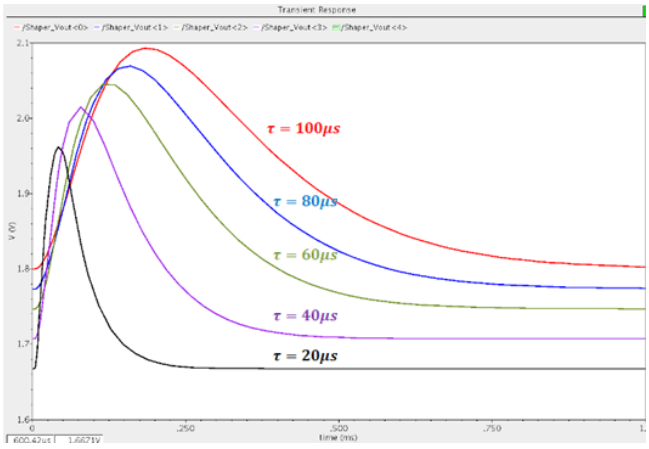

Figure 4.29 The Output Pulse for Time Constant 20us to 100us of the 3th Order Pulse Shaper

5 Conclusions

The CMOS front-end readout circuitry was designed to perform the radiation detection system in this thesis. Input MOSFET transistor optimization for detailed noise analysis is presented in three different transistor operation regions. The advanced cascade amplifier is used to implement the charge sensitive amplifier in our front-end readout circuitry. The design procedures of the 2 stage charge sensitive amplifier is provided to amplify the input charge generated from the detector. The third order of semi-Guassian pulse shaper with ICON cells is implemented to maximize the signal-to-noise ratio at the output of the shaper. Finally, the power consumption is $1.518mW$ and minimum ENC is reached at 625 electrons. The dynamic range is $\frac{100fC}{0.1fC} = 1000$. The low noise, low power, and high linearity front-end readout circuitry for radiation detection is implemented with CMOS technology in this thesis.

For the future work, the layout and the post simulation should be completed in order to realize the chip fabrication. The test measurement of the fabricated chip should be conducted in order to compare with the simulation results. In order to get an accurate test measurement results, a good test approach should be provided in our measurement.

6 References

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