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LOW-POWER LOW-DATA-RATE ANALOG FRONT-END FOR NEURAL RECORDING SYSTEM

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Abstract of the Dissertation

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An analog stage for multi-channel neural recording requires a number of wires comparable to the number of channels, leading to restriction of movement and poor scalability. To overcome this problem, an implantable neural recording system is desirable which is operated by a power and data transfer through wireless inductive coupling.

However, a data-rate problem arises when recording from a large number of multi-channel sensors in transcutaneous wireless systems, since the data rate is typically limited to few Mbps. With the limited bandwidth, a neural recording system having sampling rate of even few tens of KHz with 10-bit quantization resolution could handle only few channels of neural information simultaneously over a wireless link. A low-power low-data-rate analog front-end, for implantable neural recording system that can process 32-channel neural spikes as well as local field potential (LFP), is proposed.

32-channel low-power low-noise amplifiers with bandpass-characteristic filter stages were fabricated on AMI CMOS 0.6um technology and tested with a custom designed general purpose test station interfacing with PC. Additionally, a low-power low-noise preamplifier stage was fabricated on MITLL FD-SOI (Silicon on Insulator) 0.18um technology and tested. An efficient power harvesting system in CMOS for bio-implantable devices was designed and simulated. Based on experimental testing of the fabricated IC chips, improved designs of the analog front-end circuits were simulated, and an alternative approach for low-data-rate neural recording system was proposed.

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Chapter 1

Introduction

There is a large demand for technologies that enable neuroscientists and clinicians to record the simultaneous activity of large numbers of neurons closely spaced (i.e., on order of 10μm or less apart) in a central/peripheral nerve. Multielectrode neural recordings are becoming standard practice in basic neuroscience research, and the knowledge gained from these studies is a one of major requirements to both fundamental research in how spatial populations of somatosensory neurons encode mechanical stimuli (which occur during touch, joint movements, and muscle constractions) and the engineering of feedback-controlled functional electrical stimulation (FES) of muscles used in locomotion for paralysis victims. Recent advances in micro electro mechanical systems (MEMS) technology have produced small (less than $4mm$ in any dimension) arrays of microelectrodes containing as many as 100 recording sites [1, 2, 3]. Next-generation neural recording systems must be capable of observing 100 to 1000 neurons simultaneously in a fully implanted unit, and its integrated electronics should have characterizations of low-power, low-noise,

low-data-rate, and small-area to be fully implanted in large quantities.

This work focuses on a low-power analog front-end suitable for wired/wireless, multi-channel neural recording system. It includes a novel power harvesting system which supplies stable power to be able to process neural data and communicate with the external device. Also, It presents the design, simulation, and testing of a CMOS 32-channel analog amplifier stages for wired neural recording system and a low-power low-noise neural amplifier in SOI process. Finally, it presents a design and simulation of a CMOS low-power low-data-rate wireless neural recording system. The simulation, test results, and the improvements for fabricated chips are summarized at the end of each chapter.

Chapter 2

Neural Recording Sensors and System

2.1 Neural Recording

The development of a direct neural interface with the central and/or peripheral nervous system has been a goal of the neuroscience and electrical/biomedical engineering communities for many decades [98, 5, 6, 7]. From the neuroscience perspective, it has become clear that to better understand how the peripheral and central nervous system function, we must be able to simultaneously monitor the responses of many neurons. This is because the nervous system processes in parallel information originating from the periphery (e.g, somatosensory neurons). For example, the simple act of depressing a key on a keyboard with one digit activates from the fingerpad alone an order of 300 cutaneous mechanosensitive neurons [8]. From the electrical/biomedical engineering perspective, it has been desired to restore sensory

and motor function to people who have suffered neurological defects from trauma or disease [9]. Real progress has occurred in recording from ensemble of neurons in the cortex using non-human primate and other mammalian models [10, 11], in development of a cochlear neural prosthesis in humans [14, 15, 16, 17], and intriguing results of a cortical visual neural prosthesis [18]. Technical developments from these areas give encouragement for the development of a general neural interface that could be used for any central/peripheral nerve. Sensory information carried in peripheral nerves is used not only for haptics (sense and touch), but also provides critical information used partially in muscle feedback control. For example, the lack of sensory information carried in the medial articular nerve in conjunction with instability of the anterior cruciate ligament (ACL) results in very rapid and progressive osteoarthrosis in a dog model [19, 20]. It has been shown that mechanosensitive neurons in the joint capsule will detect the increased loads due to ACL insufficiency [21], confirming the important role of sensory neurons in proprioceptive feedback.

2.2 Multi-electrode Sensors for Central/Peripheral Nerves

Multi-electrode sensors are commonly used micro-equipments to record electrical and chemical signals. They are widely implanted from a cerebral cortex to a peripheral nerves.

Multi-electrode sensors designed for recording neural responses from the cortex generally use one or two strategies. The most common consists of an array of single electrodes (a "bed of nails", See Figure 2.1(b)) that either penetrates through the

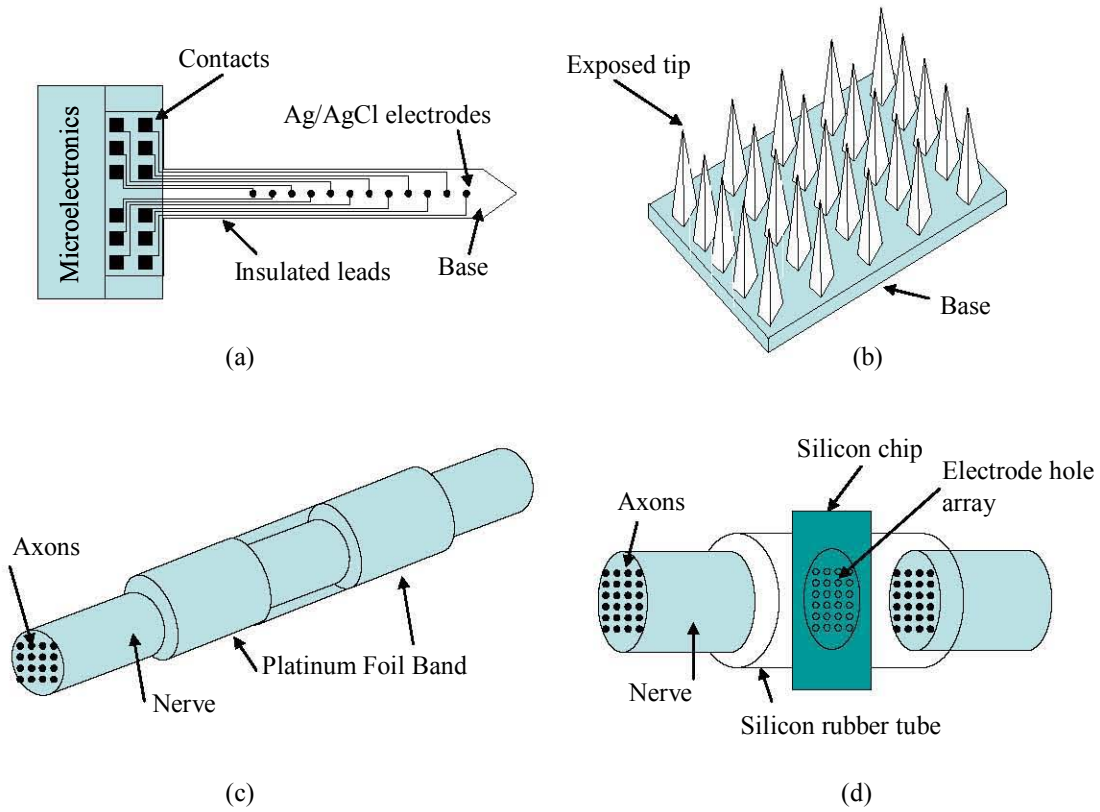


Figure 2.1: Various Microelectrodes, Part of figures taken from [88])

dura or is implanted on the surface of the cortex if the dura has been previously removed [10, 11, 12, 13, 1]. Another design is a single shaft onto which are etched recording locations [22, 23] (See Fig 2.1(a)). These designs allow a minimum linear spacial separation of about 100μm and work reasonably well for the cortex where penetration to some depth is desirable and the network of neuron cells is on the same order of spatial separation. However, either of these designs is problematic in peripheral nerves, as the electrode spatial separations are too large for recording from adjacent neurons (i.e, their axons), which are more closely packed. Multiple, simultaneous single neuron recordings have been made from peripheral nerves

[24, 25, 26, 27], however these experimental approaches cannot achieve the density of recording needed for a true peripheral neuronal "population" study. There are three major types of electrodes that have been used for simultaneously recording multiple neurons in peripheral nerves: penetrating microelectrode arrays [28, 29] (Similar to Fig 2.1(b)), regeneration [30, 31, 32, 33] (See Fig 2.1(d)) and cuff [34, 35, 36, 37] (See Fig 2.1(c)). Penetrating microelectrodes (also termed intrafascicular electrodes) have been developed in one-, two-, and three-dimensional arrays using metal, glass, and silicon substrates. They resemble the cortical design in that single or multiple electrodes are inserted into a nerve. Designs have been implemented with up to two-dozen electrodes [38], though limitations restrict the number of electrodes and their ability to record from axons spatially close together. In regeneration type electrodes, the nerve is fully transected and a sieve electrode array is implanted in between the two nerve ends. Suitable guidance channels are used to aid the axons in the nerve to regenerate through the holes. In principle and depending on the geometry and number of the holes, this electrode type could simultaneously record from many single neurons. However, this is obviously a highly invasive procedure and the regeneration of axons through the holes has had variable success [39], and has been further confounded by inappropriate and significantly incomplete innervation to the target areas [40]. In cuff type electrodes, the recording (and/or stimulating) surfaces encapsulate the whole nerve. Cuffs are less intrusive than regeneration type electrodes and are more amenable for chronic implantation, however they suffer from lack of selectivity in recording from specific regions within a nerve. Indeed, they cannot distinguish single neuron responses and are more typically used for whole nerve recordings (i.e., an integration of the neural responses of all the neurons) [41]. There has been a

trial to improve the selectivity by reshaping the nerve through flattening [42, 44], which has theoretically shown to significantly improve the selectivity of recording or stimulating from cuff electrodes [43, 45]. Research is on-going to record from hundreds, if not thousands of somatotopically arranged (and closely spaced) sensory neurons in peripheral nerves.

2.3 Biopotentials

The potentials sensed with a electrode in an organ or body is called biopotentials and have a profusion of physiological information accompanying biochemical process. The potentials hold various amplitude ranging from $0.001mV$ to $30mV$, depending where the electrode is placed. Table 2.1 summarizes the amplitude and bandwidth for different biopotentials, which electrical/biomedical engineers might be interested in. ECG (Electrocardiogram) can be detected from the heart and it has relatively large amplitude among biopotentials. It gives a clinical information in diagnostics of a heart function. On the other hand, EEG (Electroencephalogram) has the smallest amplitude and bandwidth among biopotentials, and is measured from the brain. EMG (Electromyogram) signal is utilized in any muscle diagnostic. In this work, we are focusing on neural spike and LFP (Local Field Potential) recording with bandwidth from $0.5Hz$ to $7KHz$. The activity for a few nearby neurons can be observed as neural spikes by electrodes located in the brain, as well as LFP which is the internal correlate of the EEG signals observed on the scalp [89].

Table 2.1: Summary of Biopotentials.

Biopotentials	Amplitude (mV)	Bandwidth (Hz)
ECG	1∼10	0.05∼100
EEG	0.001∼0.01	0.5∼40
LFP	0.05∼1.2	0.5∼100
Neural Spike	0.02∼1	300∼7000
EMG	0.1∼30	20∼10000

2.4 Existing Neural Recording Systems

Current state-of-the-art neural recording systems have evolved from few channels, remaining explant, wired recording, and large-area occupation to a high performance system for multi-channel (as many channels as possible), implantable, low-power, wireless recording, and small-area system. The recent published cutting-edged neural recording technology in [3] supports 100 recording channels with wireless feature. They are battery-less implantable system and operated by power harvesting technique, mainly inductance coupling principle typically used in RFID transponder. The acquired neural signals are digitized and transmitted outside of skin through inductive coil. This section reviews state-of-art neural recording systems presented in the past decade. Table 2.4 and 2.4 summarizes the published neural recording systems and commercially available systems respectively.

Many neural recording systems were developed and also currently being developed. J. Parramon and their research group lead by CNM-Barcelona has reported an implantable batteryless telemetric microsystem for EMG (electromyogram) recording [58]. It supports 2-channel recording simultaneously and is implanted in rabbits for their research studies regarding control of prosthesis through muscular biosignals. Power is transferred with a $10MHz$ inductive coupling

within up to $10mm$ and the bit rate can be programmed at either $117kbps$ or $234kbps$ for outlink and $120kbps$ for inlink with a 8-bit on-chip ADC.

Andreas Neider et al. at RWTH Aachen developed a miniature FM-stereo radio transmitter to study brain-behavior interaction in unrestrained animals [57]. The miniature FM-stereo RF transmitter has been equipped on barn owls with two independent electrodes and recorded simultaneously from the brain of barn owl. The transmitted data was decoded and analyzed with the sorted neural spikes.

Pedro Irazoqui-Pastor et al. at UCLA have recorded continuous in-vivo EEG from un-tethered rodents using an inductively powered and implantable wireless neural recording device [125]. The 4-channel IC has been designed, fabricated, and packaged in $0.25cm^3$. It has been implanted in-vivo and used to record EEGs from an un-tethered rat. The recorded signal is transmitted as FM (Frequency Modulation) version superimposed on a $3.2GHz$ carrier wave.

P.Mohseni and K.Najafi et al. at the Center for Wireless Integrated MicroSystems (WIMS) at the University of Michigan presented a four-channel telemetric microsystem featuring on-chip FM transmission of neural spikes over a distance of $0.5m$ [52]. The designed IC was packaged together with three off-chip components on printed circuit board (PCB) board including two miniature $1.5V$ batteries. They demonstrated wireless recording of neural activity from the auditory cortex of an awake marmoset monkey at several transmission distances ranging from 10 to $50cm$.

Two different researchers presented 16-channel neural amplifier array in 2003. G.A. DeMichele and P.R. Troyk et al. at Illinois Institute of Technology (IIT) presented general purpose 16-channel neural amplifier array combined with a UHF-

FM transmitter [56]. I. Obeid and P.D. Wolf et al. from Duke University have also introduced 16-channel neural amplifiers [136]. The device was tested in vivo with electrode arrays implanted in the somatosensory cortex.

E.A.Johannessen et al. at University of Glasgow in UK have developed a microelectronic pill for in-situ studies of the gastro-intestinal tract, which incorporates a four-channel microsensor array for real-time determination of temperature, pH, conductivity, and oxygen [59]. The sensors were fabricated using electron beam and photolithographic pattern integration, and were controlled by an application specific integrated circuit (ASIC), which sampled the data with 10-bit resolution prior to communication off chip as a single interleaved data stream. An integrated radio transmitter sends the signal to a local receiver (base station), prior to data acquisition on a computer. Real-time wireless data transmission is presented from a model in vitro experimental setup, for the first time.

Shoji Takeuchi and Isao Shimoyama from University of Tokyo presented a neural recording system with FM transmitter and microelectrode [55]. They only use commercially available discrete components to build their system but its size and weight are only $15mm \times 8mm$ and $0.1g$, respectively. The system was tested on a cockroach and the neural activity from the brain during a free-walk was successfully measured through the system. The system is driven by commercially available silver-oxide micro battery which can be attached on the edge of the board and is light enough to be carried by an insect [71].

Rio J. Vetter et al at the University of Michigan studied the recording performance of silicon-substrate micromachined probes in terms of reliability and signal quality [61]. They used a 16-channel probe for studying and neural recording

using a commercial 12-bit multichannel recording system provided by Plexon, Inc., Dallas, TX. Recordings were made daily for the first four weeks and then at least once weekly thereafter, from cerebral cortex. The extracellular signals were sampled at $40kHz$ and bandpass filtered from 450-$5000Hz$.

C. Chestek et al. at Case Western Reserve University (CWRU) introduced the design of a bio-compatible, implantable neural recording device for Aplysia californica, a common sea slug [64]. Extracellular neural signals ($<100\mu$V) were recorded using their preamplifier that is integrated with programmable data acquisition and control, and FSK telemetry that provides $5Kbps$ wireless neural data through $18cm$ of saltwater. A 8-cm electric dipole antenna was utilized by exposing the ends of the antenna to the saltwater and a $3V$ lithium ion battery was equipped to the recording. Neural data obtained from nerve electrodes and a wired interface to this device have $2.5\mu V_{rms}$ noise.

Roy H. Olsson III and Kendall D. Wise at the University of Michigan developed a 32-channel 256-site, fully implantable, 3-D neural recording microsystem [51]. A 4-set of 8-channel end up with 256-site recording. one channel (8-site) is selected by a multiplexer and digitized by 5-bit successive approximation ADC. They have employed a compression technique to minimize the generated data-rate since the allowable data-rate through transcutaneous wireless system is currently limited to $2.5Mbps$ [50].

Reid Harrison et al. have designed a low-power integrated circuit for a wireless 100-electrode neural recording system. The complete system receives power and commands wirelessly over a $2.64MHz$ inductive link and transmits neural data back at a data rate of $330Kbps$ using a fully integrated $433MHz$ FSK transmitter. Data

reduction was performed by combination of a low-power 10-bit SAR ADC and an array of spike detectors.

Commercially available neural recording systems are listed in the Table 2.4. Most of them [68, 69, 70] have wired interface which is not desirable due to movement restriction. ADinstruments supports wireless interface but only 8-channels can be recorded simultaneously.

	Chan-nels	Reso-lution	Sampling Rate	Size	Total Wt.	Power Diss.	Wire	Year
[54]	4	No ADC	$12KHz$	$1\times1\times0.5$ cm^3	$1g$	$0.41mW$	Wireless	2006
[125]	1	No ADC	N/A	$5\times5\times10$ mm^3	N/A	$5.8mW$	Wireless	2003
[126]	3	No ADC	$70\sim$ $138KHz$	$1.8\times1.3\times0.16$ cm^3	$1.1g$	$2.44mW$	Wireless	2003
[55]	1	No ADC	N/A	1.5×0.8 cm^2	$0.1g$	$10mW$	Wireless	2004
[56]	16	No ADC	N/A	N/A	N/A	$18mW$	Wireless	2003
[52]	3	No ADC	N/A	$1.7\times1.2\times0.16$ cm^3	$1.1g$	$2.2mW$	Wireless	2005
[57]	2	No ADC	N/A	$2.5\times1\times0.5$ cm^3	$3.1g$	N/A	Wireless	2000
[58]	2	8-bit	$30MHz$	$1.1\times1.1\times0.7$ cm^3	N/A	$22.5mW$	Wireless	1997
[59]	4	10-bit	$32KHz$	$1.6\times5.5cm^2$	$13.5g$	$12.1mW$	Wireless	2004
[60]	16	No ADC	N/A	$15\times17mm^2$	N/A	N/A	Wire	2005
[61]	16	12-bit (Off)	$40KHz$	$\sim$ $1.5\times0.8cm^2$	N/A	N/A	Wire	2004
[136]	16	No ADC	N/A	$\sim$ $9.5\times19mm^2$	N/A	N/A	Wire	2003
[62]	16	12-bit	$20KHz$	N/A	N/A	N/A	Wireless	2005
[63]	N/A	10-bit	$2MHz$	N/A	N/A	N/A	Wireless	2001
[64]	8	8-bit (Off)	$5Kbps$	N/A	N/A	N/A	Wireless	2005
[65]	32	$>$ 8-bit	$2MHz$	$4\times6mm^2$	N/A	$90mW$	Wireless	2005
[51]	64	5-bit	$20KHz$	$\sim 11mm^2$	N/A	$\sim$ $3.2mW$	Wireless	2005
[3]	100	10-bit	$15Ksps$	$27.3mm^2$	N/A	$13.5mW$	Wireless	2007
[66]	96 (Max.)	12-bit (Off)	$30Ksps$	see [66]	$16g$	N/A	Wire	2006

Table 2.2: Performance comparison of developed neural recording systems.

	Channels	Resolution	Sampling Rate	Application	Total Wt.	Power Diss.	Wire
ADinstruments [67]	8	12-bit	$2KHz$	small animal EEG/ECG	$18g$	N/A	Wireless
Neuronexus [68]	16/32	No ADC	N/A	chronic probe	N/A	N/A	Wire
Cyberkinetics [69]	128	16-bit	$30Ksps$	data acquisition	N/A	N/A	Wire
Triangle Biosystems [70]	16/32	No ADC	N/A	neural signal acquisition	$0.75g$	N/A	Wire

Table 2.3: Performance comparison of commercially available neural recording systems.

Chapter 3

Electronics for Analog Signal Processing in Neural Recording Systems

The analog signals collected from the neural sensors have to be amplified, digitized and processed to extract the desired information. There are several challenges in designing a fully integrated analog-to-digital interface for this type of application. The circuitry has to dissipate low power (to accommodate as many channels as possible), it has to be low-noise (because of the low level amplitude of the neural signals), and insensitive to the random DC offset developed at the electrode-electrolyte interface.

The amplified signal can be modulated by analog modulation scheme such as FM however it is still susceptible to noise, channel interference, and cross-talk in the multichannel environment. To make it robust, high noise-immune transmission, and

independent of channel-interference and cross-talk, the amplified and collected neural data must be converted to digital domain in proximity to the recording site.

An approach for analog-to-digital interface for sensor arrays is presented in Figure 3.1. The system consists of an array of low-noise neural amplifiers, an analog multiplexer and one or several analog-to-digital converters (ADCs, the number of ADC can be determined by power consumption estimation for the whole system).

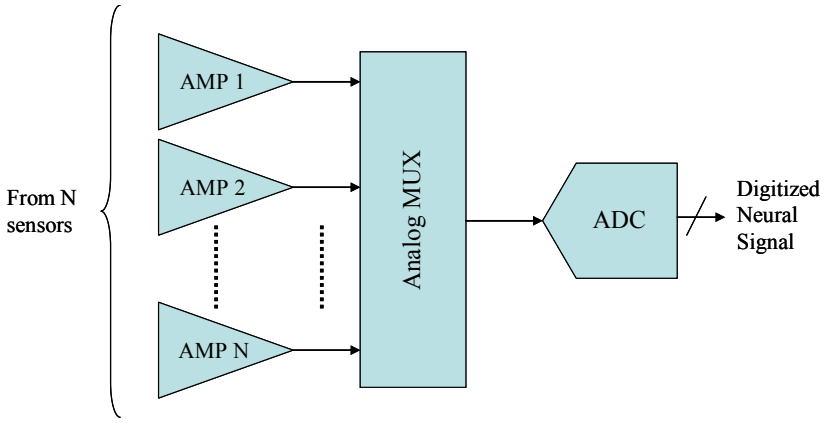


Figure 3.1: Analog to digital interface for sensor arrays

3.1 Band-Pass Characteristic Preamplifier

The most critical block in Figure 3.1 is the low-noise preamplifier ("AMP" in Figure 3.1). Its gain should be precisely controlled and it should reject the input random DC component without affecting the electrical signals generated by the peripheral nerves under study. Therefore, the frequency characteristic of the amplifiers must be a band-pass type with the lower pass-band edge of $1Hz$ (preferably less than $1Hz$) and the upper edge of 7kHz (or up to $10KHz$). Several solutions

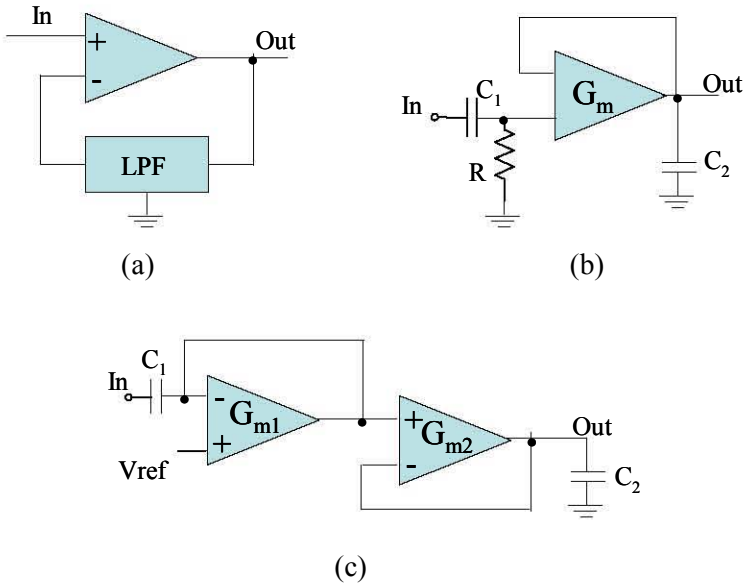


Figure 3.2: Three topologies of preamplifiers insensitive to random DC inputs

have been previously proposed in the literature to satisfy these design constraints. One possible implementation [72, 73] uses a low-pass filter (LPF) in the feedback path of an op-amp to obtain the desired high-pass characteristic at low frequencies (Figure 3.2(a)). Reference [72] uses a degenerate LPF, an integrator, to completely remove the DC component of the input signal, while in reference [73] a second-order RC filter is utilized to reduce by approximately 40dB the DC gain of the overall amplifier. The second approach [93, 74, 75, 76] for eliminating the input random DC offset is shown in Figure 3.2(b) where a low frequency high-pass RC filter is present at the front-end of the amplifier. The third approach [77, 78] to make band-pass characteristic is shown in Figure 3.2(c) where a cascade of first-order high-pass filter and first-order low-pass filter based on RC primitives has been used. The main design issue in all three cases illustrated in Figure 3.2 is the on-chip implementation of very large RC time constants. To make a very large RC time constant, an

external capacitor is employed in [72], but obviously such a solution is impractical for multiple channel implantable systems. Reference [73] uses reverse-biased junction diodes to implement high-value resistors (of the order $10^{10}\Omega$) while maintaining the capacitor values appropriate for integrated circuits. However, this approach suffers from optical drift, which reduces their reliability. References [75, 76] use a laser programmable resistor to bias a transistor which is utilized for creating low cutoff frequency of the desired high-pass filter. But this solution needs a post-fabrication process of laser trimming (which is rather expensive) and might be an impediment to the mass production of the device. References [77, 78] use capacitors for both transconductor input and output to increase small linear range which is the main drawback of the operational transconductance amplifier. However, this approach is originally considered for only band-pass function so that it needs another gain stage. References [93, 74] use two terminal pseudo MOS-bipolar resistors to set high time constant. Although the voltage difference between two terminals should be stable to maintain a constant RC time constant it allows a very simple implementation of large time constant. MOS-bipolar pseudo-resistor is a diode-connected two-terminal MOS transistor but it has very high resistance (almost $10^{12}\Omega$ if small voltage difference is guaranteed between two terminals). Figure 3.3(b) shows the structure of band-pass characteristic preamplifier using MOS-bipolar pseudo-resistor. The circuit structure is similar to the typical instrumentation amplifier (Figure 3.3(a)) but with a capacitor at each input to remove DC offset, making very large time constant together with MOS-bipolar pseudo-resistor.

The transfer function of the band-pass characteristic preamplifier in Figure 3.3(b) can be derived as equation (3.1).

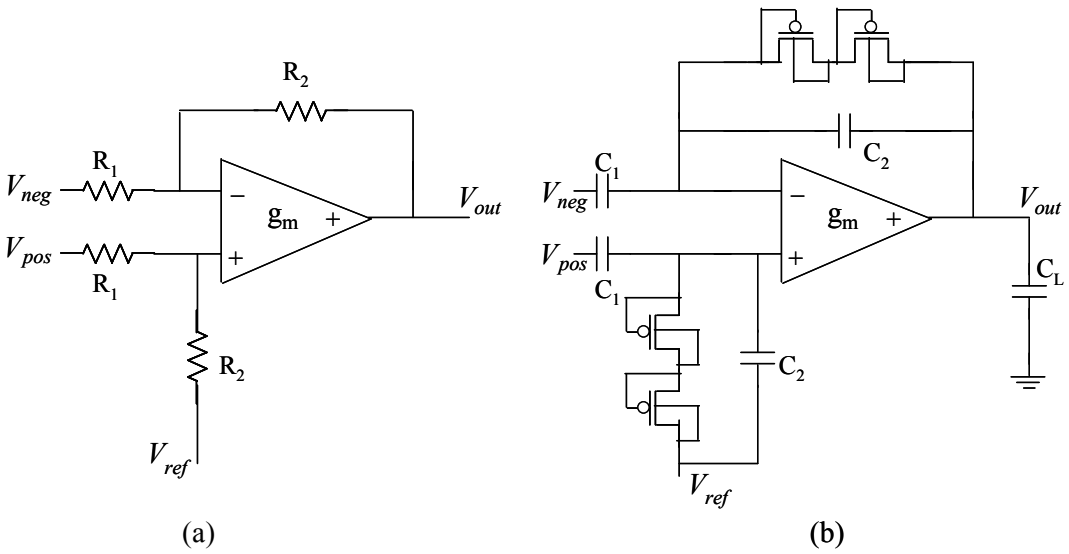


Figure 3.3: Schematics of (a) a typical instrumentation OPAMP [79] (b) a bandpass characteristic preamplifier [93].

$$V_{out} = \frac{S\frac{C_1}{C_2}}{\frac{1}{RC_2} + S}(V_{neg} - V_{pos}) \tag{3.1}$$

where R refers to resistance of MOS-bipolar pseudo-resistor.

Instead of gate-source or gate-drain connection of the pseudo MOS-bipolar device, the gate voltage can be utilized as a biasing input to set an arbitrary resistance. The MOS transistor is operated in the weak inversion region.

3.2 Small Transconductance G_m Implementation

In recent years there has been considerable research effort in the development of operational transconductance amplifiers (OTA) with very small transconductance. It is widely used in bio-medical sensor interfaces to implement filters and amplifiers.

Several OTA topologies have been developed to achieve transconductances in the order of a few nA/V with linear range up to 1.5V [80, 81, 82, 101, 84, 85].

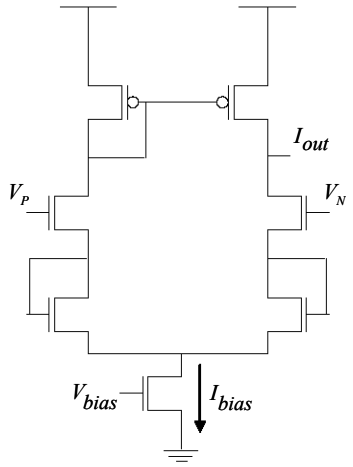


Figure 3.4: Schematics of an operational transconductance amplifier.

Lloyd Watts and Carver A. Mead introduced subthrehold MOS transconductance amplifier with increased linear range [80] in 1992. They used source degeneration scheme to extend linear region of OTA and applied it into silicon cochlea. Figure 3.4 shows the transconductance amplifier biased in subthreshold applied in the original cochlea circuit. The transconductance amplifier biased in subthreshold has a hyperbolic tangent transfer characteristic and the transconductance can be scalable via one or two diode-connected transistors on each side of the differential pair as a source degeneration. The scaled current is given by equation (3.2).

$$I_{out} = I_{bias} \tanh(\frac{k_s(V_P - V_N)}{2V_T}) \tag{3.2}$$

where k_s=k, k_s=$k^2/(k+1)$, and k_s=$k^3/(k^2+k+1)$ for no diode-connected transistor each side, one diode-connected transistor each side, and two diode-

connected transistor each side, respectively. The constant k is the same as inverse of body-effect coefficient n (n=1.6 for typical bulk CMOS process). V_T is thermal voltage of kT/q. We expect degeneration with one diode per side to widen the linear range by a factor of 2.4, and expect degeneration with two diodes per side to widen the range by a factor of 4.4. The price for the increased linear range is a decrease in the common-mode operating range and increased thermal noise injection.

A more advanced linearlization technique was introduced in 1997 [82]. Rahul Sarpeshkar, Richard F. Lyon, and Carver Mead obtained wide linear range by widening the *tanh* or decreasing the ratio of transconductance to bias current. They used several techniques such as a use of well terminals of the input differential pair transistors as the amplifier inputs, source degeneration introduced in [80], gate degeneration, and bump realization [119] to widen linear region and reduce transconductance.

A good comparative study among various schemes in terms of performance characteristics such as power consumption, active silicon area, and signal to noise ratio (SNR) is reported in 2002 [101]. Four different design techniques for obtaining low transconductances were analyzed and compared among them. These techniques were referred to as reference OTA, OTA with Current Division and Source Degeneration (SD+CD), Floating-Gate OTA with Current Division (FG+CD), and Bulk Driven OTA with Current Division (BD+CD).

A pico-ampere per volt range CMOS transconductor with 0.15mV linear range was presented in 2003 [84]. The use of complex OTA architectures also increases noise, mismatch offset, and transistor area leading design trade-offs as [101], a relatively simple and area efficient series-parallel current division scheme was applied to the

simple OTA. N-number of NMOS current mirrors and N-unity transistors are placed in series or in parallel to achieve an effective output transconductance of G_m=g_{in}/N^2, where g_{in} is input transconductance of the OTA.

A different approach to get very small transconductance is introduced in [85]. Cascading of basic transconductance and transimpedance (g_m^{-1}/g_m) elements was used to achieve a very small overall transconductance. The effective overall transconductance of the chain is the product of the transfer functions of the single stages, which allows transconductance reduction to any desired level by adding more stages to the chain. Compared to the current division approach introduced in [101], this cascading of transconductance and transimpedance approach saves silicon area and power. Because, to decrease the transconductance further in the current division approach, the mirror transistor ratios must be increased, which leads to large silicon area and sets a limit to the maximum achievable time constant.

3.3 Analog to Digital Converter

To make robust, high noise-immune transmission, and independent of channel-interference and cross-talk, the amplified and collected neural data must be converted to digital domain; On-chip analog to digital conversion is required. A neural recording system in spike detection normally prefers a high resolution of over 10-bit. For the high-resolution ADCs, delta-sigma ADC is usually considered but it suffers from idle tones while converting very low frequency signal [86, 87], which is major neural signal bandwidth. The first order incremental A/D converter [86, 87] can be a solution for digital conversion of frequency range up to few hundreds Hz. It characterizes a

hybrid between a Nyquist-rate dual slope converter and an oversampling Delta-Sigma converter. The main difference to the dual slope converter is the fixed integration period while varying in dual slope converter. It is also very similar to oversampling Delta-Sigma modulator in structure but has a reset-able integrator and counter.

The main drawback of such an incremental Delta-Sigma converter is long required time for one sample conversion. It depends largely on the resolution of converter, leading to high power consumption. The conversion periods are increased to factor of 2 for one bit resolution increment. The required clock frequency can be equated to F_{clock}=$F_{sample}(2^N+2)$, where F_{clock} refers required clock frequency, F_{sample} is the sampling frequency, and N is ADC resolution. Because of this, for the higher frequency range up to $10KHz$ which is highest frequency bandwidth of neural signals, the first order incremental ADC may not be a suitable solution.

Area and power might be two major constraints in designing an ADC in neural recording system. One option suitable under these constraints is the use of extended counting ADC [96, 129]. Extended counting ADC performs combined conversion sequence of first order incremental ADC and algorithmic ADC. In other words, for one A/D conversion, the converter passes through two stages. In the first stage, the converter acts as a first-order incremental converter to convert the most significant bits. Then in the second stage, the same hardware is used to convert the least significant bits by an algorithmic A/D conversion technique. By extended counting ADC, the required conversion time per one conversion can be dramatically reduced compared to the first order incremental ADC. For example, the required number of clocks per one sample of 13-bit A/D conversion is 16.5 with double sampling feature [129]. Another option for the digital conversion in neural recording can be

a ratio-independent algorithmic ADC [128]. The total conversion time per one A/D conversion is linearly proportional to the resolution as $4N$, where N is resolution. However, it uses only one amplifier and one latch to the complete conversion while most similar structures need one additional comparator with an amplifier and a latch. Less power consumption can be expected by this property. Additional power saving was achieved by a dynamically biased operational amplifier.

3.4 Power Harvesting System for Bio-implantable Devices

In order to supply enough power for neural signal processing in an implantable system, most interfaces capable of transmitting the neural information use wires. An analog stage for multi-channel recording requires a number of wires equal to the number of channels, leading to restriction of movement and poor scalability. Indeed, studies have shown that exposure of enriched environment is beneficial for faster recovery from brain injuries [46, 47]. In order to avoid the spacial confinement, a wireless neural recording system supplied by small battery can be equipped as an option however it is still too large to fit in cranial implantation. Additionally, it requires a hole to be implanted with the battery in skull, leading a serious infection to the epidermis [48, 49]. Safer and promising alternative to the problem is using wireless power transfer or harvesting through inductive coupling. The initial principle of the techniques was taken from RFID communication [137]. Testing and emulating the effect of human tissue by introducing water bearing colloids between two coils, it was shown that the power transfer through inductive coupling within short distance

results in high efficiency [123]. The block diagram of an inductive coupling power harvesting system for implantable devices is illustrated in Figure 3.5. The transponder (in the right side of the figure) consists of a clock recovery, a power recovery, and a modulation/data processing block. The reader (in the left side of the figure) supplies power through inductive coupling and recover data from a transponder side.

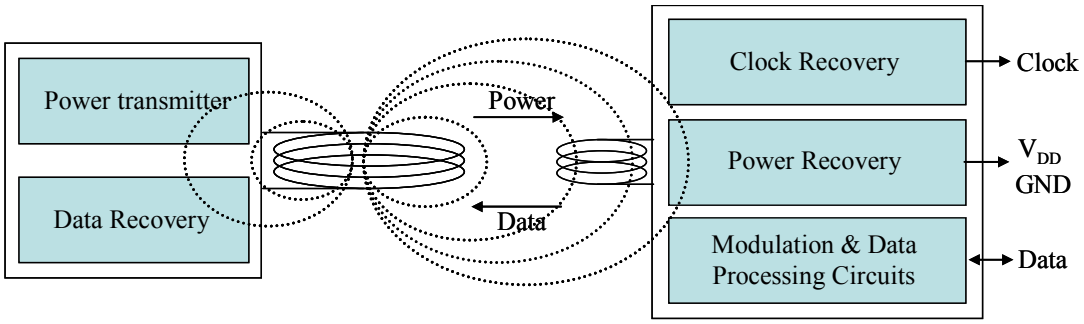


Figure 3.5: Block diagram of inductive coupling telemetry system for implantable devices.

Chapter 4

Low-Power Low-Noise Neural Amplifier in 0.18μm FD-SOI Technology

4.1 Summary

For recording of neural signals from large population of neurons, stringent constraints are imposed on the design of neural amplifiers. We have designed neural amplifier in Fully Depleted Silicon-on-Insulator (FD-SOI) technology in order to achieve lower power consumption, smaller area, and better noise efficiency factor compared to the standard bulk processes. A symmetric pseudo resistor was realized with resistances on the order of $10^{15}\Omega$, enabling a low cut-off frequency of 0.6mHz. The designed neural amplifier occupies an area of $0.004mm^2$, with simulated performance demonstrating an input-referred noise of $3.07\mu V_{rms}$ and a

power consumption of 6μW. The fabricated chip was tested and the improvements are discussed.

4.2 Introduction

The development of a direct neural interface with the central and/or peripheral nervous system has been a goal of the neuroscience and biomedical engineering communities for many decades. The knowledge gained from neural recording is one of the main requirements to both fundamental research in how spatial population of somatosensory neurons encode mechanical stimuli (which occur during touch, joint movements, and muscle constrictions) and the engineering feedback-controlled functional electrical stimulation (FES) of muscles used in locomotion for paralysis victims [98, 99].

The most critical block in neural recording system is low-power low-noise neural amplifier which is the first stage in the neural recording system. There have been considerable research efforts in the design of low-power low-noise neural amplifiers in recent years in bulk CMOS processes [93, 100, 102, 103, 104]. MOS-bipolar pseudoresistor element was used to achieve very low cut-off frequency in these designs.

To achieve lower power consumption, smaller area, and better noise efficiency factor, FD-SOI process [107], was used in the design of the amplifier. FD-SOI process results in parasitic capacitance reduction due to dielectric reduction, smaller leakage current, and high noise immunity from on-chip digital circuitry [108, 109]. Since the conventional bulk CMOS technology has the serious drawback of high leakage current as the transistor feature size is scaled down, design in bulk CMOS technology

would meet an unavoidable problem in terms of power and noise, which are the most important metrics for neural amplifier design. As the design of neural recording system targets to implement fully implantable chip with integrated power harvesting and telemetry, neural amplifiers and analog-to-digital converters, integration of such a system in 3D technology could offer considerable advantages. Different functional blocks of the system could be designed in different vertical tiers, reducing significantly the overall area and decreasing the effects of interconnections. For example, large inductor needed for power harvesting in inductive coupling link could be designed in back RF metal layer and could occupy the whole 2D area of the chip on that metal level.

We designed low-power, high noise-efficiency-factor (NEF) neural recording amplifier having a fully differential structure to minimize the effects from digital circuitry and fully symmetric MOS resistor element. Simulation results are presented in the following section.

4.3 Neural Amplifier Design

Figure 4.1 shows the schematic of amplifier design. The whole structure of the neural amplifier is similar to previous design [100] so that the midband gain A_M is set by C_1/C_2, and the bandwidth by $g_m/A_M C_L$, where g_m is the transconductance of the operational transconductance amplifier (OTA).

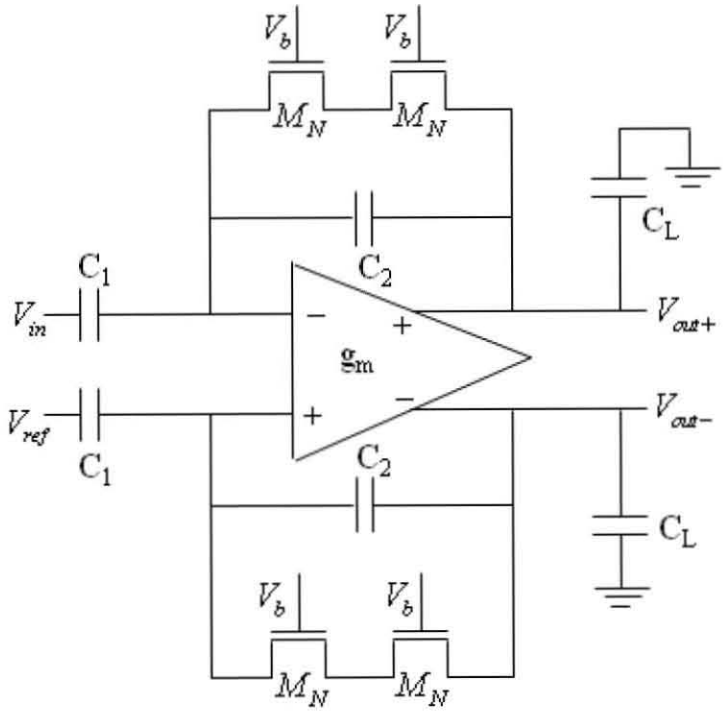


Figure 4.1: Schematic of fully differential neural amplifier in MITLL 0.18μm FD-SOI Process.

4.3.1 Symmetrical MOS resistor element

The cut-off frequency of DC rejecting high-pass filter has to be set at very low value, in mHz range, due to frequency content of the neural signal. To avoid using large off-chip capacitor, large on-chip resistor is needed. Using MOS transistor operating in subthreshold region as a high-resistive element was first proposed in [105]. In [93], MOS-bipolar devices acting as pseudoresistors are used to create high floating resistances in the range from $10^{11}\Omega$ to $10^{14}\Omega$. However, the diode-connected PMOS devices give unsymmetrical resistance. For the negative V_{GS} voltage, the devices behave as diode connected PMOS transistors, while for the positive V_{GS}, they behave as parasitic p-n-p bipolar transistors. The resistance will depend on the sign of voltage

across the transistor. This causes dependance of the cut-off frequency of the high-pass filter on the input signal and introduces distortion of the output signal. The value of the resistance is not controlled.

In FD-SOI process, MOS transistor operating in subthreshold can provide higher resistance than in bulk process and also a symmetrical one with respect to sign of the voltage across it. If the gate voltage is much lower than drain and source voltage for NMOS transistor, lower than 300mV for minimum size square transistor, the equivalent circuit represents two back-to-back diodes between source and drain. Figure 4.2 shows the simulated current-voltage characteristic of NMOS transistor, with size of 0.6μm $\times$ 0.6μm, with the gate voltage fixed at 0.2V and voltage across the pseudo-resistor varied from -200mV to 200mV, with the common-mode value set at 750mV. The equivalent resistance is on the order of $10^{15}\Omega$ for a linear region of almost 200 mV and is not dependent on the gate voltage. If the gate voltage is further increased, the transistor will behave as transistor in subthreshold region with the body-effect coefficient being almost equal to one in the bulk-process, as the body is not fully depleted until gate voltage is lower than drain-source voltage. Figure 4.3 shows the simulated current-voltage characteristic of NMOS transistor for this case with the gate voltage fixed at 0.6V. The dependence of the equivalent resistance on the biasing voltage V_b of the NMOS element (M_N in Figure 4.1) is shown in Figure 4.4.

To reduce the distortion due to large output signals two series connected pseudo MOS elements can be used so that the total time constant is set to $2R_MC_2$, where R_M refers to resistance of pseudo MOS element. Therefore, the low cut-off frequency of neural amplifier is determined by $1/(2\pi 2R_MC_2)$.

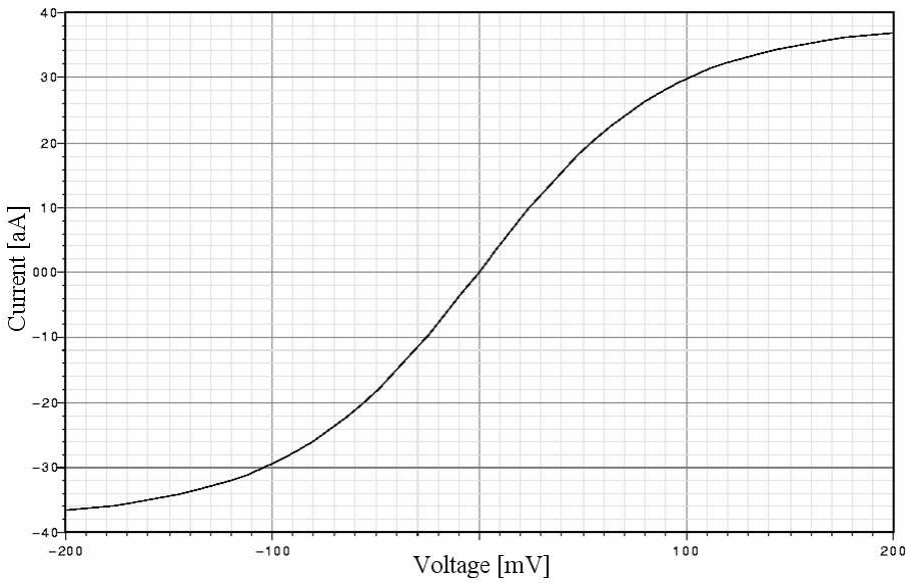


Figure 4.2: Simulated current-voltage relationship of NMOS element (M_N in Figure 4.1) for voltage Vb set at 0.2 V.

4.3.2 Low-Noise Low-Power OTA design

Since FD-SOI devices offer near-ideal body effect coefficient of unity (1.6 for bulk CMOS device), they are expected to have 30-40 percent higher saturation current than in a bulk devices with similar parameters [108]. This makes it possible to achieve the same performance at lower power level.

Figure 4.5 presents the schematic of operational transconductance amplifier (OTA) [93, 100, 101]. Basic circuit structure is a current-mirror based OTA [106] with two cascode transistors for each output. Since there is no noise contribution for adding cascode transistors they can be used to increase OTA gain without affecting the performance. Also, the output voltage swing is limited by the linear range of the high-resistive element, not by the cascode transistors. The main trade-offs in the OTA design are between noise, power, and stability. If we only consider the

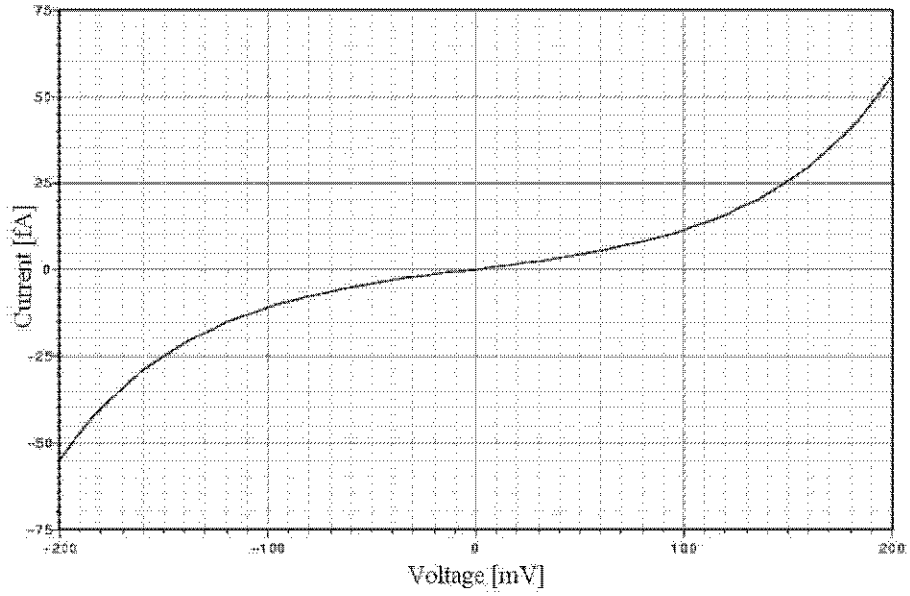


Figure 4.3: Simulated current-voltage relationship of NMOS element (M_N in Figure 4.1) for voltage Vb set at 0.6 V.

power consumption, the maximum performance may be obtained when the value of the transconductance/drain current ratio (g_m/I_d) is the largest. However, the input referred thermal noise of OTA is given as

$$\overline{v_{in,thermal}^2} = \frac{16kT}{3g_{m1}}[1 + \frac{g_{m3}}{g_{m1}} + \frac{\frac{g_{m3}^2}{g_{m5}}}{g_{m1}} + \frac{g_{m7}\frac{g_{m3}^2}{g_{m5}^2}}{g_{m1}}]\Delta f \tag{4.1}$$

g_m/I_d ratio and size of transistors should be considered to minimize input referred thermal noise contribution. As total power consumption is determined by biasing current, we have chosen a lower biasing current. From the noise analysis, input transistors M_1 and M_2 should be sized with as large W/L ratio as possible so that a maximum g_m/I_d ratio is obtained. In the same manner, the noise contribution of transistors M_3 through to M_8 can be minimized by choosing small W/L ratio

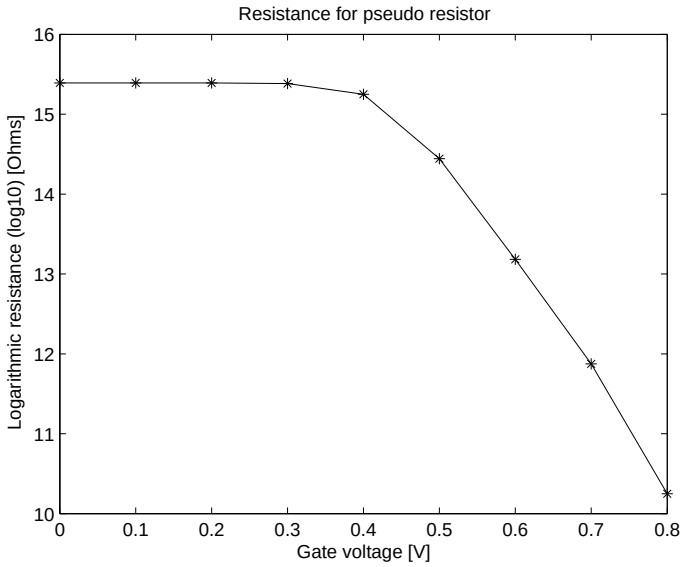


Figure 4.4: Equivalent resistance of NMOS element as function of gate voltage Vb).

or minimizing g_m/I_d ratio. Increasing the length of these transistors gives rise to parasitic capacitances, causing second pole of OTA to move closer to dominant pole created by load capacitor C_L and reduces phase margin. This effect is reduced in FD-SOI process, since the parasitic capacitance is smaller than in bulk process and larger phase margin is obtained. Further minimization of noise contribution can be achieved by sizing transistors M_5 and M_6 properly so as to make higher $g_{m5,6}/I_d$ ratio than $g_{m3,4}/I_d$ ratio. Effect of flicker or $1/f$ noise is minimized by choosing pMOS transistor for inputs and by increasing gate area of the transistors in design. The input transistors M_1 and M_2 are designed as H-gate transistors with separate source bulk connection to improve the matching between them at the expense of increased area. The sizes of all transistors in OTA and their respective g_m/I_d ratios are given in Table 4.1.

Table 4.1: Transistor sizes and their respective g_m/I_d ratios.

Device	**W/L(μm)**	$I_d(\mu A)$	$g_m/I_d(V^{-1})$
$M_{1,2}$	210/0.5	1	34.08
$M_{3,4}$	0.6/9.6	1	5.22
$M_{5,6}$	1/9.6	1	7.14
$M_{7,8}$	1.6/6	1	4.62
$M_{9,10}$	3.2/0.8	1	11.33
$M_{11,12}$	1.6/0.8	1	24.86
$M_{13,14}$	8/4	2	8.33

4.3.3 Common mode feedback circuit

For the implementation of common-mode feedback circuit, we have chosen continuous-time circuit shown in Figure 4.6. The common-mode output voltage is set to $V_{DD}/2$ or $0.75V$. If the output common-mode level increases, current of M_{15} and M_{18} will increase and the current of $M_{16,17}$ will decrease. This causes increment in V_{CMFB} and makes the V_{SG} of $M_{7,8}$ decrease, followed by decrease in common-mode output voltage.

4.4 Simulation Results

The circuit was simulated using Cadence SpectreS simulator with BSIMSOI version 3.1 level 11 transistor model. Since the desirable amplifier gain is 40dB or 100, we set C_1 to 5pF and C_2 to 50fF. The lower parasitic capacitances in FD-SOI process enable use of smaller capacitors in the design of amplifier, significantly reducing the area of the amplifier. 8.5pF capacitors are used as load capacitor, C_L. Figure 4.7 presents the simulated transfer function of neural amplifier. Table 4.2 shows the performance summary of the designed neural amplifier. The gain was simulated as

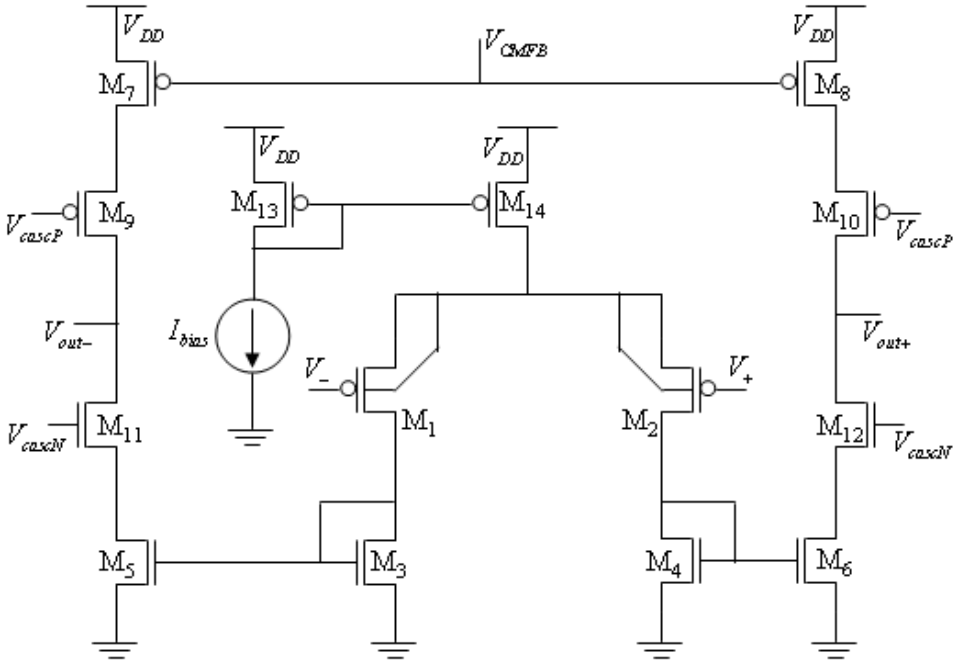


Figure 4.5: Schematic of operational transconductance amplifier used in low noise amplifier

39.5dB in passband, from 0.000635Hz to 7.1kHz. The simulated phase margin was 78 degrees. The low cutoff frequency is 0.000635Hz which is quite low due to very high resistance of symmetrical resistor. Since we use only 2μA as biasing current total supply current is almost 4μA leading to total power consumption of 6μW. The current consumption from biasing circuits is excluded here. Integrated input referred noise was simulated as $3.07\mu V_{rms}$ and the noise efficiency factor (NEF) is calculated as 2.8. $1/f$ noise parameters are currently not available, but we are expecting that $1/f$ noise contribution would not increase the noise level significantly, as shown in [93]. The layout of the amplifier occupies an area of $0.004mm^2$ and is shown in Figure 4.8.

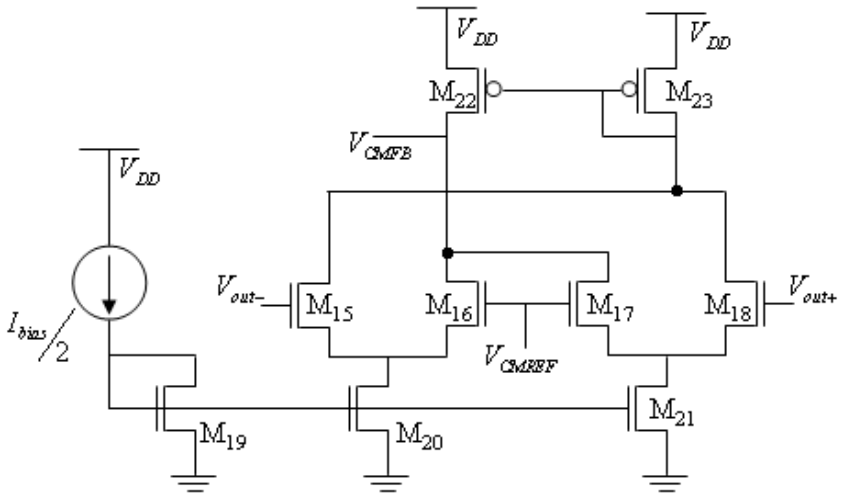


Figure 4.6: Schematic of continuous-time common mode feedback circuit

4.5 Measurements

The designed neural amplifier was fabricated through MIT Lincoln Laboratory 0.18μm 3-Tier FD-SOI technology. The amplifier was designed on the Tier one while an ADC is on the Tier 2 and power recovery circuit with a coil was fabricated on the Tier 3. Figure 4.9 shows a microscope image for the fabricated chip. Only Tier 3 can

Table 4.2: Performance summary of designed neural amplifier

Parameter	**Neural Amplifier in SOI**
Supply voltage	1.5V
Supply current	4μA
Gain	39.5dB
Phase margin	78 degrees
Low frequency cutoff	635μHz
High frequency cutoff	7.1kHz
Input referred noise(μV_{rms})	3.07
Noise efficiency factor	2.8
Area	0.004 mm^2

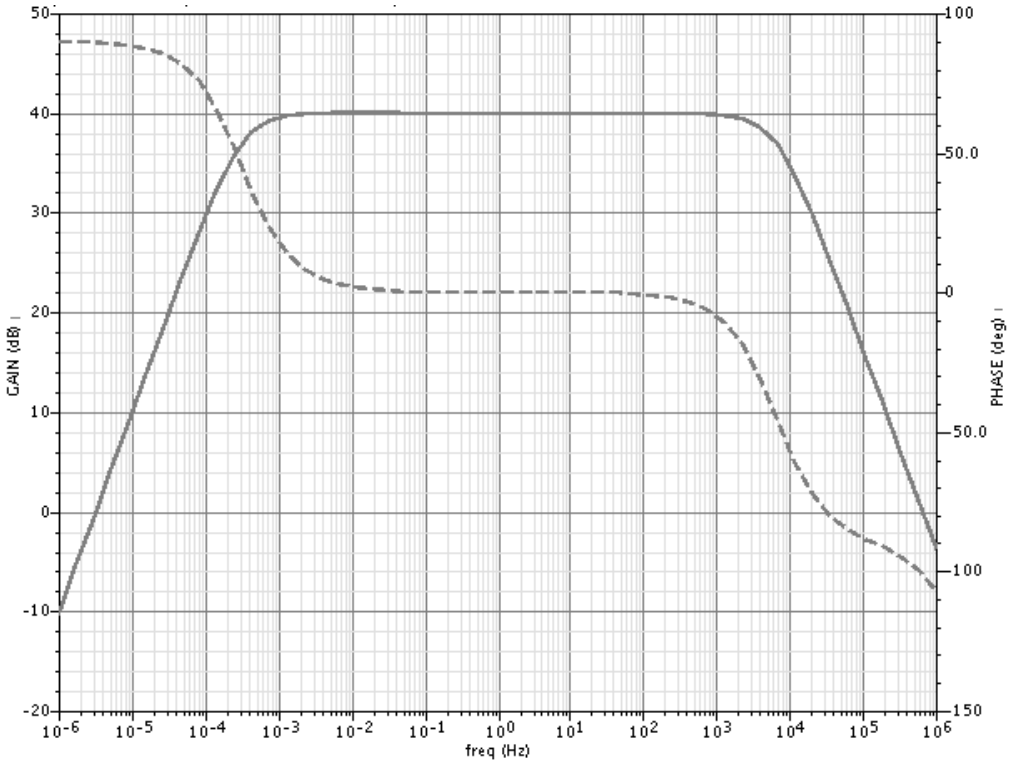


Figure 4.7: Simulated transfer function of amplifier. Midband gain is 39.5dB. Low frequency rolloff occurs at 0.000635Hz, high frequency rolloff at 7.1kHz. Phase margin is 78 degrees.

be taken by microscope, therefore we can see a big coil on it.

The chip is tested with a custom designed general purpose mixed signal test station equipped with PC interface as well as 32-channel analog frontend introduced in Chapter 6. The test station is interfaced to PC through data acquisition card NI-6259 (National Instruments) for characterization and real time measurement. Test station is comprised of a motherboard and a daughter board. A motherboard consists of interface circuitry to PC and FPGA, digital-to-analog converters for providing biasing voltages, 3.3V power regulators. A daughter board contains the designed

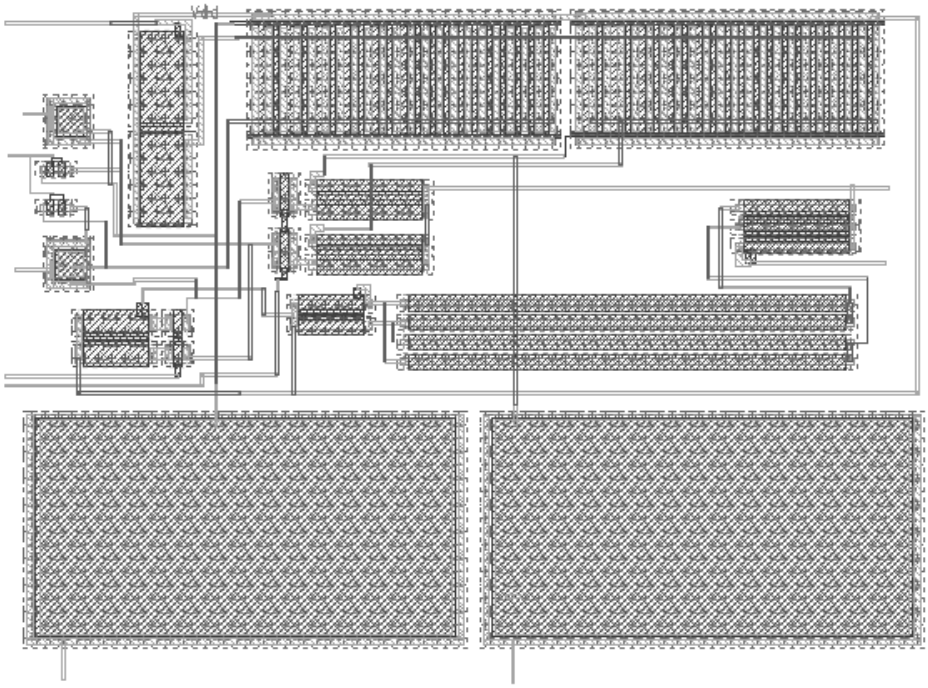


Figure 4.8: Layout of the designed neural amplifier.

ASIC with a socket and interface connectors providing a connection flexibility to motherboard through wire-up. Figure 4.10 shows a picture of the teststation that is the daughter board equipped on a motherboard. The testing environments are the same as what we have done in 32-channel analog frontend design except daughter board I/O interface.

The chip is supplied by a 1.5V powered by analog output from NI-6259 card. It has total 18 pin interfaces: 2 signal inputs, 12 voltage biasing, 2 signal outputs, one Vdd, and a ground.

Figure 4.11 and 4.12 presents a capture of measured transient response for the designed FD-SOI preamplifier and the FFT plot, respectively. It characterizes a gain of 1.5 with $60Hz$ power line interference at $1KHz$ $3mV$ input sinusoid wave. It also

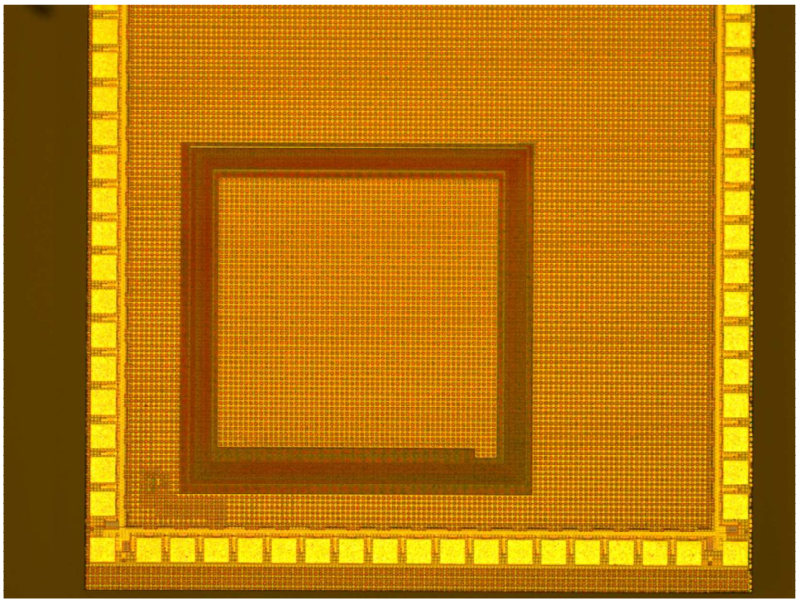


Figure 4.9: Microscope image for the first layer of the fabricated neural amplifier.

shows a deviated common-mode voltage which is out of control. There can be possibly several reasons for this behavior. One can be the transistor operating region. Four NMOS transistors M3, M4, M5, M6 in Figure 4.5 and two current sources M20 and M21 in the Figure 4.6 were not operated in the deep saturation region. Actually, they are under moderate inversion region and have been designed as too long transistors to minimize input referred noise. Additionally, the threshold voltage might be subject to a lot variation among transistors on the same die which is major drawback of Fully depleted SOI technology. The corner simulation and mismatch Monte Carlo simulation can be utilized to see the imperfections but unfortunately only mismatch Monte Carlo simulation is available at this time from MIT process provider. The 100-times statistical transistor mismatch were simulated by Monte Carlo simulation and plotted from the Figure 4.15 to 4.22. Also, package parasitic capacitance and

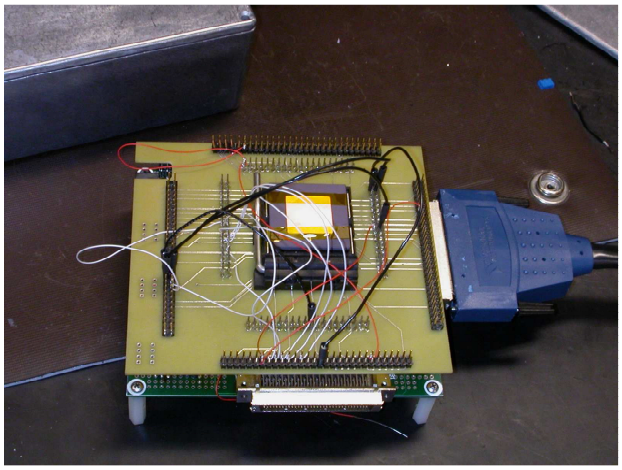


Figure 4.10: A daughter board equipped test station for the designed amplifier.

resistance as well as PCB board parasitics might affect to the performance.

MITLL provides NMOS and PMOS variation models for the Monte Carlo simulation but not capacitor variation model. The capacitor might have only ± 1 percent capacitance variation but we have assumed ± 5 percent variations for capacitors C_1,C_2,C_3, and C_4 in Figure 4.13 and run Monte Carlo simulation with extreme combinations of capacitance variation. Table 4.4 summarizes the applied capacitance combinations for 5 Monte Carlo simulations: Normal, Mismatch1, Mismatch2, Mismatch3, and Mismatch4. For each capacitance mismatch combination, 100 times Monte Carlo simulations at 27^oC were performed with variations of threshold voltage (VTHO), physical length (LINT), and width (WINT). The parameters var-n-vtho, var-p-vtho, var-lint, and var-wint linearly sum respectively with the default VTHO, WINT, and LINT parameters in the NMOS and PMOS, thus simulating a linear threshold voltage and physical dimension shift. The applied variations for parameters var-wint, var-lint, var-p-vtho, and var-n-vtho,

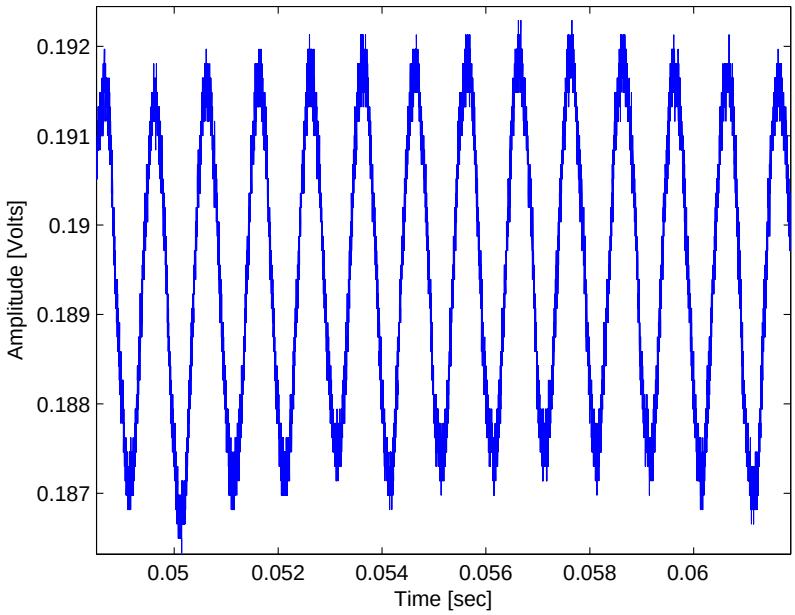


Figure 4.11: A transient response in testing for the designed amplifier on FD-SOI.

during simulation are shown through Figures 4.14, 4.16, 4.18, 4.20, and 4.22 for corresponding capacitance mismatch. The variation values are applied with a little bit bigger values than MITLL's collected data. Their process target range and robustness range was borrowed in Table 4.3. A magnitude and phase margin was also plotted for each case, and Figure 4.15, 4.17, 4.19, 4.21, and 4.23 represent magnitude and phase margin variations. Table 4.5 summarizes the maximum and minimum values for magnitude and bandwidth variations.

Table 4.3: Target and Robustness Values for Global Parameters [110]

Parameter	Target min.	Target max.	Robust min.	Robust max.
VAR-N-VTHO	-75mV	+75mV	-200mV	+100mV
VAR-P-VTHO	-75mV	+75mV	-100mV	+100mV
VAR-LINT	-20nm	+20nm	-30nm	+30nm
VAR-WINT	-50nm	+50nm	-	-

Table 4.4: Applied Capacitance Variations for Monte Carlo Simulation

Capacitors	Normal	Mismatch1	Mismatch2	Mismatch3	Mismatch4
C1	5.00541pF	4.75514pF	5.25568pF	4.75514pF	5.25568pF
C2	5.00541pF	4.75514pF	5.25568pF	5.25568pF	4.75514pF
C3	50.054fF	52.5567fF	47.5513fF	52.5567fF	47.5513fF
C4	50.054fF	52.5567fF	47.5513fF	47.5513fF	52.5567fF

Table 4.5: Magnitude and Bandwidth Responses for Monte Carlo Simulation

Mismatches	Max. variation	Min. variation
Normal	39.7dB @0.792Hz∼6.904KHz	38.57dB @0.497Hz∼8.038KHz
Mismatch1	38.86dB @0.758Hz∼7.384KHz	37.82dB @0.485Hz∼8.679KHz
Mismatch2	40.55dB @0.831Hz∼6.396KHz	39.32dB @0.515Hz∼7.499KHz
Mismatch3	39.66dB @0.789Hz∼6.881KHz	38.54dB @0.5Hz∼8.03KHz
Mismatch4	39.66dB @0.789Hz∼6.881KHz	38.54dB @0.5Hz∼8.03KHz

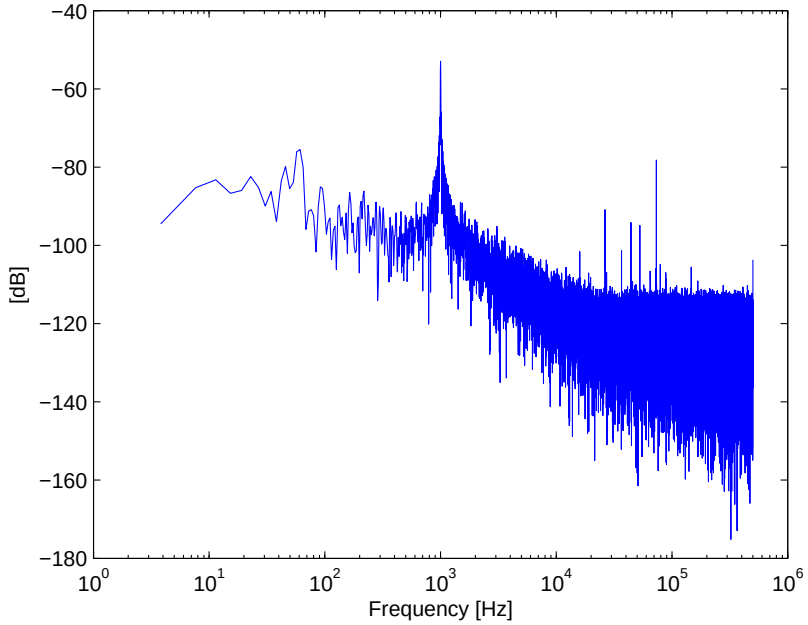


Figure 4.12: A FFT response for the captured transient response in the Figure 4.11.

4.6 Conclusion

Modern implantable neural recording systems should accommodate thousands of recording channels to be able to record signals from large populations of neurons. The neural amplifier, most critical components in the design, should consume less power and area, and also have high noise immunity to digital switching in subsequent analog to digital converter, implemented on the same substrate. FD-SOI technology enables design of neural amplifier with better power and noise performance than in bulk technologies. This was demonstrated through design and simulation of a neural amplifier using symmetrical pseudo resistors in MITLL 0.18μm FD-SOI process.

The designed neural amplifier was fabricated and tested on the custom designed test station. Through Monte Carlo simulation, the effect for the variations of

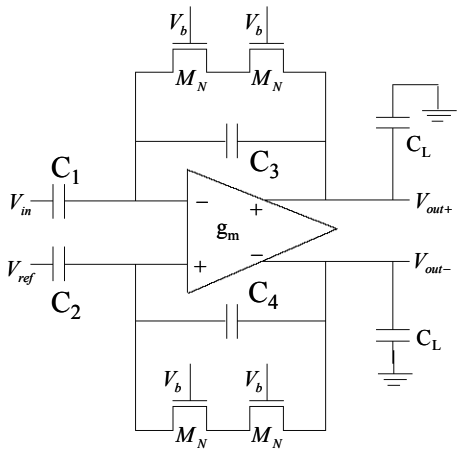
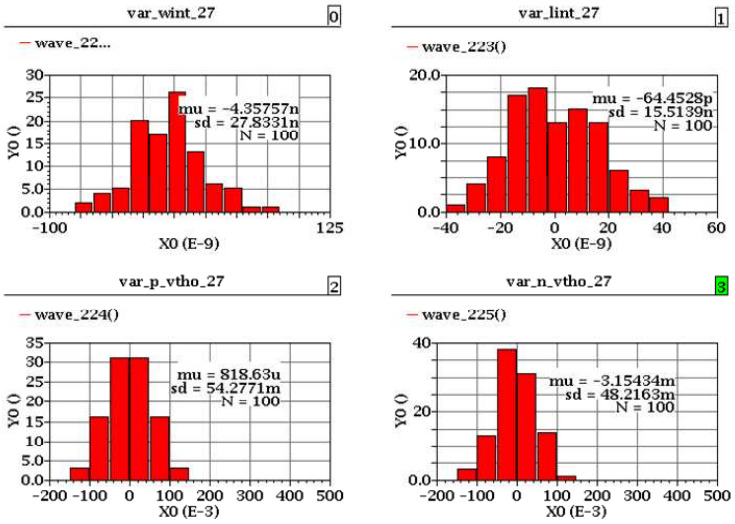


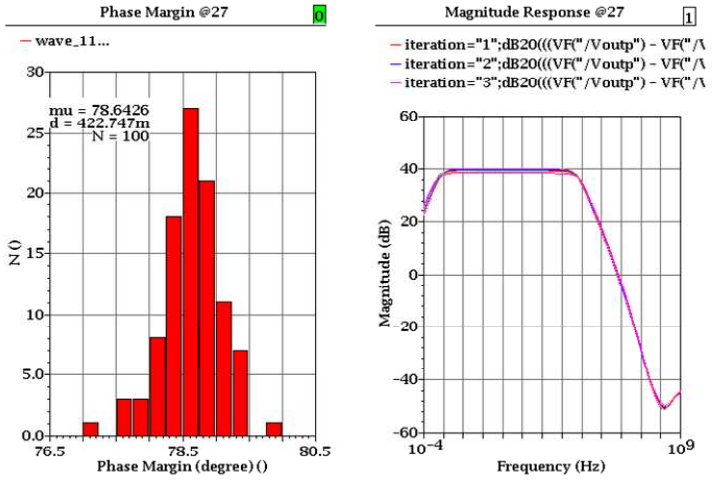
Figure 4.13: Amplifier structure and the capacitor names for the Monte Carlo simulation.

parameters and capacitors were summarized. Acceptable level of magnitude, phase, and bandwidth variations were shown in the Monte Carlo simulations. The test board noise as well as transistors working on the edge of saturation region might have affected to the performance of fabricated amplifier.



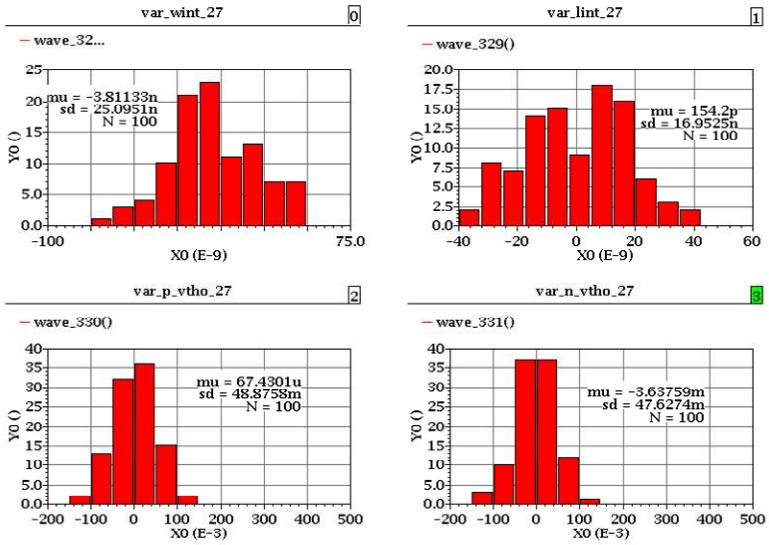
0% C_1, 0% C_2, 0% C_3, and 0% C_4

Figure 4.14: Applied parameter variations in 100 times Monte Carlo Simulations at room temperature. No capacitor mismatches applied.



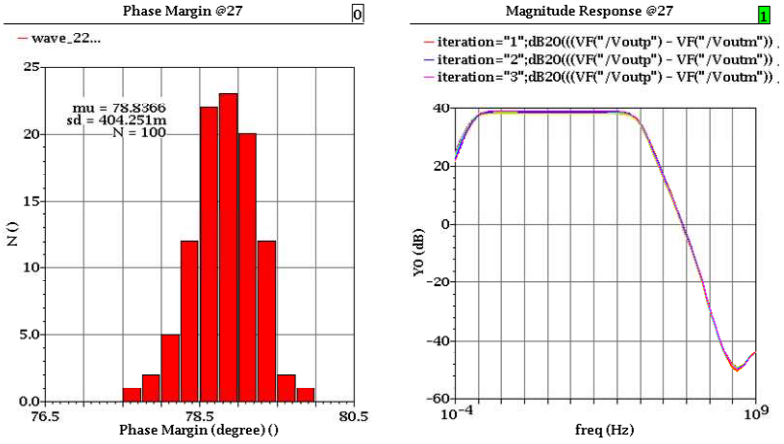
0% C_1, 0% C_2, 0% C_3, and 0% C_4

Figure 4.15: Phase margins and magnitude responses for 100 times Monte Carlo simulation. No capacitor mismatches applied.



-5% C_1, -5% C_2, +5% C_3, and +5% C_4

Figure 4.16: Applied parameter variations in 100 times Monte Carlo Simulations at room temperature. Capacitor values for mismatch1 in Table 4.4 were applied.



-5% C_1, -5% C_2, +5% C_3, and +5% C_4

Figure 4.17: Phase margins and magnitude responses for 100 times Monte Carlo simulation. Capacitor values for mismatch1 in Table 4.4 were applied.

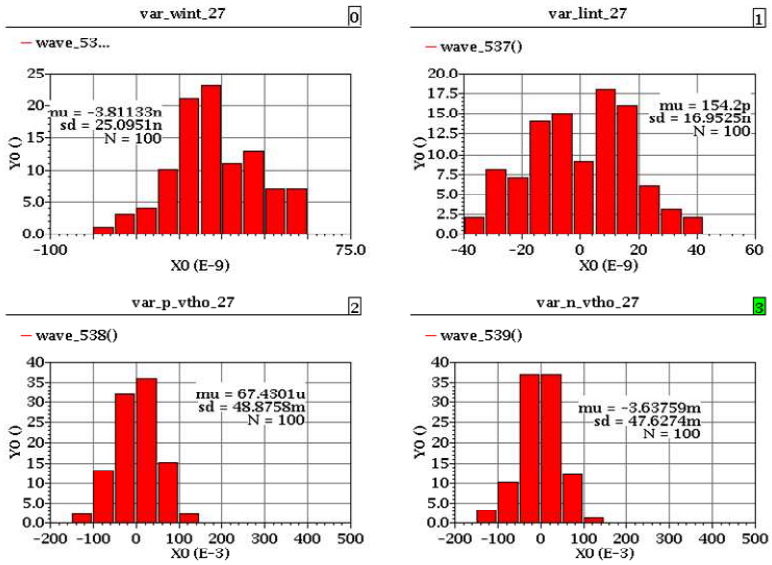


Figure 4.18: Applied parameter variations in 100 times Monte Carlo Simulations at room temperature. Capacitor values for mismatch2 in Table 4.4 were applied.

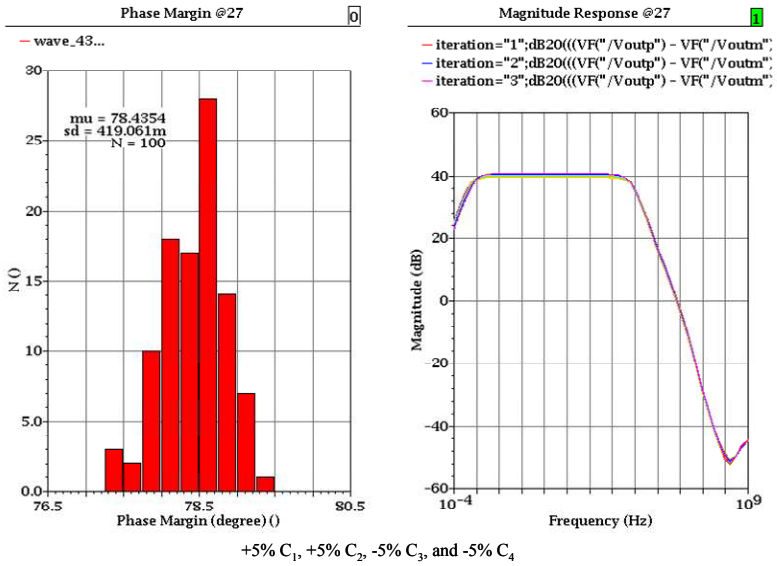
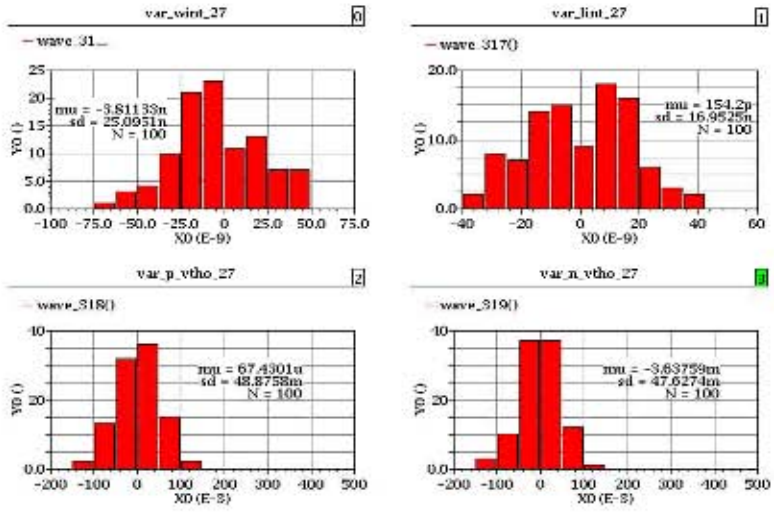
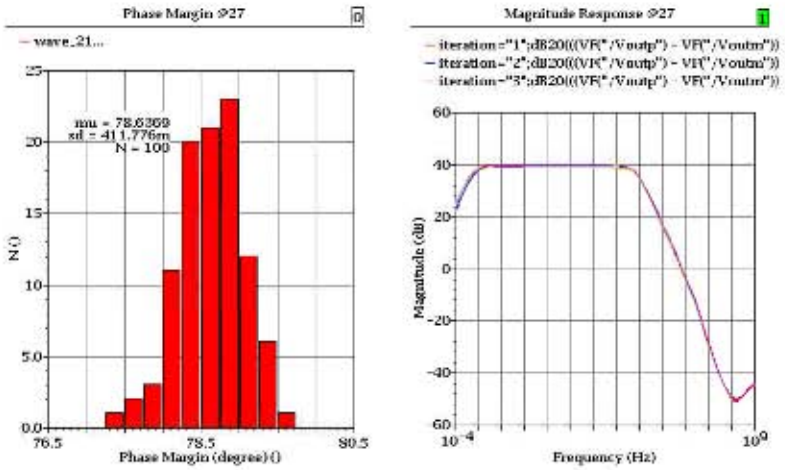


Figure 4.19: Phase margins and magnitude responses for 100 times Monte Carlo simulation. Capacitor values for mismatch2 in Table 4.4 were applied.



-5% C_1, +5% C_2, +5% C_3, and -5% C_4

Figure 4.20: Applied parameter variations in 100 times Monte Carlo Simulations at room temperature. Capacitor values for mismatch3 in Table 4.4 were applied.



-5% C_1, +5% C_2, +5% C_3, and -5% C_4

Figure 4.21: Phase margins and magnitude responses for 100 times Monte Carlo simulation. Capacitor values for mismatch3 in Table 4.4 were applied.

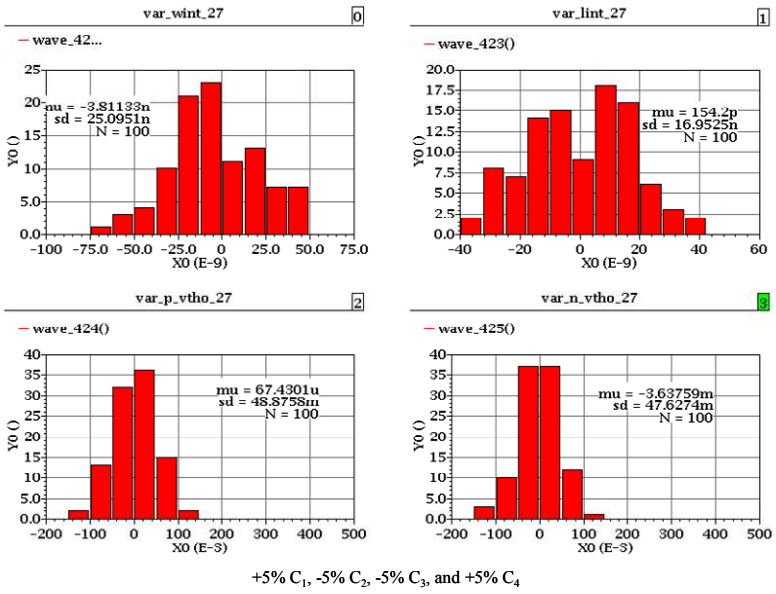


Figure 4.22: Applied parameter variations in 100 times Monte Carlo Simulations at room temperature. Capacitor values for mismatch4 in Table 4.4 were applied.

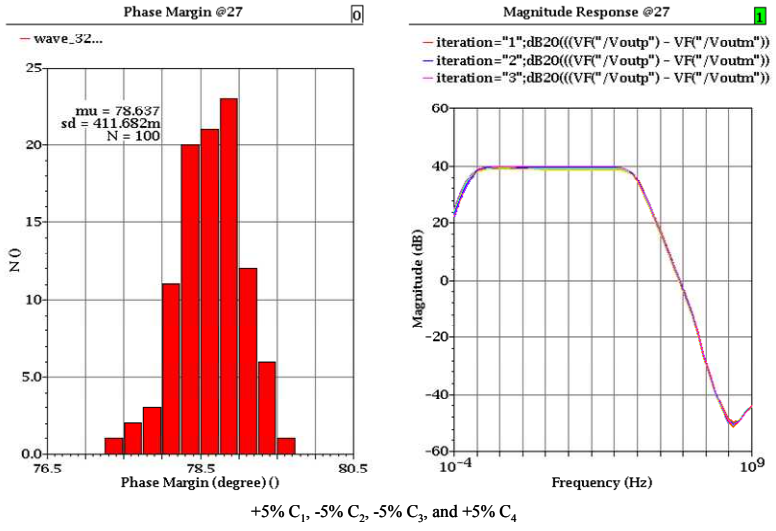


Figure 4.23: Phase margins and magnitude responses for 100 times Monte Carlo simulation. Capacitor values for mismatch4 in Table 4.4 were applied.

Chapter 5

An Efficient Power Harvesting System

5.1 Summary

Power transfer through inductive coupling highly relies on the coupling factor and ultimately on distance between coils. A design of low-power, high-efficient CMOS implantable power harvesting system for low coupling factor is presented in TSMC 0.18μm technology. A clamping charge pump and LDO (Low-Drop-Out) regulator together make the system highly-efficient at $5mA$ load. A low-power high-PSRR CMOS voltage reference provides a temperature-insensitive reference ranging between 0^oC and 80^oC to the designed 3.3V LDO.

5.2 Introduction

An implantable neural recording system is becoming one of most important components in the field from a neuro-science research to an implementation of human-machine interfaces. The capability of transferring large population of neural signals through inductive coupling is a critical bridge to capture and monitor brain/peripheral electrical activities and give freedom of locomotion. Bio-implabtable system such as multi-channel stimulators, neural amplifiers, and their supporting mixed signal circuitry etc. need stable and strong-enough electrical power to gather and process the neuronal information. Previous energy harvesting system [123] was successfully designed and implemented with high inductive coupling factor k. A simplified model of the inductively coupled system was proposed [123] and re-presented in figure 5.1. A recovered power u_2 relies on many parameters according to equation (5.1) and is proportional to its coupling factor k between two coils. It is determined for the air coupling case empirically [123] as in equation (5.2).

$$u_2 = \frac{\omega k \sqrt{L_1 L_2} i_1}{\sqrt{(\frac{\omega L_2}{R_L} + \omega R_1 C_1)^2 + (1 - \omega^2 L_2 C_1 + \frac{R_1}{R_L})^2}} \tag{5.1}$$

$$k = \frac{r_{transponder}^2 r_{reader}^2}{\sqrt{r_{transponder} r_{reader}} (\sqrt{x^2 + r_{reader}^2})^3} \tag{5.2}$$

where $r_{transponder}$, r_{reader} are coil radii for transponder and reader, respectively and x is the distance between them. As a distance is getting longer the factor k is smaller to the third power and the received power at the transponder can be low as not to recover the required power and data. Therefore, a charge pump or DC-DC converter must be considered to boost input power voltage, which should be used in

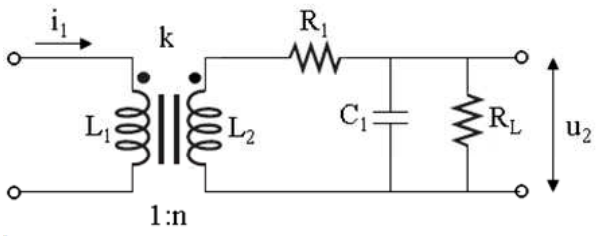


Figure 5.1: Simplified model of a inductively coupled system.

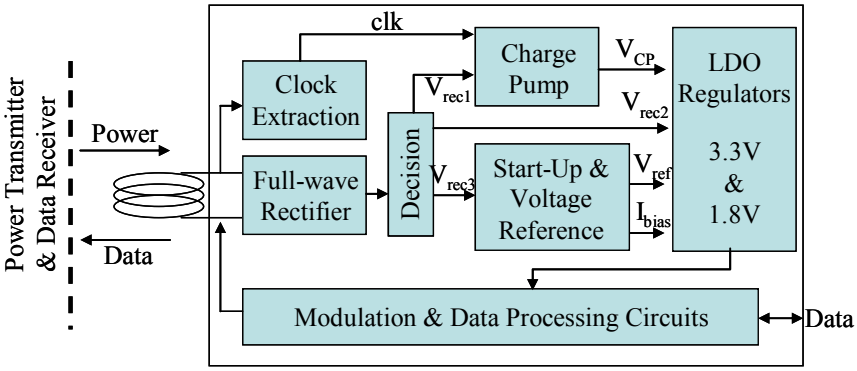


Figure 5.2: Block diagram of power harvesting system.

case low coupling factor k.

In this chapter, we present a low-power power harvesting system including a reliable charge pump (DC-DC converter), a temperature-insensitive voltage reference, and an efficient 3.3V LDO regulator in TSMC 0.18μm technology.

Figure 5.2 presents the proposed system block diagram. It consists of several sub-systems: Clock Generation, Full-wave Rectifier, Decision block, Charge Pump, Voltage Reference with Start-Up, 1.8V and 3.3V LDO Regulators, and Modulation and Data Processing Circuits. Through the inductive coupling, the input rectified voltage can be varied with certain voltage amplitude. In case enough power to the transponder it doesn't need to be processed by charge pump and directly goes to

LDO input, however it needs to be boosted in case of low coupling factor. A zener clamping circuit with a decision block can be utilized to detect lower coupling factor as well as protect following circuits. If the voltage from rectifier is not as much as an input of 3.3V LDO that makes stable output of 3.3V, the output of decision is connected to charge pump (V_{rec1} is activated and V_{rec2} is deactivated). If it is high enough to regulate the output of 3.3V LDO, the output of decision is shorted to input of 3.3V LDO regulator (V_{rec2} is activated and V_{rec1} is deactivated). The input of Start-Up and Voltage Reference could take any voltage level (V_{rec3}) between them. The utilized clock for the charge pump is $200kHz$ and it can be generated by Clock Generation from the initially recovered $4MHz$ clock. The Start-Up and Voltage Reference provides stable and ideally temperature-independent reference as well as biasing current to LDO regulaotrs. The LDO regulators can provide dual voltage power 3.3V and 1.8V to maximize the system power efficiency.

5.3 Design of Charge Pump

Charge pump (or DC-DC up converter) is used for generating higher voltages than regular power supply voltage. It has been typically utilized to produce high voltage for programming of nonvolatile memories, such as EEPROM, Flash memories [111], and driving analog switches in switched capacitor circuits [112]. A designed charge pump is dedicated to boost weakly rectified voltages and supply power for a 3.3V LDO regulator.

5.3.1 Charge Pump Selection

Most widely used charge pumps are originally based on Dickson charge pump [113] and clock booster (also called voltage doubler) [114]. Both structures of charge pump offer a capability of N-stage series connection, which ideally gives an output voltage equal to $(N+1)V_{DD}$. The efficiency and reliability must be taken into account to choose a structure in not only charge pump itself but whole system including LDOs. Considering 1.8V input rectified voltage, since the target LDO output is 3.3V the required charge pump output must be at least a voltage allowing a pass-transistor in LDO operated in saturation region but also it should not be too hgih to deteriorate LDO efficiency and power dissipation, which is directly determined by LDO input or charge pump output voltage. A single-stage charge pump might be the best choice if it is charaterized with small-loss and less-parasitic effects.

If all parasitic capacitances, clock frequency, and pumping capacitor size are neglected for a first order analysis, output voltage for Dickson structure is $2V_{DD}$-V_{th} while voltage doubler has a $2V_{DD}$. It has been proposed [112] to get rid of diode threshold voltage in Dickson structure, however added circuit techniques called CTS (Charge Transfer Switches) give another parasitic capacitance resulting in charge loss. Additionaly, V_{gs} for added switches and diode-connected transistors sufferred from gate-voltage stress of $2V_{DD}$ periodically which may give reliability issues in standard CMOS low-voltage devices.

5.3.2 Voltage Doubler Design and Operation

Figure 5.3 and 5.4 present the designed charge pump or voltage doubler. A core voltage doubler consists of two capacitors C_1, C_2, two cross coupled NMOS

transistors M_1, M_2, and two PMOS pass devices M_3, M_4. A source node of M_1 and M_2 has $2V_{DD}$ (assuming driving clock of capacitors uses the same V_{DD}) every clock cycle alternately and transfer higher voltage charge to output V_{CP} through transistors M_3 and M_4. The back gates of $M3$ and $M4$ are always connected to highest voltage or output ensuring no body effect. On the output side, two off-chip zener diodes, Analog Clamping, and Clock Modulator are used to ultimately control clock signals to be low ripple outputs as well as clamp unnecessarily-high voltages. It is good to remind that an unnecessarily boosted output makes LDO efficiency low. Whenever charge pump output is over the target ouput voltage which is programmed by zener diodes and Analog clamping, the following clock stops working, or if the charge is kept pumping but it needs to minimize the output ripple and maintain output level, Clock Modulator modulates pulses to make it smooth. When the charge pump output is over 3.6V the clamping zener diodes conduct and give the current to Analog Clamping. This current is mirrored by M_8 and make the clpEN node pull down. cpEN signal is finally transferred to clrz node of D-FlipFlop (DFF) in Clock Modulator. It is pointed out that D node is always connected to V_{DD} and DFF is cleared upon clpEN.

Figure 5.5 shows charge pump output voltage Vcp and the modulated clock $clkCP$ in Clock Modulator. When Vcp is over the 3.6V an Analog Clamping pulls down and clear the DFF. It makes Vcp discharged until pull clpEN up and clock start pumping again. Modulated clock keep the Vcp ripple voltage small and simulated ripple voltage is measured as less than $15mV$.

To increase driving capability, two 0.33μF off-chip capacitors (C_1,C_2) and $200KHz$ clock are utilized to achieve 5mA loading capability. One $200nF$ off-chip smoothing capacitor (C_{OUT}), two 3.3V zener diodes are also used in this design.

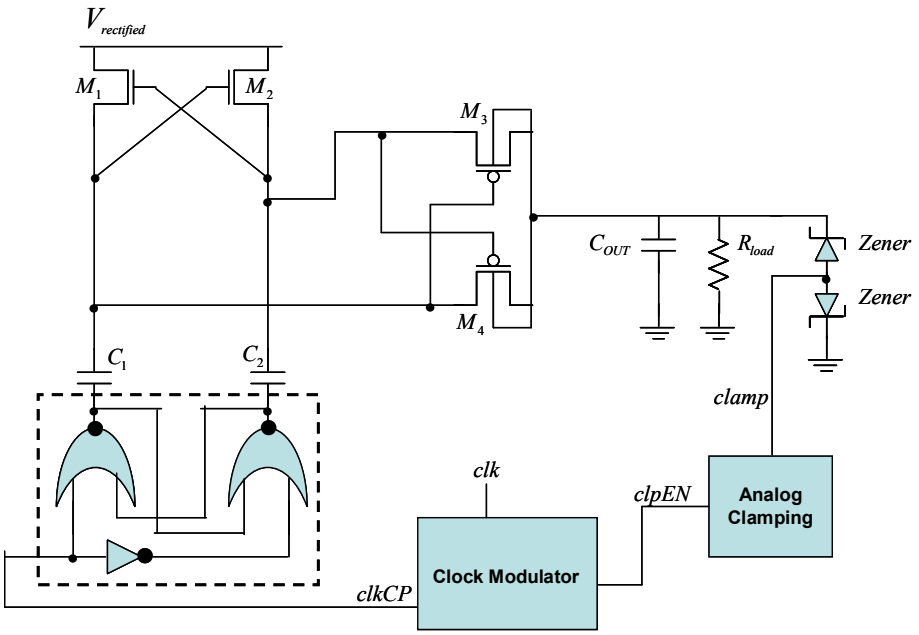


Figure 5.3: Schematic of charge pump using analog clamping and clock modulator.

5.4 A CMOS Voltage Reference Design for Implantable Devices

Voltage reference is an essential functioning block and widely used in industrial applications, home appliances, computers, sensor nodes, and implantable medical devices.

Its temperature requirement is to maintain a constant voltage in a range between -45C and 155C in industry applications, while implantable medical devices have relatively less-stringent temperature requirements. It needs a temperature range such that a life organ can maintain the life.

The previously designed voltage references [115, 116, 118] use several P-type parasitic bipolar transistors in CMOS to implement Bandgap reference voltage,

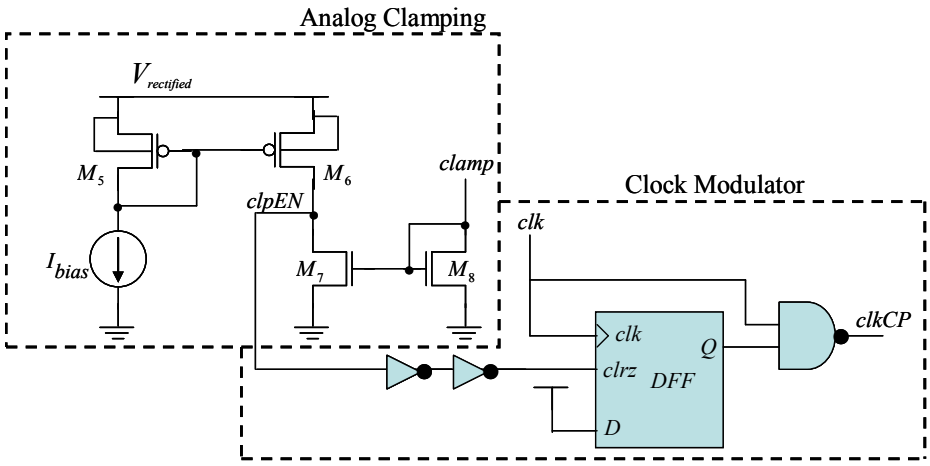


Figure 5.4: Circuit diagram of analog clamping and clock modulator.

although they are leaky devices due to their low beta. The leakage current is inevitable by the relation of $I_b = I_c/\beta$.

A voltage reference making use of weak inversion region of standard CMOS devices is presented in figure 5.6. It consists of three parts: Start-up (M_{18}, M_{19}, C_1, C_2), cascode biasing loop generating PTAT ($M_1 \sim M_{14}$ and M_{15}, M_{16}, R_2), and diode-connected NMOS (M_{17}).

Conventional start-up itself always consumes current even after it takes away from zero biasing state. The start-up used in this design works only if it is in zero-state, and consumes no more current after on. The initial use of this start-up was introduced in [119].

The presented biasing loop is a popular structure introduced in textbooks [120, 121]and references [122, 119, 123] but wide-swing current mirrors are employed to improve Power Supply Rejection Ratio (PSRR) because power rail fluctuation noise coming from full-wave rectifier may affect its performance. Transistors M_9 to M_{14}

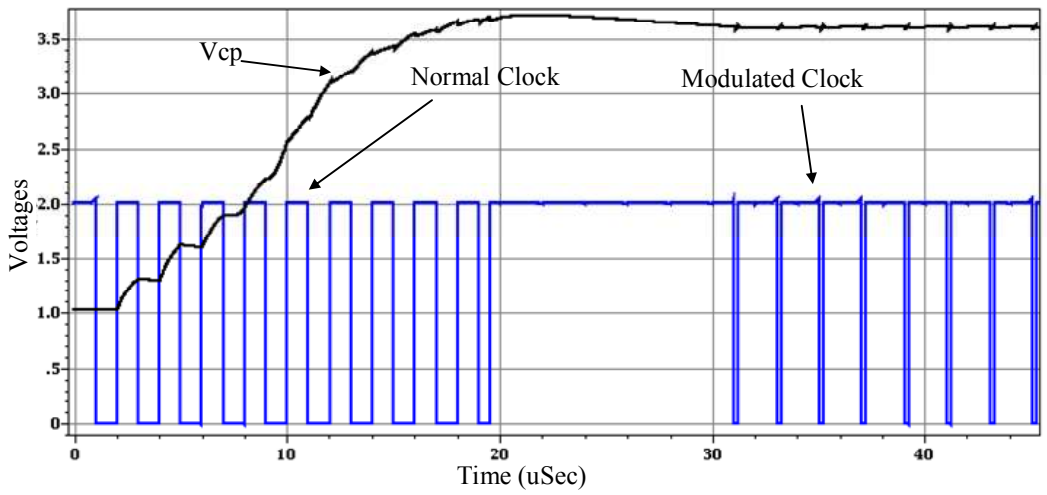


Figure 5.5: A capture of output and modulated clock signal for the charge pump.

give biases to cascode devices. Transistor M_7 is N-times bigger than M_8 and both transistors are operated in subthreshold region.

The current I_1 and I_2 are set equally by transistors M_1 to M_8, and it ends up with $V_{gs7} + V_{R1} = V_{gs8}$, where V_{R1} is the voltage across R_1. By subthreshold current equation (5.3), we can get a PTAT (proportional to absolute temperature) voltage as equation(5.4).

$$I_1, I_2 = N \times I_\phi \times \exp^{\frac{\kappa V_{g7} - I_1 R_1}{V_T}} = I_\phi \times \exp^{\frac{\kappa V_{g8}}{V_T}} \tag{5.3}$$

$$I_1, I_2 = \log(N) \frac{V_T}{R_1} \tag{5.4}$$

where I_ϕ, κ are characteristic current, body-effect coefficient, repectively and V_T=kT/q.

The same amount of the current I_1, I_2 is copied to I_5. There is a diode-

connected NMOS transistor biased in weak inversion region and it has an interesting voltage-temperature characteristic: The gate-source or drain-source voltage is almost linearly decreased (there is a small distortion due to logarithmic terms) as increasing temperature [117, 124]. By combining this characteristic with PTAT in equation (5.4), temperature-compensated voltage reference can be achieved as equation (5.5).

$$V_{ref} = \log(N)\frac{V_T}{R_1}R_2 + V_{gs17}(T) \tag{5.5}$$

Figure 5.7 shows the simulation plot in Cadence for reference voltage (V_{ref}) to temperature (C). Voltage variation over the range between -45^oC and 135^oC is $5.8mV$ but the range from 0^oC to 80^oC, which we are mostly interested in the implanted applications, is only $2.2mV$. The reference voltages at 0^oC, 27^oC, 38^oC, and 80^oC are $454.6mV$, $453.6mV$, $452.4mV$, and $454mV$, respectively.

Figure 5.8 presents power supply rejection ratio. It performs less than -47dB up to 10kHz and -36dB up to 100kHz. The total power consumption including all three parts in 1.8V power is only $11.3uW$.

5.5 An Efficient LDO regulator

A highly-efficient LDO regulator is acheived by the optimized charge pump and low-dropout voltage of LDO, which has maximum efficiency of 94.38 percent at $5mA$ load. The LDO efficiency is defined as equation (5.6) and it can be maximally achieved by minimum difference of input-output voltage (dropout voltage) while LDO keeps output regulation.

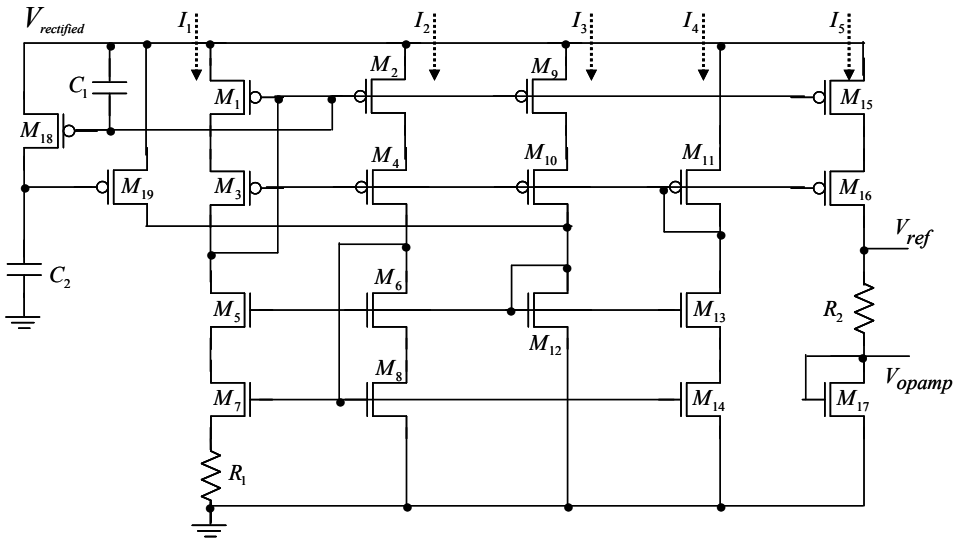


Figure 5.6: Schematic diagram of the designed CMOS voltage reference.

$$Efficiency = \frac{I_o V_o}{(I_o + I_Q)V_i} \tag{5.6}$$

where quiescent current $I_Q = I_i - I_o$.

In order to get higher efficiency and lower power dissipation, the designed LDO uses PMOS pass-transistor (by using NMOS pass transistor, V_{DD} inherently should be at least more than threshold voltage higher than output of LDO. Because of this, charge pump might need another stage to be a tripler). The two-stage amplifier with one zero compensation is used in LDO amplifier and ensures its stability. Figure 5.9 shows a $3.3V$ LDO having PMOS pass-transistor. The input of LDO uses boosted output voltage from charge pump. From charge pump design, it normally has $3.45V$ produced by $1.8V$ rectified voltage and 5mV ripple voltage by $200kHz$ clock. Table 5.1 summarizes simulated LDO performance for 1μA and $5m$A loading. A designed LDO can keep the output voltage with ranges from 1μA to $5m$A loading. It is

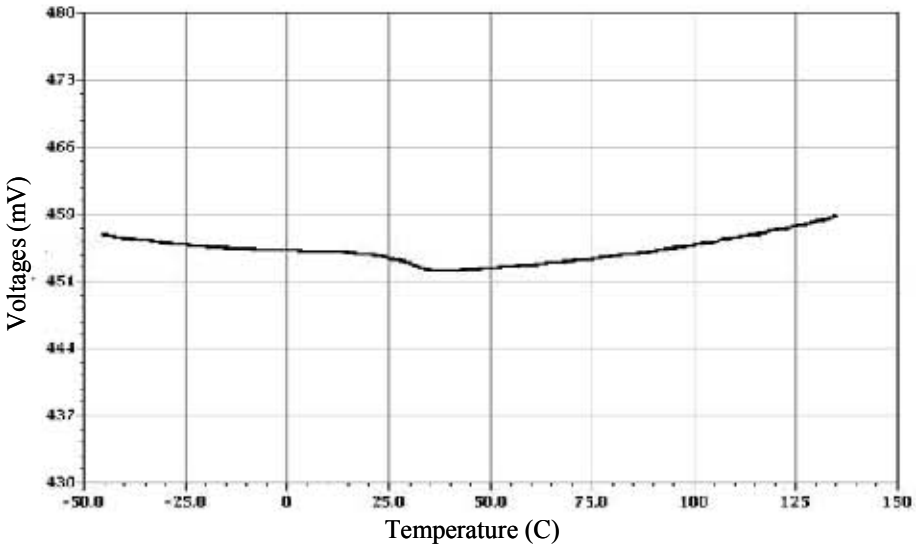


Figure 5.7: Simulated plot of reference voltage Vs. temperature.

simulated with 453.6mV voltage reference, 3.45V Vcp, $42k\Omega$ of R_1, $10k\Omega$ of R_2, and a 5pF load capacitor. Efficiency is maximized as output loading goes up to $5m$A.

5.6 Conclusions

This section presents a design of CMOS implantable power harvesting system in TSMC 0.18μm technology for low-coupling factor. High-efficient harvesting system

Table 5.1: Summary of Simulated LDO Regulator.

Loading	1μA	$5m$A
Phase margin	44.87^o	78.7^o
Output	$3.293V$	$3.292V$
PSRR	-57.74dB@1kHz -23.07dB@200kHz	-57.09dB@1kHz -20dB@200kHz
Quiescent current	52.78μA	54.95μA
Efficiency	1.77 percent	94.38 percent
Power dissipation	0.158μW	0.78mW

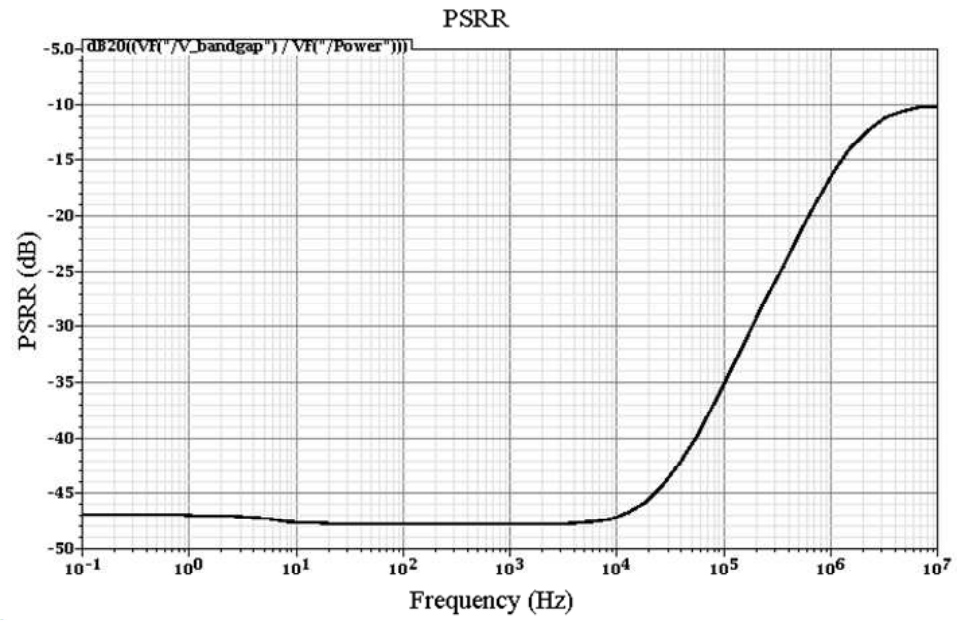


Figure 5.8: Power Supply Rejection Ratio (PSRR) for the designed voltage reference.

can be achieved by the proposed voltage doubler offering low-drop-out voltage for LDO. Analog Clamping and Clock Modulator technique in the charge pump can be utilized to other power recovery modules to implement a high-efficient system. A low temperature-dependent voltage reference using weak-inversion region can be successively applied to a bio-medical devices.

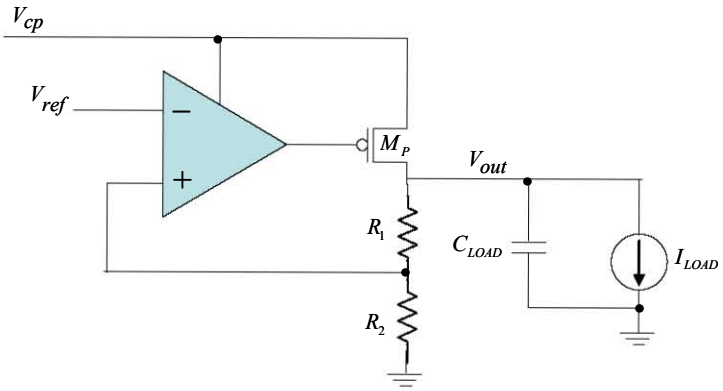


Figure 5.9: Schematic diagram of 3.3V LDO.

Chapter 6

Low-Power High-Resolution 32-channel Neural Recording System

6.1 Summary

A design of low-power 32-channel neural recording system working with on-chip high-resolution A/D converters is presented. A neural front-end including low-noise fully differential pre-amplifier, gain stage, and buffer consumes only 56μW. Two 13-bits extended counting A/D converters running at 512KHz sampling rate are integrated with 32 neural front-ends on a chip. The experimental prototype was designed in 0.6μm CMOS process. With a 3.3V power supply, total power consumption of the chip is 22mW and the whole system occupies an area of $3mm \times 3mm$.

6.2 Introduction

Recording from large population of neurons using multi-electrodes is indeed becoming a necessary procedure not only to research neuronal activities in central/peripheral nervous system but also to develop neural prosthesis. To better understand how the nervous system functions, we must be able to simultaneously monitor the responses of many neurons in small animals. To utilize advances in fabrication of MEMS structures that enable microelectrode arrays, there is need for recording systems able to record data and communicate gathered information to recording station in such a way that animal movement is restricted in minimal way. VLSI solutions offer low noise, small feature size and modularity. We are investigating design of VLSI microsystem for recording of neural signals from array of microeletrodes mounted on a head of a small animal. The headstage would have data link and would receive power through USB2 cable connection. The chip-on-board technology would be used for volume reduction and would enable interface to different sensor arrays.

Integrated circuits for neural recording have been designed for the past few decades [3, 91]. There are several design challenges in terms of noise, power, size, and resolution of analog-to-digital converter (ADC) due to the limited design resources. It should accommodate as many processing channels as possible while having properties of low power and low noise. Size and weight were the major constraints in our design. We have designed 32-channel analog neural recording system integrated together with 13-bit extended counting ADC in $3mm \times 3mm$ using 0.6μm CMOS technology.

6.3 Analog System Design for Neural Signal Acquisition

Figure 6.1 represents the schematic diagram of designed 32-channels neuronal recording system. 16 neural front-ends are multiplexed with one ADC, and the exactly same front-ends and an ADC are duplicated for another 16-channels processing so that total of 32 neural front-ends and two ADCs are integrated on a chip. To communicate digitized neural signals from ADCs, there would be FPGA board interface as well as USB 2.0 connector outside the chip.

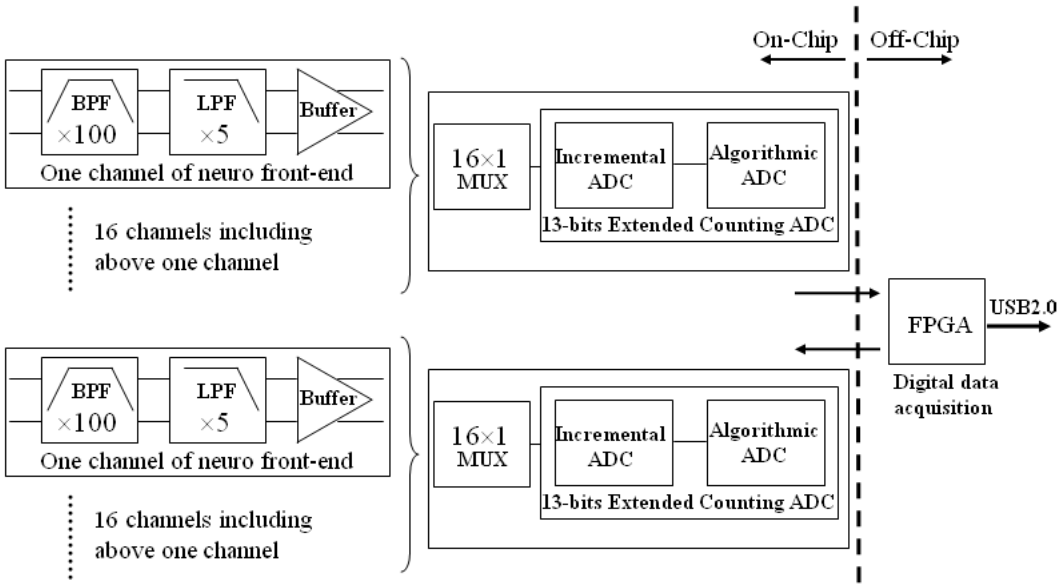


Figure 6.1: Schematic diagram of designed 32 channel neural recording system.

Figure 6.2 shows the schematic diagram for one channel of designed neural front-end. Since the circuit simultaneously processes neural signals from 32-electrodes, each channel of neural front-end should consume low power, occupy small area, and

also have high noise immunity to digital switching in subsequent analog to digital converter on the same substrate. It consists of three parts: (A) pre-amplifier, (B) gain stage and (C) buffer. All three parts use fully differential structures in order to achieve high common mode noise rejection and high noise immunity to digital switching. In the very first stage of the system, pre-amplifier amplifies micro-range (at most 1mV [103], typically 100μV [93]) neural signal from electrode one hundred times and only in the range from 100Hz to 7kHz. This is because extracellular neural action potentials, which we want to record, have frequency components in the range of 100Hz - 7kHz [93, 94]. The gain of this stage is limited by the linearity of pseudo-resistors. Another stage with the gain of 5 is added to maximize the dynamic range before analog-to-digital conversion. The second gain stage also has low-pass frequency characteristic, providing sharper roll-off at cut-off frequency of 7kHz in pre-amplifier. The third part, buffer, is necessary as input stage for ADC.

Figure 6.4 represents the simulated frequency response for each neuronal recording front-end. It amplifies the neural signal up to almost 54 dB (500 V/V) in the range between 100 Hz and 7 kHz. The second order pole is located around 7 kHz so that it rolls off at 40dB/dec.

6.3.1 Pre-amplifier Design

Figure 6.2(A) shows the structure of designed pre-amplifier. It is similar to previous design [100] so that the midband gain A_M is set by C_1/C_2, and the bandwidth by $g_m/A_M C_L$, where g_m is the transconductance of the operational transconductance amplifier (OTA). To implement very low cut-off frequency high resistive MOS elements (M_P are used. The resistance of PMOS element is up to the

order of $10^{13}\Omega$ depending on a biasing voltage (V_{REG}). The total time constant is set to $2R_PC_2$, where R_P refers to resistance of MOS element. Therefore, the low cut-off frequency of neural amplifier is determined by $1/(2\pi 2R_PC_2)$.

For the design of OTA in pre-amplifier, fully-differential telescopic operational amplifier, shown in Figure 6.3, is chosen with consideration of high gain, stability, and low-noise properties. By maximizing the gain of OTA, the effect of parasitic capacitances at the input of OTA could be reduced. It also makes it possible to use smaller C1 and C2 capacitors to set the gain. Cascode transistors increase OTA gain without degrading the noise performance. The smaller output voltage swing of the telescopic structure is not critical, since the output voltage swing is limited by the linear range of the high-resistive element (M_P), and not by the telescopic structure. The main trade-offs in this OTA design are between noise, power, and size. If we only consider the power consumption, the maximum performance may be obtained when the value of the transconductance/drain current ratio (g_m/I_d) is the largest. However, the input referred thermal noise of OTA is given as

$$\overline{v_{in,thermal}^2} = \frac{16kT}{3g_{m1}}[1 + \frac{g_{m7}}{g_{m1}}]\Delta f \tag{6.1}$$

g_m/I_d ratio and size of transistors should be considered to minimize input referred thermal noise. As total power consumption is determined by biasing current, we have chosen a lower biasing current. From the noise analysis, input transistors M_1 and M_2 should be sized with as large W/L ratio as possible so that a maximum g_m/I_d ratio is obtained. In the same manner, the noise contribution of transistors M_7 and M_8 can be minimized by choosing small W/L ratio or minimizing g_m/I_d ratio. Increasing the

length of these M_7 and M_8 transistors is limited by available space. Effect of flicker or $1/f$ noise is minimized by choosing PMOS transistor for inputs and by increasing gate area of the transistors in design.

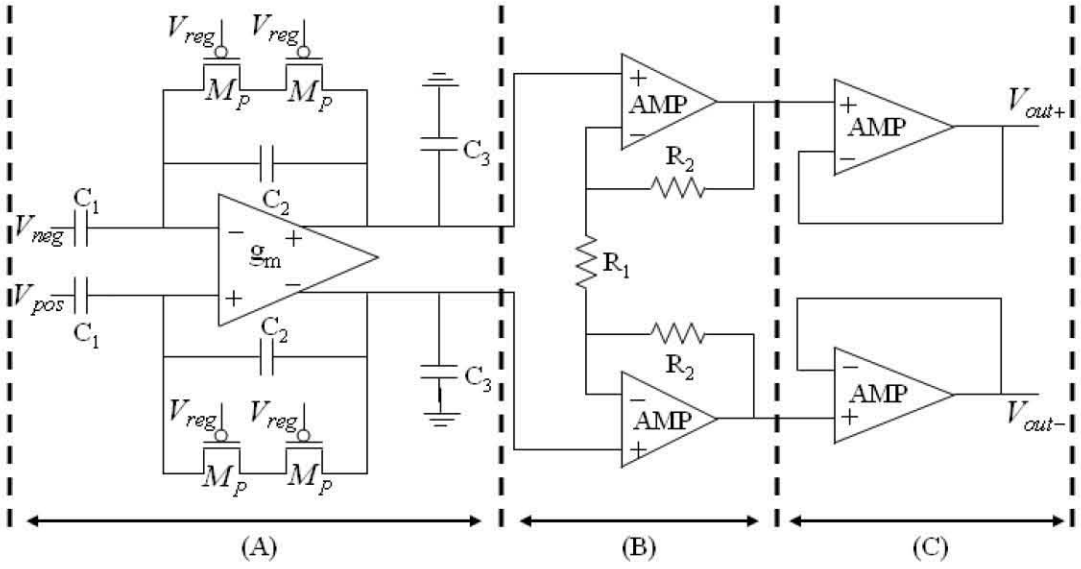


Figure 6.2: Schematic diagram for a channel of neuro front-end including (A)pre-amplifier, (B)gain stage, and (C)buffer.

For the implementation of common-mode feedback circuit, we have chosen continuous-time circuit shown in Figure 6.3. The common-mode output voltage is set to $V_{DD}/2$ or $1.65V$. If the output common-mode level increases, current of M_{15} and M_{18} will increase and the current of $M_{16,17}$ will decrease. This causes increment in V_{CMFB} and makes the V_{SG} of M_{11} decrease, followed by decrease in common-mode output voltage.

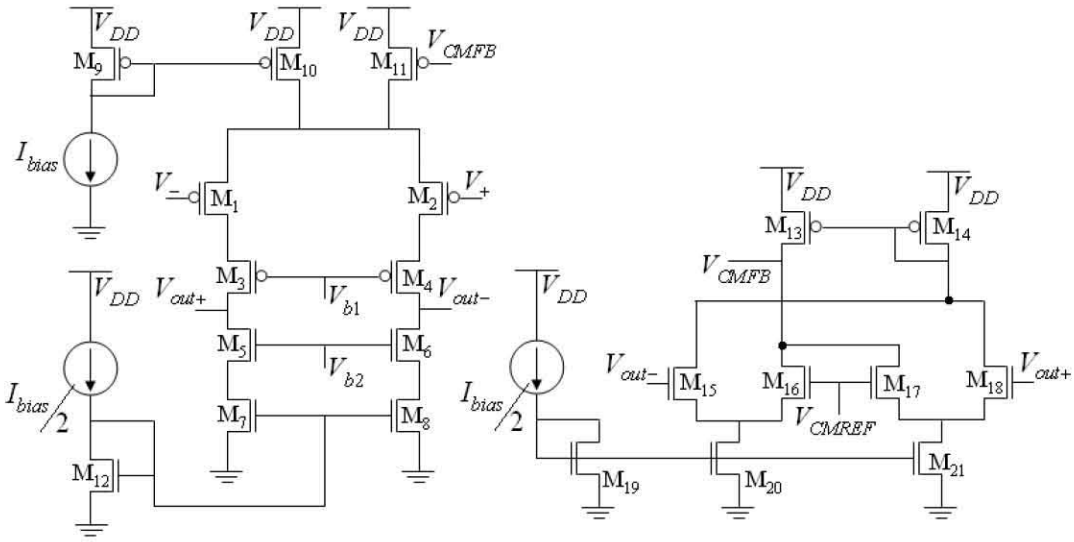


Figure 6.3: Schematic diagram of pre-amplifier with a continuous-time common mode feedback circuit.

6.3.2 Gain stage and buffer design

Figure 6.2 also shows the gain stage and buffer. The structure of gain stage is basically non-inverting opamp. It has two resistors (R1 and R2) that create gain of 1+(R2/R1). The gain stage also provides additional low-pass filter with cut-off frequency of 7 kHz. There are two stages inside this gain stage: OTA and output pmos source follower to drive resistive loads. The low-pass cut-off frequency is set by both transconductance of the OTA and input capacitance of the source follower.

The gain stage is followed by a buffer which will drive subsequent multiplexer. The gain and phase margin should be considered in this buffer design because the amplified signal should settle down before following ADC starts the data conversion. The folded cascode op-amp is used in this buffer design and it has gain of around 1200 and over 80 degrees of phase margin.

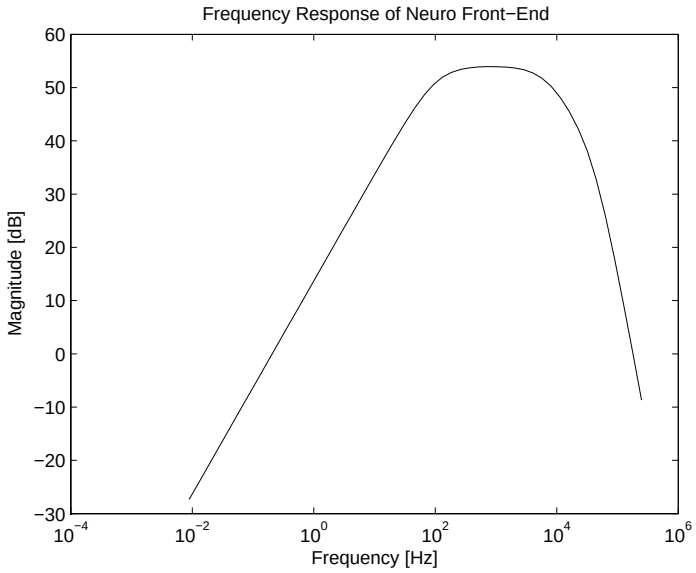


Figure 6.4: Frequency response of a neuro front-end.

6.4 Design of Low-Power High-Resolution ADC

To reduce the noise introduced in communication, on-chip A/D conversion is required. The neural recording system in this prototype requires a resolution of 13-bit and a bandwidth of up to 1MHz. Area and power are two major constraints in designing the ADC.

Under the specifications stated above, an extended counting is chosen as the architecture of our ADC, where a compromise of resolution and speed is achieved [96]. The converter passes through two stages. In the first stage, the converter acts as a first-order incremental converter to convert the most significant bits. Then in the second stage, the same hardware is used to convert the least significant bits by an algorithmic A/D conversion technique. The total conversion cycles of one sample is 16.5 clocks for 13-bit resolution. The designed ADC were published and the details

Table 6.1: Parameters for simulated preamplifier.

Parameter	Perfomance
Gain	39.5dB
Gain bandwidth	$100Hz$ to $7kHz$
Input noise	$3.35\mu V_{rms}$
Power consumption	13.68μW
Noise efficiency factor	3.18
Phase margin	105 degree
Area	$0.0482mm^2$

were presented in [129, 130].

6.5 Simulation Results and Layout

The circuit was simulated using Cadence SpectreS simulator and BSIM3 version 3.1 transistor models were used with $1/f$ noise parameter of KF = 6×10^{-27} (PMOS), KF = 3×10^{-25} (NMOS), and AF = 1 (PMOS and NMOS). Table6.1 summaries the performance of simulated pre-amplifier. Both gain stage and buffer in one channel of neuro front-end occupie only $0.0172mm^2$ and consume 42.34μW. Total power consumption for single channel of neuro front-end is about 56μW.

6.6 Measurements

The designed 32-channel analog front-end for neural recording system was fabricated together with two extended counting ADCs on a area of $3mm \times 3mm$ through MOSIS AMI 0.5μm 2 poly 3 metal layer CMOS technology. Figure 6.5 shows a microscope image for the fabricated chip.

The chip is tested with a custom designed general purpose mixed signal test

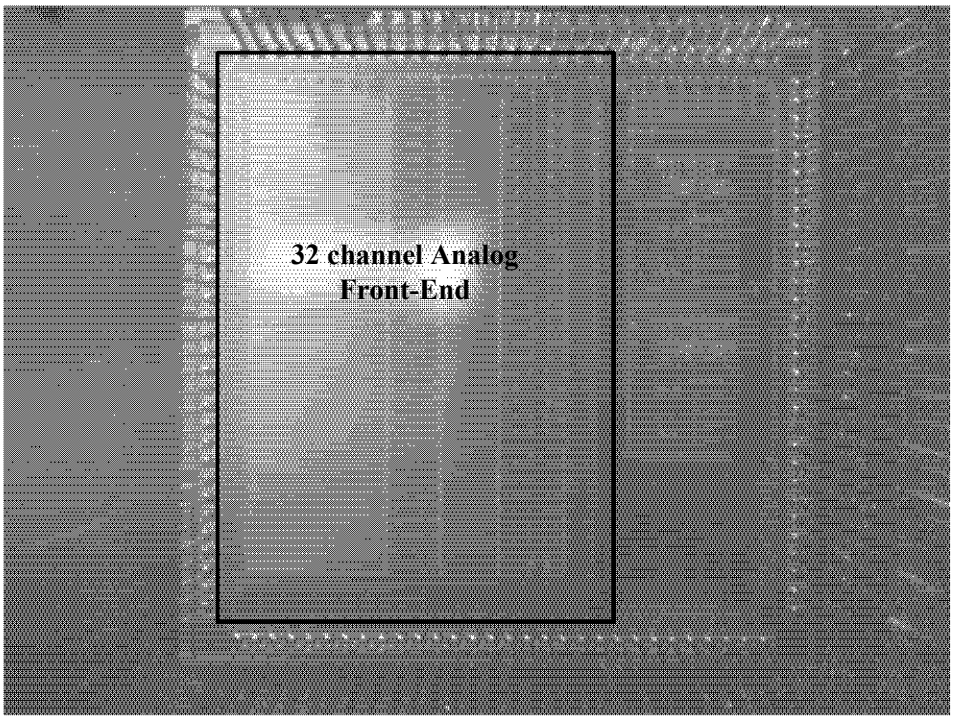


Figure 6.5: Microscope image of the fabricated 32-channel neural recording system.

station equipped with PC interface. The test station is interfaced to PC through data acquisition card NI-6259 (National Instruments) for characterization and real time measurement. Test station is comprised of a motherboard and a daughter board. A motherboard consists of interface circuitry to PC and FPGA, digital-to-analog converters for providing biasing voltages, 3.3V power regulators. A daughter board contains the designed ASIC with a socket and interface connectors providing a connection flexibility to motherboard through wire-up. Figure 6.6 and 6.7 show a picture of the motherboard and the daughter board equipped on a motherboard, respectively.

The chip is supplied by a 3.3V regulator which is powered by 5V analog output

from NI-6259. Among 32 channels of front-ends, due to limited number of I/O port, only 32nd design among the channels was left for testing purpose and has total 18 pin interfaces: 2 signal inputs, 12 voltage biasing, 2 signal outputs, one Vdda, and a ground.

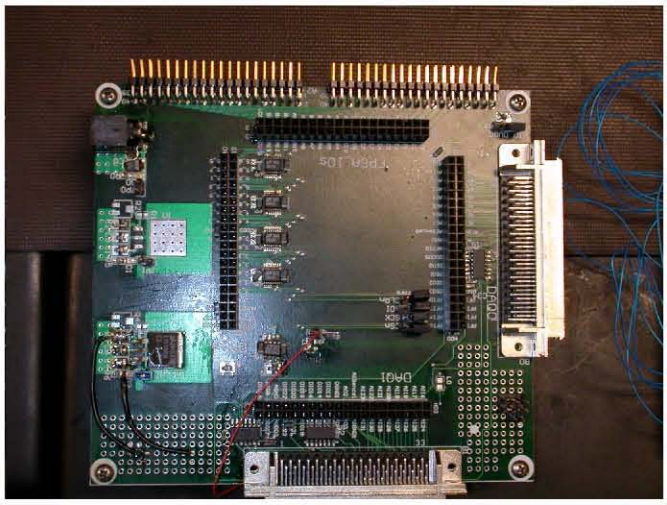


Figure 6.6: A custom designed motherboard.

Figure 6.8 presents a capture of measured transient response for the designed 32nd channel. It characterizes a gain of 150 with a signal distortion at $1KHz$ $3mV$ input sinusoid wave. From additional testing, there is unacceptable distortion for other frequency ranges and various inputs. Figure 6.9 shows a plot for FFT response of the captured transient response. We can find unwanted high-frequency components, and it represents a large deviation from the simulation results, which is gain of $54dB$ or $500V/V$ in the range from $0.5Hz$ to $7KHz$.

From the review of schematics and diagnostics in testing, the major problem arises from a common-mode feedback circuit in the preamplifier. The common-mode voltage is supposed to be a half of Vdd which is $1.65V/V$ but it has been under

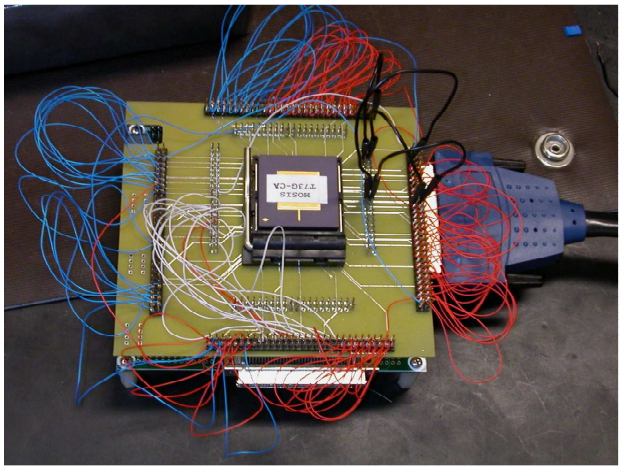


Figure 6.7: A picture of daughterboard-mounted test station.

Table 6.2: Magnitude Response for Preamplifier Corner Simulation where V_{reg}=0.514V

Corners	Bandwidth (Hz)	Maximum (dB)
TT	283.3∼8.052K	39.91 @1.5KHz
SS	209.4∼7.827K	39.92 @1.266KHz
FF	1.945K∼10.24K	39.77 @5.241KHz
SF	2.86K∼10.56K	39.79 @5.24KHz
FS	1.95∼7.941K	39.95 @102.3Hz

control. Two NMOS load transistors M7, M8 and two current sources M20 and M21 in Figure 6.3 are working under out of saturation. Transistor M7, M8, M20, and M21 were sized with very small W/L ratio to minimize input-referred noise even with a small bias current. Due to the very long transistor aspect, the transistors were biased on the edge of saturation region.

Transistor mismatches and their variation in a process might also contribute to the deviation in the testing results. It can be simulated by corner simulation. Figure 6.10 and 6.11 show the corner simulation results for the preamp and whole

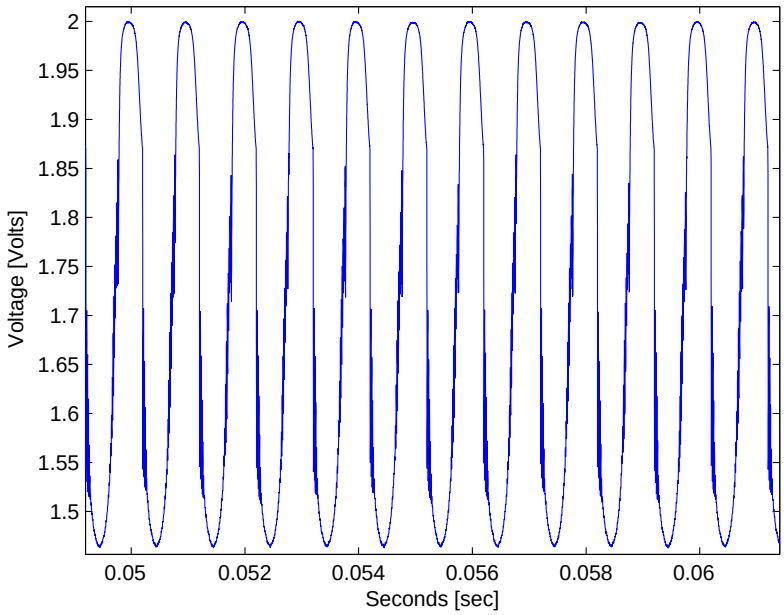


Figure 6.8: A transient response for the designed analog frontend.

32nd analog processing channel, respectively, and Table 6.2 and 6.3 summarize their characteristics. Five MOSFET corner models in AMI 0.6μm technology are acquired from a MOSIS service and used in the corner simulation. The corner model is named with a combination of NMOS and PMOS process: TT (Typical NMOS - Typical PMOS), SS (Slow NMOS - Slow PMOS), FF (Fast NMOS - Fast PMOS), SF (Slow NMOS - Fast PMOS), and FS (Fast NMOS and Slow PMOS). Almost all parameters are different among models but the major difference between corners is a threshold voltage. Since a current consumption and transistor speed is mainly determined by threshold voltage they are named by Fast or Slow.

In the corner simulations, the gate biasing voltage $Vreg$ for the preamplifier in the Figure 6.2 was set to have the frequency range from $300Hz$ to $7KHz$ at TT

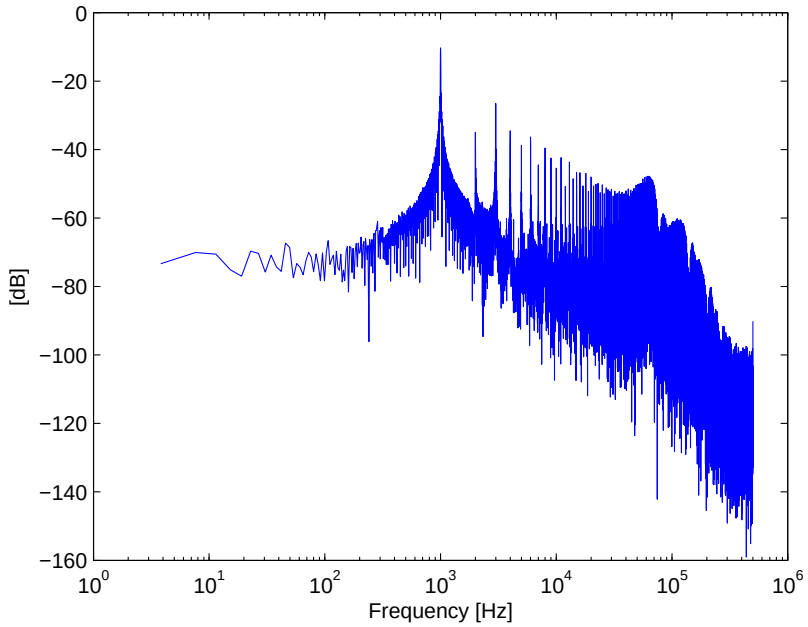


Figure 6.9: A FFT response for the captured transient response in Figure 6.8.

corner. For the lower cut-off frequency of $300Hz$, a 0.514V of $Vreg$ was biased in the circuit. However, the applied biasing $Vreg$ voltage was not changed when each corner simulation ran. By the comparing figure 6.11 and 6.10, the shape of magnitude response for the whole frontend corner is similar to the preamplifier except gain. Large cut-off frequency variations are observed for the lower cut-off frequency because of the threshold voltage variation among corner models. Also, large gain and bandwidth distortion are occurred in the preamplifier as of showing a sharp drop of magnitude in especially SF corner. It affects to the whole frontend system, and the abrupt change of magnitude happens when the transistors in amplifier go out of saturation.

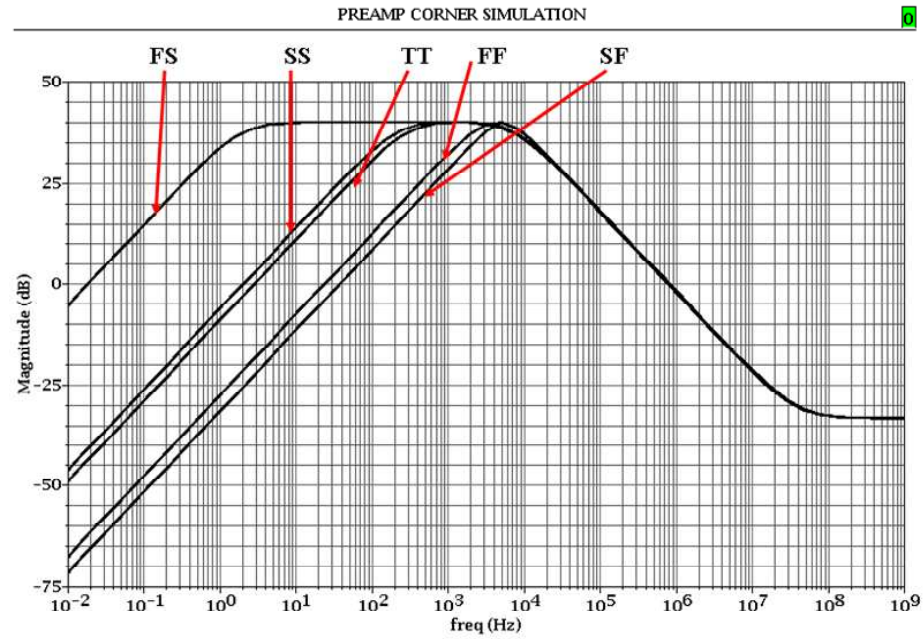


Figure 6.10: Five corner simulation results for the designed preamplifer.

6.7 Improvements

The previously designed analog acquisition system including a preamplifier and a gain-LPF stage has a deviated magnitude response from what we have simulated. Some of transistors, mainly in preamplifier, are working in the linear region rather than saturation region at corner simulations. A new design of a preamplifier and a gain-LPF stage with output buffer were simulated in both time and frequency domain using acquired in-vivo cerebral neural data from a rat in the Cold Spring Harbor Lab., New York.

The improved system has the same structure as in Figure 6.2. For the preamplifier, the transistor sizes and biasing current have been designed differently from previous one. It has been ensured that all transistors work in saturation region

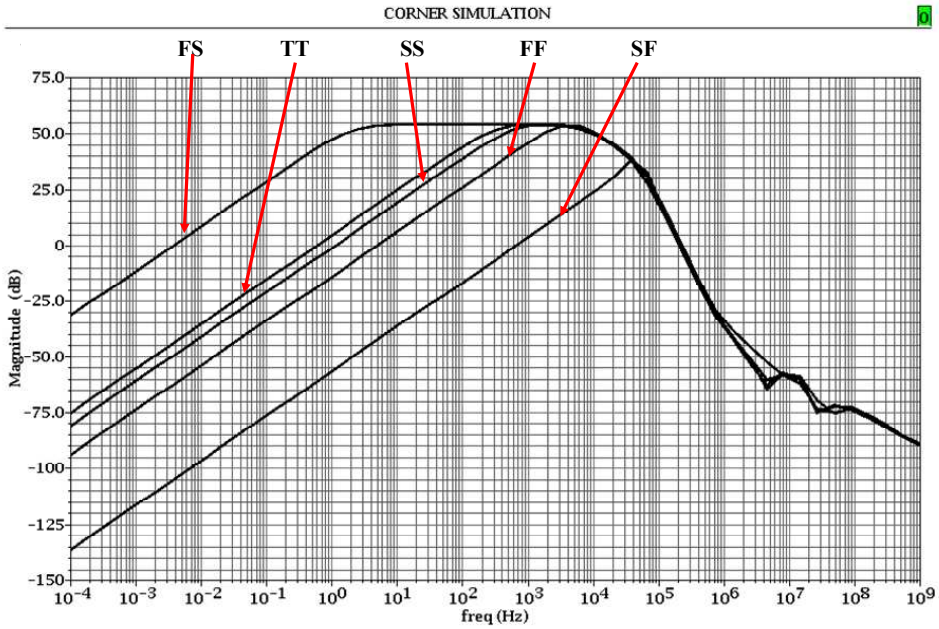


Figure 6.11: Fiver corner simulation results for the designed frontend.

for all corners. Instead, the biasing current of the preamplifier was increased to minimize input-referred noise and transistors were sized properly not to be very long.

Table 6.4 summarizes performances for the improved fully-differential preamplifier. It has a bandwidth from $321Hz$ to $9.27kHz$ but input noise was integrated only up to $8.2kHz$ which is the channel bandwidth.

For the gain-stage, the same resistive feedback structure as in the gain stage of

Table 6.3: Magnitude Response for Whole Frontend Corner Simulation where V_{reg}=0.514V

Corners	Bandwidth (Hz)	Maximum (dB)
TT	298.4∼7.921K	53.92 @1.5KHz
SS	550.9∼7.978K	53.9 @1.961KHz
FF	1.922K∼10.59K	53.4 @4.462KHz
SF	30.05K∼53.58K	38 @37.93KHz
FS	2.05∼7.721K	53.95 @82.4Hz

Table 6.4: Simulation results for improved fully-differential preamplifier.

Parameters	Perfomances
Gain	39.84dB
Gain bandwidth	$321Hz$ to $9.27kHz$
Input noise up to $8.2kHz$	$2.8\mu V_{rms}$
Power consumption	52.56μW
Supply voltage	3.3V
Noise efficiency factor	4.86
Phase margin	78.3 degree

Table 6.5: Simulation results for improved differential gain-LPF stage.

Parameters	Perfomances
Gain	20dB
Gain bandwidth	$24.24kHz$
Input noise	$16.51\mu V_{rms}$
Current consumption including bias	9.444μA
Power consumption	31.165μW
Supply voltage	3.3V
Phase margin	78.6 degree

Figure 6.2 was used. However, the inner amplifier structure has been changed from a mirror opamp with class-A output stage to a cascode mirror opamp with class-AB output stage. Figure 6.12 shows the improved opamp with a class-AB output stage. The cascode transistors M9, M10, M11, and M12 were added from previous design to increase the gain, and class-AB output stage was used to increase efficiency, driving capability, and output swing range. The quiescent current through the last common-source transistors M21 and M22 is only 1.43uA but they can drive large capacitive load, for instance, analog-to-digital converter (ADC). A large swing output stage is preferable to the following stage which is input of ADC, since the bigger reference of ADC results in higher signal to noise ratio (SNR). Table 6.5 summarizes the performance of the designed gain-LPF stage.

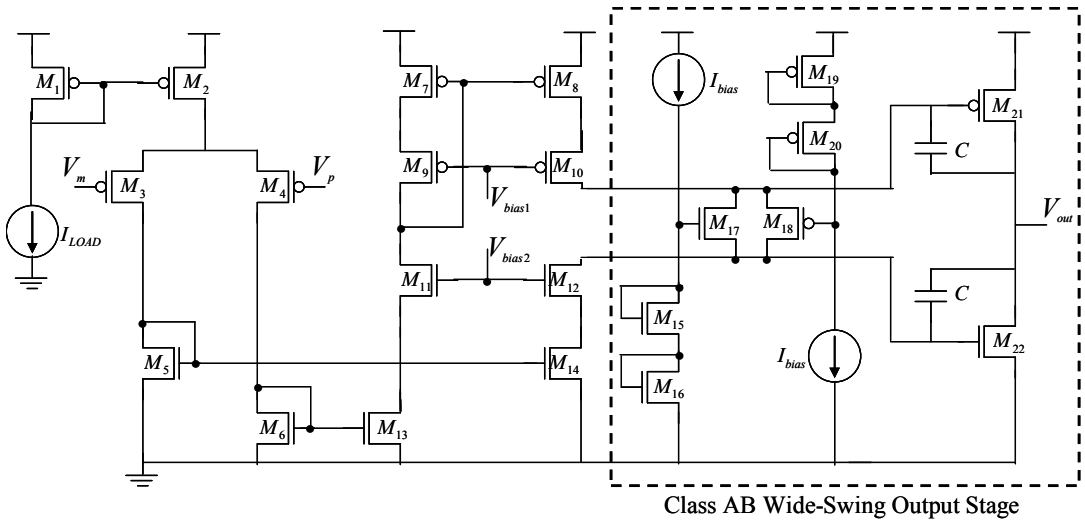


Figure 6.12: A newly designed amplifier for gain-LPF stage. Wide swing class AB output stage is utilized.

Figure 6.13 shows the magnitude response for the improved channel design. The channel design has a gain of $60dB$ in the bandwidth between $321Hz$ to $8.2kHz$.

The improved designs were simulated using in-vivo cerebral neural data as a schematic input. The raw data has been collected from a rat in the Cold Spring Harbor Lab., New York. The raw data and the simulation results in Cadence are plotted in the Figure 6.14. The input raw data is represented in the fifth row tabbed as Vp. It contains Local Field Potential (LFP) as well as neural spikes. Tabs named a and b are the preamplifier positive and negative output, respectively. Likewise, Voutm and Voutp are the negative and positive outputs of the gain-LPF stage, respectively. Figure 6.15 presents the differential plots from a and b as well as from Voutm and Voutp. The first row tabbed diffAB is the differential plot from preamplifier outputs a and b. Similarly, the second row tabbed diffVout is the gain-LPF differential outputs Voutp and Voutm. The output of gain-LPF stage is 10-times bigger than preamplifier

output. The low-frequency LFP was eliminated by bandpass characteristics.

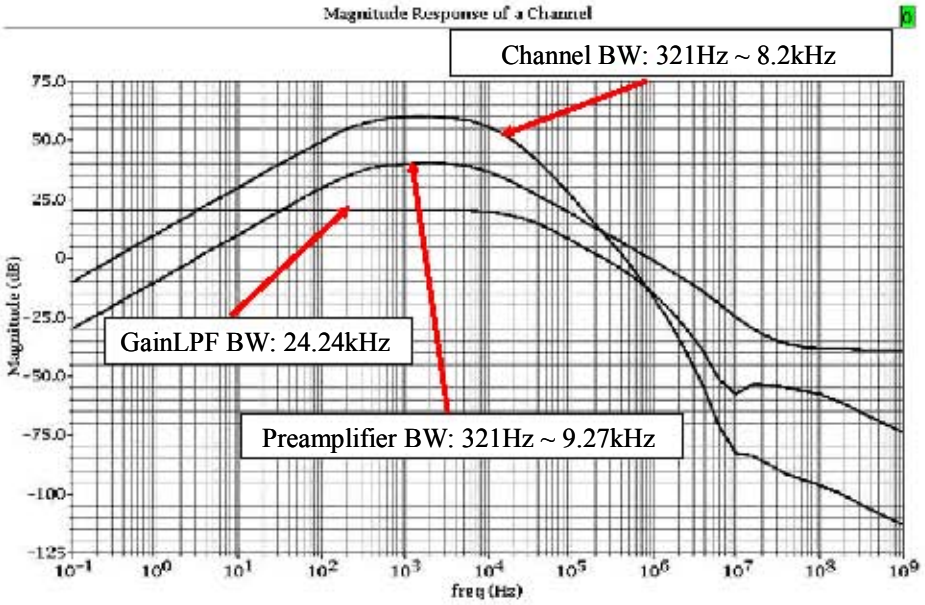


Figure 6.13: Improved frontend magnitude response.

Figures 6.16, 6.17, 6.18 present the corner simulation plots for the improved preamplifier, gain-LPF stage, and the combined two stages, respectively. There are variations at the lower cut-off frequency since the lower cut-off frequency depends on the high-resistive pseudo transistors M_P and C_2 in Figure 6.2 (A). The biasing voltage for gate of M_P is always set to $560mV$ in these five corner simulations, and the $560mV$ is a biasing voltage only for the TT corner to have $321Hz$ lower cut-off frequency. Since each MOS corner model gives different threshold voltage the constant biasing voltage for high-resistive elements M_P cannot guarantee the $321Hz$ cut-off frequency for all corners. Except threshold voltage variation that is lower cut-off frequency variation, there is acceptable variation among corners and no sharp deviation of magnitude response. Table6.6 summarizes the magnitude corner responses for the

Table 6.6: Magnitude Response for Improved Channel Corner Simulation where V_{reg}=0.560V

Corners	Bandwidth (Hz)	Maximum (dB)
TT	323∼8.05K	59.82
SS	51.73∼8.36K	59.86
FF	564∼9.5K	59.82
SF	884∼9.67K	59.71
FS	0.85∼8.82K	59.82

improved channel design.

6.8 Conclusions

This work presents a design of low-power neural recording system mounted as head-stage on small animal, with on-chip 13-bits extended counting A/D converters. All 32 channels of neuro front-ends and two 13-bit A/D converters are integrated into a $3mm$ by $3mm$ chip area in 0.6μm CMOS process. Based on the analog frontend test, the major problems in the design were analyzed, and the improved design of frontend was proposed.

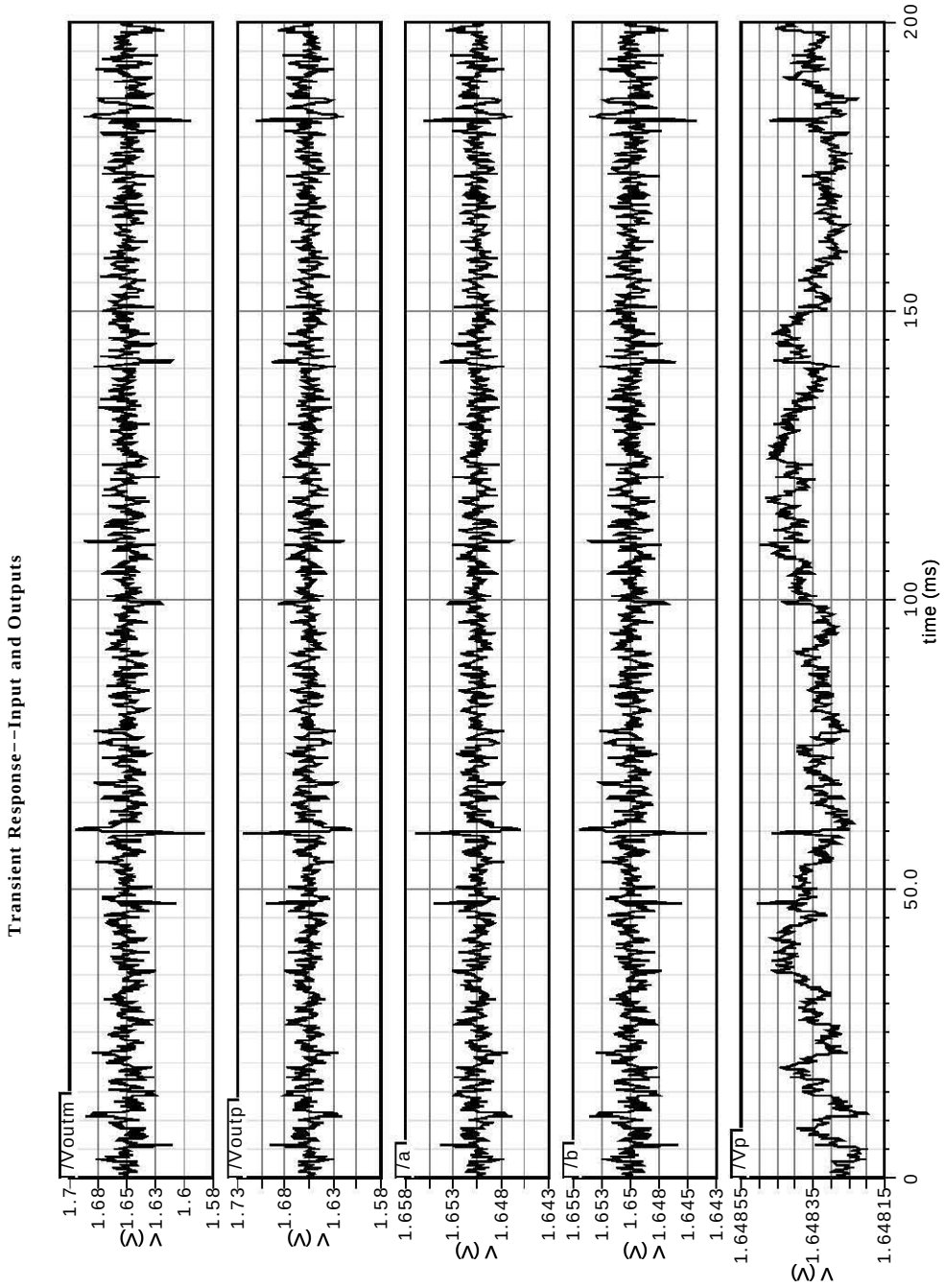


Figure 6.14: Improved frontend transient response.

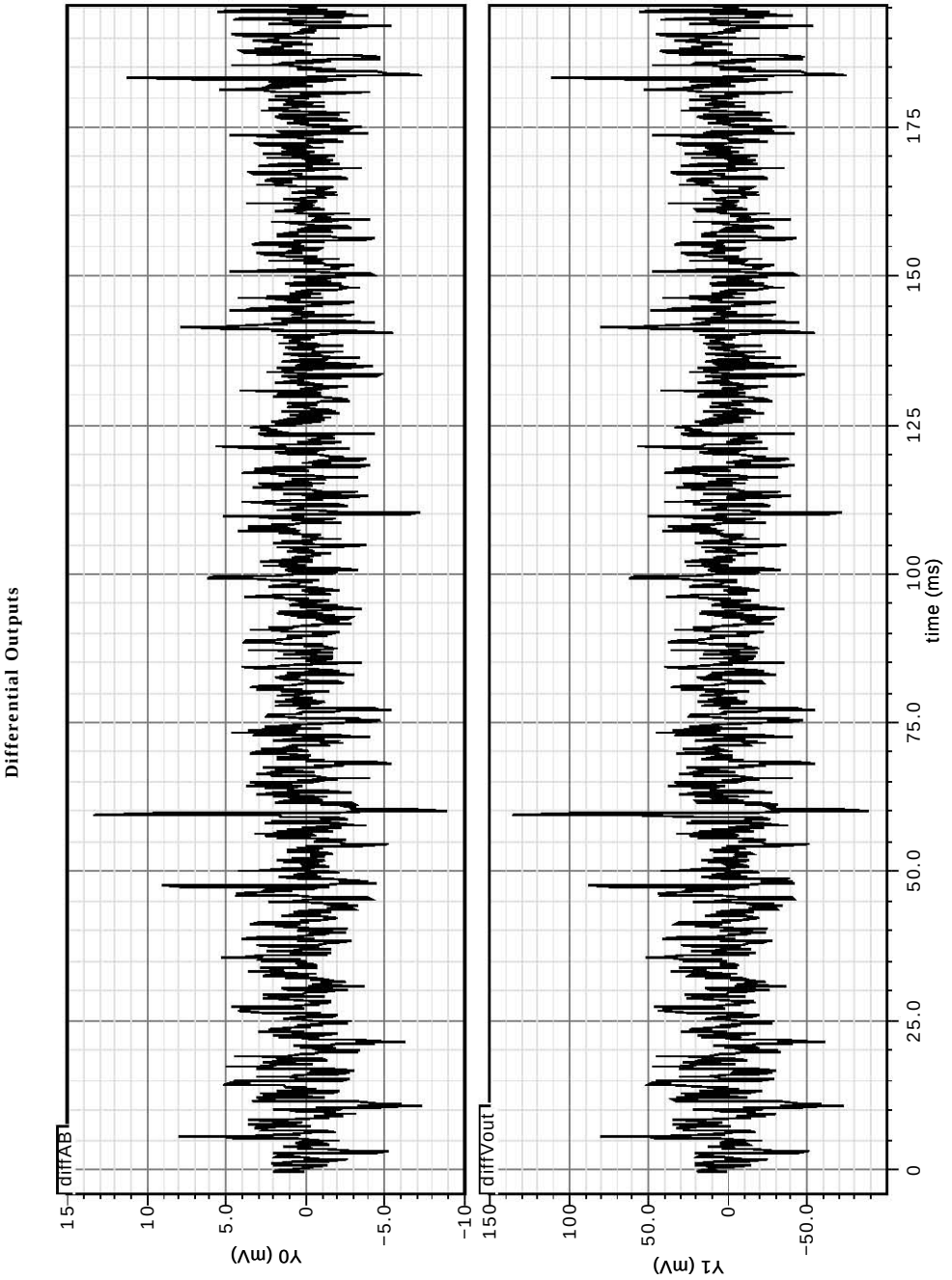


Figure 6.15: Improved frontend differential response.

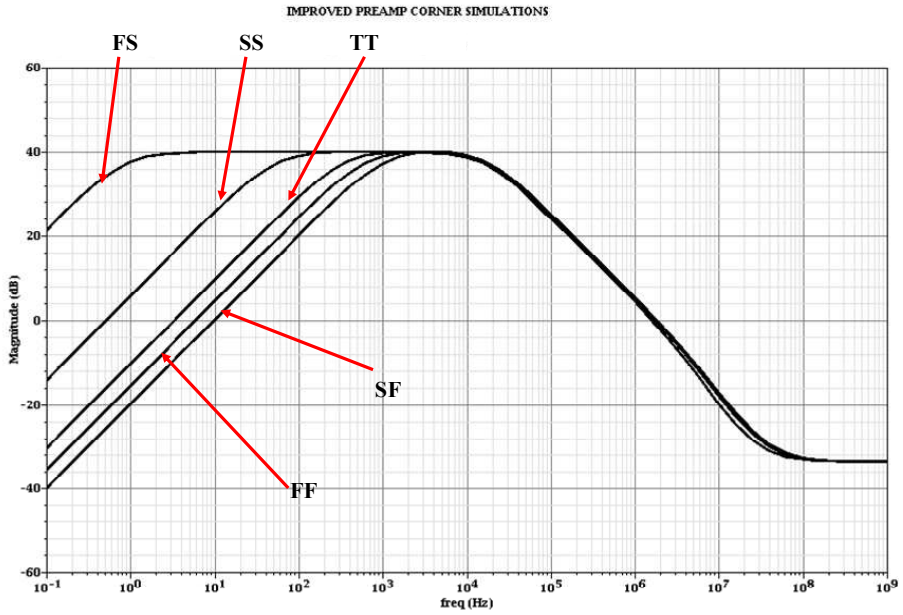


Figure 6.16: Improved preamp corner simulation.

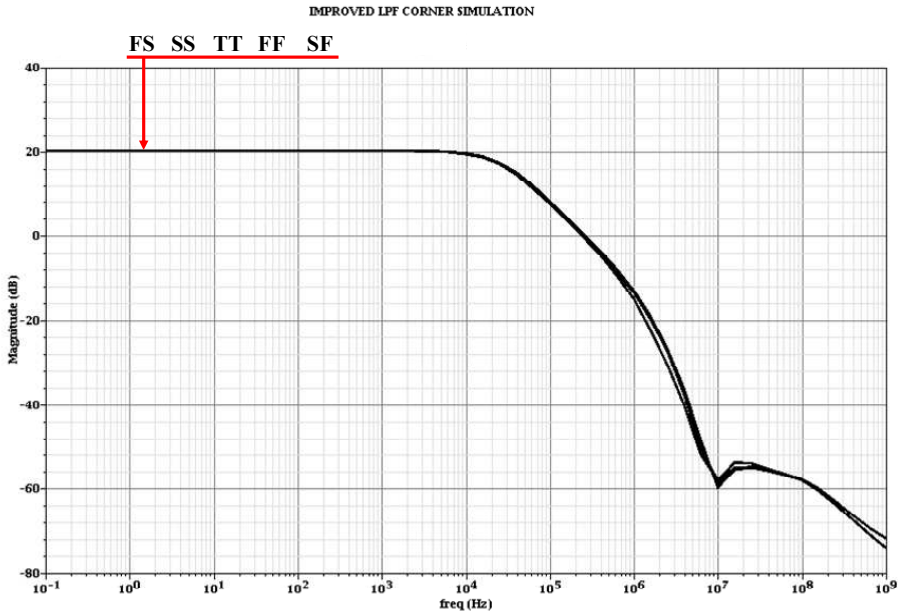


Figure 6.17: Improved LPF-AMP corner simulation.

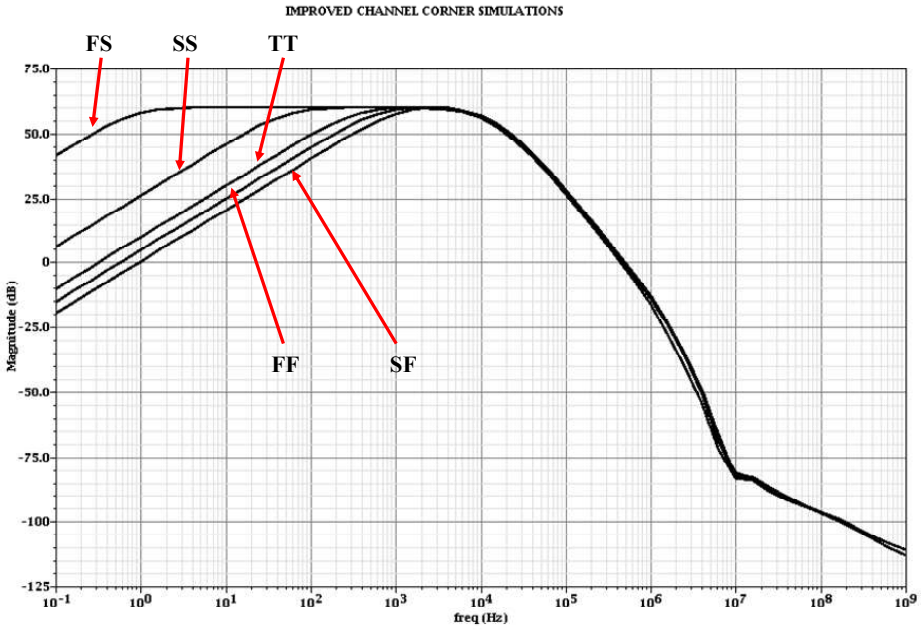


Figure 6.18: Improved channel corner simulation.

Chapter 7

Adaptive Spike Detection for Low-Power Low-Data-Rate Wireless Neural Recording System

7.1 Summary

A design of small, low-power, low-data rate, wireless 32-channel neural recording system for small animal head-stage is presented.

A neural pre-amplifier has low-input-referred-noise of $2.24\mu V_{rms}$ and consumes 57.82μW. To enable digital telemetry with optimized bandwidth under size and power constraint for small-animal headstage, we propose to separately record spikes and local-field potentials. An adaptive spike detector using absolute value algorithm accompanied with 7th-order all-pass delay filter provides accurate on-chip acquisition of spike waveform in duration of $2ms$. Additionally, an area-efficient adaptive spike

detection system without use of all-pass filter is presented. A low-power 10-bit and 5-bit resolution A/D converters running at $22Ksamples/s$ for active spikes and $200samples/s$ for local field potential, respectively, can be integrated with the proposed system. Using adaptive bandwidth control, we achieve reduction of data-rate up to seven times which provides compatibility to $1Mbps$ Ultra Low Power Bluetooth technology. Total power consumption of single channel excluding ADCs is 108.92μW in 3.3V power supply.

7.2 Introduction

Recording and collection of large population of neural signals in small animal is required to investigate bio-physiological activities in central and/or peripheral nervous system. There is a need for a system able to record all informative data and communicate the gathered data with a recording station in such a way that animal movement is restricted in minimal way.

Existing systems for multi-channel recording mainly use analog headstage requiring a number of wires equal to the number of channels, leading to restriction of movement and poor scalability. Most of these systems use pre-amplifier and front-end filtering to improve the signal-to-noise ratio before transmission to a remote data logger. Wireless transmitting devices might solve that problem, but current generations based on analog multiplexing also scale poorly and are susceptible to noise [125, 126]. The design of a headstage with on-chip analog-to-digital conversion would enable digital telemetry of neural signals in their entirety, however high-data-rate in multi-channel implementation is concern and efficient control of bandwidth is

necessary. To control the bandwidth and transmit all informative data, we need to transmit effective spike shapes accurately at higher sampling rate, enabling off-chip digital spike sorting, while local field potentials can be acquired at lower resolution and lower sampling rate.

We have investigating a design of wireless VLSI micro-system for recording of neural signals from array of micro-electrodes mounted on a head of a rat-like small animal. The head-stage would interface with an Ultra Low Power Bluetooth technology [127], previously called Wibree, which consumes only a fraction of the power of the classic Bluetooth, can be powered by a small and light button cell battery and supports data-rate of 1Mbps. A higher resolution ADC can be utilized whenever an active spike is detected, and a lower resolution ADC is adequate for recording of local field potential (LFP). The chip-on-board technology would be used for volume reduction and would enable interface to different sensor arrays.

We have considered 32-channel analog neural recording system integrated together with an adaptive spike detector using absolute value algorithm in 0.6μm CMOS technology.

7.3 Low-Power Low-Data-Rate System Design

Figure 7.1 shows single channel of the system block diagram for the proposed low-power, low-data-rate neural recording system. It consists of a pre-amplifier, 7th order all-pass delay filter, an adaptive spike detector using absolute value algorithm, high-pass filter, low-pass amplifiers, 10-bit ADC and 5-bit ADC. In the pre-amplifier, since the peak-to-peak voltage of input spike train and LFP, in case of removal of

random DC offset, are micro-range (at most 2mV_{pp} for spikes, typically 200μV_{pp} and about 2mV_{pp} for LFP). Neural signals from a electrode are amplified fifty times only in the range from ideally less than 1Hz to 7kHz. This is because the linear range of the all-pass filter and the adaptive spike detector (ASD) in the figure is set to 200mV_{pp}. A high-pass filter (HPF) is used for selection of only spike bandwidth. ASD is to adaptively set a detection threshold by a multiplication factor which would be adjusted high or low by external digital signal. A linear phase all-pass delay filter allows the previously amplified spikes to preserve the shape of waveforms in band of interests with certain amount of delay. Two low-pass filter amplifiers (LPF-AMPs) before two ADCs are not only to enlarge input dynamic range of ADC but also work as anti-aliasing filters for the digitization (A 7kHz band-width LPF-AMP for active spikes, and 100Hz band-width LPF-AMP for LFP). For the 10-bit ADC, a low-power, small-size, ratio-independent algorithmic-type ADC [128] can be considered for this application. It will be activated by the one bit spike acknowledge signal from the ASD. Whenever an active spike signal is detected the ADC runs at $22Ksamples/s$. For the 5-bit ADC, a successive approximation-type ADC running at $200samples/s$ can be considered for recording of LFP. Since it is low resolution only few pico-farads capacitors will be utilized for a binary-weighted capacitor array. Digitized data will be processed in the off-chip and interfaced with Ultra Low Power Bluetooth chip for wireless transmission.

7.3.1 Pre-Amplifier Design

Figure 7.2 shows the structure of designed pre-amplifier which is based on our previous design [129]. Pre-amplifier is especially designed for taking action

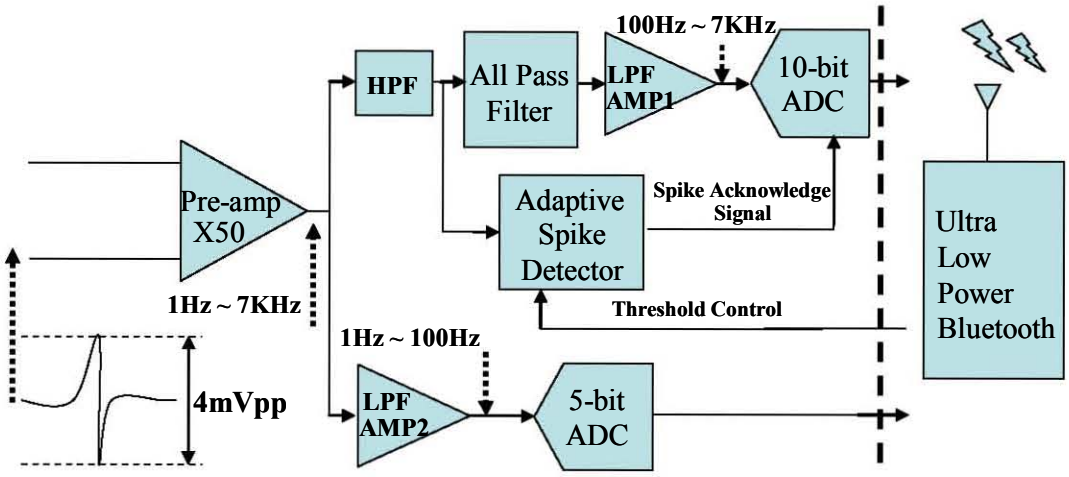


Figure 7.1: A single-channel system diagram for the proposed adaptive neural recording system.

potential with local field potential (LFP) which have frequency components in the range of 0.538Hz - 9.58KHz. The bandwidth is set by $g_m/A_M C_L$, where g_m is the transconductance of the operational transconductance amplifier (OTA), A_M is midband gain set by C_1/C_2, and C_L is load capacitance seen from output of the pre-amplifier. Low cut-off frequency is determined by $1/(2\pi 2 R_P C_2)$ using resistance (R_P) of a pseudo PMOS element, up to the order of $10^{13}\Omega$ depending on a biasing voltage (V_{RES}). For design of OTA in pre-amplifier, wide-swing current-mirror operational amplifier is utilized with consideration of high gain, stability, and low-noise properties. By maximizing the gain of OTA, the effect of parasitic capacitances at the input of OTA could be reduced. It also makes possible the use of smaller C1 and C2 capacitors to set a gain. Capacitors C_1, C_2 are set to 7.5pF, 150fF respectively. The designed preamplifier has gain of $33.95dB$ and $2.24\mu V_{rms}$ input-referred noise in the band of interest.

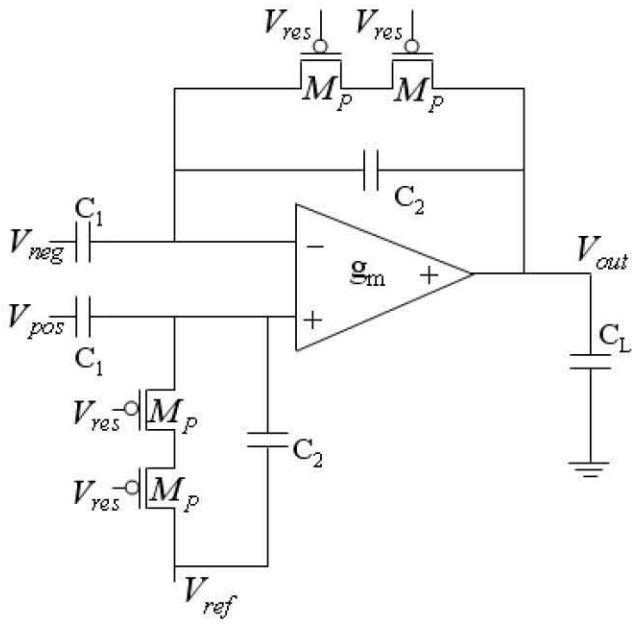


Figure 7.2: Schematic diagram for a low-input-referred-noise pre-amplifier.

7.3.2 Design for Two LPF-AMPs and HPF

The preamplified neural signal has to be processed by high-pass filter (HPF) and low-pass-filter amplifiers (LPF-AMP1, LPF-AMP2). Figure 7.5 shows the schematic diagram of LPF-AMP (left figure) and HPF (right figure). In order to process the spike signal from the preamplifier to be band-limited and further amplified it needs to be 10 times more gain ideally in the range of $100Hz$ to $7KHz$. A first-order gm-C high-pass filter is designed to have $103.7Hz$ cut-off frequency, and LPF-AMP1 which has gain of 10 has been designed. The inner-amplifier in the LPF-AMP1 is cascode mirror amplifier with class-AB output stage, as in the Figure 6.12 in the Chapter 6. Power consumption for the HPF and LPF-AMP1 is 0.439nW and 6.468μW, respectively. For the process of local field potential, low cut-off frequency LPF-AMP2 is required. The same structure of LPF-AMP in Figure 7.5 is used, but

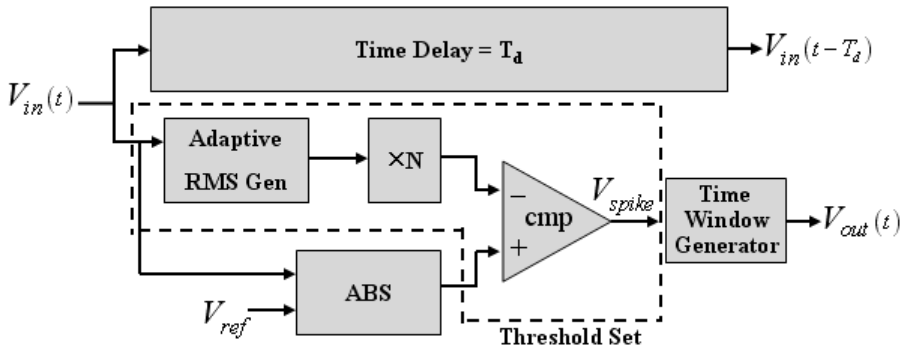


Figure 7.3: A block diagram of the adaptive spike detector using absolute value algorithm.

a mirror amplifier with class-AB stage is used for the inner amplifier. It has a gain of 10 and bandwidth of $153Hz$. It consumes 8.849μW.

7.3.3 Adaptive Spike Detector using Absolute Value Algorithm

Iyad and Patrick [131] have compared spike-detection algorithms for wireless brain-machine interfaces. They found that, in systems with limited computational resources, taking the absolute value of the neural signal before applying a threshold is just as effective for detecting spikes as applying more elaborate energy-based detectors using digital signal processing techniques. Based on their research, Figure 7.3 presents a proposed block diagram for an analog spike detector using an absolute value algorithm. It comprises four main building blocks: adaptive real-time threshold set block, absolute value block (ABS), Time delay block, and time window generator block. The adaptive real-time threshold set block was first introduced and validated by Harrison [132, 133]. It performs spike detection using a specified multiple (N in

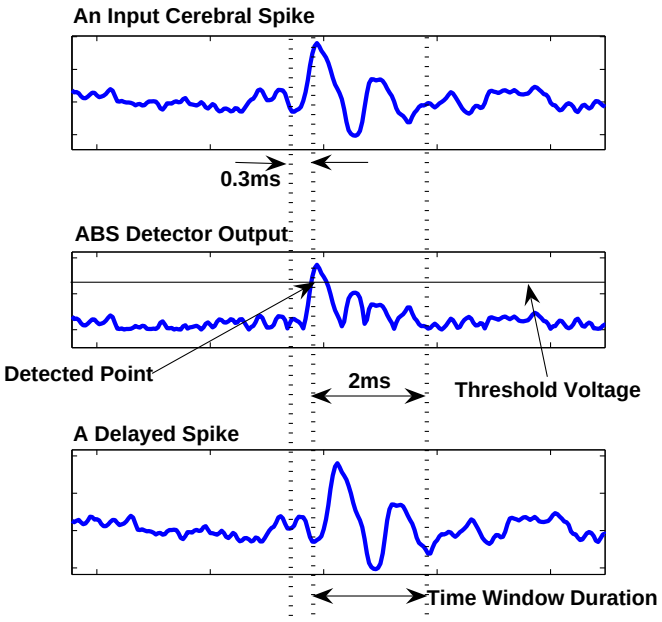


Figure 7.4: Typical specifications for a cerebral spike from a rat. This in-vivo data was acquired by Cold Spring Harbor Lab., New York. The threshold value was set by the adaptive spike detection algorithm in MATLAB.

Figure 7.3, usually 2 to 7) of the background noise rms value. ABS block generates absolute value with respect to common mode reference for input neural signal. Time window generator block produces 1-bit digital enable signals for $2msec$, that is required time period for successful recording of an active spike shape. Time delay block makes $0.3msec$ delay time without loss of any frequency component. It allows to record the entire waveform of detected spike. The delay is set based on observation that an active spike typically has $0.3msec$ time period before its waveform first reaches the estimated threshold value, and it would be already late to record a shape of neural spike even as soon as the adaptive detector recognizes it as a neural spike. Figure 7.4 shows the specifications for a detected neural spike.

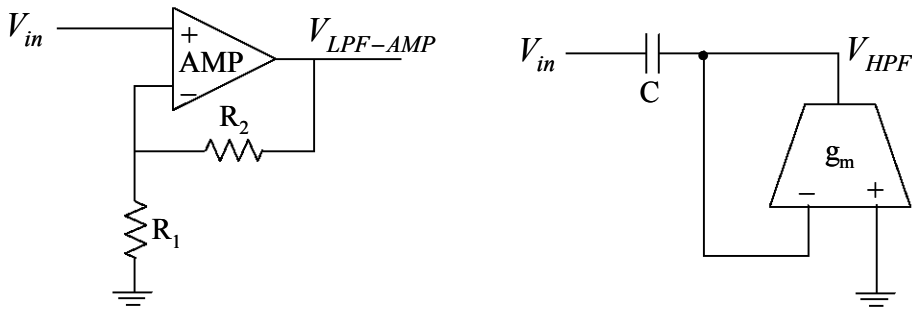


Figure 7.5: Schematic diagram of LPF-AMP (left) and HPF (right) used in the adaptive neural recording system.

Figure 7.6 represents waveforms through the proposed adaptive spike detector without/with the ABS in Matlab simulation, and plots the generated time window signals. As in the first row of the figure, it is observed that some negative spikes might be created by a cell as well as positive spikes. It can be detected by ABS (in the second row of the figure) and creates a time window for $2msec$ after delay time of $0.3msec$ as in the third row of the figure. If a consecutive spike hits the threshold during generating of $2msec$ time window for the previous one time window generator will reset the timer and extend $2msec$ more from that instant.

Circuits for Adaptive Spike Detector

Figure 7.7 depicts the implemented adaptive spike detector with ABS. Adaptive threshold set block in right side of figure 7.7 follows the topology in [132, 133]. Comparator A is used in feedback loop and setting $V_{1\sigma}$ to the rms level of the input waveform. This voltage is amplified by a constant level (usually 2 to 7) by the ratio of R1 and R2. The voltage, $V_{threshold}$, results in adaptive threshold voltage. Absolute value (ABS) circuit consists of two identical operational transconductance amplifiers

(OTA) and two identical PMOS cascode mirrors, rather than one OTA with one PMOS current source and one NMOS current sink introduced in [134], to reduce a current mismatch error between NMOS and PMOS. The designed ABS circuit was simulated in Cadence with an in-vivo cerebral signal collected from a rat. Figure **??** presents the transient response from the ABS circuit using input in-vivo neural signal. The first row in the figure is the simulated output from the ABS circuit, and their input signal is shown in the following row, amplified in-vivo spike signal from a rat. The absolute value of spike signal was referenced by 1.65V.

Figure 7.9 shows the schematic diagram of switched comparator. An inverter amplifier and a latch are utilized for the low power implementation, and they are running with two non-overlapping clocks.

For the time window generator, both analog and digital time window generators (TWG) can be considered to implement resetable time window function. While a digital TWG requires several-bits counter with decoding logics, an analog TWG needs a couple of capacitors and transistors. Analog TWG is preferable for low-power and small size implementation. To generate a resetable $2msec$ time window, an analog timer introduced in [90] was modified and simulated in Cadence. Figure 7.10 represents a schematic diagram of time window generator. It consists of three conceptual parts: (a) current reference (b) resettable timer (c) comparator. When a trigger is on the drain node of M_2 transistor is charged to V_{DD}. As soon as trigger is off it starts to discharge through M_2 transistor at the W/L ratio between transistors M_1 and M_2. In the current reference in the part (a), the current through M_1 is set by the frequency of non-overlapping clocks clk1 and clk2, C_2, and voltage difference between V_{DD} and equilibrium voltage on the top plate of three capacitors C_2 C_3 C_4

in clk2 phase. The stabilized current through M_1 transistor can be expressed as:

$$I_D(V_A) = f_{clk1,2} C_2 (V_{DD} - V_A) \tag{7.1}$$

where $I_D(V_A)$ is the saturation current of M_1 transistor and $f_{clk1,2}$ is frequency of non-overlapping clocks clk1 and clk2. By a size ratio of transistors M_1 and M_2, the size of C_1, and the clock frequency, the discharge current through M_2 can be well controlled. The following comparator consisting of $M_3 \sim M_8$ compares between the discharging node (drain node of M_2) and equilibrium voltage (V_A) of top plate of three capacitors C_2 C_3 C_4 in clk2 phase. When the two node voltages are getting similar by the discharge, the comparator ouptut has to be decided but it may not decide correctly instantaneously due to switching noise. The comparator is followed by a latch operating on clk1 phase so that the glitch noise effect can be avoided. The generated time window is determined by:

$$T = \frac{C_1}{MC_2} T_{clk1,2} + \frac{1}{2} T_{clk1,2} \tag{7.2}$$

where $T_{clk1,2}$=$1/f_{clk1,2}$, M=$(W/L)_{M2}/(W/L)_{M1}$. Figure 7.11 shows the behavior of time window generator by two separate triggers when M=1/16, $f_{clk1,2}$=$22kHz$, C_1=$2.7pF$, and C_2=C_3=C_4=$1pF$. After a trigger is activated and switched-off (the first row in the figure), the discharge is started so that the voltage tabbed d (the second row in the figure) is decreasing at constant slope. The time window is generated as soon as the trigger is on, but it is reset if another trigger is activated within $2msec$ (the third row in the figure).

Whole adaptive spike detector in Figure 7.7 was simulated for $150msec$ in

Cadence design environment with in-vivo spike signals from a rat. Figure 7.12 shows the simulation results. The first row represents the input in-vivo cerebral signal ranges from $321Hz$ to $8KHz$. The binary signals in second row are detected spike triggers, and finally, the $2msec$ time window signals are generated (the third row in the figure). The resistor ratio R2/R1 in the Figure 7.7 was set to 2 in this simulation. The magnified view of spike detection was captured in Figure 7.13: a magnified spike in the first row, adaptive threshold and absolute value of the spike in the second row, detected spike trigger in the third row, and time window signal in the last row.

All-pass Delay Filter Design

All-pass time delay filter is designed to make $0.3msec$ delay without loss of spike waveform. A 7th order filter is chosen to set $0.3msec$ delay and comprises one first-order and three second-order all-pass filters in a series starting with the first-order filter. A structure for discrete version of higher order all-pass filter and its coefficients was introduced in [135]. It was converted to its gm-C version for VLSI implementation. Figure 7.14 presents gm-C version of first-order and second-order all-pass filter structure. Their transfer functions are summarized in equation (1) and (2) respectively.

$$H_{1st}(s) = \frac{s - \frac{g_{m1}}{C}}{s + \frac{g_{m1}}{C}} \tag{7.3}$$

$$H_{2nd}(s) = \frac{s^2 - \frac{g_{m2}}{C_2}s + \frac{g_{m1}g_{m2}}{C_1C_2}}{s^2 + \frac{g_{m2}}{C_2}s + \frac{g_{m1}g_{m2}}{C_1C_2}} \tag{7.4}$$

The designed 7th order all-pass filter has $0.3msec$ delay up to 3dB bandwidth

Table 7.1: Summary of Simulated Power Consumption.

Building Block	Power consumption	Bandwidth
Pre-amplifier	57.82μW	$0.538Hz \sim 9.58KHz$
Adaptive spike detector	35.244μW	–
7th-order all-pass filter	0.54μW	$6.9KHz$
LPF-AMPs for spike	6.468μW	$8.56KHz$
LPF-AMPs for LFP	8.849μW	$153Hz$
HPF	0.439nW	$103.7Hz \sim$
Total consumption	108.92μW	–

Table 7.2: Produced Data-Rate by Proposed System.

	Ch.	Occupation	Fs	Resolution.	Data-Rate
Spikes	32	0.14	$22Ks/s$	10bit	985600bps
Others	32	1	$200s/s$	5bit	32000bps

of 7kHz and it has almost linear phase up to the bandwidth. Figure 7.15 presents the simulated magnitude and phase response of all-pass filter in Cadence. All three second-order filters use 1 pF capacitors and the very first filter, first-order filter, uses 2 pF capacitor. All designed transconductors have $200mV$ linear range and their transconductance range from $2nA/V$ to $15nA/V$.

7.4 Simulated Power Consumption and Data-Rate Improvement

The designed circuits were simulated in 3.3V power supply using Cadence SpectreS simulator. Table 7.1 summaries the power consumption of each simulated block. The total power consumption of single channel system excluding ADCs is 108.92μW.

It is known that spike firing rate for small animals is distributed widely from

$10 spikes/sec$ to $90 spikes/sec$ [136]. The spike firing rate from cerebral cortex of a rat is $50 \sim 60 spikes/sec$. Table 7.2 summarizes the tremendously reduced data-rate by the proposed adaptive spike detection system. Without adaptive system with the same specifications, the produced data-rate is $7040000 bps$. The proposed system reduces the data-rate almost 7 times.

The occupation rate of spikes in one second in Table 7.2 was calculated by assuming that maximum firing rate is $70 spikes/sec$. Since recording time for each spike is $2 msec$ the percentage occupied by spikes in one second is 14%. The total produced data-rate is $1017600 bps$ ($985600 bps$+$32000 bps$ in Table 7.2) which is less than $1 Mbps$ ($1048576 bps$). It allows us to transmit 32 channel neural data accurately using $1 Mbps$ Ultra Low Power Bluetooth technology.

7.5 A Low-Data-Rate Adaptive Spike Detection without Analog All-Pass Filter

The designed 7th-order cascade all-pass filter consists of 7 capacitors and 14 transconductors which may occupy large area. Ideally, it has to be a constant delay time for all the frequency components in the band of interests but the designed cascade filter has nonlinear delay time from $5 KHz$. Recent investigations have demonstrated that leap-frog (LF) structure is advantageous over the cascade configuration [138, 139, 141]. Leap-frog multiple-loop feedback (LF MLF) OTA-C filters offer better passband magnitude sensitivity, maximum input voltage, and magnitude frequency response considering OTA nonideality effects over IFLF and cascade OTA-C filters [140, 141]. However, LF MLF OTA-C filters need to have

much more number of transconductors than cascade structure (Almost 2-times more transconductors are required).

Much more robust and less sensitive delay element implementation can be achieved by digital delay elements and the proposed adaptive spike detection can be implemented together with digital delay elements. Figure 7.16 shows an alternative adaptive spike detection for neural recording. Basically, the position of delay elements are switched with 10-bit ADC. The ADC converts amplified and filtered neural spikes to the digital domain first, and then the detected spike signal is enabled by spike enable signal which is time window signal from Adaptive Spike Detector. The digital delay elements should hold the digitized spikes during $0.3msec$. The $0.3mSec$ delay can be implemented by 66 D-flipflops (assumed, sampling rate of $22KSamples/s$ for 10-bit ADC). This has the same functionality as the system in Figure 7.1 but without all-pass filter which may introduce a signal distortion, nonlinearity of delay, and large area consumption.

However, in the adaptive spike detection system using digital delay elements, the 10-bit ADC and 66 D-flipflops are continuously operating and may consume more power compared to the previous system in Figure 7.1 in which the ADC operates only when spikes are detected.

A fully differential structure can be adapted to minimize effects from digital switching noise. The structure of a preamplifier and a LPF-AMP can be taken from parts (a) and (b) in Figure 6.2 in Chapter 6, respectively, and the inner-amplifier for the LPF-AMP can be taken from Figure 6.12 in the same Chapter, improved amplifier with a class-AB output stage. The structure of BPF-AMP can be taken from single-ended version of bandpass amplifier which has been introduced in Figure 7.2. Gain

of preamplifier, BPF-AMPs, and LPF-AMP in Figure 7.16 have been set to be a reference voltage of 1V in two ADCs, since a linear range limitation of all-pass filter is not present.

7.6 Conclusions

This work presents a design of low-power, low-data-rate, wireless head-stage for small animals, 32-channel neural recording system. It is compatible with $1Mbps$ Ultra Low Power Bluetooth technology using button cell battery. The proposed adaptive neural recording system with all-pass filter can be improved with digital delay elements. This low-data-rate adaptive neural recording might be implanted with communication achieved with inductive link.

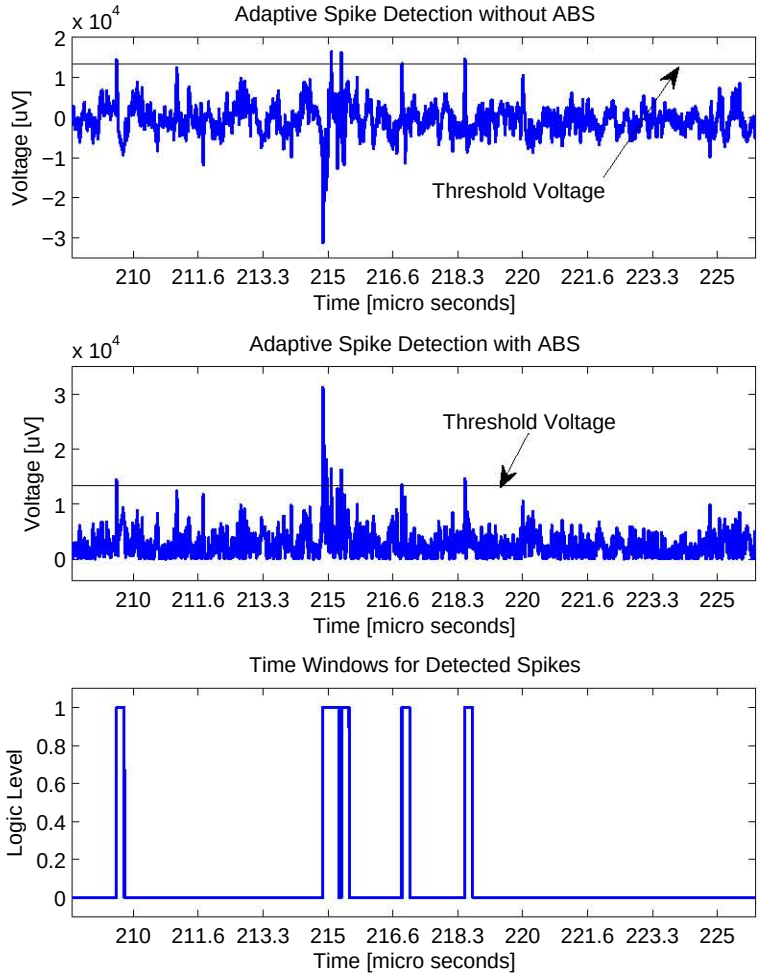


Figure 7.6: Comparative views of adaptive spike detector without ABS (figure in the first row) and with ABS (figure in the second row). The detected spikes allow to produce time window signals (figure in the third row).

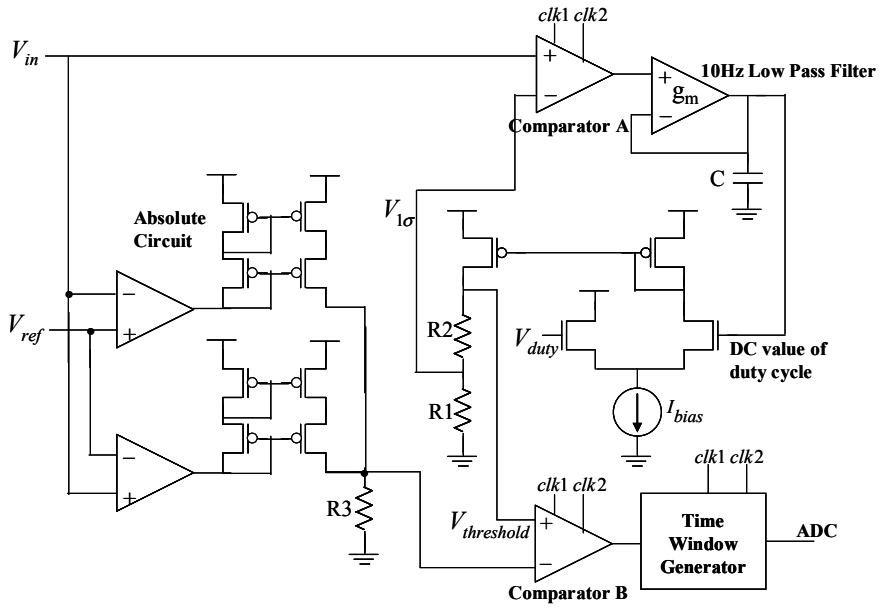


Figure 7.7: A schematic of the adaptive spike detector using absolute value. An absolute value circuit was adopted to implement absolute value algorithm and adaptive threshold set scheme was from Harrison's [132, 133].

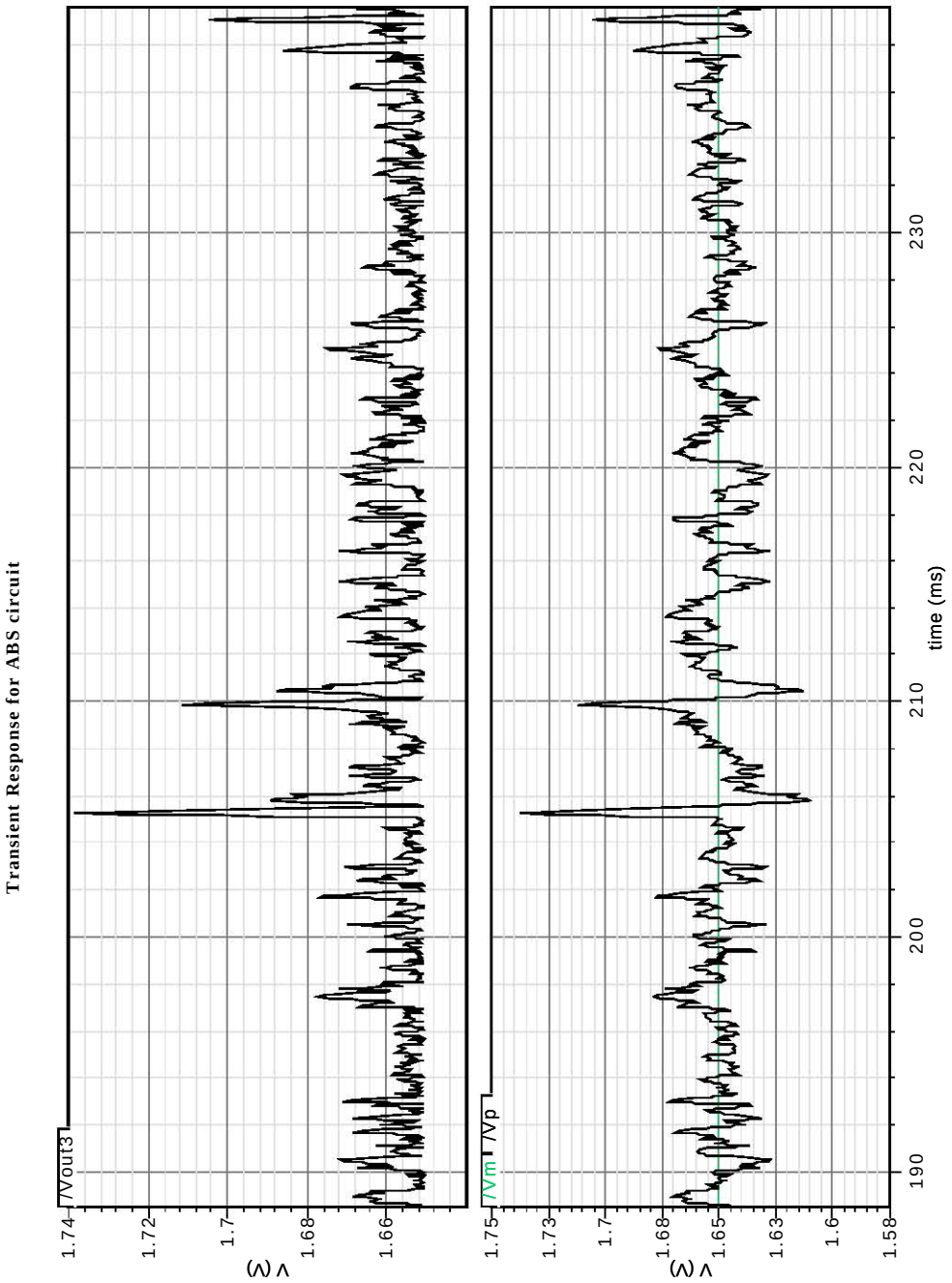


Figure 7.8: Transient response of absolute value circuit.

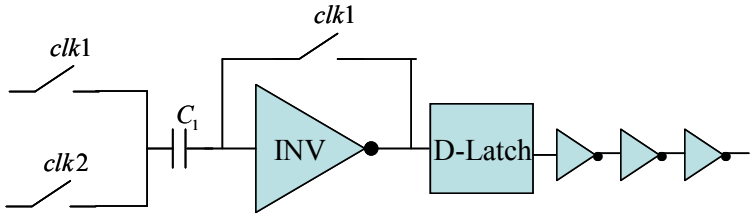


Figure 7.9: Schematic diagram of switched comparator.

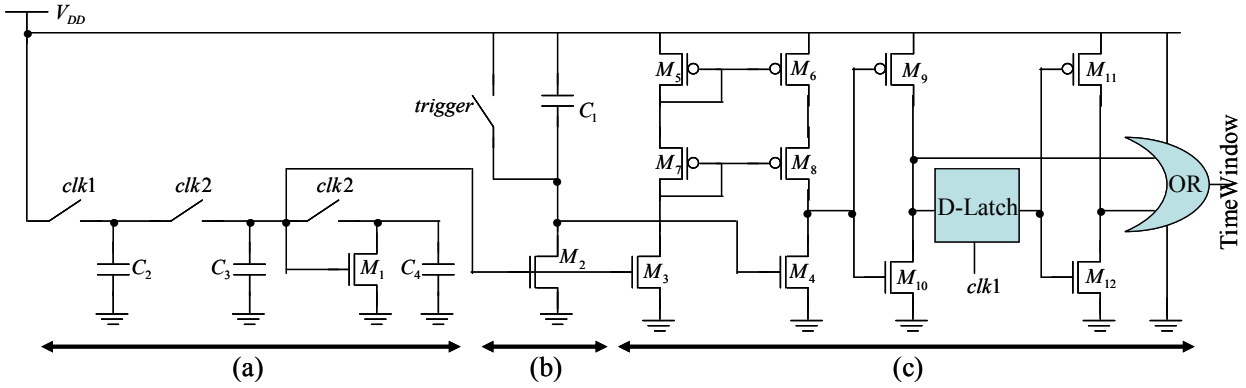


Figure 7.10: Schematic diagram of time window generator: (a)current reference (b)resettable timer (c)comparator.

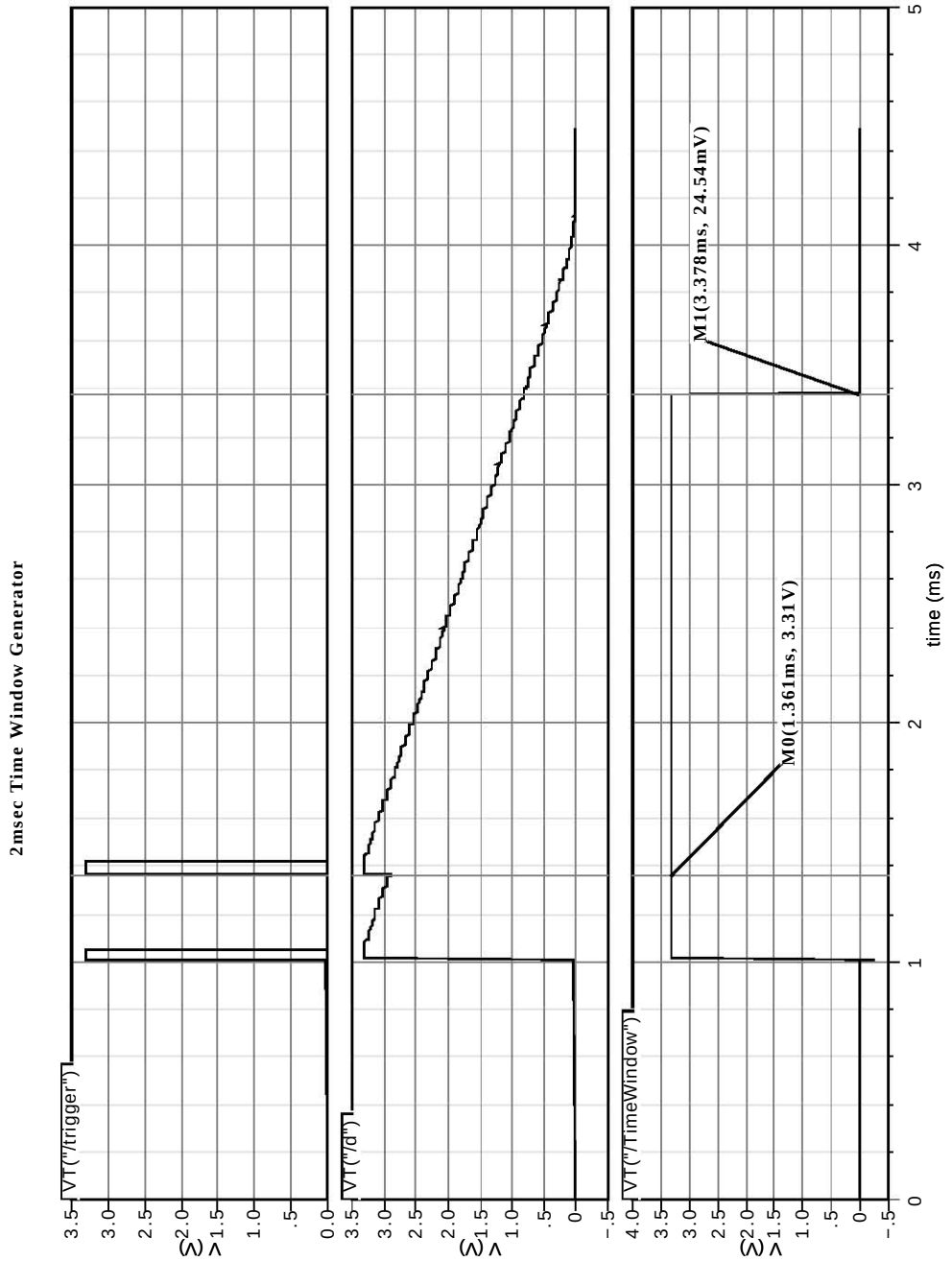


Figure 7.11: Transient response of the designed time window generator. Simulated time window is holding high for $2.017 mSec$ once a trigger is activated.

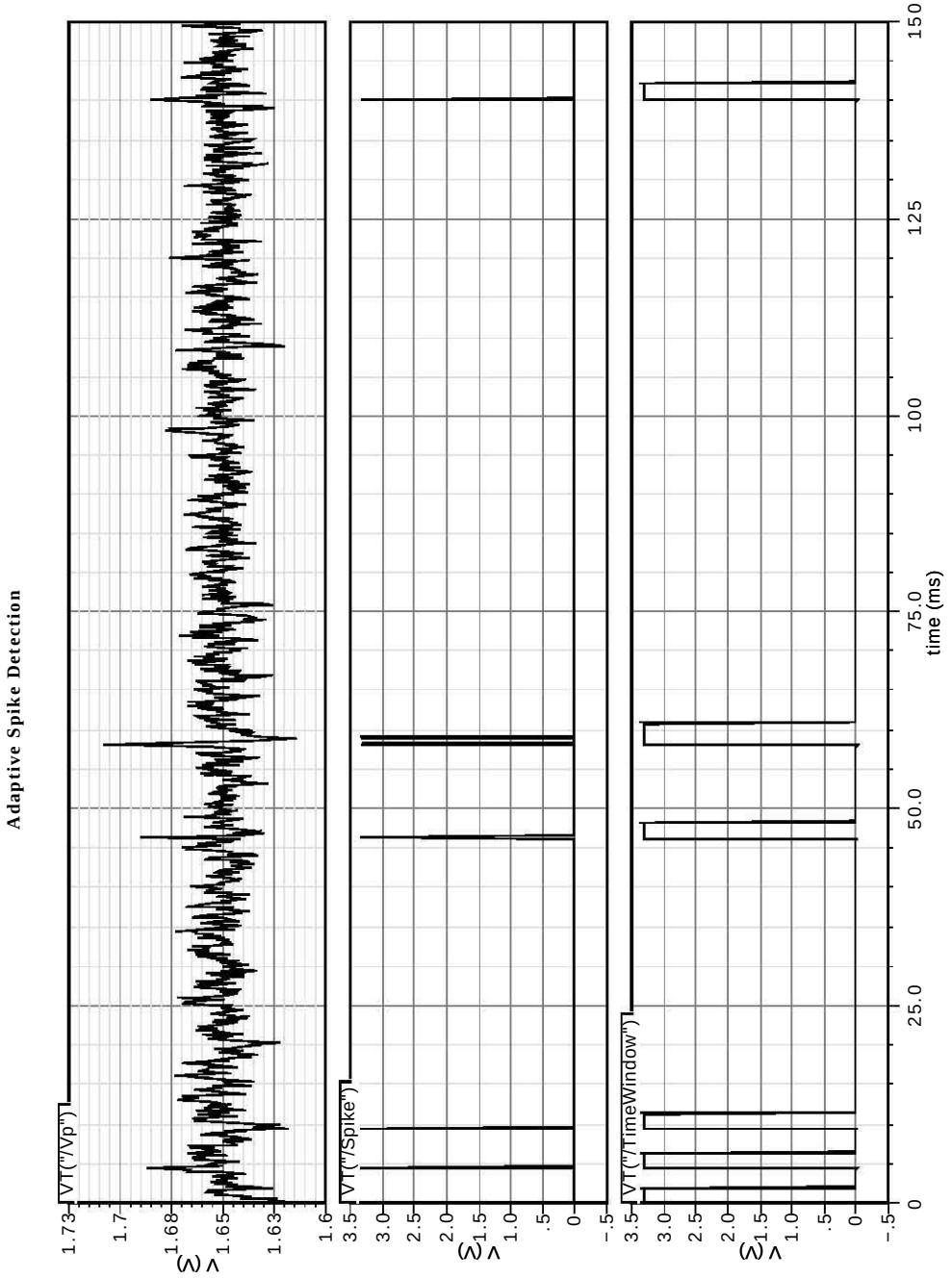


Figure 7.12: Transient simulation of adaptive spike detector for 150msec.

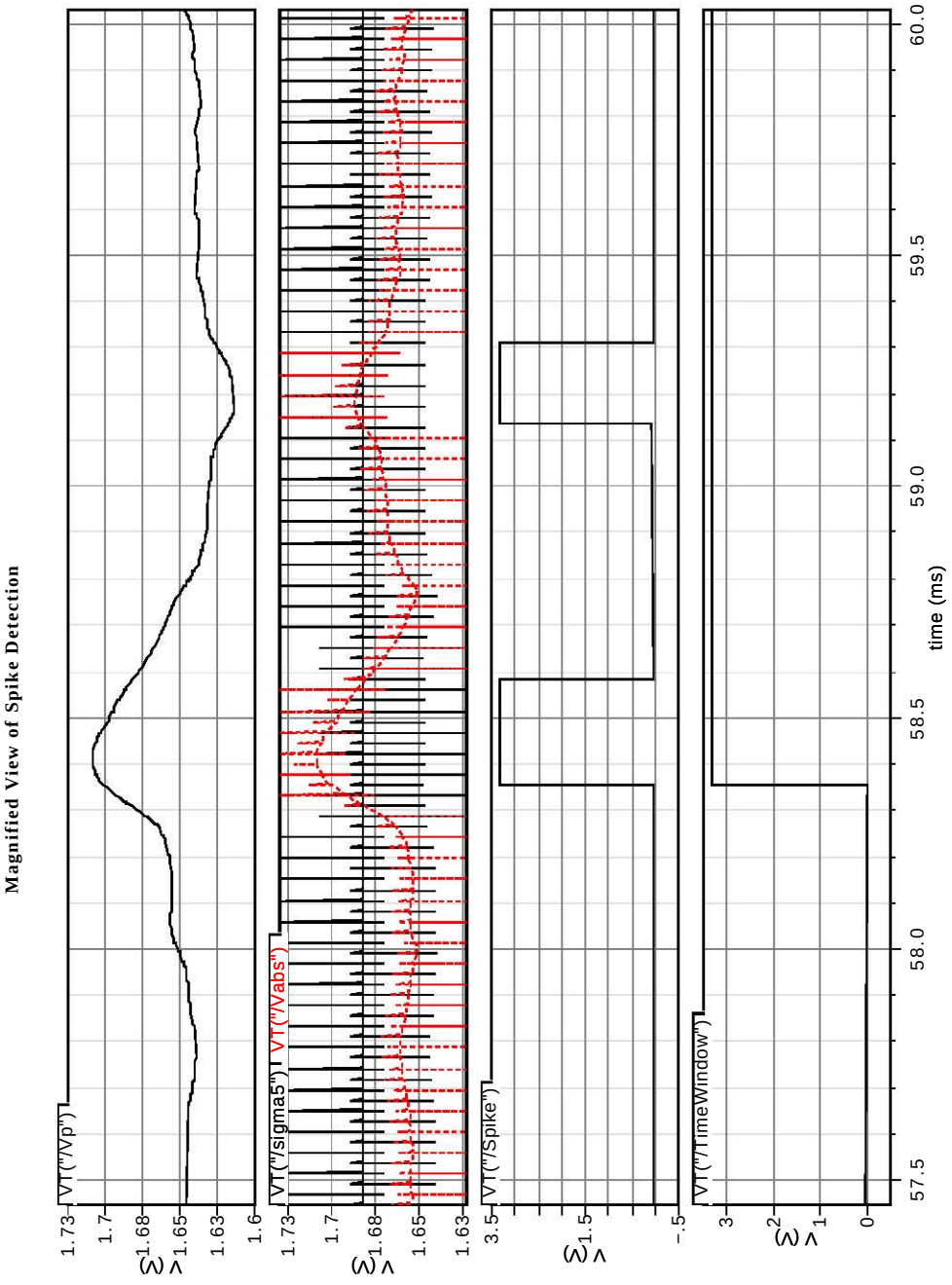


Figure 7.13: Magnified view of spikes and the detection.

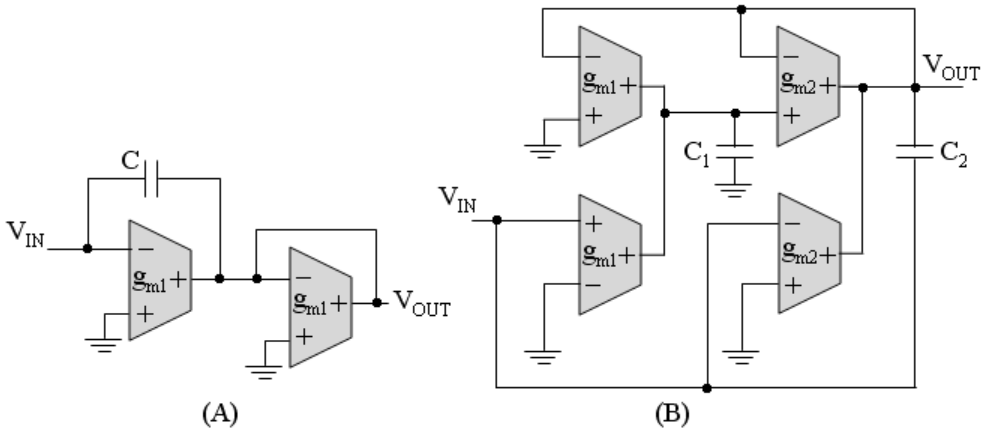


Figure 7.14: A first-order (A) and second-order (B) all-pass delay filter circuit.

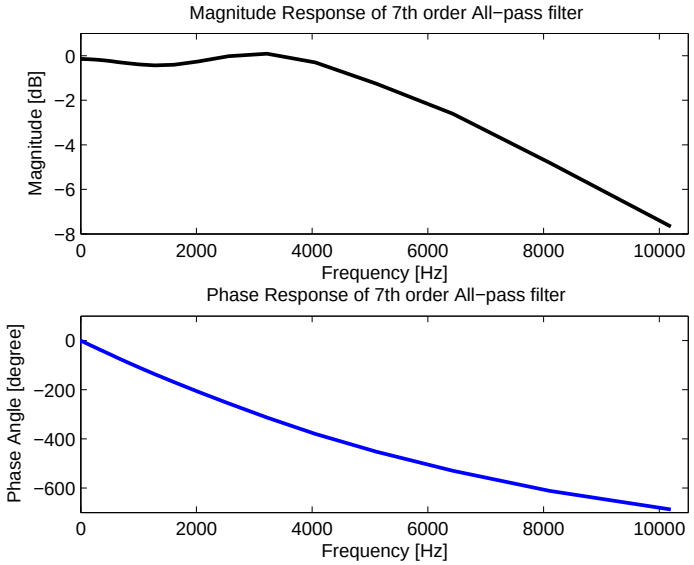


Figure 7.15: Magnitude and phase response of simulated 7th-order all-pass filter in Cadence.

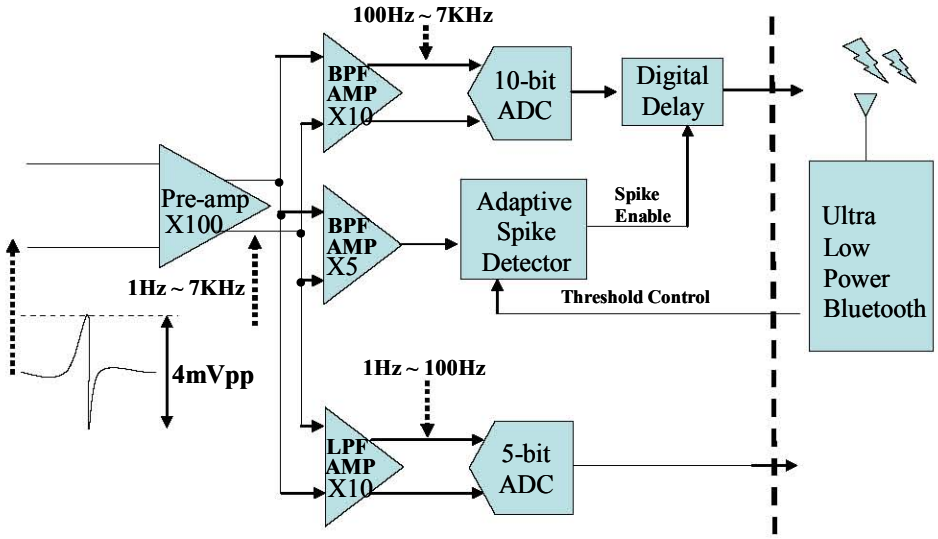


Figure 7.16: Block diagram of adaptive spike detection without analog all-pass filter.

Chapter 8

Conclusion and Future Work

This work presents a low-power analog front-end suitable for wired/wireless, multi-channel neural recording system.

Since acceptable data rate is typically limited to few Mbps (2 to $3Mbps$) in transcutaneous communication, when recording from a large number of multi-channel sensors in transcutaneous wireless systems, data-rate reduction is one of the critical issues in current wireless neural recording system. Using the adaptive spike detection techniques introduced in this work, we managed to reduce the data-rate almost 7 times while neural signals up to $7KHz$ bandwidth are recorded with high resolution.

An analog front-end for neural recording in CMOS and a preamplifier in FD-SOI were fabricated and tested. The discussion and improvements were considered at the end of each chapter. An adaptive spike detection scheme and associated circuits were introduced and simulated. The developed circuits and techniques can be applied to the implantable, wireless, low-power, and low-data-rate neural recording system. It includes a novel power harvesting system which supplies stable power to be able to

process neural data and communicate with the external electronics.

The implementation and testing of the considered adaptive spike detection system remains as a future work. The digitized neural data in multi-channels should be transferred in a wireless scheme. Before the transmission, multiplexing from multi-channels and compression of the large volume data can be researched as an issue. Also, the integrating multi-channel analog front-end with the adaptive spike detection together with multi-sensor arrays can be considered as a further research, fabrication, and test.

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