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Electron Transport Through Aluminum Oxide Tunnel Barriers and OPE-Based Molecular Junctions

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Abstract of the Dissertation

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This work presents results of a study of electron transport through aluminum-oxide based tunnel barriers and single-molecule transistors. Both systems have the potential for a dramatic increase of the density and performance of integrated circuits with critical dimensions well below the scaling limits of the conventional semiconductor technology. Studies of these two systems are also united by a common experimental approach - measurement of very small (down to 10^{-14} A) currents within a broad temperature range (from 4.2 K to 350 K).

Transport properties of $(Nb/)Al/AlO_x/Nb$ tunnel barriers have been studied for structures formed by (i) thermal oxidation and (ii) plasma oxidation, before and after their rapid thermal post-annealing at temperatures up to 650ºC. The post-annealing results in a substantial increase of the barrier height of the thermally formed aluminum oxide, which (within a broad range of RTA temperatures) may be substantially higher than that of the plasma-

grown AlO_x barriers. This fact, together with high endurance of annealed barriers under electric stress, may eventually lead to the fabrication of AlO_x and SiO_2 / AlO_x layered ("crested") barriers for advanced floating-gate memories.

Electron transport through single molecular devices has been studied for structures of three types: (i) co-planar Au electrodes with 5-nm-scale gaps formed by e-beam lithography, (ii) co-planar Au electrodes with 1 - 2 nm-scale gaps formed by electromigration, and (iii) nanowires crosspoints with vertical gaps of 3 to 5 nm formed by under-etched aluminum oxide layers. Two types of Oligo(Phenylene Ethynylene) based molecules (with or without naphthalene diimide groups working as acceptors), capped with iso-cyanide terminal groups, have been investigated. For both molecules, nonlinear current-voltage curves with discrete current steps, due to tunneling through one or a few molecules, have been observed, and their dependences on the gate voltage and temperature have been studied in detail.

Key Words: electron transport, aluminum oxide, crested barrier, rapid thermal annealing, single-electron transistor, electromigration, molecular junction.

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Chapter 1

Introduction

The field of semiconductor electronics has been the most significant technological advance of the past half century. Since the introduction of the integrated circuit in the late 1950s, the number of individual transistors that can be placed on a single integrated circuit chip has approximately doubled in every 18 months (as first pointed out by Gordon E. Moore of Intel, so this trend has been dubbed Moore's Law). The demand for higher computing power and larger data storage capacity has been the driving force in the past decades for more advanced chip technology. Fundamentally, the integrated circuit (IC) industry has employed the "top-down" approach, in which the devices are fabricated by processes such as optical Si lithography, doping thin-fim deposition, etching and metallization. The key advantage is that the parts are both patterned and built in place so that no assembly step is needed.

As the size of the individual electron device approaches nanometer scale, we are approaching the physical limit of top-down silicon technology [1], including transistor scalability, device performance and power dissipation [2]. When the device size is shrinking to the nanometer scale (< 10 nm), the tunnel dielectric will suffer from direct tunneling [3] and severe stress-induced leakage current [4], [5]. The huge intensity of heat generated by millions of transistors will also result in chip performance degradation or even function failure. Lithographic techniques used to produce the circuitry on the silicon wafers are limited by the wavelengths at which they work. While the silicon-based technology may still serve as a mainstream platform for most IC technologies in the next 15 - 20 years, alternative technologies have been suggested in terms of channel materials, transistors, circuits and system-level architectures [10].

Memory is one of the most important parts of any contemporary electronics devices, including all modern computers, cell phones, digital cameras, portable digital audio/video players [6], [7]. It can store data for a certain period of time dependent or independent of external power supply based on

its volatility. Most forms of modern random access memory provide volatile storage, including high speed dynamic random access memory (DRAM) and static random access memory (SRAM), which means they lose all data when the system is powered down. Nonvolatile memories can retain the stored information without power, *e.g.*, read-only memory (ROM), flash memory, *etc.* At the moment, flash memory is the fastest growing segment of the memory market because of its portability and non-volatility. However, flash memory has slow program and erase speed (μs and ms scale, respectively), compared to that of CMOS logic (ns), primarily due to the requirement of 10-year retention time and reliability concerns. It would be a great achievement to develop a non-volatile memory system with both fast speed comparable to volatile RAM and the 10-year retention ability, such as "NOVORAM" [13] - [18], a highly scalable, non-volatile, floating gate, random-access memory. Such technology would not only save space and energy, but also allow for computers to be turned on and off with the simple press of a button, bypassing the annoyingly slow start-up sequence.

For a floating gate memory (or "flash" memory), silicon dioxide is widely used as the tunnel dielectric. To keep scaling down the transistor as Moore's law demands, the tunnel barrier engineering has been intensively studied. For example, a high-k dielectric, such as Al_2O_3 or Si_3N_4, is physically thicker than SiO_2 for the same equivalent oxide thickness (EOT), hence substantially reducing the leakage current due to direct tunneling. Another option is to use layered "crested" barriers [13]. At the optimum choice of the potential barrier heights (*i.e.* conduction band offsets) of the layers and their dielectric constants k, such "crested" barriers could change their transparency by more than 16 orders of magnitude at mere doubling of the voltage applied to the barrier, which is favorable for "NOVORAM" applications.

Other alternative nanodevice concepts, for example, quantum interference devices or single-electronics, offer some potential advantages over MOSFETs, including a broader choice of possible materials. Unfortunately, the minimum features of these devices (*e.g.*, the single-electron transistor island size) for room-temperature operation should be below ~ 1 nm. Since the relative accuracy of their definition has to be of the order of 10%, the absolute accuracy should be of the order of an angstrom or less, far too small for the current and even realistically envisioned future lithographic techniques.

This is why there is a rapidlly growing consensus that the impending crisis in the microelectronics progress may only be resolved by a radical paradigm shift from lithography to bottom-up fabrication. In the latter approach, the smallest active devices should be formed in some special way, ensuring their fundamental reproducibility. Opposite to the top-down method, the bottom-

up approach offers much more scalable materials and devices, more flexible material choices, high component packing density and low power dissipation, by employing inexpensive chemistry to promote self-assembly of complex mesoscopic architectures. While the traditional semiconductor technology is reaching the end of the roadmap, molecular nanotechnology opens doors leading to molecular level engineering. The nanoscale components can be inorganic nanocrystals such as nanotubes and semiconductor nanowires, or organic molecular components such as molecular monolayers, molecular wires, single molecules and supramolecules with different architectures. There are a great number of molecular species available, with the potential to be tailored for different device applications by chemical synthesis and surface engineering. These molecular components have great potential in building ultra-dense, low power and low cost computing chips.

However, integrated circuits consisting of molecular-size devices alone are hardly viable, because of their limited functionality. For example, the voltage gain of a 1-nm-scale transistor, based on any known physical effects (*e.g.*, the field effect, quantum interference, or single-electron charging), cannot exceed one, *i.e.*, the level necessary for the operation of virtually any active analog or digital circuits. This is why the only plausible way toward high-performnce nanoelectronic circuits is to integrate nanoscale (*e.g.*, molecular) devices, with the connecting nanowires, on top of CMOS chips whose field-effect transistors would provide the circuit with the necessary additional functionality, in particular high voltage gain. The practical implementation of such hybrid integration, of course, faces several hard challenges, in particular that of interfacing the nanowires with cruder, lithographically-defined CMOS-level wiring. We believe that the recent suggestion of a specific species of CMOS/nanodevice hybrids, called "CMOL" (standing for CMOs/MOLecular circuits) [11] has opened an efficient way for the solution of the interfacing problem.

A CMOL circuit would combine an advanced CMOS subsystem with two mutually perpendicular arrays of parallel nanowires and similar nanodevices formed at each crosspoint of the nanowires. The reason for this topology is that parallel nanowire arrays may be fabricated by several high-resolution patterning technologies, such as nanoimprint or interference lithography. These novel technologies cannot be used for pattering of arbitrary integrated circuits, in particular because they lack an adequate layer alignment accuracy; fortunately the crosspoint topology does not require such alighment. This approach requires a nanodevice formation process that also does not need lithographic patterning.

The purpose of this thesis work was two-fold: (1) to explore the possibilities of implementation of specially engineered "crested" barriers for fast,

scalable, nonvolatile random-access memories; and (2) to study single-electron integrable molecular devices for the possible future use as sub-10-nm crosspoint latching switches in CMOL circuits. The outline of the thesis is as follows.

In Chapter 2 we give an introduction to the layered "crested" barriers and their advantages over traditional SiO_2 tunnel barriers. The main transport mechanism is based on direct tunneling and the calculation of tunneling current will be demonstrated. The transmission coefficient may be calculated by joint solution of the Schrödinger and Poisson equations.

Chapter 3 describes the fabrication and electrical characterization of aluminum oxide barriers grown by thermal and plasma oxidation of aluminum thin film, with rapid thermal post-annealing of the resulting junctions. The barrier parameters, such as barrier height, and barrier thickness have been extracted from numerical fittings employing the quantum tunneling model. TEM characterization of these barriers will be also presented. Some initial experimental data for the double layer barriers, combining these two types of AlO_x, are also shown.

A brief introduction to electron transport in single-molecule junctions will be given in Chapter 4, with a brief summary of current experimental techniques to realize molecular devices. We are particularly interested in oligo(phelene-ethylene) based molecules with, or without the center naphthalene diimide acceptor group.

In Chapters 5-7, we investigate electron transport through single molecular devices for three types of structures: (i) co-planar Au electrodes with ∼ 5 nm gaps formed by e-beam lithography, (ii) co-planar Au electrodes with 1 ∼ 2 nm gaps formed by electromigration, and (iii) nanowires crosspoints with vertical gaps of 3 ∼ 5 nm formed by under-etched aluminum oxide layers. We use two types of oligo(phenylene-ethynylene) based molecules capped with iso-cyanide terminal groups: (i) molecular wire-like OPE chains with one or two rings in the middle; (2) molecular transistor-like OPE-NDI (naphthalenedi-imide) chains, where the NDI group is served as a single-electron island in the middle. Their current-volatage characteristics and dependences on the gate voltage and temperature have been studied in detail. We have observed nonlinear current-voltage curves with either conductance peaks or Coulomb blockade with single-electron addition energy above 100 meV.

Chapter 2

Crested Tunnel Barrier: Simulation and Barrier Engineering

In this chapter, we first introduce the concept of crested tunnel barriers and their applications on nonvolatile memory devices. A charge transport model is presented to calculate the tunneling current through layered barriers. The numerical algorithm is based on the joint solution of Schröinger equation and Poisson equation. Barrier engineering will be discussed to find the optimized barrier parameters.

2.1   Operating Principle in Flash Memory

The demand for non-volatile semiconductor devices has grown rapidly in recent years. Among the different categories in non-volatile semiconductor devices including ROM, EPROM, EEPROM, *etc.*, flash memory has been considered as of the most interest. The basic operating principle for flash memory lies in the charge storage in the floating gate of a metal-oxide semiconductor field effect transistor (MOSFET), as illustrated in Figure 2.1 a. Charge is stored on the floating gate of flash memory after electrons are transported through the tunnel oxide from the channel generated in the silicon substrate. The tunnel oxide, usually silicon oxide, must be sufficiently thin for high electric field to induce tunneling of electrons toward the floating gate, but still thick enough to trap the charges in the conduction band of the floating gate. Upon the removal of the gate voltage, the field in the tunnel barrier should be small to prevent charge from tunneling back to the substrate. By applying appropriate voltages to the control gate, source, and drain electrodes, charge carriers travel

through the tunnel oxide and are stored on the floating gate even after the voltages are removed. The amount of charge stored on the floating gate of the MOSFET can be modified to alternate between two distinct values, usually defined as the "0" erased state and the "1" programmed state, as shown in 2.1 b.

The state of a flash memory device is detected by applying a gate voltage V_G with a value between the two possible threshold voltages. In one state, the transistor conducts current, while in the other state, no current flows. Even if the power supply is interrupted, the stored charge will keep the requested memory state for later use.

2.2   What's a Crested Tunnel Barrier

The programming speed in nonvolatile floating-gate memory cells is rather slow for standard silicon dioxide barriers (of the order of miliseconds). The main reason is that such uniform barrier cannot combine the low transparency necessary for long retention time with the high transparency necessary for fast write/erase time. This drawback limits the application of floating-gate memories to compete with random-access memories and flash memories.

The crested barrier concept proposed by Likharev [13] provides an exciting opportunity for the radical improvement of nonvolatile semiconductor memories. By carefully engineering the barrier profile, we could obtain memories with high programming speed comparable to DRAM (~ 10 ns) and long retention time (~ 10 years) at the same time. The transparency of such barriers is much more sensitive to the applied voltage than the traditional uniform layers, due to the faster decrease of tunnel barrier height. As a result, it could be used in fast, bit-addressable nonvolatile random access memories (NOVORAM), a leading candidate for multi-terabit memory chips with scalability.

The schematic representation of a floating gate memory is shown in Figure 2.1 a. with three corresponding conducting band edge diagrams (Figure 2.2). The solid lines represent the diagrams at $V = 0$, while dotted lines show the effective band-offset after voltage V is applied.

(1) Uniform barrier: Usually we use three parameters to describe the potential of the oxide with uniform barriers: the average barrier height ϕ_a ($\phi_a = (\phi_B + \phi_C)/2$), barrier asymmetry $\Delta\phi = \phi_C - \phi_B$, and the barrier thickness d, where ϕ_B and ϕ_C are the tunnel barrier heights at the oxide interfaces with the base electrode and the counter electrode. It is widely used in conventional floating gate memory devices, *e.g.*, silicon oxide. Although it could retain a few years retention time, the write/erase time is in millisecond range, much slower than the current DRAM (~ 10 ns). The reason is that the
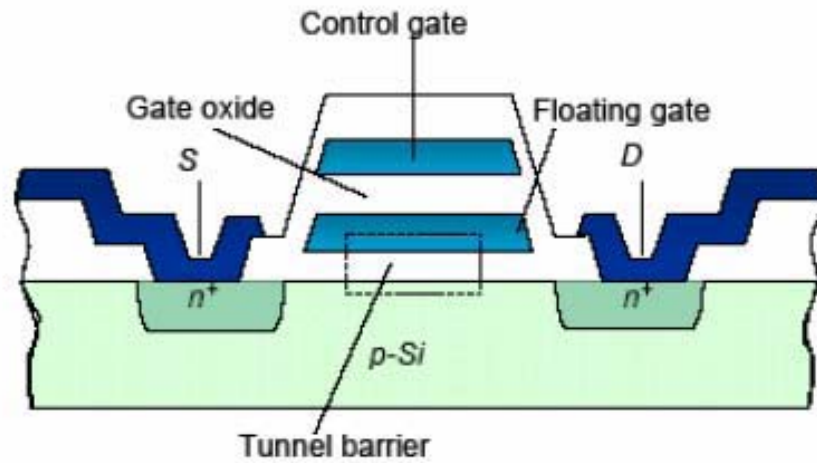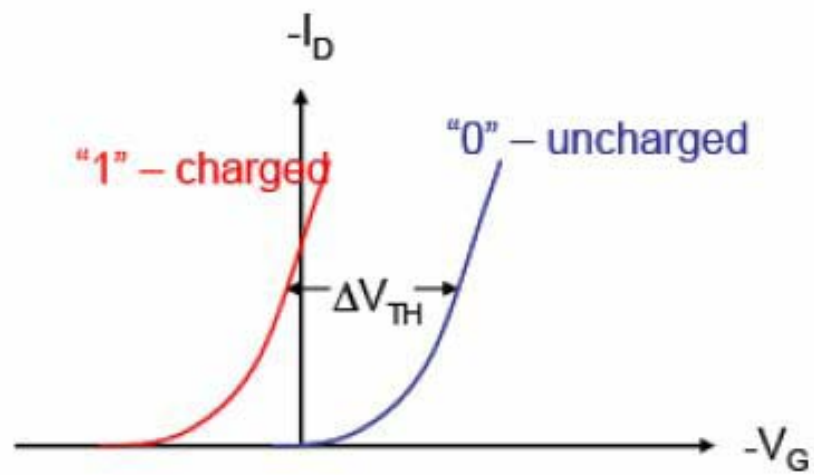
Figure 2.1: a. Schematics of a floating gate memory; b. Influence of charge of the floating gate on MOSFET's current.
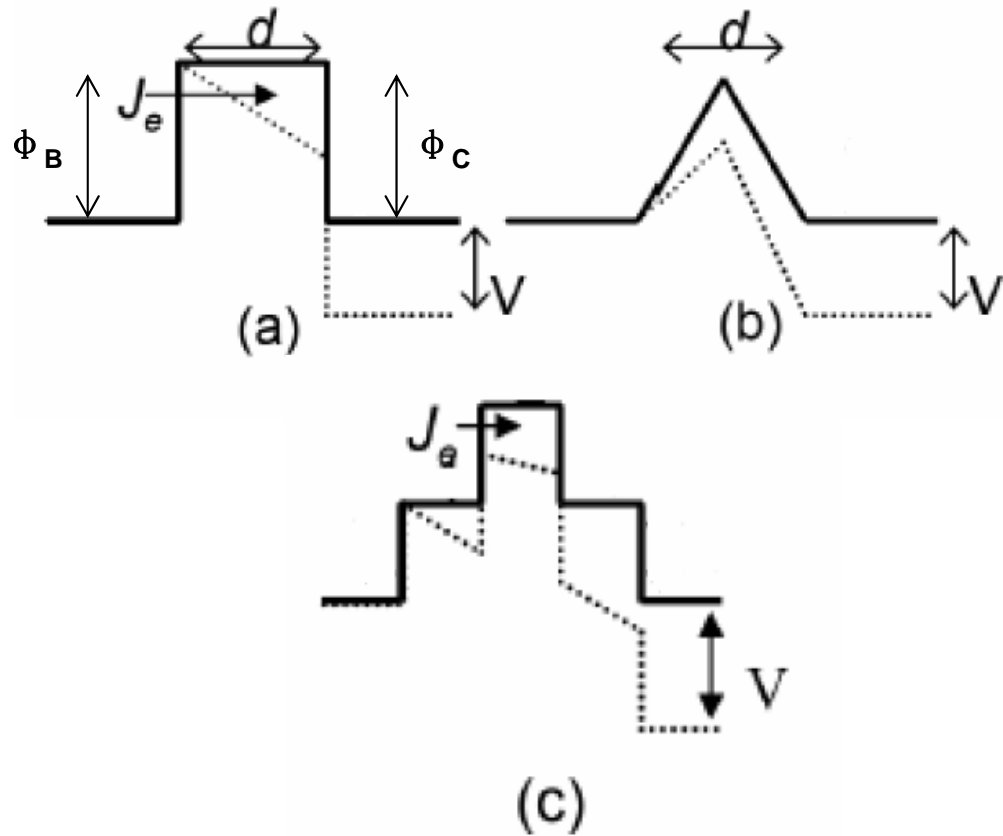
Figure 2.2: Conduction band edge diagrams of various type of tunnel barriers: (a) a typical uniform barrier; (b) idealized crested barriers (c) crested, layered barriers. Dashed lines show the barrier tilting caused by applied voltage V.

barrier transparency depends slowly on the applied electric field. The highest part of the barrier (close to the source electrode) is weakly affected by the applied voltage $\phi_{max}(V) \approx \phi_{max}(0)$.

(2) Triangular or "crested" barrier refers to a tunnel barrier with the highest barrier height in the middle and gradually decreasing side barriers toward the conducting electrodes. The transparency of this type of barrier is much more sensitive to the applied electric field, due to the fact that maximum potential (close to the middle of the barrier) is strongly dependent on voltage V: $\phi_{\max}(V) = \phi_{\max}(0) - eV/2$. Calculations [13] show that the floating gate recharging time could change from 10^8 s to 10^{-8} s when the voltage changes from V_0 to $2V_0$ (here, V_0 characterize the maximum voltage created by stored charge). This dramatic improvement enables possible applications of such barriers in NOVORAM. The implementation of crested barriers is straightforward, if the barrier shaping may be achieved with either a gradual change of the layer composition [28], [29], or by modulation doping [30] in A_3B_5 compounds. However, the maximum barrier height for these materials is too small to provide sufficient retention time at room temperature. For most wide-bandgap materials, it is not yet possible to make such graded barriers that are compatible with current technology.

(3) A layered tunnel barrier may be fabricated by stacking two or three layers of dielectric materials with appropriate barrier parameters and suggested as an alternative to the triangular barriers. Calculations [13] show that the layered barrier could perform as good as the triangular barrier, by combining, say, a three-year retention time with a 10-ns programming time. The electric field necessary for write/erase can be as low as ~ 6 MV/cm, which ensures high endurance of such barrier under electric stress. At the optimum choice of their potential barrier heights and dielectric constants, the transparency of the tunnel barrier can be changed to more than 16 orders of magnitude by merely doubling the applied voltage. The applications of the layered barriers include bit-addressable nonvolatile random access memories (NOVORAM), fast single- and few-electron memories, electrostatic data storage (ESTOR) systems [14] - [18].

2.3 Calculation of Tunneling Current Through Metal-Insulator-Metal Junctions

Based on the free electron approximation [9], the coherent tunneling current through typical metal-insulator-metal devices may be calculated by jointly solving Schröinger equation and Poisson equation. Assuming that the energy

of the tunnel electron and the transverse component of the momentum are both conserved, the tunneling current density is given by:

$$J = \frac{em_e}{2\pi^2\hbar^3} \int_0^\infty dE_x \int_0^\infty dE_\perp \mathcal{T}(E_x, E_\perp)[f_L(E_x, E_\perp) - f_R(E_x, E_\perp)]. \quad (2.1)$$

where $\mathcal{T}$ is the transmission coefficient; E_x, $E_\perp$ are the local energy and the transverse energy of a tunneling electron; m_e is the effective mass of the transverse electron and f_L, f_R are the equilibrium Fermi-Dirac distribution functions in the left and right electrodes.

For anmetal-insulator-metal (MIM) junction, we could use a 1D model to describe the barrier profile. The tunneling current density includes the carrier transport in both directions between two metal contacts. In the case of $T = 0$, the Fermi energy function of the metal is written as:

$$f_i(E_x, E_\perp) = \begin{cases} E_{fi} & \text{if } E_x \leq E_{fi}, \\ 0 & \text{if } E_x > E_{fi}, \ i = L, \ R. \end{cases} \quad (2.2)$$

where E_{fL} and E_{fR} are Fermi energies of the left and right metal electrodes respectively. The current density J could be simplified as:

$$\begin{aligned} J &= J_{L->R} - J_{R->L} \\ &= em_e/(2\pi^2\hbar^3)\left\{ eV \int_0^{E_{fL}-eV} \mathcal{T}(E_x)dE_x + \int_{E_{fL}-eV}^{E_{fL}} \mathcal{T}(E_x)(E_{fL} - E_x)dE_x \right\}. \end{aligned}$$
$$(2.3)$$

For the case of $T > 0$, we assume that the electrons are distributed according to equilibrium Fermi-Dirac distribution in the left and right electrodes, determined by the bulk Fermi levels on the respective sides of the barrier:

$$\begin{aligned} f_L(E_x, E_\perp) &= 1/(1 + \exp(\frac{E_x+E_\perp-E_{fL}}{k_BT})), \\ f_R(E_x, E_\perp) &= 1/(1 + \exp(\frac{E_x+E_\perp-E_{fL}+eV}{k_BT})). \end{aligned} \quad (2.4)$$

The current density is thus given by:

$$j = \frac{em_e}{2\pi^2\hbar^3}k_BT \int_0^\infty \mathcal{T}(E_x)dE_x \int_0^\infty [f_L(E_x, E_\perp) - f_R(E_x, E_\perp)]dE_\perp. \quad (2.5)$$

After integration over the transverse energy $dE_\perp$ for the second integral, we obtain:

$$j = \frac{em_e}{2\pi^2\hbar^3}k_BT \int_0^\infty \mathcal{T}(E_x)ln(\frac{1 + e^{(E_{fL}-E_x)/k_BT}}{1 + e^{(E_L-E_x-eV)/k_BT}})dE_x. \quad (2.6)$$

This is called the Tsu-Esaki formula. The logarithmic term is called the supply

function.

2.4   Transmission Coefficients

The key quantity in the tunneling current is the transmission coefficient $\mathcal{T}$. Several methods of its calculation have been developed. One of the most commonly used is the WKB (Wentzel-Kramers-Brillouin) approximation. The wavefunction is approximated as an exponential function, and the amplitude or the phase is taken to be slowly changing. For a simple trapezoidal tunnel barrier, the transmission coefficient $\mathcal{T}$ is given by:

$$|\mathcal{T}|^2 \approx \exp(-2 \int_0^d dx [\frac{2m_e}{\hbar^2}(U(x,V) - E)]^{\frac{1}{2}}), \qquad (2.7)$$

where $U(x,V)$ is the potential function of the barrier at the applied voltage V, d is the width of the barrier. The probability of barrier penetration is exponentially dependent on the product of the barrier height and thickness.

Although the WKB approximation provides good estimation for the transmission coefficient $\mathcal{T}$, it has drawbacks, especially for the thin and sharp barriers for metallic electrodes in a few nanometer range. It is questionable to apply the formula to gate stacks with ultra-thin interfacial oxide layer with thickness comparable to the de Broglie wavelength of the tunneling electron, since the method does not include quantum mechanical interferences of the incident and reflected waves at the interfaces it does not properly treat the transmission near the band edges or through propagating states [20]. Our calculations [19] have shown a significant difference between WKB calculation and the exact solution for 1-nm-thin barriers, which is equivalent to be a $\sim 3\%$ error for average barrier height ϕ_a and $\sim 10\%$ error for effective barrier thickness d_{ef} $(= (m_e/m_0)^{1/2}d$, where m_0 is the electron mass).

A more accurate way to calculate the transmission coefficient $\mathcal{T}$ is obtained by numerically solving the Schrödinger equation and Poisson equation. We solve for $\mathcal{T}$ using transfer matrix formalism [27]. By breaking the potential barrier into N square pieces (Figure 2.3), the transmission coefficient can be calculated to arbitrary precision within the independent-electron picture. For each slice i, the Schrödinger equation can be solved analytically. Assuming that a one-band parabolic dispersion model is used for all the dilelectric layers, we use plane wave functions to describe the incoming and outgoing electrons through each slice:

$$\psi(x) = A_i e^{ik(x-X_i)} + B_i e^{-ik(x-X_i)}, \quad X_i < x \le X_{i+1} \qquad (2.8)$$
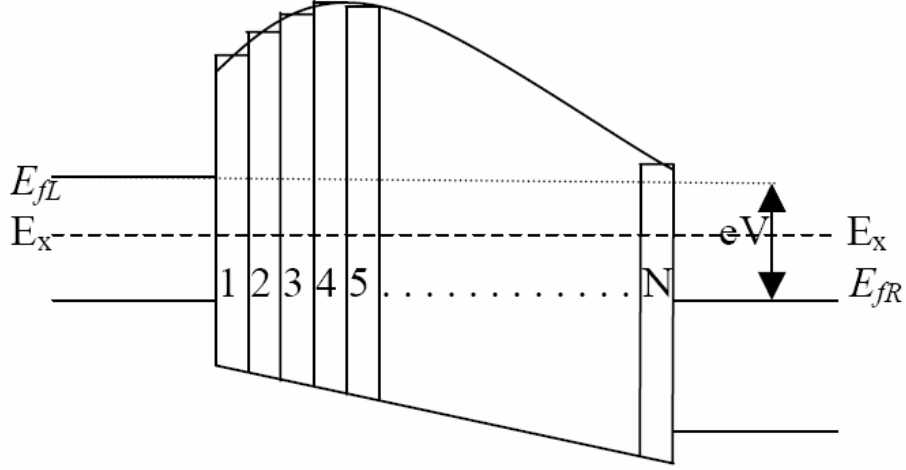
Figure 2.3: Illustration of the potential barrier divided as N equal pieces.

with

$$k = \sqrt{2m(E - U)}$$

where U is the potential energy of the barrier, and X_i is the position of the ith slice. The boundary conditions require continuity of the wave function and its spatial derivative, which satisfy:

$$\psi(x)|_{x=X_i^-} = \psi(x)|_{x=X_i^+} \tag{2.9}$$

$$\frac{1}{m_i^-}\frac{d\psi(x)}{dx}\Big|_{x=X_i^-} = \frac{1}{m_i^+}\frac{d\psi(x)}{dx}\Big|_{x=X_i^+} \tag{2.10}$$

where the + and - symbols are used for the left and right sides of a specific interface X_i.

As a result, we obtain 2×2 matrices: $\mathbf{b}_{i+1,i}$ from boundary conditions and the propagation matrix $\mathbf{p}_{i+1}$ for i^{th} slice as follows:

$$\begin{pmatrix} A_{i+1} \\ B_{i+1} \end{pmatrix} = \mathbf{p}_{i+1}\mathbf{b}_{i+1,i} \begin{pmatrix} A_i \\ B_i \end{pmatrix}. \tag{2.11}$$

Matrices $\mathbf{p_i}$ and $\mathbf{b_{i+1,i}}$ are expressed as follows:

$$\mathbf{p}_i = \begin{pmatrix} e^{jk_i a} & 0 \\ 0 & e^{-jk_i a} \end{pmatrix}; \mathbf{b}_{i+1,i} = \frac{1}{2}\begin{pmatrix} 1 + k_i m_{i+1}/k_{i+1}m_i & 1 - k_i m_{i+1}/k_{i+1}m_i \\ 1 - k_i m_{i+1}/k_{i+1}m_i & 1 + k_i m_{i+1}/k_{i+1}m_i \end{pmatrix} \tag{2.12}$$

For the whole barrier, we obtain:

$$\begin{pmatrix} A_{N+1} \\ 0 \end{pmatrix} = \tau_{N+1} \begin{pmatrix} A_0 \\ B_0 \end{pmatrix} \tag{2.13}$$

where the inverse of $\tau_{N+1} = \mathbf{b}_{N+1,N}\mathbf{p}_N\mathbf{b}_{N,N-1}\ldots\mathbf{p}_2\mathbf{b}_{1,0}$ is also called the "transfer matrix". The transmission coefficient $\mathcal{T}$ is calculated to be:

$$\mathcal{T} = \frac{m_L k_R}{m_R k_L} \left| \frac{A_{N+1}}{A_0} \right|^2 = \frac{m_L k_R}{m_R k_L} |\tau_N(1,1)|^2 \tag{2.14}$$

where m_L and m_R is the effective electron mass, $\hbar k_{L,R}$ is the x component of the momentum of electron in left/right electrodes, $|A_0|^2$ is the amplitude of the incoming wave function in the left electrode, $|A_{N+1}|^2$ is the amplitude of the outgoing wave function in the right electrode. The tunneling current can be computed easily after the transmission coefficient $\mathcal{T}$ has been obtained.

For layered tunnel barriers with different barrier height and dielectric constant, the electrons tunneling into the dielectric create an electrostatic potential. To account for this effect, we solve the 1D Poisson equation and Schrödinger equation in a self-consistent manner, which results an increase the average barrier height substantially [19]. We also account for hot electron relaxation in classically allowed region of the barrier by introducing an exponential decay in the "propagation" matrix ($e^{jk_i a}$ to $e^{jk_i a}e^{-a/L}$). The parameter L is the inelastic relaxation length, which is typically of around 0.1 - 0.5 nm. Such relaxation suppresses the current resonances due to the over-barrier reflection [31].

2.5   Selection of Barrier Parameters

There are several factors that need to be taken into account when selecting the appropriate materials to demonstrate a crested barrier. The key parameters to characterize a tunnel barrier include the barrier height, dielectric constant, thickness and effective mass of each dielectric layer.

The barrier height U relates to work function W of the metal electrode and electron affinities χ of the dielectric by $U = W - \chi$, where W is defined as the difference between the vacuum level and the Fermi energy of the metal electrode and χ is the difference between the vacuum level and the conduction band level of the dielectric. U is the most important parameter that will determine the barrier performance. Ideally, the barrier height of the center layer is expected to be 1 - 2 eV higher than that of the side layers. The fast suppression of such barrier under applied voltage will enhance the fast change

Material	Dielectric Constant	Band gap (eV)	φ_B - Si (eV)	φ_B - Au (eV)	φ_B - Nb (eV)	Effective mass
SiO_2	3.9	9	3.5	4.0	3.2	0.5
Al_2O_3	9	9	2.8	3.4	2.6	0.2 - 0.5
Si_3N_4	7.8	5.3	2.4	2.9	2.1	0.4
HfO_2	18	6	1.5	2.1	1.3	0.2
$ZrSiO_x$	12.6	6	1.5	2.1	1.3	-
ZrO_2	25	5	1.4	2.0	1.2	-

Table 2.1: List of values of dielectric constant, band gap and conduction band offset for various dielectric materials [20] - [26] .

of the tunnel current.

Dielectric constant for different tunnel layers will also affect the performance of the barrier. High-k dielectric has low leakage current at low bias due to the increased physical thickness (corresponding to the same EOT for Si). Under applied bias, the voltage redistributes over the barrier layers in the way that the electric field in each layer is inversely proportional to their dielectric constant. At the high field, the high-k layer has only a minor impact on the magnitude of the tunneling current. The barrier height of the high-k dielectric becomes an important factor for the crested barrier to realize high current at high voltages. The best combination would be high-k layer with high barrier height in the center and low-k layer with low barrier height on both sides. It is challenging to find materials that meet these requirements since most high-k dielectrics usually have low band-offsets and vice versa. However, incorporating high-k dielectrics into the crested barrier even as side layers still give a better performance than using the uniform silicon dioxide barrier. Table 2.1 lists the reported dielectric constants, band gaps and conduction band offset of interesting dielectric materials. In addition, the effective mass m_e and physical thickness d of each layer will affect the performance of crested barriers as a whole $(m_e/m_0)^{1/2}d$.

In summary, to build a crested barrier with steep $I - V$, we need to consider the electron affinity and dielectric constant of the dielectrics, the work function of the metal electrode and the effective thickness of each layer. A high-k dielectrics is desirable to be incorporated in the stack to improve the low field performance. High conduction-band offset for a dielectric is a must for the center layer.

It is a challenge to find an appropriate combination of materials for crested barrier layers. Experiments [34] indicate that just a few known CMOS-compatible materials may combine the barrier height sufficient for thermionic

current suppression at room temperature (above 1.5 eV), with the necessary high breakdown field (above 10 MV/cm) and negligible trap-assisted tunneling. The list of such candidate materials is essentially limited to (1) silicon dioxide; (2) low-trap density silicon nitride [32], [33]; (3) aluminum oxide grown by a variety of methods including thermal [37] and plasma [38] oxidation.

Chapter 3

Transport Through $\mathrm{AlO_X}$ - based Tunnel Barriers

3.1   Background

As mentioned in Section 2.5, in the beginning of our work it seemed that aluminum oxide represents a good material choice for fabrication of crested barriers for nonvolatile random access memories (NOVORAM) [18], since it has high dielectric constant, large band gap and large barrier height. Together with their good thermal and mechanical stability, aluminum-oxide barriers serve as the basic components of devices used in low-temperature superconductor electronics, including superconducting quantum computing, metallic single-electronics and spintronics.

   Aluminum oxide has been intensively investigated for the past decade, however, literature data concerning properties of these barriers are scattered rather broadly, especially in the range of relatively high oxygen exposure, $E \geq 10^5$ Pa-s corresponding to specific zero-field conductances below $\sim 10^{10}\ \Omega^{-1}m^{-2}$. For thermally grown oxides [37], the average tunnel barrier height U are in the range from 1.7 eV to 2.5 eV [39] - [45], but values as low as 1.2 eV [46], and as high as 4.75 eV [47], or even 20 eV [48], have also been derived from the data. Similarly, for plasma-grown layers [38], most reported values of barrier height are in the range from 1.7 to 2.3 eV [49] - [52], but numbers as high as 3.6 eV have also been claimed [53]. The published results for the apparent barrier asymmetry are scattered even more, from a few tenths of eV all the way up to 6 eV [47], and the only apparent consensus is that the barrier is always higher at the top interface (near the counter electrode). The most important sources of these differences are probably those of the film fabrication, including the substrate temperature that has not always been carefully monitored, and dif-

ferent counter electrode materials. The scattering of the results may be also attributed to the variety of techniques used for barrier height measurement, including I-V curve fitting methods [39], [40], [42]-[45], [47], [48], [50]- [53], photoelectric effect [41], [43], [49] and ballistic electron emission spectroscopy [46].

In addition, the effect of thermal annealing on tunnel barriers is also very interesting to study. It was noticed previously that post-annealing may improve tunneling magnetoresistance of junctions between magnetic layers [54]-[60]. Some changes in the average barrier height at annealing were noticed in references [54], [56], and [57]-[60]. However, the change was typically small (due to low annealing temperature), so that no definite conclusions could be drawn even about the sign of the effect.

In this chapter, we will discuss detailed studies on thermally grown and plasma grown aluminum oxide. We have carried out current-voltage measurements for these tunnel barriers. Using the quantum tunneling model based on joint solution of Schrödinger and Poisson equations, we have extracted the barrier parameters (barrier height, barrier thickness, *etc.*) for aluminum oxide barriers, which will be used for further design of crested barriers.

3.2   Sample Fabrication

3.2.1   Thermally/Plasma Grown AlO_x as Single-Layer Barriers

Two types of samples were obtained respectively from Prof. J. Luken's fabrication laboratory (SBU) (2-inch deposition tool) and Hypres, Inc. (6-inch tool in industrial environment). Table 3.1 and 3.2 show all the wafers with single aluminum oxide layers as tunnel barriers, grown by thermal (TO) or plasma oxidation (PO) with processing parameters including base electrode, oxidation pressure, oxidation time, and rf-plasma power.

For simplicity, we will describe the fabrication process at SBU here. The oxide layers have been grown on 2-inch silicon wafers ($\rho = 10 \ \Omega * cm$) covered by 500 nm of thermally grown SiO_2, in a cryopumped vacuum system with a base pressure close to 2×10^{-7} torr, as components of standard Nb-trilayer junctions.

First, a 150-nm-thick niobium base film has been deposited using dc-magnetron sputtering at a rate of 1.6 nm/s. Then, without breaking the vacuum, a 10-nm-thick aluminum film has been deposited by the same method at a lower speed (0.5 nm/s). It is well known that at these conditions aluminum wets the niobium surface, forming a smooth uniform coating [61].

Wafer	Base Electrode		Al Interlayer	Thermal Oxidation	
	Metal	Thickness	(nm)	Pressure	Time
		(nm)		(Torr)	(min)
Crest 2	Nb	150	8-10	2.5	10
Crest 5	Nb	150	8-10	100	40
Crest 12	Nb	150	8-10	100	2400
KL669	Nb	150	8-10	100	40
VJCB 4	Nb	50	3	100	50

Table 3.1: Thermal Oxidation Process Parameters

Wafer	Base Electrode		Al Interlayer	Plasma Oxidation		
	Metal	Thickness	(nm)	Pressure	Time	Power
		(nm)		(mTorr)	(min)	(W)
Crest 19	Nb	150	8-10	15	10	50
N3081	Nb	150	8-10	15	10	50
VJCB2	Nb	125	6	15	10	50
VJCB3	Nb	125	6	75	10	50
VJCB6	Nb	50	6	15	3	50
VJCB7	Nb	50	5	15	30	50
VJCB14	Nb	50	6	15	10	50
VJCB13	Al	50	-	15	10	50
VJCB17	Al	50	-	15	10	10
VJCB18	Al	50	-	15	10	100
VJCB20	Al	50	-	15	10	250
VJCB21	Al	50	-	5	10	100

Table 3.2: Plasma Oxidation Process Parameters

After that, the aluminum film has been oxidized either thermally at room temperature or in oxygen plasma. In the former case, a well-monitored amount of ultra-high-purity (semiconductor-grade) oxygen has been let into the vacuum chamber for a certain time. The same gas has been used for the plasma oxidation, but in this case a 13.56 MHz source has been connected, via a tuned resonant circuit, to a dc-insulated copper plate on which the substrate had been mounted. This has resulted in a 50 W rf plasma discharge and wafer dc self-biasing to approximately -80 V relative to the ground (vacuum chamber walls). The wafer has been kept at room temperature by its thermal anchoring to the water-cooled copper plate.

After oxidation, the chamber has been pumped down to the base pressure and a niobium 100-nm-thick counter-electrode has been deposited in situ in the same way as the base electrode. The fabrication had been completed by sample patterning into junctions of various area (3×3, 30×30, and 300×300 μm^2) using optical lithography with PMMA resist and reactive ion etching in SF$_6$ plasma. Here, the same photoresist mask was first used for the counter electrode shape definition using RIE, and later for a lift-off of a sputtered 150-nm-thick SiO$_2$ insulation layer from the junction surface (the so-called self-aligned lift-off process). The lift-off has opened contacts of junction counter electrodes with the following thicker niobium wiring layer (300 nm), with wiring configured for four-point measurements. Figure 3.1 shows the layout of the chip, where the green square area corresponding to a tri-layer junction.

We have fabricated 5 wafers under thermal oxidation with different oxygen exposures. Two of them were reproduced at Hypres, Inc. and SBU at different time, in order to check the reproducibility of these wafers. A total of 12 wafers have been fabricated under plasma oxidation at SBU and Hypres, Inc., to study the oxide behavior under different oxygen exposure conditions (pressure, time and power). A digital control system responsible for plasma oxidation has been developed in order to change these parameters precisely. Among them, wafers "Crest 19", "N3081", "VJCB2" and "VJCB14" have been fabricated under the same oxygen exposure conditions.

3.2.2 Thermally/Plasma Grown AlO$_x$ as Double-layered Barriers

Single-dielectric layers have been fabricated to learn about the physical and electrical characteristics of the individual layers, in order to understand and design multi-layer samples. We have tried the two-layer samples with PO-grown and TO-grown aluminum oxides.

Table 3.3 lists the set of wafers with double-layer aluminum oxide barriers,

Chip Top View   Wafer Top View
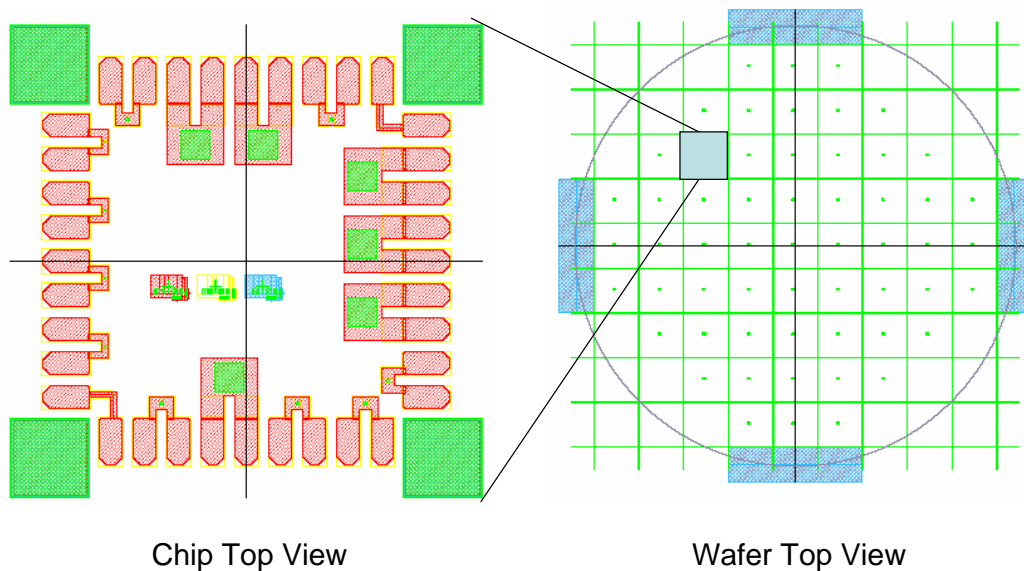
Figure 3.1: Left: Layout (top view) of our chip containing 18 junctions with three different areas $3 \times 3, 30 \times 30, 300 \times 300 \ \mu m^2$. Right: Top view of the whole wafer.

which contains $PO - AlO_x$ and $TO - AlO_x$ heterostructures. The aluminum oxide has been grown in the same method as described above (Section 3.2.1) at SBU and Hypres, Inc. Most wafers have the plasma oxidized layer as the first tunnel barrier, followed by sputtering a thin aluminum layer with thickness varying from 1 nm to 3 nm. The second thin aluminum layer has been thermally oxidized under the same condition as wafer "Crest 2" or "Crest 5" without breaking the vacuum. Wafer "VJCB15" has the reverse aluminum oxide heterostructure from the others. The thermally oxidized layer has been first fabricated, followed by a deposition of relatively thick aluminum layer (3.8 nm) and plasma oxidized under the same condition as wafer "Crest 19".

3.3 Post Fabrication - Rapid Thermal Annealing

Rapid thermal anneal (RTA) is a process used in semiconductor device fabrication, which consists of heating a single wafer at a time in order to affect its electrical properties. Unique heat treatments are designed for different effects. Wafers can be heated in order to activate dopants, change film-to-film or film-to-wafer substrate interfaces, densify deposited films, change states of grown

Wafer	Oxidation Type	Base Electrode		Al Layer	Oxidation Condition		
		Metal	Thickness		Pressure	Time	Power
			(nm)	(nm)	(mTorr)	(min)	(W)
N3080	Plasma	Nb	150	8-10	15	10	50
	Thermal			1.0	2500	10	-
N3094	Plasma	Nb	150	8-10	15	10	50
	Thermal			1.3	100000	40	-
N3096	Plasma	Nb	135	13	15	10	50
	Thermal			1.3	100000	40	-
VJCB15	Thermal	Al	50	-	100000	40	-
	Plasma			3.8	15	10	50
VJCB16	Plasma	Al	50	-	15	10	50
	Thermal			1.5	100000	40	-
VJCB19	Plasma	Al	50		15	10	50
	Thermal			3.0	100000	40	-

Table 3.3: Processing parameters of PO / TO double-layer aluminum oxide tunnel barriers.

films, repair damage from ion implantation, move dopants or drive dopants from one film into another or from a film into the wafer substrate.

Several 5×5 mm^2 chips from each wafer have been subjected to rapid thermal annealing (RTA) in inert atmosphere (N$_2$ or Ar), using the rapid thermal module (Model No. RTM 2016-M-2F-FC) made by Process Products Corporation and capable of providing temperature excursions from room temperature to 1250ºC at heating rates up to 300ºC/sec and cooling rates of approximately 100ºC/sesc. The specimen can be held at constant temperatures accurately ±2.5ºC. Specimen temperature is automatically controlled by a built-in programmable "Micristar" controller. The power controller provides power to Tungsten halogen lamps arranged around the quartz chamber, which are designed to provide infra-red (I. R.) energy, either directly or being reflected onto the specimen. The "Micristar" controller is also used to control the process gas (*e.g.*, nitrogen) by setting their sequence and flow paths using air operated valves.

After initial electrical characterization for quality checking, the samples have been loaded into the quartz chamber and placed close to the thermal couple (within 0.005 inches) to prepare for the heating. The inert gas (N$_2$ or Ar) has been letting into the chamber. After waiting for over 30 minutes (long enough to let the inert gas be filled in the chamber), the chamber has been pre-warmed up to 200ºC in 20 seconds for soft starting the system, which in-

sures a consistent starting point for each run and prolongs the life of the lamps. Following this pre-conditioning of the oven, the heating temperature has been increased very fast in a speed of $50 - 100^{\circ}$C/sec, reaching the targeted temperature in only a few seconds. The sample has been kept at this temperature for a certain time, usually 30 to 180 seconds. After the heater was turned off, the chamber has been immediately cooled down by water cooling and venting. We have studied the effect of annealing temperature and annealing time on both thermally oxidized and plasma oxidized aluminum oxide structures, which will be discussed later.

RTA were also done in Yale University by X. Wang under similar conditions. The annealing results for samples from the same wafer are reproducible with each other.

3.4 HR-TEM Characterization of AlO_x Structures

Let us first look at the physical properties of as-grown and annealed AlO_x structures using high resolution transmission electron microscopy (HRTEM). HRTEM is used to study the physical thickness and morphology of aluminum oxide films. HRTEM is an imaging mode of the transmission electron microscope (TEM) that allows the imaging of the crystallographic structure at atomic scale. Z-contrast imaging allows us to study the oxide barrier thickness and crystallinity of our samples due to different mass of the elements in each layer. The resolution is about 1Å. All the TEM analysis has been done at Brookhaven National Lab by R. F. Klie and L. H. Zhang.

3.4.1 Thermally Grown Aluminum Oxide

Wafer "Crest 5" and "VJCB4" have been made from SBU tools under similar oxidation conditions, except that "Crest 5" had niobium base electrode while "VJCB4" had aluminum base electrode. Two TEM images of selected samples from wafer "VJCB4" are shown in Figure 3.2. We observe a very thin aluminum oxide layer of only 1 - 2 nm. In some areas the Nb top-layer penetrates through the AlO_x layer into the aluminum layer. The bottom aluminum layer does not seem to be continuous, which could be the results of the artifacts of TEM slice preparation rather than those of the sample fabrication.

After the sample (from wafer "Crest 5") has been rapid thermally annealed at 400°C for 30 seconds, we could see a much more clear interface between Al and AlO_x layers. The film thickness appeared to increase after annealing. The picture quality is affected by the fact that the base Nb electrode is

a. As-grown Aluminum Oxide **b. Annealed Aluminum Oxide**
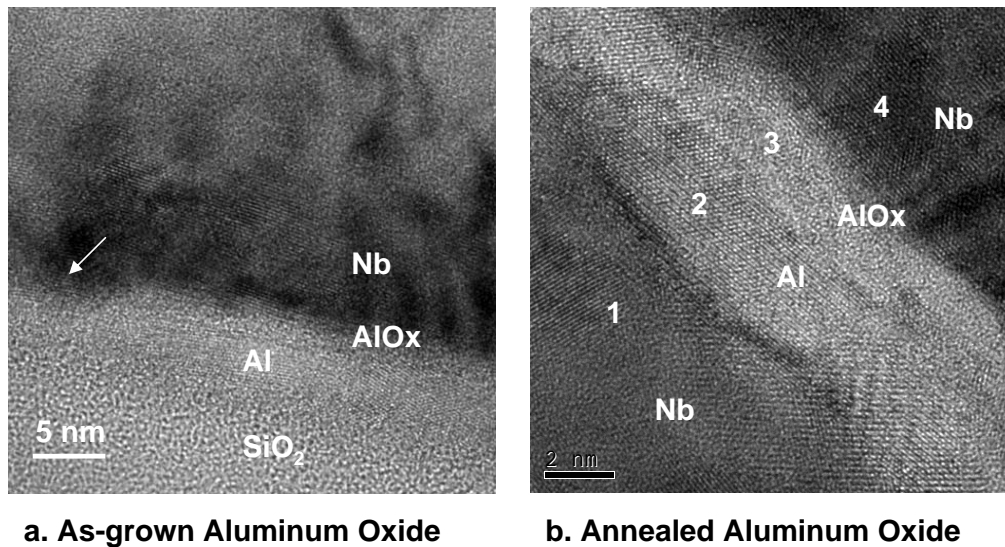
Figure 3.2: High resolution TEM picture of thermally grown aluminum oxide: (a) as grown sample from wafer "VJCB4"; (b) annealed sample from wafer "Crest 5". The annealing conditions are as follows: heating temperature = 400ºC, ramping rate = 25ºC/min, heating time (at 400ºC) = 2 minutes, Chamber oxygen pressure $\sim 5 \times 10^{-8}$ Pa.
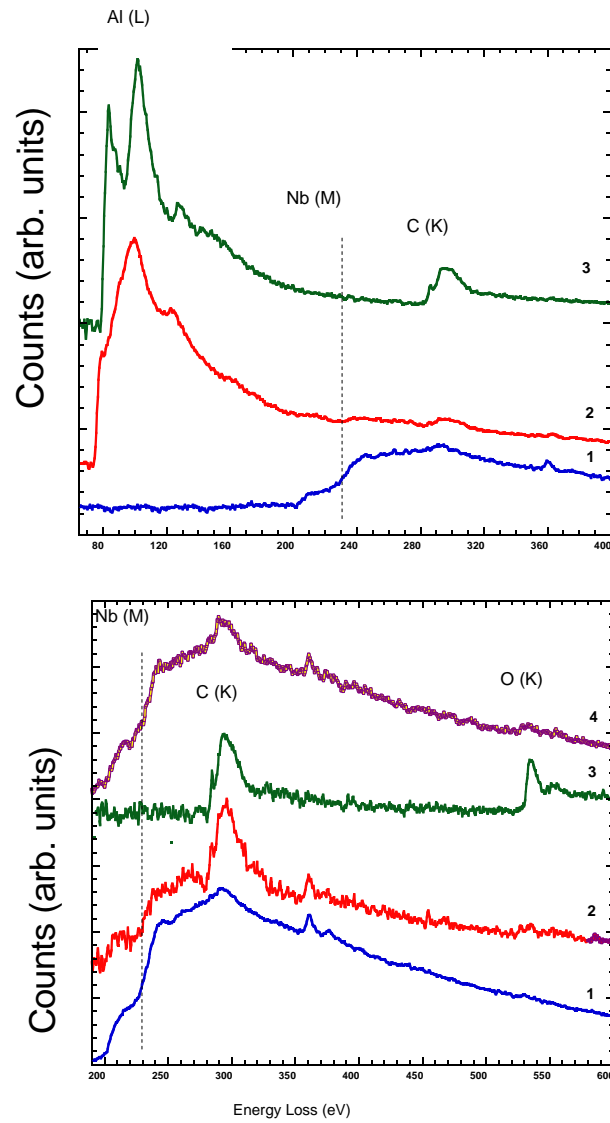
Figure 3.3: Results of the electron loss spectroscopy for two energy ranges from the positions indicated in Figure 3.2: (1) Nb base electrode (2) Al layers (3) AlO_x layer, and (4) Nb counterelectrode. The spectra are background subtracted, and corrected for multiple scattering contributions. The carbon K-edge present in all the spectra stems from the carbon build-up during the spectrum acquisition and is apparently not a feature of the initial sample structure.

relatively thick and polycrystalline, so its surface is uneven at a-few-nanometer scale. Nevertheless, the images reveal an amorphous AlO_x layer with a thickness of ~ 3 nm. Figure 3.3 shows the electron energy loss spectroscopy across the sample at four different positions: bottom Nb, Al, AlO_x and top Nb. The Al L-edge of the AlO_x layer shows a much stronger first peak, usually indicating an amorphous oxide. An interfacial layer is visible between AlO_x and top Nb layer.

3.4.2   Plasma Oxidized Aluminum Oxide

Samples from wafer "Crest 19" have a thick Nb base electrode (~ 150 nm). It is difficult to make specimen thin enough for TEM analysis because thick Nb layer tends to peel off easily when cutting to slices. Wafer "VJCB2" has been fabricated in the same plasma-oxidation condition (50 W rf-plasma, 15 mTorr×10 minutes) as "Crest 19" except using aluminum base electrode instead of Nb, fabricated particularly for TEM imaging purpose. Samples with higher plasma oxidation pressure (15 W, rf-plasma, 75 mTorr×10 minutes) have been also investigated by TEM imaging.

Let us first look at plasma oxide with 50 W oxidation power. Figure 3.4a shows a TEM image in a cross-sectional view with Nb electrode on top and the silicon substrate on the bottom. From TEM images, we could see a relatively continuous layer of Al film by its crystalline structures from aluminum oxide layer by its amorphous property. The Al and AlO_x layers is about 5 nm and 4 nm thick, respectively. The Z-contrast image (Figure 3.5) also shows directly the difference between the heavy Nb electrode (Z=41), and the lighter Al, AlO_x, and SiO_2 layers.

Similar structures are found for plasma oxide with 75 mTorr oxidation pressure, with a slightly thicker aluminum oxide thickness of 5 nm. The total thickness of Al/AlO_x is about 10 nm. From the EELS plot (Figure 3.6), it is interesting to note here that the O K-edge signal in the AlO_x film appears stronger than in the 50-W plasma sample ("VJCB2", Figure 3.5), indicating a higher O-concentration in the plasma grown AlO_x-layers under higher pressure. Moreover, the Al L-edge of the AlO_x layer shows a much stronger first peak, usually the sign of an amorphous oxide.

3.5   Electrical Characterization for (Nb/)Al/AlO_x/Nb Barriers

Direct $I - V$ measurements of both as-oxidized and annealed junctions have been carried out both at room and liquid-helium (4.2 K) temperatures. Volt-
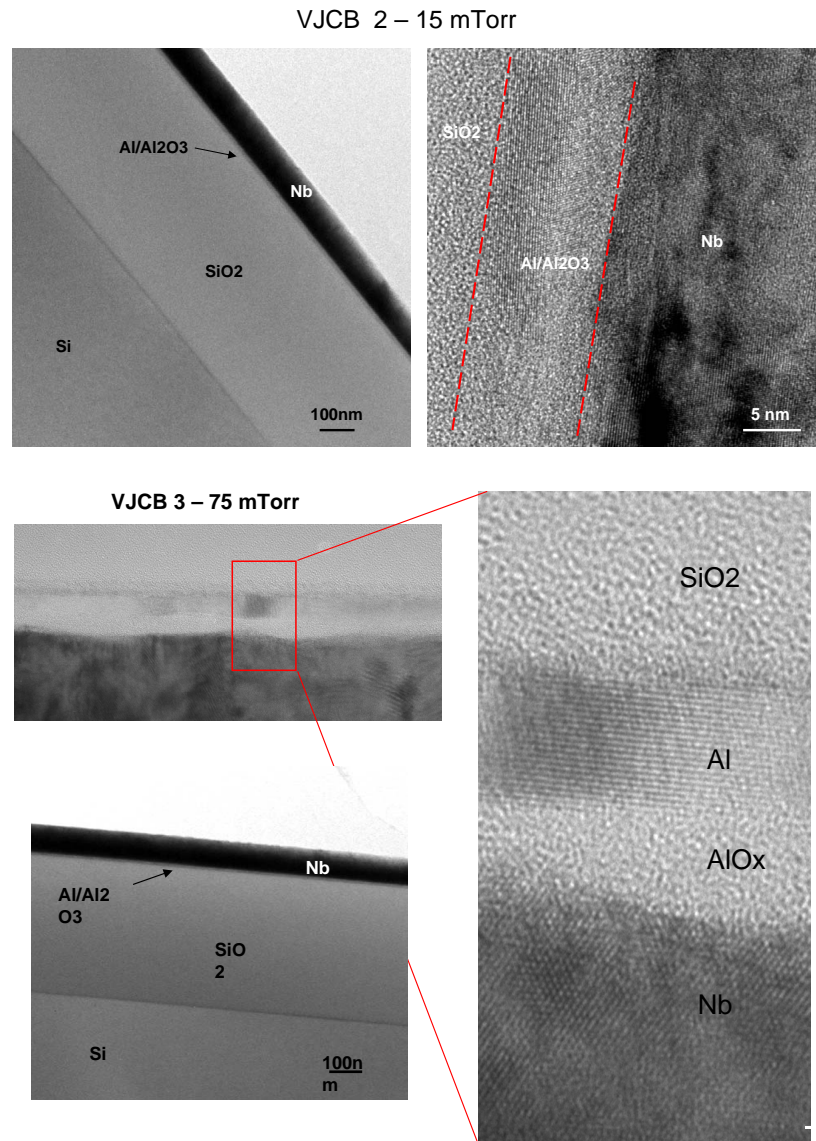
Figure 3.4: High-resolution transmission-electron-microscope images of plasma-grown aluminum oxide layers with different oxygen exposures (a) 15 mTorr (b) 75 mTorr.
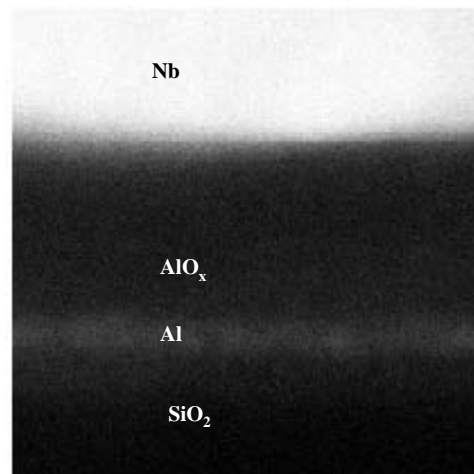
a. Z-contrast image of Sample VJCB2.
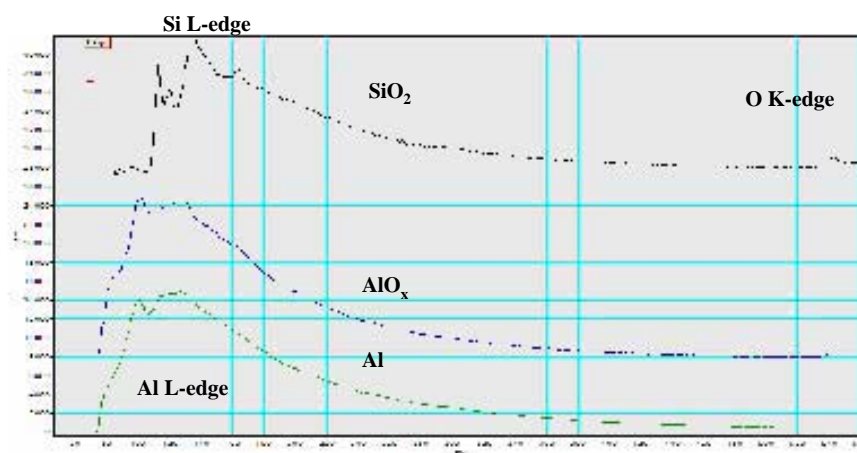
b. EELS spectra from the indicated layers.

Figure 3.5: Z-Contrast images and EELS spectroscopy of 15-mTorr plasma-grown aluminum oxide.
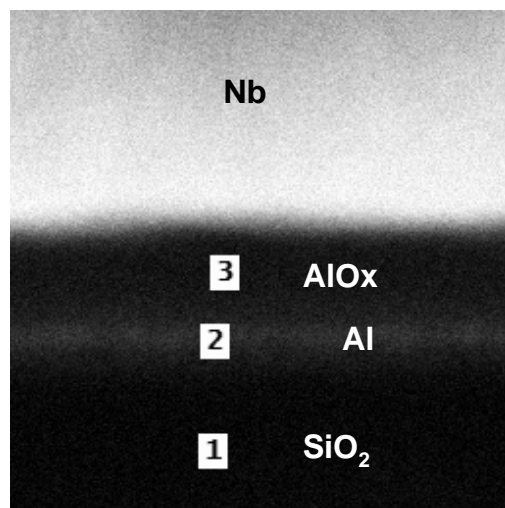
a. Z-contrast image of sample VJCB3.
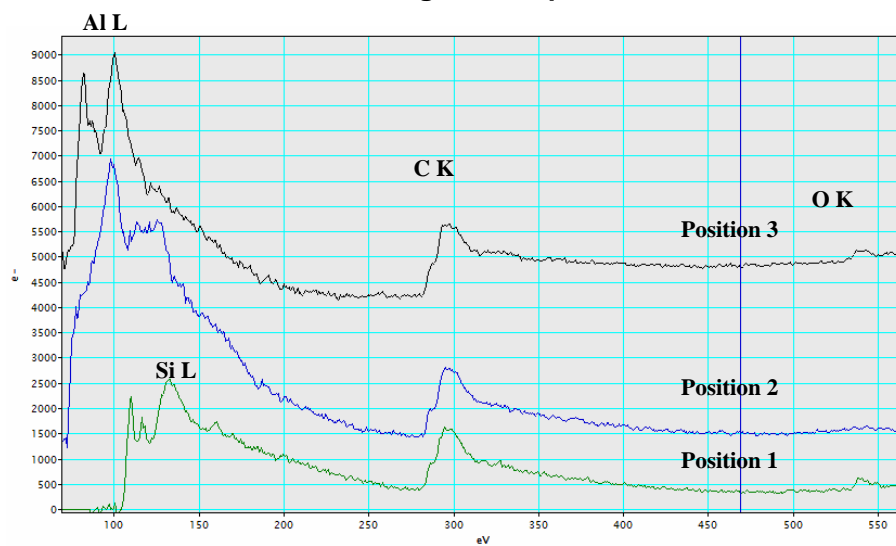
b. EELS spectra from the position indicated in a.

Figure 3.6: Z-Contrast images and EELS spectroscopy of 75-mTorr plasma-grown aluminum oxide.

age sweeps with gradually growing amplitude have been used to characterize transport up to the very onset of hard breakdown. A Keithley 6430 sub-femtoammeter has been used to record all the $I - V$ measurements with a special low-noise, high sensitive setup (see Appendix A.).

3.5.1 $TO - AlO_x$ with Different Oxygen Exposures

Let us first focus on thin thermally grown oxides with different oxygen exposure conditions separated by two orders of magnitude intervals (Table 3.1). The specific differential conductance $G \equiv dI/dV$ as a function of dc voltage V is shown in Figure 3.7 for three typical 3×3 μm^2 samples from wafer "Crest 2", "Crest 5" and "Crest 12". The zero conductance is decreased from 2.6×10^9 $\Omega^{-1}m^2$ to 0.027×10^9 $\Omega^{-1}m^2$ with the increase of oxygen exposure. The junctions exhibited "hard" breakdown at a certain voltage V_{br} ranging from 0.8 V for thinner barriers to 1.6 V for thicker barriers. Approximately at 0.1 V below the breakdown, small irrevocable changes of junction properties ("soft breakdown") might be noticed. Outside of the soft breakdown region, the $I - V$ curves were quite reproducible, both across the chip and across each wafer. Two features are noticeable here: (i) A hysteretic loop at positive voltages (positive potential of the Nb counter-electrode) between ~ 0.45 V and ~ 0.6 V, especially pronounced for thinner barriers, which may be explained by recharging of surface trap states at the AlO_x/Nb interface; (ii) A virtually non-hysteretic excess current at negative voltage ranges, starting from the origin and persisting almost to -1.0 V.

We have fit the $I - V$ curves with the effective mass model that has been described in Chapter 2 based on the direct electron tunneling theory, using simple trapezoidal shaped barrier profile for thin oxide layers. The Fermi energies E_F of electrode metals are chosen from the free electron gas estimates [35]: $E_F = 11.7$ eV for aluminum and $E_F = 5.3$ eV for niobium. The best fit curves are shown in Figure 3.7 with open points.

There are three major fitting parameters: the average barrier height $U = (\phi_B + \phi_C)/2$, the barrier asymmetry $\Delta = \phi_C - \phi_B$, and the effective barrier thickness $d_{ef} = d(m_{ef}/m_0)^{1/2}$ (m_0 is the electron mass). ϕ_B and ϕ_C are the barrier heights at the interfaces with, respectively, the base electrode (Al) and counter electrode (Nb). With the increase of oxygen exposure of 4 orders of magnitude, the average barrier height is increased by 6%, while the effective barrier thickness is increased from 0.83 nm to 1.08 nm.
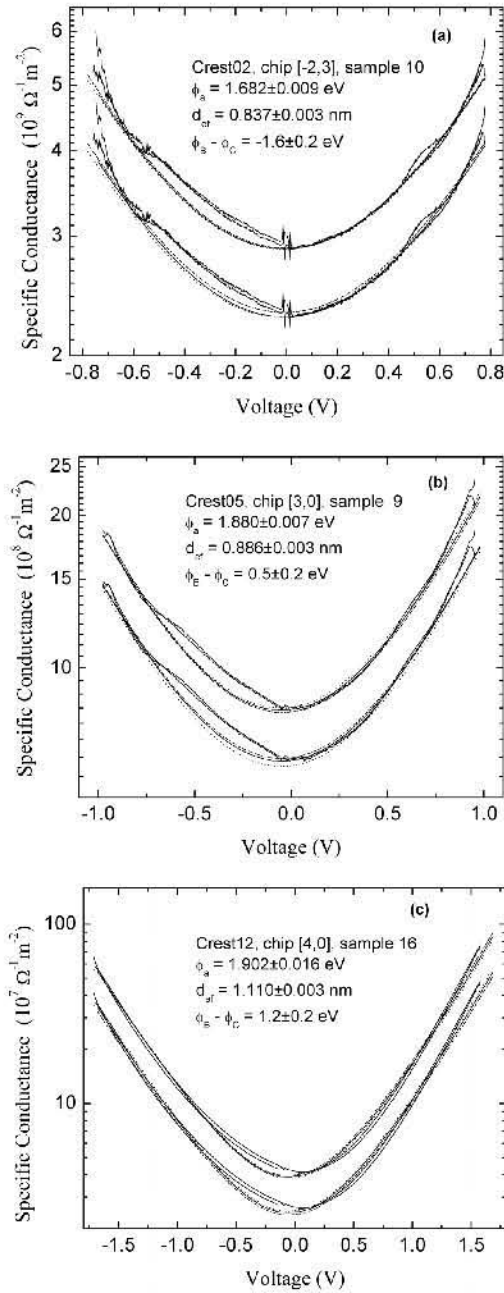
Figure 3.7: Fitting experimental data using the direct tunneling theory for thermally oxidized aluminum with different exposure (a) Crest 2 (b) Crest 5 (c) Crest 12. Two experimental plots on each panel are the same besides a vertical offset. Solid lines show best-fit curves, while dashed and dash-dotted curves are the results of variation of average barrier, effective barrier thickness.

3.5.2 Annealing Effects on $\mathrm{TO-AlO_x}$ Layers

Several chips from two representative wafers "Crest 5" (SBU, 2-inch wafers) and "KL669" (Hypres Inc., 6-inch wafers) have been subjected to rapid thermal annealing treatment from 300ºC to 650ºC. The two wafers have been fabricated under the same oxidation conditions but with different deposition tools. The samples have been annealed in Ar atmosphere for 30 seconds. The junctions, both before and after post-annealing, were highly reproducible, with the rms on-chip (junction to junction) variation of low-voltage conductance from as low as 0.8% to $\sim 20\%$ (comparable with reported results [36]).

Figure 3.8 shows the semi-log plot of the low temperature (4.2 K) specific differential conductance $g(V)$ $(g(V) = A^{-1}dI(V)/dV)$ of representative junctions from these two wafers, both before and after RTA at various annealing temperatures. The resulting zero conductances G_0 from two wafers are in the same range for the same annealing temperature, and $I-V$ curves are generally close to each other. It is obvious that the low-temperature conductance drops sharply starting above 300ºC by almost six orders of magnitude by ~ 500ºC for both wafers. Generally, annealing leads to a considerable improvement of the junction quality: (1) The hard breakdown voltage V_{br} increases from 1.0 V to 4.0 V (2) The $I-V$ (or $G-V$) curves show virtually no hysteresis or "soft breakdown" up to the hard breakdown. More quantitatively, for "Crest 5" samples, the charge to breakdown, measured at room temperature for samples annealed at 450ºC, stays above $\sim 10^5$ C/cm^2, which is a few orders of magnitude higher than the level typical for industrial grade SiO$_2$ barriers.Here the largest difference between two deposition tools is the more strongly expressed cusps at $V \sim 2.5$ V at annealing temperatures above 500ºC for samples made at Hypres, Inc. Also, there is a minor "cusp" contribution to low-voltage conduction for annealed samples: 400ºC ~ 500ºC for SBU samples and 450ºC for Hypres samples.

In order to understand the dramatic drop of junction conductance after post-annealing, we have used the theoretical fits to extract essential tunnel barrier parameters of the AlO$_x$ layers. The good reproductivity of the junction $I-V$ curves, and their weak temperature dependence (the conductance increases by only $\sim 15\%$ between 4.2 K and 295 K, as shown in Figure 3.9) are consistent with the assumption of direct tunneling of electrons through the barrier. Also, the tunneling current shows the characteristic sharp increase at the onset of the Fowler-Nordheim region. We have fitted experimental data of differential conductance $G(V)$ $(G(V) = dI(V)/dV)$ with the results of the "microscopic" (non-WKB) theory of such tunneling [45] through multilayered tunnel barriers. The advantage of fitting the semilog $G(V)$ plots rather than $\ln I(V)$ curves is that in the former case the peculiarities of low-voltage behav-
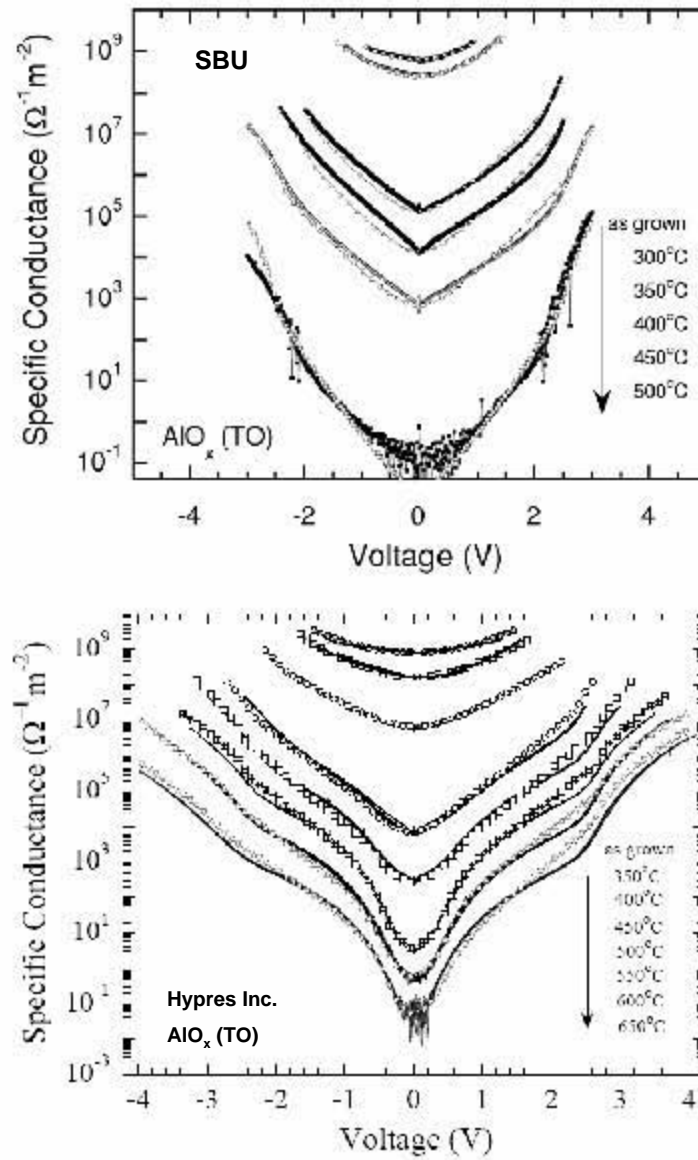
Figure 3.8: Nonlinear low temperature (4.2 K) specific conductance $g(V) = A^{-1}dI(V)/dV$ of thermally grown tunnel junctions fabricated at (a) SBU (b) Hypres, Inc., both annealed in Ar for 30 seconds. Junctions from different areas give the same specific conductance. Curves with open points are the best theoretical fits.
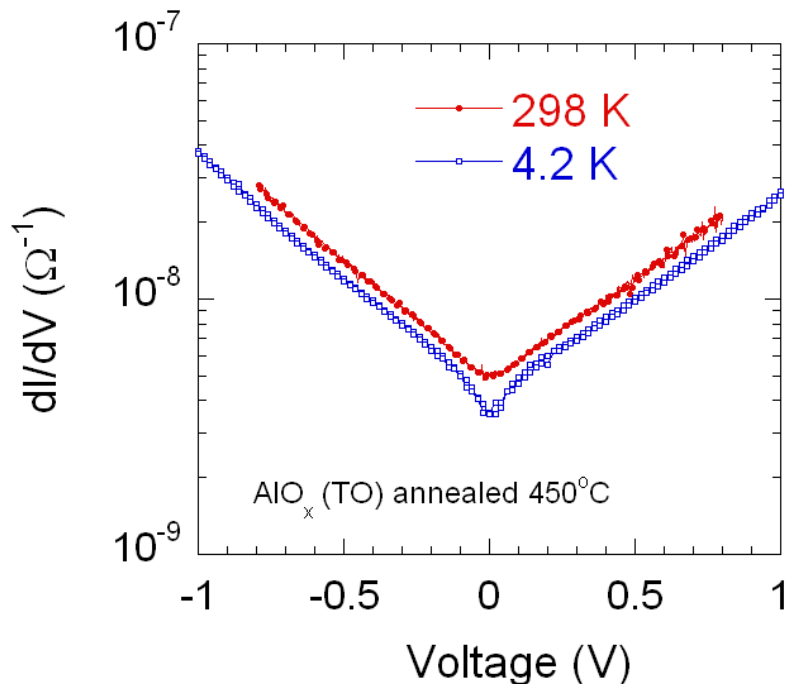
Figure 3.9: The nonlinear dynamic conductance $G(V) = dI(V)/dV$ of a typical 450ºC annealed sample from wafer "Crest 5", both measured at liquid helium and room temperatures.

ior are revealed more clearly. Curves with open points present our theoretical fitting results.

Let us look at the minor "cusp" contribution $G_h \propto |V|^{\alpha-1}$ to the conductance (and hence $I_h \propto sgn(V) \times |V|^\alpha$ to the current) at low voltage ranges. Similar observation were discussed by other groups [63] - [66]. Figure 3.9 shows that this current component is more sensitive to the temperature than the current at higher voltages, though this temperature dependence is still much weaker than that for the Poole-Frenkel conductance mechanism [67]. A possible reason for the I_h component is some type of hopping (trap-assisted tunneling) strongly affected by the Coulomb interaction of the hopping electrons. In fact, it may be best fitted with the values ($\alpha = 1.8 \pm 0.1$ for Crest 5) that are relatively close to that of the classical Mott-Gurney law ($\alpha = 2$) for space-charge-limited current [68]. A better agreement would be hard to expect, since the Mott-Gurney model implies that the layer thickness d is much larger than the localization radius a of a typical trap, and the thickness of our barriers ($d \sim 2$ - 3 nm as shown below) is comparable with the estimated value

~ 1 nm. For the best fitting, we have subtracted I_h from the data, although the fitting results are appropriate even for the raw data.

For samples from SBU, a relative good fitting of the data may be achieved with the traditional trapezoidal (*i.e.*, one-layer) model of the barrier for all annealing temperatures. However, for samples from Hypres, Inc., the one-layer trapezoidal model is good only for samples with annealing temperature $T_A < 400$ºC. For higher annealing temperature $T_A > 450$ºC, the data could not be fit well using less than three layers, even five layers are needed for temperature higher than $T_A > 550$ºC, implying a layered structure of the oxide. This is not too surprising, since the complex interface chemistry, as well as trapped charge impurities [69] may provide interfacial layers with properties different from the oxide bulk.

Although the $I-V$ curve fitting gives very definite results for the effective thickness $d_{ef} = (m_{ef}/m_0)^{1/2}d$ of the layers, it cannot distinguish the contributions from the effective mass m of the tunneling electron and from the physical thickness d of the barrier. In fact the expression for d_{ef} is exact only within the WKB approximation. We have checked that the microscopic theory gives results that may be approximated with the formula $d_{ef} = (m_{ef}/m_0)^\beta d$ with the value of β very close to 0.5. For samples from "Crest 5", $\beta \approx 0.502$.

In order to estimate the physical barrier thickness d (and hence the effective mass m_{ef}), we have measured the specific capacitance C_0 of the annealed "Crest 5" junctions. We have used a RC circuit with an AC function generator and a oscilloscope to measure the capacitance. The standard resistor of 100 KΩ was connected in series with our device. Both high and low frequencies (*e.g.*, 100 KHz and 10 KHz) were applied. By measuring the voltage drops at the device, we could extract the capacitance value of the junction. The specific capacitance has turned out to be close to 2.8 ± 0.7 μF/cm^2. Assuming that the dielectric constant of the aluminum oxides is within the range 9 ± 1 [21], the capacitance values imply that the physical thickness of oxides is 2.85 ± 0.75 nm, which is close to the observed AlO$_x$ thickness from HRTEM images. Using the effective thickness determined by our best fitting, we estimate the effective mass for the thermally grown oxide to be $(0.35 \pm 0.20)m_0$. These values are in a reasonable agreement with the theoretical result $0.4m_0$ [70].

Now let us discuss the change of the barrier height and barrier thickness for wafer "Crest 5" and wafer "KL669" along with the annealing temperatures respectively.

Annealed $TO - AlO_x$ from SBU

One-layer trapezoidal model has been used for the fittings for all annealing temperatures. We have found that the average barrier height U of the ther-

mally grown oxide increases repidly at annealing temperatures above 300ºC: from an initial value of ~ 1.8 eV to ~ 2.45 eV, and remains close to this values up to 600ºC. The observed increase of the average barrier height is also correlated with an increase of the effective barrier thickness (0.9 nm $\sim$ 2.2 nm), a $\sim 65\%$ increase in the breakdown electric field, and a reversal of the barrier asymmetry from negative to slightly positive.

Annealed $TO - AlO_x$ **from Hypres, Inc.**

We have applied multi-layer barrier profiles for the fitting here. The barrier height of the middle layer is virtually constant of around 2.0 ± 0.1 eV up to 400ºC. Then, it starts to increase gradually at 450ºC, and by 650ºC approaches 2.9 ± 0.4 eV. Also, the effective barrier thickness increases from 0.8 ± 0.1 nm to 2.5 ± 0.2 nm with an over $\sim 60\%$ increase of the hard breakdown electric field. This change is almost identical with what we see from SBU samples, within the experimental errors.

However, we have observed a rise of the side layers with potential height at ~ 0.5 eV for the annealing temperature from 450ºC to 650ºC (Figure 3.10). This had not been observed in SBU samples. The existence of these layers with low barrier height might indicate the diffusion of chemisorbed species O_2^- or O_2 at the interface [72], with some oxygen released from the middle layer as a result of Al_2O_3 formation. Here for annealing temperature $T_A > 450$ºC, the potential profiles of thermally grown oxide barriers become "crested" [13], though the thickness of this layer alone is apparently too small for any known useful applications.

3.5.3 $PO - AlO_x$ **with Different Oxygen Exposure and Power**

Now let us describe the situation with plasma oxidized samples. Three separate wafers (VJCB6, VJCB2, and VJCB7) have been fabricated by 15 mTorr oxygen plasma for 3, 10, and 30 minutes under 50 W rf-power. Figure 3.11a shows the specific conductance $g(V)$ curves measured at 4.2 K for typical junctions from these wafers. The curves are separated by less than one order of magnitude, and their overall shape is almost identical to each other. It means that the oxygen exposure does not affect the process of plasma oxidation as much as that of the thermal oxidation. In the first few minutes, the plasma oxide was formed very quickly and the adsorption of oxygen has reached its saturation level. More oxygen exposure does not help to change the thickness of $PO - AlO_x$ abruptly.
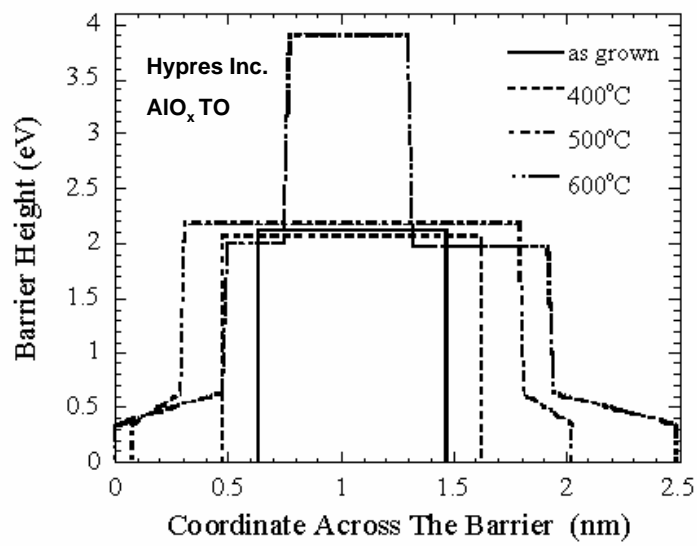
Figure 3.10: Barrier profile giving best fitting results for a thermal oxide. The effective mass is $0.35m_0$.
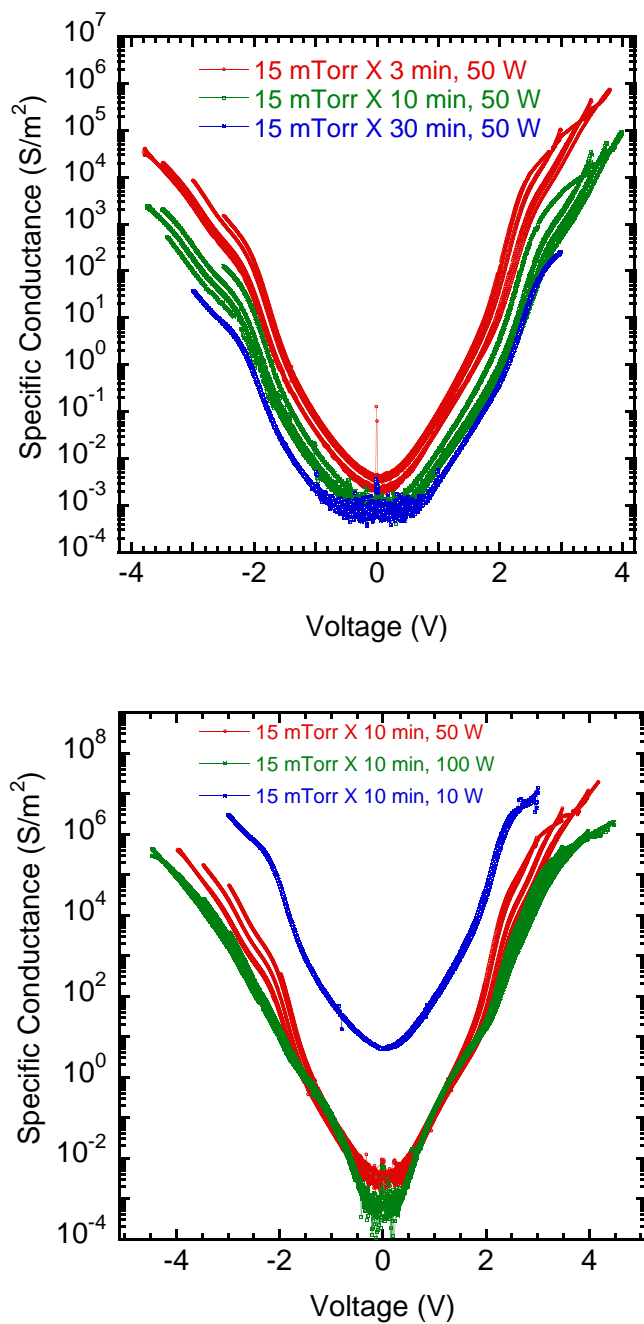
Figure 3.11: Nonlinear specific conductance for plasma grown aluminum oxide with different fabrication conditions: (1) different O_2 exposure time: 3 minutes, 10 minutes and 30 minutes; (2) different rf-power: 10 W, 50 W and 100 W, at low temperature (4.2 K).

The effect of rf plasma power has also been investigated. We have fabricated three wafers in the same oxygen exposure level (15 mTorr × 10 minutes) but with different plasma power of 10 W, 50 W, 100 W and 250 W. The rf plasma power system is newly installed and can be digitally tuned to different power levels with more accuracy. With the increase of power, we observe the zero-bias conductance drops sharply from 10 W to 50 W and saturates after for higher power. Samples fabricated under the maximum 250 W rf-power have many shorts due to difficulty to *etch* the aluminum oxide layer uniformly.

3.5.4 Annealing Effects on $PO - AlO_x$ Layers

Samples from $PO - Al_Ox$ with oxygen exposure (15 mTorr × 10 minutes) have been subjected to rapid thermally annealing to different temperatures from 350ºC to 650ºC. We have investigated two types of samples from wafer "Crest 19" and "VJCB17", fabricated under different rf-plasma power (50 W and 10 W). Similar to the thermally grown samples, the hard breakdown voltage increased from 4.0 V to 4.6 V and the $I - V$ curves show virtually no hysteresis during continuous voltage swees up to V_{br}. However, we have observed a dramatic difference between effects of annealing temperature upon the plasma-grown oxides with different oxidation power.

For samples oxidized under the standard rf-power of 50 W, the low-voltage conductance of $PO - AlO_x$ only drops below two orders of magnitude even when the annealing temperature has been raised to ~ 550ºC. For annealing temperature higher than 600ºC, *e.g.*, $T_A = 650$ºC, we observe the decrease of the breakdown voltage to 3.9 V and the reduction insulator quality. We know that the melting point for aluminum (oxide) is 660ºC. For annealing temperature higher than 650ºC, the bottom aluminum layer (unoxidized aluminum) could be close to the melting state, thus degraded the aluminum oxide quality.

Following the same fitting procedures discussed above, we first applied traditional trapezoidal barrier profile for the fitting, which could generally give a relative good fitting, but with the sacrifice of the high-voltage data, especially at negative voltage range. Better fitting is provided by the three layer model, as shown in Figure 3.12. The average barrier height of the plasma-grown oxides remain practically unchanged at around 2.0 V, while the effective barrier thickness $d_{ef} = (m_{ef}/m_0)^{1/2}d$, increased from 2.8 nm to 3.8 nm.

In order to estimate the effective oxide thickness, we have performed the capacitance measurements for annealed $PO - AlO_x$ samples (50 W). The specific capacitance has turned out to be close to 2.2 ± 0.1 $\mu F/cm^2$ for as-oxidized sample, 2.1 ± 0.3 $\mu F/cm^2$ for sample annealed at 400ºC, and 1.6 ± 0.2 $\mu F/cm^2$ for annealing temperature at 600ºC. Assuming that the dielctric constant of aluminum oxide is 9 ± 1 [21] - [23], the extracted barrier physical thickness
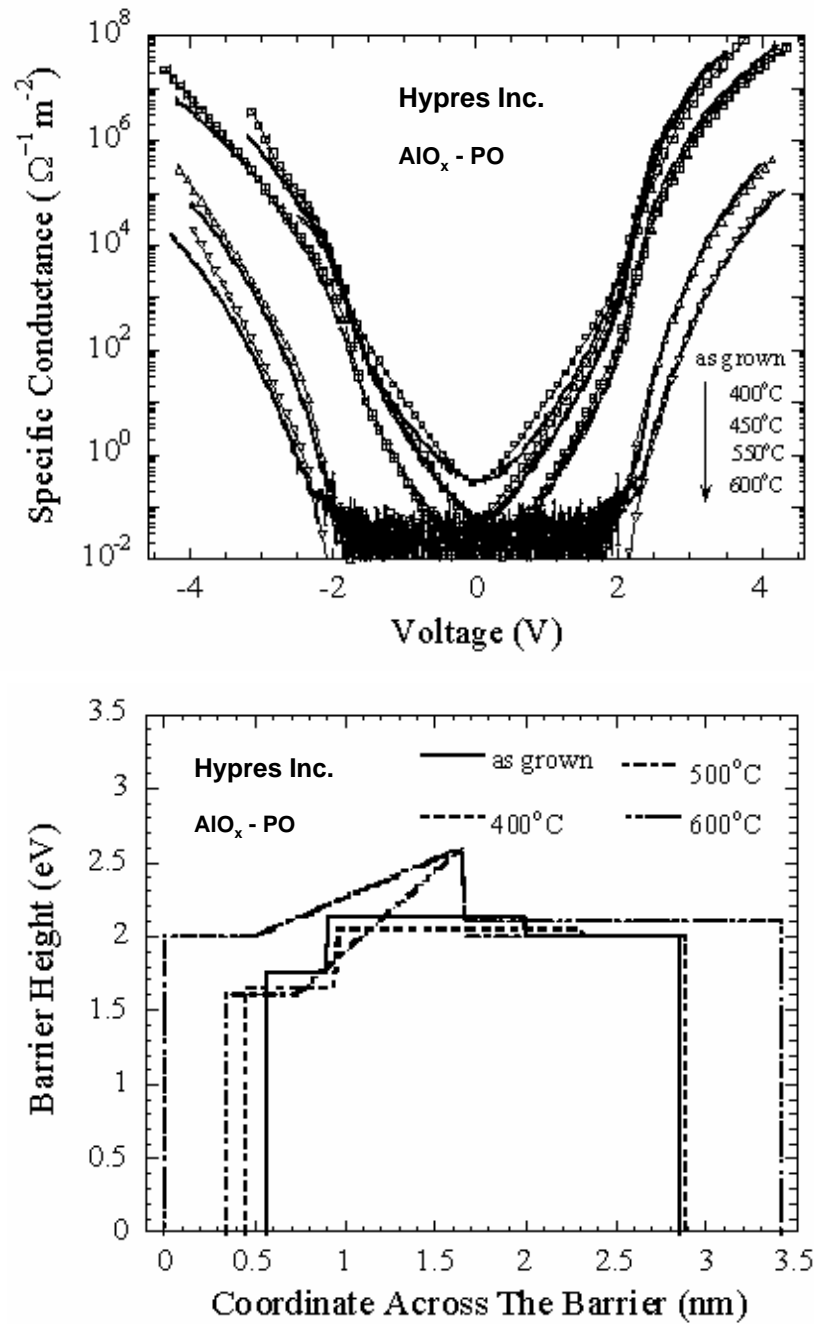
Figure 3.12: (a). Specific differential conductance of plasma grown tunnel juc-
ntions (from Hypres, Inc.) with best theoretical fits (open points) for annealing
temperature up to 600ºC. (b) The barrier profile giving the best theoretical
fitting.

increases from 4.0 ± 0.4 nm to 5.7 ± 0.6 nm. This is also very close to what we observed from HRTEM images. Based on the barrier physical thickness, we estimated the effective mass $m_{ef} = (0.45 \pm 0.05)m_0$, remaining the same for as-grown and annealed samples.

For samples oxidized under low rf-power of 10 W, the low-voltage conductance of the $PO - AlO_x$ samples drops about four orders of magnitude (Figure 3.13). As the annealing temperature become higher than 500ºC, the zero-voltage conductance saturates to the same order of magnitude as that of "Crest 19" with standard or higher powers. Samples that annealed at the same temperature but with different annealing time also show a decrease in the zero conductance, especially for low annealing temperatures, until the saturation limit. The same annealing effect could be achieved for either longer annealing time at relatively lower temperature, or higher annealing temperature but with shorter exposure time. For example, the IV characteristics of oxides annealed at 350ºC for 3 minutes is very similar to those annealed at 400ºC for 30 seconds. As Figure 3.13 shows, the rapid thermal annealing results in a dramatic improvement of the junction endurance to high electric field. In particular, it increases the breakdown dc fields above 10 MV/cm at room temperature. At liquid helium temperature (4.2 K), it reaches above 15 MV/cm, substantially beyond those for the best SiO_2 layers we are aware of.

Another striking feature of these junctions is their high charge-to-breakdown Q_{BD}, defined as $\int I(t)dt$ before breakdown, which is generally used to evaluate the programming endurance of the sample. For our junctions, Q_{BD} is virtually independent of the applied voltage waveform. The measured Q_{BD} for annealed "VJCB17" samples may exceed 10^5 C/cm^2, much higher than $\sim 10^1$ C/cm^2 for typical SiO_2 layers used in flash memories. Figure 3.14 shows a more adequate plot, the maximum number of writing cycles $N \equiv Q_{BD}/CV$, plotted versus the calculated write time scale $\tau = CV/I(V)$, where C is the junction capacitance, V is the high applied voltage and $I(V)$ the current corresponding to the applied voltage. We have observed that at semi-optimized post-processing, the junctions can combine a 20-ns-scale write time with $\sim 10^{11}$ write cycles and ~ 1-second-scale retention time $\tau_R \equiv C/G(0)$, where $G(0)$ is the zero-bias conductance. The 20-ns-scale writing time is acceptable for most applications currently using DRAM chips. Such barriers also have great potential in the application of FGRAM (Floating-Gate-Random-Access-Memory), for at least some embedded RAM applications (in particular in mobile phones and consumer electronics microcontrollers), which currently serve as the main drive for the integrated circuit technology progress. The cell and matrix structures of FGRAM is very similar to NOVORAM. The only major difference between them is the necessity to refresh FGRAM contents periodically, just like this is

being done in dynamic random-access memories (DRAM).

3.5.5 Discussion: Formation of Aluminum Oxide

We have observed a dramatic difference between the annealing effects on thermally grown and 50 W rf-plasma-grown aluminum oxides. Theoretical fitting (based on the direct tunneling theory) tells us that the average barrier height for $TO - AlO_x$, post annealed at temperature close to 500ºC, is substantially $\sim 25\%$ higher than that in the $PO - AlO_x$ layers. In light of the recent experimental X-ray Photoelectron Spectroscopy (XPS) studies [73]-[75] and theoretical analysis [76] of aluminum oxidation at various temperatures, the following picture seems most plausible.

The oxides formed by both methods at relative low temperatures (below ~ 300ºC) are amorphous [74], while their rapid thermal annealing should lead to their gradual ordering, eventually leading to the formation of Al_2O_3 nanocrystals (as in the case of high temperature oxidation [73]-[76]) that the amorphous phase is more stable at the metal/oxide interfaces; hence one can expect that the crystallization, leading to higher tunnel barrier, starts first in the middle of the barrier. This fact is surpported by the fact that the barrier profiles giving the best fits for our tunneling data, have a peak in the middle, as shown in Figure 3.12. One may expect the gradual crystallization to depend on the initial state of the oxide. In particular, since the plasma oxide is formed in a more agitated atomic environment, it should be more thermodynamically stable than the thermal oxide. As a result, its transformation into Al_2O_3 should happen at higher temperatures (or, equivalently, at much longer annealing at the same temperature).

3.6 Simulation Results

Up to now, we have investigated the single aluminum oxide layers in detail. The fact that the thermal and plasma oxides show different annealing behaviors, offers the possibility of using these materials in layered (*e.g.*, "crested") barriers for advanced floating-gate memories and other applications. Figure 3.15 shows the tunnel current density $J \equiv I/A$ and the corresponding time scale τ of floating gate recharging calculated for three promising layer combinations with aluminum oxide: (i) annealed $TO - AlO_x$ / annealed $PO - AlO_x$, (ii) thin SiO_2 / annealed $PO - AlO_x$, and (iii) thin SiO_2 / very thick $PO - AlO_x$ layer. The simulation results for double-layer tunnel junctions formed between n-doped silicon an a metallic counter-electrode, is obtained by using our best fits for aluminum oxides and the commonly accepted
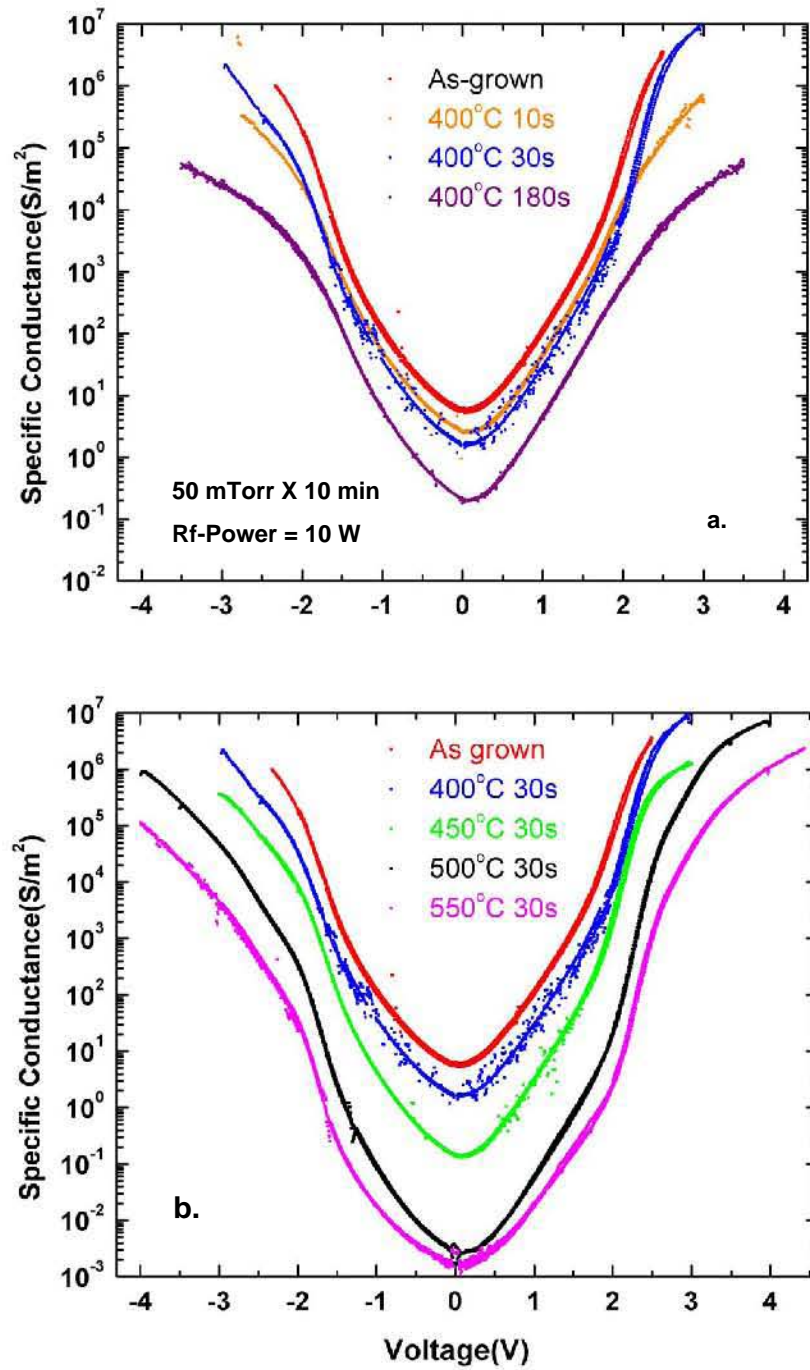
Figure 3.13: Specific differential conductance $G \equiv A^{-1}(dI/dV)$ of junctions from wafer VJCB17 as a function of applied voltage V, for (a) various durations and (b) temperatures of the rapid thermal post-annealing.
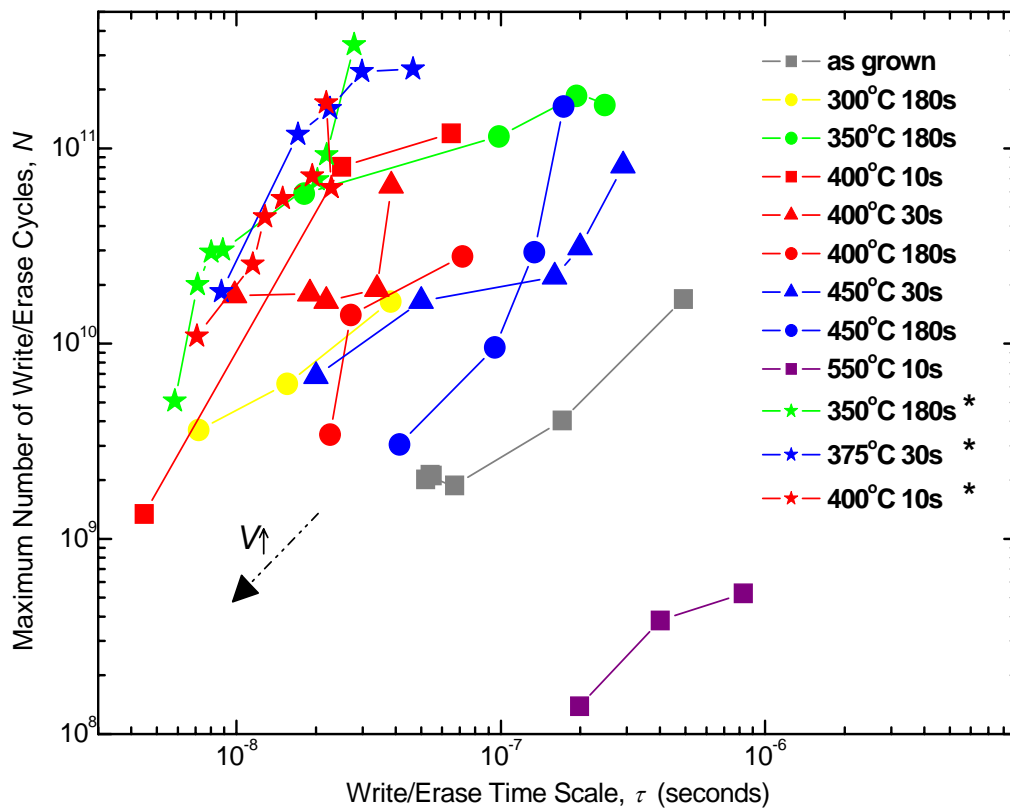
Figure 3.14: Field endurance vs. write/erase speed for junctions from wafers VJCB17, for several sets of RTA time and temperature.

parameters for Si and SiO_2.

$TO - AlO_x$ / $PO - AlO_x$ **Combination**

The plot shows that the all-aluminum oxide layered barrier may sustain a 10-year retention time (standard for nonvolatile memories) at voltage below 1.5 V, while the voltage increase to ~ 4 V (*i.e.*, by a factor less than 3, enabling a simple NOR structure of memory blocks) would cause the gate recharging in ~ 10 μs. Such write/erase time is still too long for RAM applications. Note, however, that the voltage applied to each of the layers would be below 2.2 V, ensuring high endurance: charge-to-breakdown well above $10^5 C/cm^2$, corresponding to more than 10^6 rewrite cycles. This option may be attractive for low-voltage flash memories, especially because there are good prospects of increasing the barrier endurance even further by using higher post-annealing temperatures[77].

Thin SiO_2 / $PO - AlO_x$ **Combination**

The results for option $SiO_2/PO - AlO_x$ barriers, are even more interesting. At $V = 3.2$ V (or higher) such a barrier with voltage about 1.6 V across each layer. For electric fields that are so low, we could not even measure the charge-to-breakdown experimentally, but a simple extrapolation of the high-V data gives an estimate of $\sim 10^{15} C/cm^2$, corresponding to $\sim 10^{11}$ rewriting cycles, which are sufficient for RAM applications. The drawback of these barriers would be a relatively short retention time (100 s at 1.5 V). Too short for nonvolatile memories, this time is still sufficiently long for DRAM-like memories with periodic refresh.

Thin SiO_2 / **thicker** $PO - AlO_x$ **Combination**

In principle, we could fabricate a thick plasma grown aluminum oxide by adjusting various fabrication parameters. The simulation result of a double-layer junction formed by a thin SiO_2 layer with a relatively thicker plasma grown aluminum oxide provide the best performance. If the $PO - AlO_x$ thickness is increased to ~ 6.5 nm, the retention time (at $V < 2$ V) would increase beyond 10 years, the industrial standard for nonvolatile memories, though the floating gate recharging time would increase to ~ 100 nanoseconds (at $V = 5.0$ V). This is somewhat slower than what required for the implementation of the original idea of NOVORAM. However, nonvolatile memories based on such barriers would still be faster than the usual flash [62], while operating at lower voltages.
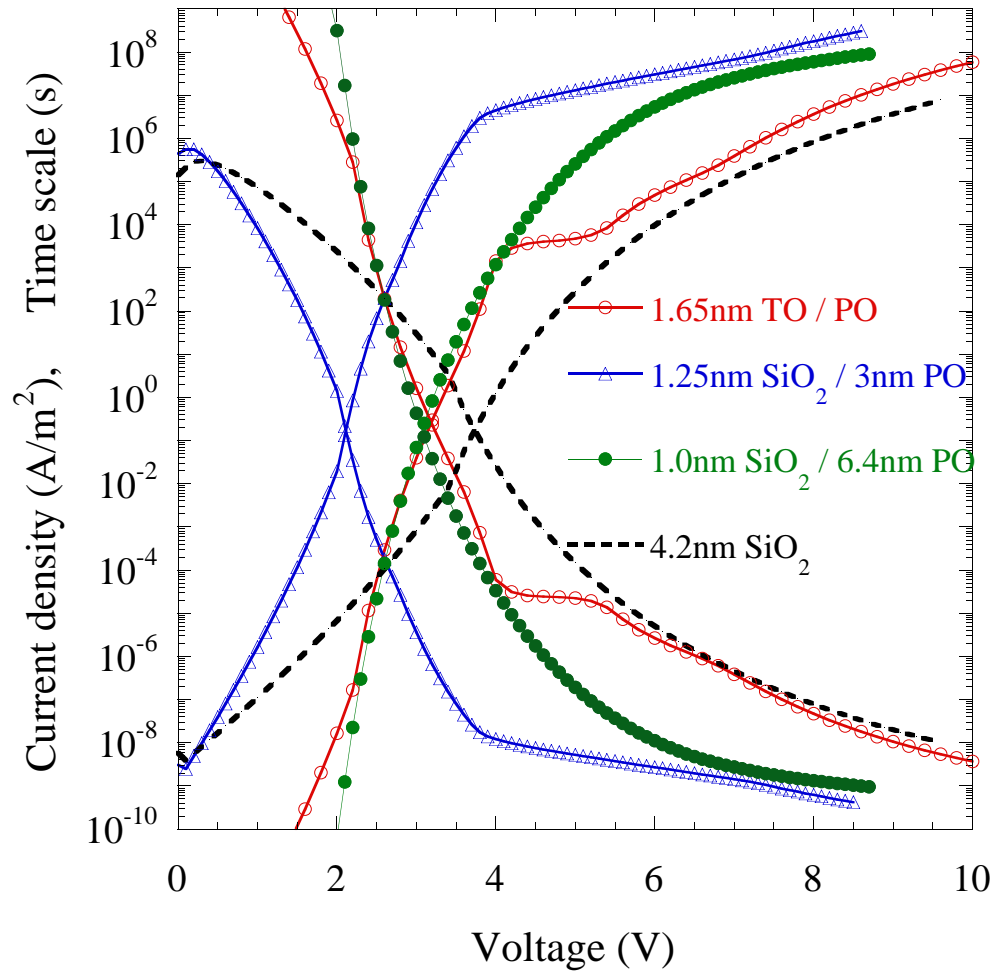
Figure 3.15: Current density $J(V) = I(V)/A$ (ascending curves) and the corresponding time scale $\tau \equiv C_0 V/J(V)$ (descending curves) as functions of the applied voltage for two layered barriers, which calculated using the data fitting results and common accepted values, and for comparison, a uniform SiO_2 layer which has the same J_0 as the thin two-layer barrier at zero voltage.

These estimates should be, of course, looked upon with caution, since the calculations shown in Figure 3.15 imply that the two layers, which had been grown and measured separately in our experiments, may be considered without a substantial change of their properties, assuming that the interfacial chemistry at layer co-deposition would not cause substantial changes of their potential profiles. It is more probable that the sequential deposition of the layers will cause at least a moderate change of their parameters and, hence, a deviation from these predictions. Note, however, that these changes may be either detrimental or beneficial for the crested barrier properties. Moreover, some barrier parameters (*e.g.*, thickness of the plasma-grown layer) can be easily changed to compensate for undesirable barrier alteration and to improve the crested barriers performance even further.

3.7 Implementation of Double-Layer Aluminum Oxides

We have fabricated 6 wafers with $TO - AlO_x/PO - AlO_x$ double layers at both Hypres, Inc. and SBU. Most wafers have been fabricated using $PO - AlO_x$ as the first layer for two reasons (i) better option for implementation of crested barrier; (ii) the strong power of rf-plasma may damage the thin layer of thermally grown aluminum oxide during the fabrication. Figure 3.16 shows the $I - V$ characteristics of such combined layers, measured at 4.2 K. Although we did see a lowering of the zero-bias conductance compared to $PO - AlO_x$ alone, the conduction change range is too small and the overall $I - V$ characteristics is very similar to that of $PO - AlO_x$. The effect of thermally grown aluminum oxide is not prominent here, even after rapid thermal annealing. If we use the fitting parameters for these two layers, the predicted $I - V$ curve show a smaller zero-bias conductance by at least two orders of magnitude than the actual value.

The interfacial aluminum layer is crucial for fabrication of double layer structure. If the layer too thin (~ 1 nm), the interface may not be continuous at all. Instead, there will be aluminum grains on the surface instead of the continuous layer, which could become traps that will store charge during the transport, causing the current switching. Indeed, as Figure 3.17 shows, when the applied voltage is swept back and forth to high voltage (above 3.0 V), we have observed the switching effect. When voltage is swept from 0 to maximum positive voltage V_{max}, the current follows the previous traces. When voltage is swept back to the negative voltage range, the current density jumps to a higher value, indicating the trapping of the electron charge. These charges will
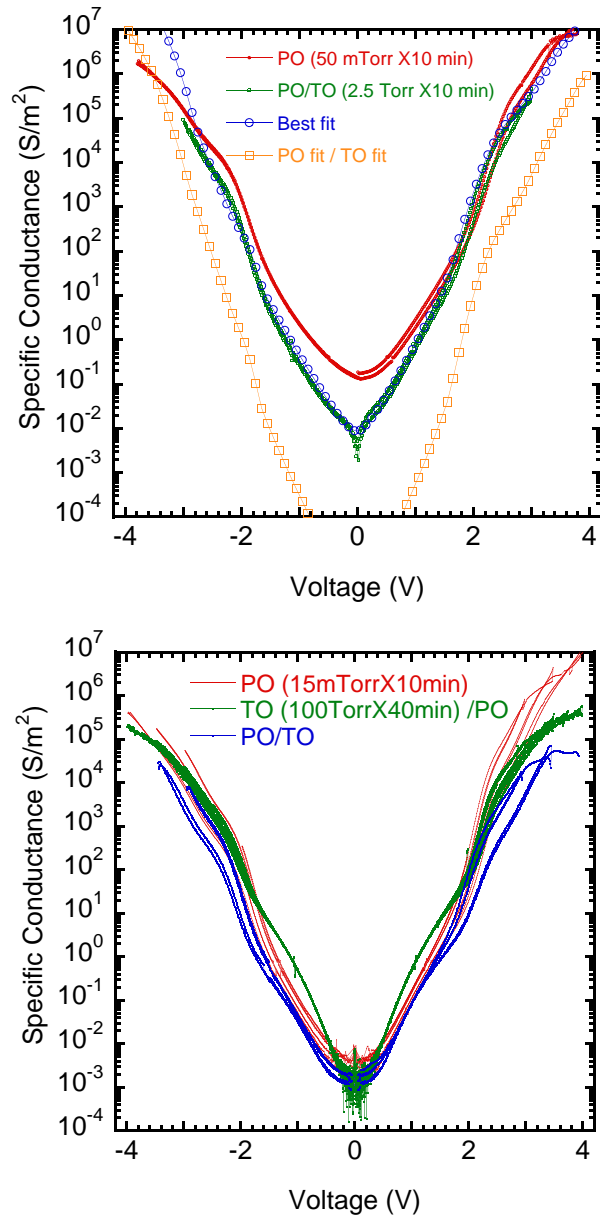
Figure 3.16: Specific differential conductance $G \equiv A^{-1}(dI/dV)$ of junctions from double-layer aluminum oxide as a function of applied voltage V, for (a) low-O_2-exposure-TO/PO with fits and (b) various combination of TO/PO layers.
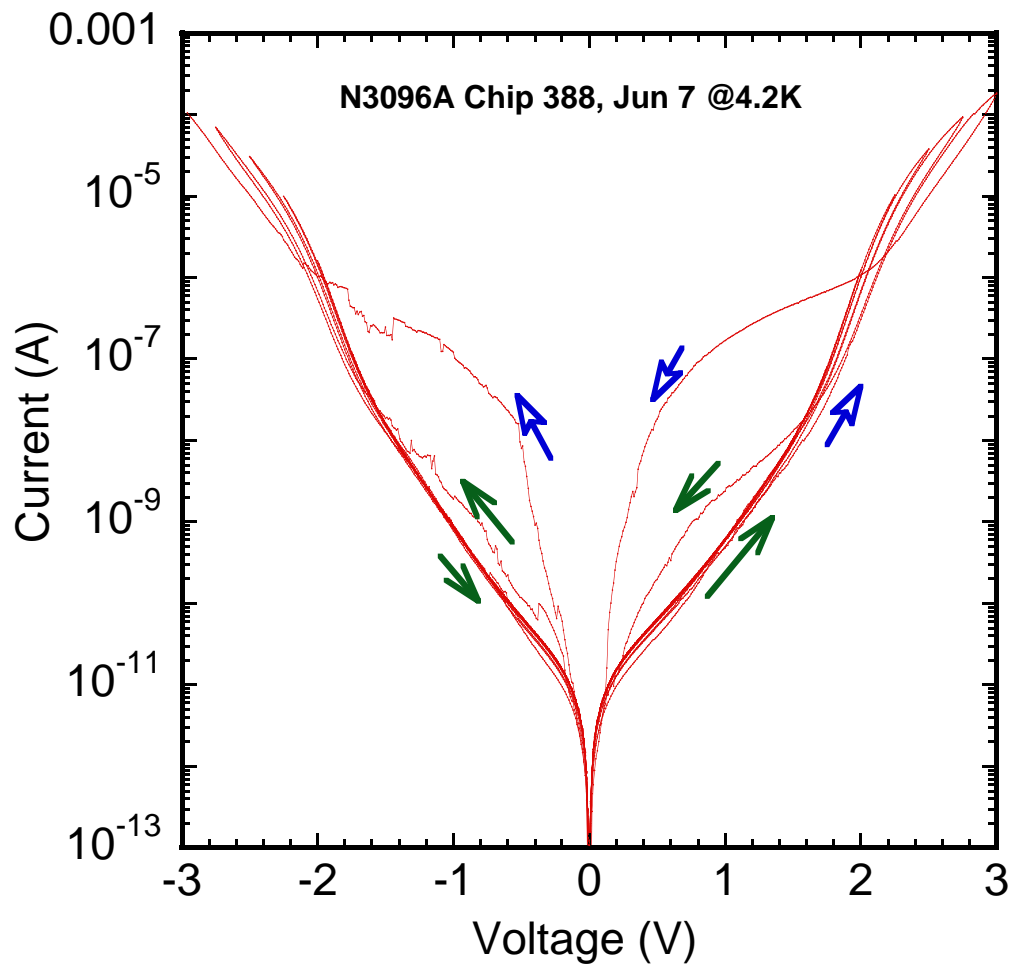
Figure 3.17: $I - V$ plot for a double-layered tunnel junction (wafer "N3096") with switching effect.

be erased after the voltage is swept back from $-V_{\max}$ to 0. The same process is quite repeatable, even at higher $V_{\max}$. So far, we have observed such samples in only one wafer. If the interfacial aluminum layer is too thick, there will be unoxidized aluminum layer left in the middle, not forming the crested barrier we expected.

3.8   Conclusions

Transport properties of $(Nb/)Al/AlO_x/Nb$ tunnel barriers have been studied for structures formed by (i) thermal oxidation and (ii) plasma oxidation, before and after their rapid thermal post-annealing at temperatures up to 650ºC. The electron transport through such barrier is dominated by direct tunneling in electric fields up to ~ 10 MV/cm. The post-annealing results in a substantial increase of the barrier height of the thermally formed aluminum oxide, which (within a broad range of RTA temperatures) may be substantially higher than that of the plasma-grown AlO_x barriers. This fact, together with high endurance of annealed barriers under electric stress, may eventually lead to the fabrication of AlO_x and SiO_2/AlO_x layered ("crested) barriers for advanced floating-gate memories.

Other experimental work has shown that layered barriers made of several material combinations (e.g. $Si_3N_4/SiO_2/Si_3N_4$ [79], [80], SiO_2/ZrO_2 [81], $HfON/Si_3N_4$ [82]) can indeed improve the barrier transport sensitivity to voltage in comparison with the traditional SiO_2 barriers. Unfortunately, the conductivity change range demonstrated so far have not been sufficient for the full implementation of the NOVORAM concept. So far, our attempts to combine thermally grown oxides with plasma grown oxides to form crest barriers have not been successful. As a by-product, we have fabricated quasi-uniform aluminum oxide layers with very high transport properties, including high endurance to electric field exceeding 10 MV/cm, and extremely high values of charge-to-breakdown (close to 10^6 C/cm^2). These properties may be used in FGRAM with cell structure similar to NOVORAM for at least some RAM applications. We believe that such memories, after a modest improvement, may become the RAM of choice for integrated circuits beyond the 32-nm ITRS technology node.

Chapter 4

Electron Transport in Single-molecule Devices

In this chapter, we first give a brief introduction to electron transport through single molecule junctions, including both the two-terminal and three-terminal molecular devices. Basic concepts of single-electron transport theory will be reviewed briefly followed by a few examples of experimental realization of these interesting devices. Then we focus on the molecules that we have actually used in most of our experiments.

4.1 Introduction to Single-molecule Devices

As the conventional silicon-based devices are approaching their physical limit (below 10 nm), alternative materials have been proposed for using in making nanoscale devices to further extend the expiration date of Moore's Law. Among these novel materials, single molecules have become one of the most promising candidates due to their unique properties. First of all, the physical size of most simple molecules is within merely a few nanometers by nature. Molecules can be self-assembled onto material surfaces easily, usually by soaking the support structures in the molecular solution for a few hours. Some molecules would stand up on the metal surface and form a uniform layer and can be used to create large arrays of identical devices. In addition, molecules are very flexible for further refinements and functional terminal groups or substituents can be easily added via chemical reactions. With their tremendous diversity and distinct functionalities, individual molecules may be used as different components of integrated circuits, such as transistors, diodes, switches, memory devices and more.

To build a useful electron device, molecules have to be electrically wired

to the outside world reliably by macroscopic metal electrodes. Though silicon-based electronics traditionally relies on three-terminal devices, such as transistors, most studies in molecular electronics to date have focused on two-termianl devices, due to the difficulty in putting a third gate electrode close enough to the molecule. However, these two-terminal devices can still exhibit interesting behaviors important for future applications, including rectification [83], negative differential resistance [84] and conductance switching effects [85]. In this section, we will give a brief review some of the unique properties of molecular electronics devices.

Molecular Rectifier

A molecular diode or rectifier is an important component in molecular electronics. In 1974, Aviram and Ratner [83] first proposed that a $D - \sigma - A$ molecule could behave as a current rectifier, similar to a $p - n$ junction with asymmetric current-voltage curves. Here, D represents an electron-donor with relatively low ionization energy, A is an electron-acceptor with relatively high electron affinity, and σ is a saturated covalent molecular bridge connecting D and A. In such molecules, the state $D^+ - \sigma - A^-$ is expected to be more energetically accessible than $D^- - \sigma - A^+$, which allows an electronic current to flow only in one direction and blocked in the opposite direction. Such Aviram-Ratner molecuar diodes have been demonstrated experimentally using Langmuir-Blodgett films [86] sandwiched between two planar electrodes. The single-molecule diode has also been demonstrated in a asymmetric molecule consisting of two different weakly coupled conjugated units [87], [88]. One may also expect rectification to arise from asymmetric molecular devices that do not necessarily have donor-acceptor groups. Using different molecule-electrode contacts can achieve diode-like current-voltage curves as well [89], [90].

NDR Effect

The term negative differential resistance (NDR) refers to the counter-intuitive phenomenon of decreasing current with increasing voltage in the current-voltage characteristics of a device. It was first discovered in the Esaki diode, and then in semiconductor quantum well heterostructures, in which the effect is due to interband tunnelling or resonant tunnelling. In molecular devices, NDR has been observed in nitro-substituted oligo(phenylene ethynylene) (OPE), the most widely studied conjugated molecules [84], [91]-[94]. A detailed explanation of its origin is rather complicated for these devices. NDR-like behaviors have also been reported in other molecular systems [95]-[98], and the theoretical understanding involves charging/reduction, structural changes, and electrochemical reactions [99]-[104]. For eventually useful device application, the decrease in current with increasing voltage must be reproducible and robust.

Molecular Switches

The conductance of a molecular switch can be reversibly changed between two states along with the applied voltages. This is very important in applications to molecular memory and logic devices. An example of such a device uses mechanically interlocked bisable complexes, such as catenanes and rotaxanes in Langmuir-Blodgett films [107]. OPE derivatives have been suggested as another candidate for molecular switches [85], [106]. The proposed switching mechanisms to date include charge trapping, structural changes or configuration changes in the molecules [104], and bias-driven changes in the molecule/electrode hybridization [109]. Two-terminal molecular switches have been reported in STM (Scanning Tunneling Microscope) experiments that showed current-induced structural changes in molecules adsorbed on the surfaces [105]. Though this type of experiment will continue to provide the basic knowledge of switching effects, reproduciblity and integrablity still require a lot of intensive investigations for building practical devices.

Molecular Transistors

Molecular transistor consists of molecules in contact with three terminals: source, drain and gate electrodes, similar to a conventional field-effect transistor in silicon based devices. Theoretical models have suggested that the conductance of a single molecule could be modulated with a gate electrode. However, it is difficult in practice to place the gate electrode close enough to the molecules to have effective gate coupling between them. Several gate configurations have been proposed in recent years, including back-gate, electrochemical gate and molecular gate. Among them, back gate is the most widely used approach in current experiments. The source and drain electrodes are fabricated on top of a gate electrode, separated by a thin layer of oxide. Two types of gate materials are frequently used: (1) heavily doped silicon substrate with thermally grown silicon oxide (a few hundred nanometers) on top, and (2) thin aluminum layers with either a native oxide or thermally grown oxide of a few nanometers. Since the separation between the source and drain electrodes is nanoscale, we have to pay attention to the electrode geometry to prevent the possible screening effect for the gate. Various experiments have shown interesting single electron effects, such as Coulomb blockade [160], [110], [111] and Kondo effects [160], [161] in a single molecule or a small number of molecules.

4.2 Fabrication Methods of Single Molecule Junctions

The underlying scheme to measure transport through single molecules is conceptually simple: a molecule is connected by two electrodes. A bias voltage is applied between the electrodes and the current flowing though the device is measured by a multimeter. However, these nano-scale transport measurements could be realized only after the development of necessary experimental techniques for nanoelectrode formation, such as scanning tunneling microscopy (STM) and e-beam lithography techniques. Figure 4.1 lists the current popular fabrication methods of molecular junctions.

Techniques based on STM and conducting probe AFM have been employed to examine numerous molecules (Figure 4.1a). Molecules are deposited on top of a conducting surface that acts as one electrode and a metallic scanning probe tip is used as the other electrode. This technique has the advantage of being able to image and to measure the transport properties of individual molecules. For example, one can establish individual molecular junctions by moving the tip into and out of contact with a substrate in a solution containing the sample molecules by monitoring the junction conductance. The main advantage of this method is its ability to repeatedly form thousands of molecular junctions in which molecules are directly connected to two electrodes [114]. However, the interpretation of the $I - V$ characteristics are complicated by the tunneling barrier inherent to the feedback mechanism of the STM tip. It also requires a relatively high level of instrumentation and not applicable for building electron-device in integrated circuits.

The mechanical-break-junction (MCBJ) technique [115]-[116] (Figure 4.1b) has been successfully used to measure the conductance of a single molecule. This method uses a narrow metallic wire attached to a flexible substrate that is subsequently bent until it breaks, producing a gap whose separation can be adjusted to a very fine length resolution. The molecules are introduced either by placing a drop of solution with molecules and allowing it to dry or by exposing the fractured surfaces to a gas that adsorbs on the metal. Contact is re-established between the fracture surfaces by precise piezoelectric control of the substrate bending. Although the mechanical stability of an MCBJ at low temperature (~ 4.2 K) is high [117], [118], reliable temperature-dependent measurements are difficult to obtain due to thermal drifts.

Another popular technique used in most single-molecule experiments is the electromigration technique [158] (Figure 4.1b). An e-beam-patterned metal constriction is formed either on an oxide-covered Si surface or on a thin aluminum oxide/ aluminum layer, where both substrates serve as back gate to

(a) SPM Technique

• STM
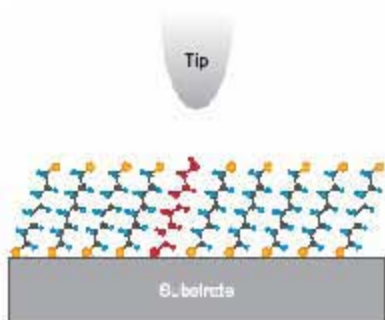
• AFM
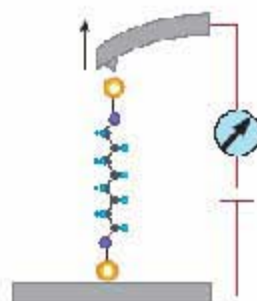
(b) Planar Devices

• Mechanical break junction
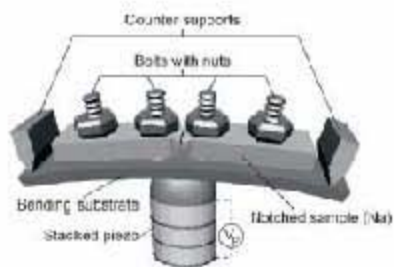
• Electrodeposition
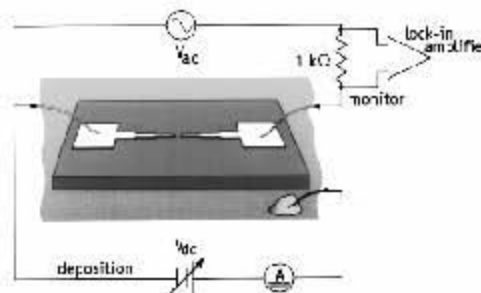
• Nanopore
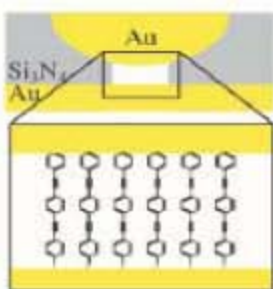
• Electromigration
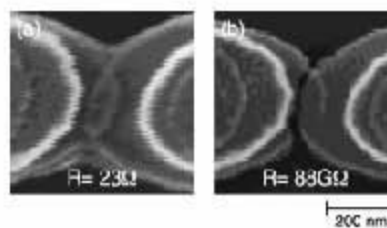
Figure 4.1: Various experimental techniques for measuring single molecule conductance.

the junction. The sample is placed at cryogenic temperature after immersion in solution. When a high current is passed through the constriction, electromigration-induced junction breaking occurs. Due to the stochastic nature of the process, every junction differs at atomic scale. The method relies on statistical analysis of many samples and the yield is usually $\sim 10\%$. This method enables the construction of single-molecular transistors and allows gate-dependent and temperature-dependent measurements.

Two other unconventional nano-fabrication techniques are also shown in Figure 4.1b. One can first fabricate two electrodes with relatively large separation, with subsequent metal deposition by electrochemical methods until the two electrodes merge. This process can be controlled to produce electrodes with a nm-size gap, which is usually called the electrodeposition method. Another technique is usually used for studying more than one molecule, which is called the nanopore method. In this technique, a small hole of diameter less than 10 nm is first fabricated in a thin silicon nitride membrane and molecules are sandwiched between the top and bottom electrodes through the hole. However, it is impossible to know the structure of the organic layer and the top evaporated layer could damage the organic molecules.

4.3 Basic Concepts in Single-electron Transport Theory

In a single-molecule junction, the energy levels of the molecule are quantized. Let us consider the case of a single-molecule single-electron transistor. Figure 4.2 shows the schematic of such a junction, where the molecule or quantum dot is surrounded by three electrodes: source. drain and gate. All three electrodes are capacitively coupled to the molecule. A potential change in any of them will cause an electrostatic energy change in the molecule. Let the barrier at either source or drain contact be opaque enough that it serves as a tunnel barrier. The number of electrons on the molecule N is then well defined. The electron transport is allowed only between the molecule and source/drain electrodes. The energy level inside the molecule will not change with the source-drain bias. However, it could be shifted up or down by changing the potential of the gate electrode.

The general theory of single-electron transistor with a substantially discrete spectrum of electron states of the island has been developed by Averin and Korokov [119], [120]. The main assumption is the rates of electron tunneling in and out of the island to be sufficient low, compared to the island energies (~ 1 eV). The island energy E_k has been assumed to follow a quasi-particle
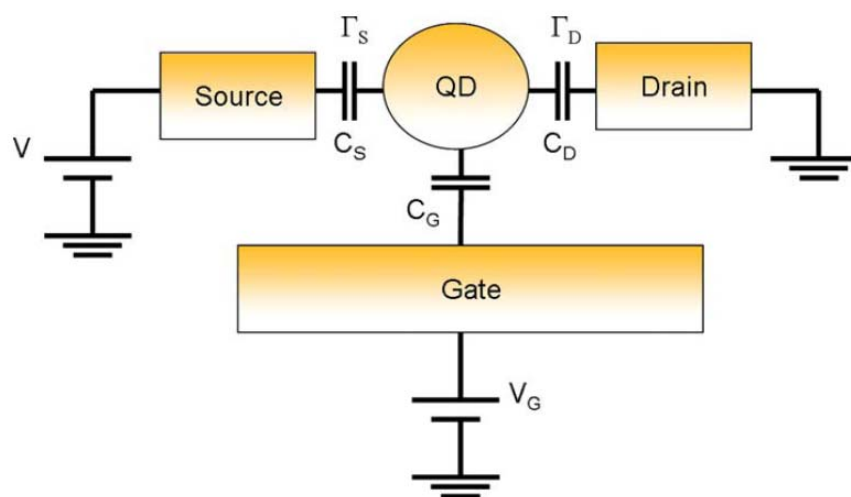
Figure 4.2: A schematic of a single-molecule single-electron transistor. The molecule is capacitively coupled to three electrode: source, drain and gate. Charge can tunnel into and out of the molecule from the drain and source electrodes, with tunneling rates of $\Gamma_D/\hbar$ and $\Gamma_D/\hbar$.

model:

$$E_k = U(n) + \sum_i \varepsilon_i p_i = \frac{(ne - Q_0)^2}{2C_\Sigma} + \sum_i \varepsilon_i p_i \qquad (4.1)$$

where $Q_0 = C_G V_G + const$, $n = n(k)$ is the number of electrons on island in its quantum state number k, and C_G and $C_\Sigma = C_S + C_D + C_G$ are the transistor capacitances [121], [122], which have be assumed to be independent of N and of applied voltages V and V_G, $U(N)$ is the single-electron charging energy, ε_i is the kinetic energy of the electron on the ith quasiparticle level, and $p_i = 0$ or 1 are level occupancies (with the sum of all p_i equal to N). Let us define μ_S and μ_D to be the Fermi level of the corresponding source and drain electrode. The difference between these levels is determined by the applied source-drain volatage: $\mu_S - \mu_D = eV$. The expression for the total electrostatic energy W of this system [123] is:

$$W = (ne - Q_0)^2 / 2C_\Sigma - eV[n_1 C_S + n_2 C_D]/C_\Sigma + const. \qquad (4.2)$$

where n_1 and n_2 are the number of electrons passed through the tunnel barriers, so that $n = n_1 - n_2$. According to the orthodox theory, the electron tunneling rate Γ depends solely on the reduction ΔW of the electrostatic energy of the system, which can be expressed as

$$\Gamma(\Delta W) = (1/e)I(\Delta W/e)[1 - \exp(-\Delta W/k_B T)]^{-1} \qquad (4.3)$$

At small source-drain voltage V there is no current, since any tunneling event would lead to an increase of the total energy ($\Delta W < 0$) and hence the tunneling rate is exponentially low. This suppression of dc current at low voltages is known as the Coulomb blockade. In other words, the current is blocked due to the charging addition energy.

When the applied bias is higher than the threshold voltage V_c, the Coulomb blockade is overcome and at much higher voltages the dc $I - V$ curve exhibits quasi-periodic oscillations around the linear asymptotes. The threshold voltage is a periodic function of the gate voltage with period given by $\Delta V_G = e/C_G$. Here Q_0 changes by e and may be exactly compensated for by one of the electrons tunneling to/from the island. This periodic dependence is also called "Coulomb blockade oscillations". The effect of the gate voltage is equivalent to the injection of charge $Q_0 = C_G V_G$ into and island and thus changes the balance of the charges at tunnel barrier capacitances C_S and C_D, which determines the Coulomb blockade threshold V_c. V_c is also called the degenerate point in the Coulomb blockade.

Usually we plot the differential conductance as a function of source-drain bias voltage V and gate voltage V_G in a color-scale diagram. Two lines with

higher conductance values are visible, which corresponds to the conductance peaks. When the $k + 1$ level of the quantum dot E_k is aligned to the Fermi level of the source (μ_S), the slope of the line is positive and defined by:

$$V = \frac{C_G}{C_G + C_D}(V_G - V_c) \qquad (4.4)$$

Similarly, the alignment condition between the quantum dot and the drain electrode is given by:

$$V = -\frac{C_G}{C_S}(V_G - V_c) \qquad (4.5)$$

In a $dI/dV - V - V_G$ plot (Figure 4.3a), we could obtain information about the capacitance ratio among the three capacitance by measuring the slopes of dI/dV. Figure 4.3b shows the $dI/dV - V - V_G$ plot for three different charge states of a quantum dot: 0, -1, and -2 states, corresponding to the k, $k + 1$ and $k + 2$ electron states respectively. The Coulomb blockade region between the two degeneracy points V_{c1} and V_{c2} is called the Coulomb diamond. One important parameter we could obtain from Figure 4.3 is the charge addition energy E_a. Point A denotes a crossing point between two differential conductance lines for the source alignment of the -1 state and the drain alignment for -2 state. The bias at the crossing point A is $|eV_{c1}| = E_C + \Delta E$. If the level spacing can be estimated independently, the charging energy E_C can be measured from V_{c1}. In conclusion, in a $dI/dV - V - V_G$ plot, a dI/dV line with positive slope corresponds to the case where a charge state of the quantum dot is aligned to the Fermi level of the source electrode. A dI/dV line with a negative slope corresponds to the case where another state is aligned to the Fermi level of the drain electrode. The bias at the crossing point corresponds to the energy difference between the two states and the charging energy.

Now let us discuss the condition to observe such single electron transport behaviors. First, the charge addition energy should be much larger than the thermal energy $k_B T$. Otherwise, thermal fluctuation effect will dominate and the Coulomb blockade effect will be washed out. The charging energy E_C increases as the dot becomes smaller. For example, for a metal sphere with radius R, $E_C = e^2/(4\pi\epsilon_0 R)$. For a metal sphere with a 1 μm diameter in vacuum, the charging energy is 1.44 meV that is observable only at cryogenic temperatures. For a metal sphere with 100 times smaller radius $R = 10$ nm, the charging energy increases to 144 meV, which is large enough to be observable even at room temperature ($k_B T = 25.9$ meV for T= 300 K). (We should pay attention that the local electrostatic environment is also important for estimating the charging energy besides the quantum dot's size.)

The number of electrons on the molecule should also be well-defined.

(a)

Slope= $C_G / (C_G + C_D)$

Charge Degeneracy

V_{SD}

Slope= $-C_G / C_S$

V_G

(b)

A

P1

$(E_C + \Delta)/e$

P2

V_{SD} 0   -1   -2

V_{C1} $[(E_C + \Delta)/e](C_{tot}/C_G)$ V_{C2}

V_G
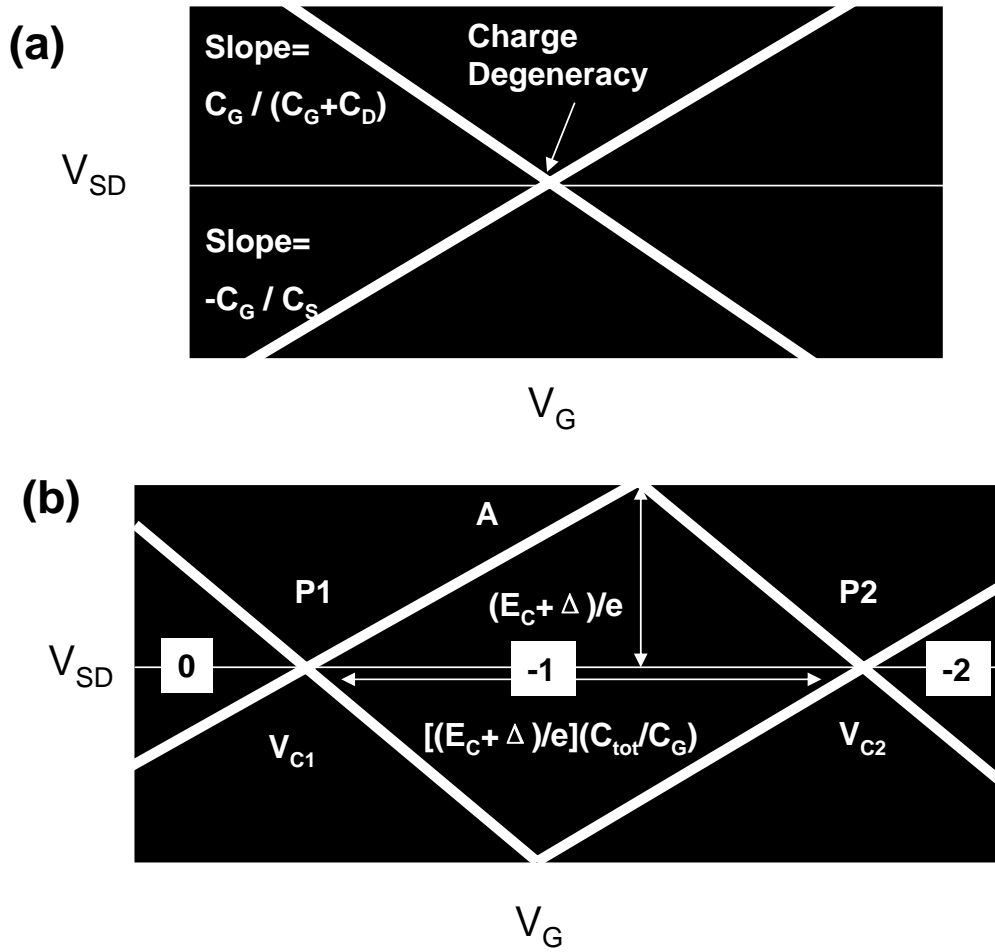
Figure 4.3: Coulomb diagram for a generic single electron transistor: plot of the differential conductance as a function of V and V_G. (The brightness is proportional to the differential conductance): (1) a single-level quantum dot; (2) a quantum dot with multiple charge states.

which requires resistive contact or weak coupling between the molecule and the leads. Quantitatively, the contact resistance needs to be larger than the quantum resistance $h/e^2 \sim 25.8$ KΩ. When a molecule is inserted into a junction, the molecular levels are broadened, which is the result of the tunnel coupling to the source and drain electrodes. Let us define the tunneling rate of the source and drain electrodes Γ_S and Γ_D as the number of electrons that will tunnel through the tunnel barrier per unit time. The life time τ of an electron on the dot is expressed as $\tau \sim (\Gamma_S + \Gamma_D)^{-1}$. The intrinsic broadening is proportional to $\gamma = h(\Gamma_S + \Gamma_D)$ as a consequence of the Heisenberg energy-time uncertainty principle ($\tau\gamma \sim h$).

In summary, the assumptions for realizing the single-level quantum-dot regime are listed as follows:

1. Single-electron transport: $E_C + \Delta E >> k_B T$;

2. Quantum-dot regime: $\Delta E >> k_B T$;

3. Single-level quantum dot: E_C, $\Delta E >> eV$;

4. Negligible intrinsic broadening: $\gamma << k_B T$.

4.4   Interesting Molecules

In this section, we will focus on the examples of extensively studied wire-shaped molecules, such as alkanes and oligo(phenylene-ehtynylene)s (OPE). These molecules can be roughly divided into two categories: saturated and conjugated chains, according to the molecular bond's property. The molecules used in all our experiments are based on OPE units, which have been fabricated in Prof. Andreas Mayr's group at Stony Brook University [187]. Their molecular structures and functions will be introduced, as well as the properties of the terminal groups.

4.4.1   Alkane Chains

One of the extensively studied saturated molecules is the alkane chain consisting of saturated C-C bonds (σ bond) terminated by linker groups (*e.g.*, by thiols) that bind with the metal electrodes (*e.g.*, Au, Ag, Pt, or Ag). σ bond is the strongest type of covalent bond. The molecules usually have large gaps ($\sim$ 8 eV) between their highest occupied molecular orbitals (HOMO) and lowest unoccupied molecular orbitals (LUMO), so they are usually considered as the poorly conducting wires or insulators. Because of their robustness, alkane chains (*e.g.*, alkanethiol [$CH_3(CH_2)_{n-1}SH$]) can form a stable

self-assembled monolayer on metal surface. Various transport measurements through alkane chains [124] have shown that the conductance (G) is found to decrease exponentially with increasing molecule chain length (L), described by $G = A*exp(-\beta L)$, where A is a constant and β is the tunneling decay constant varying between $\sim 0.7 - 0.9$ Å^{-1}. Due to the temperature independence, it is suggested [125] that the electron tunneling is main transport mechanism in these molecules. By comparing various experiments on alkane molecules, the absolute conductance value varies from one another. The electrode-molecule contact geometry is another important factor that will affect the overall transport of metal-molecule-metal junctions. Whether the molecules interact with the electrodes by chemical bonding or physical contact, the current flow can differ up to three orders of magnitude for alkane thiol-based junctions [126].

4.4.2   Oligo(Phenylene-Ethylene)s and Their Derivatives

Because the tunneling rate is exponentially decreased with the molecular length, the conductance is too small to be measured for alkane chains longer than 2 - 3 nm. The conjugated molecules (such as Oligo(Phenylene-Ethylene)s) are better candidates for long-distance charge transport, which consist of alternating double/triple bonds with delocalized π electrons. Compared to alkanes, these molecules have much smaller HOMO-LUMO gaps (~ 3 eV) and thus are more conductive. The tunneling decay parameter β is found experimentally and theoretically to be $0.2 - 0.6$ Å^{-1} for non-resonant electron tunneling through π-bonded molecules [127]-[129], which is smaller than that of the saturated molecules, hence leading to higher tunneling efficiency.

Besides the more efficient transport in OPE-based molecules, the easy synthetic flexibility to alter their chemical moieties makes them good candidates to study various effects on the electron transport properties [130] - [137]. For example, by controlling the electron donating and withdrawing of the substituents on the OPE molecules, their conductances are expected to experience a big change. Other interesting effects have been observed in these molecules as well. OPE $-$ NO$_2$ molecules exhibits interesting negative differential resistance [131], [133] and stochastic conductance switching phenomenon [138], [139].

Direct conductance measurements of conjugated OPE molecules have been reported using different experimental approaches [142]: such as nanopores [140], conducting-atomic force microscopy (cAFM) [92], Scanning tunneling microscopy (STM) [138], cross-wire technique [143], mechanically controlled break junction (MCB) [141], and hybrid-SAM assembly [139]. Results shows that charge transport can happen over a larger distance than alkanes. When

the length of the molecule is increased, tunneling will be replaced by hopping as the dominant charge transport mechanism.

Because of the rich structures in OPE molecules, the molecule conformation is as important as the nature of electrode-molecule contact for charge transport [143] - [145]. Experiments shows that at low temperature the phenyl rings show very little tendency to rotate with stable perpendicular configurations, resulting low or reduced conductance, while at relatively higher temperatures, the rings are able to rotate freely with respect to each other which allows the planar geometry and hence increasing the charge transport efficiency [145]. Different contact geometries also affect the charge transport in the molecules. Strongly asymmetric current-voltage characteristics has been observed in symmetric molecules due to the different contact environments. In a word, the HOMO-LUMO gap, the rotational configurations and the electrode-molecule contact are all important for charge transport. In addition, the inelastic scattering and local heating need to be considered.

4.4.3 Mayr's Molecules

Most of the OPEs discussed above are using thiols (OPE-SH) as their linker groups to bind to the metal electrodes. Because thiols are very easily oxidized in air, all sample / device preparations are done in inert gas or vacuum. However, it is almost inevitable for the prepared sample to be exposed in oxygen during the transport process to characterization devices from vacuum chamber. This is why it was desirable to have more stable linker group attached to the molecules so that the self-assebly can be done at ambient system without changing the molecular properties. The molecules used in our studies have the diisopropylphenylisocyanide unit as the terminal groups ($OPE - N \equiv C$) [187]. Nitrogen and carbon are connected through a triple bond with a positive charge on nitrogen and a negative charge on carbon. The bulky substituents next to the isocyanide group prevent polymerization and attacking by other reagents, hence it is much more stable and can be used for self-assembly in ambient system (Appendix B).

Given that -NC/noble metal junctions exhibit lower conduction barriers than corresponding thiol-based junctions, it is important to understand the attachment mechanisms of isocyanide-termianated molecules to the metal wires. The nature of the aryl-NC-metal bond is complicated by possible multiple bonding interactions with the metal substrate [147]. For commonly used transition metal electrodes (*e.g.*, Au), aryl-NC- typically results in a σ bond via donation by the carbon lone pair to the metal substrate. When the metal has filled d orbitals capable of overlapping the π^* antibonding orbitals of the $-N \equiv C$ moiety, a back-donation π-type bond also may form [146] (Figure

4.4).

Figure 4.4 illustrates three types of molecules that we are mot interested in: (1) molecular wire: simple OPE chains with $n=1, 2$; (2) molecular transistor: OPE-NDI (naphthalenediimide) chains with $n=1, 3$, NDI group is used as a single-electron island in the middle; (3) suggested single-electron latching switch [148] - [150], where the arendiimide groups were chosen for single-electron islands due to their strong electron acceptor properties [151] - [154]. In particular, naphthalenediimide can form a stable radical anion [155]. The transistor island is connected to two electrodes by means of short conducting OPE chains that are terminated by isocyanide alligator clips. A parallel conducting chain connects the trap island to the dendritic wire only. The connection between the single-electron trap and the axon is an insulating structural elements, keeping the trap at a fixed distance from the wire. The benzyl-arylether links between the two conducting wires are also insulating structural elements that controlling the distance between the trap island and the transistor island. Since the proposed latching switch is still in scratch, we have studied the first two types of the molecules in three support structures which will be discussed in the next chapters.
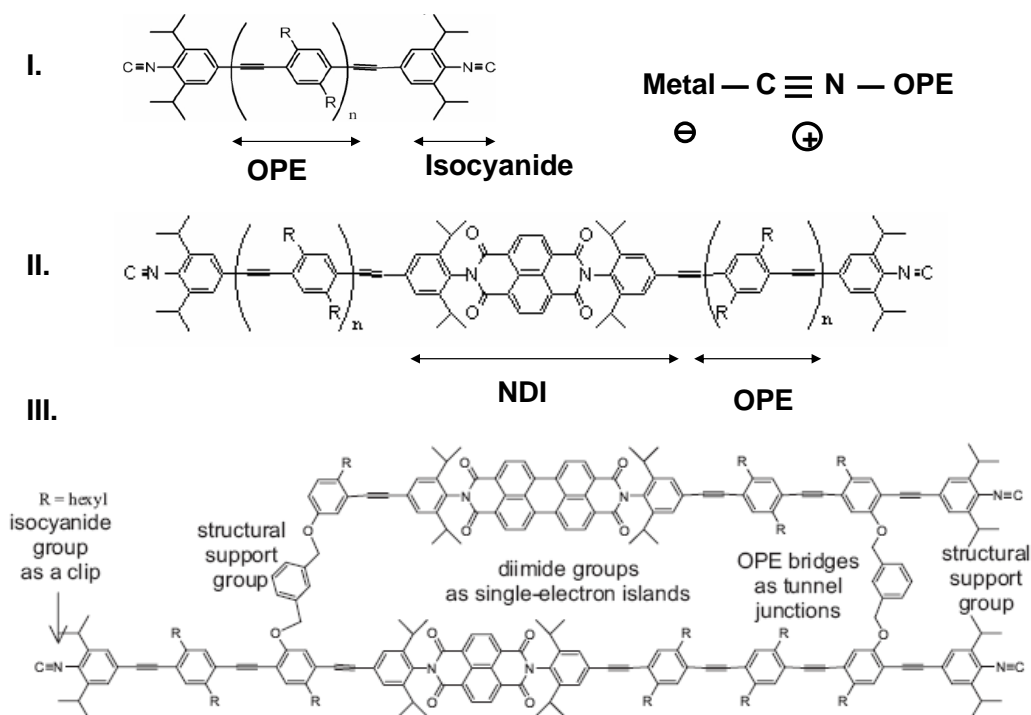
Figure 4.4: Three types of molecules suggested in our experiment: (a) oligo(phenylene-ehtynylene)s bridges with isocyanide terminal group. n is the number of OPE rings between the two end groups. For $n = 1$, molecular length $l = 2.2$ nm; for $n = 2$, $l = 2.9$ nm; (b) SET type molecules with naphthalenediimide group as the acceptor in the middle. n is the number of OPE rings between the acceptor and the end group. For $n = 1$, $l = 4.8$ nm; for $n = 3$, $l = 9$ nm; (c) suggested molecular single electron latching switch. The possible bonding structures for isocynide with metal electrode is illustrated on the top right panel.

Chapter 5

Molecular Junctions Based on Co-planar Gaps

In the beginning of this work, the relative advantages of the structures for molecular transport studies (reviewed in the previous chapter) were not clear. This is why we have tried a few of them. The most straightforward idea is to put individual molecules directly between the gap of two nanometer-separated metal electrodes, provided that the length of the molecules matches the nano-gap size. Due to the current limitation of electron beam lithography, the lowest gap separation we could obtain is around 5 to 10 nm [156]. Only molecules with the length in this range would be possible used to bond with the metal electrodes.

5.1 Fabrication of Nanogap by E-beam Lithography

The devices have been fabricated on highly doped 2-inch (50 mm) silicon substrates covered with 500 nm of SiO_2, using a combination of optical, electron-beam lithography and photoresist/lift-off process. Figure 5.1 shows the fabrication procedures. A two-layer photoresist PMMA/P(MMA-MAA) has been spun on the surface of silicon oxide and exposed to electron beam (in the area that would later become nanowires) with a small discontinuous area in the middle (which would be used as a mask for the definition of the nano-gap after development). Thermal evaporation has been used to deposit a 4-nm-thick layer of Cr as a sticking layer followed by a 10-nm-thick Au film. After lift-off treatment, two Au nanowires with a nanometer-scale gap has been formed and ready for the deposition of molecules. Figure 5.2 shows two SEM (Scanning Electron Microscope) images of two 100-nm-wide gold nanowires with gap size

below 10 nm. The top view of our 5×5 mm^2 chip with a total of 18 devices is also shown. The thick wiring provided good electrical connection to the contact pads. The produced gaps varied from 5 to 70 nm. The yield of good support structures with separation below 10 nm was below 15%.

5.2   Molecular Deposition Method

In the planar electrode configuration, in order to match the formed gap size (5 - 10 nm), we have studied long molecules (SET-type: OPE-NDI) of 8 - 9 nanometers. The sample with bare electrode structures has been ultrasonically soaked in acetone for $1 \sim 2$ minutes and rinsed with isopropanol (IPA), to remove any organic residue. Then the chip has been brought into a plasma chamber for two minutes in pure oxygen. The leakage current through the gap has usually been measured before the deposition of molecules to check the background current. Then the sample has been soaked in molecular compound (OPE-NDI with $n = 3$ in toluene) for 1 to 24 hours for self-assembly with various concentrations (0.1 mM $\sim$ 10 mM). The sample has been thoroughly rinsed with pure toluene and completely dried under nitrogen flow. We have measured the sample at both room and liquid helium temperatures.

5.3   Electrical Characterization and Discussion

We have measured 25 chips (i.e., about 450 devices) before and after molecular deposition. There were about 70 devices with less than 10 nm separation gaps. After the initial cleaning process, we have measured the leakage current through the devices. Figure 5.3 shows the $I - V$ characteristics for two typical junctions (without molecules) measured at both room and low temperatures. Even at 1.0 V, the magnitude of the resulting current is very small ~ 0.1 pA.

   Then the samples have been transfered to the molecular solution for self-assembly overnight. If there was one or a few molecules sitting right between the gap and bond with both electrode, the current through the junction was expected to be significant different from the bare-electrodes. However, out of 70 devices, we have only found 2 devices showed nonlinear $I - V$ curves (Figure 5.4). All other junctions showed only a leakage current of the order of pA. The two interesting devices showed conductance peaks at: (1) 0.1 V and 0.3 V; and (2) 0.5 V and 0.8 V. Their conductance is also different by three orders of magnitude. Now it is time to ask if the observed nonlinear $I - V$ is due to the incorporation of molecules. The usual method is to introduce the third electrode - gate electrode. However, at this very early stage, we have not

1. Spin coating of resist

silicon/SiO2

2. Lithography light mask
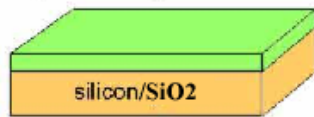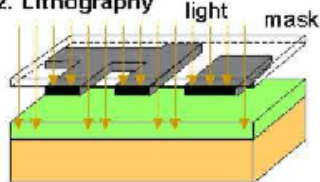
3. Resist development
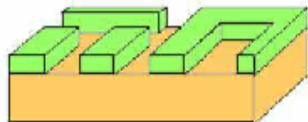
4. Metal coating

5. Lift-off of metal film
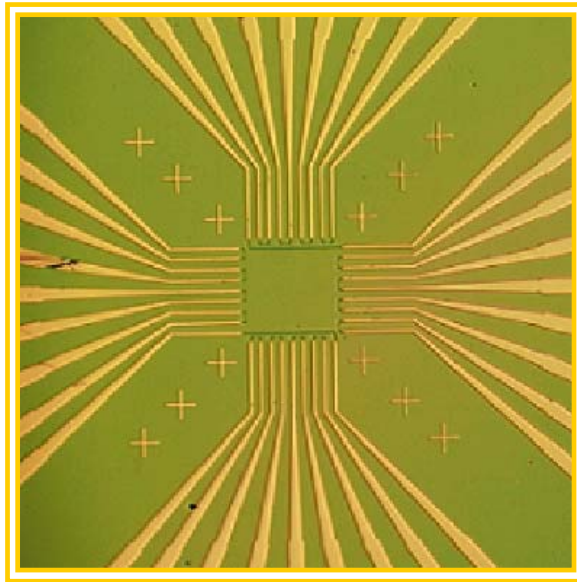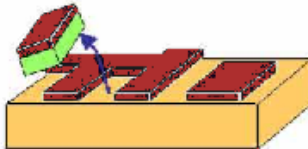
Top view of the 5x5 mm^2 chip

Figure 5.1: Fabrication procedure: (a) Schematic presentation of the fabrication procedure to make nanowires with a 10 nanometer gap. (b) Top view of an actual chip with 18 junctions.
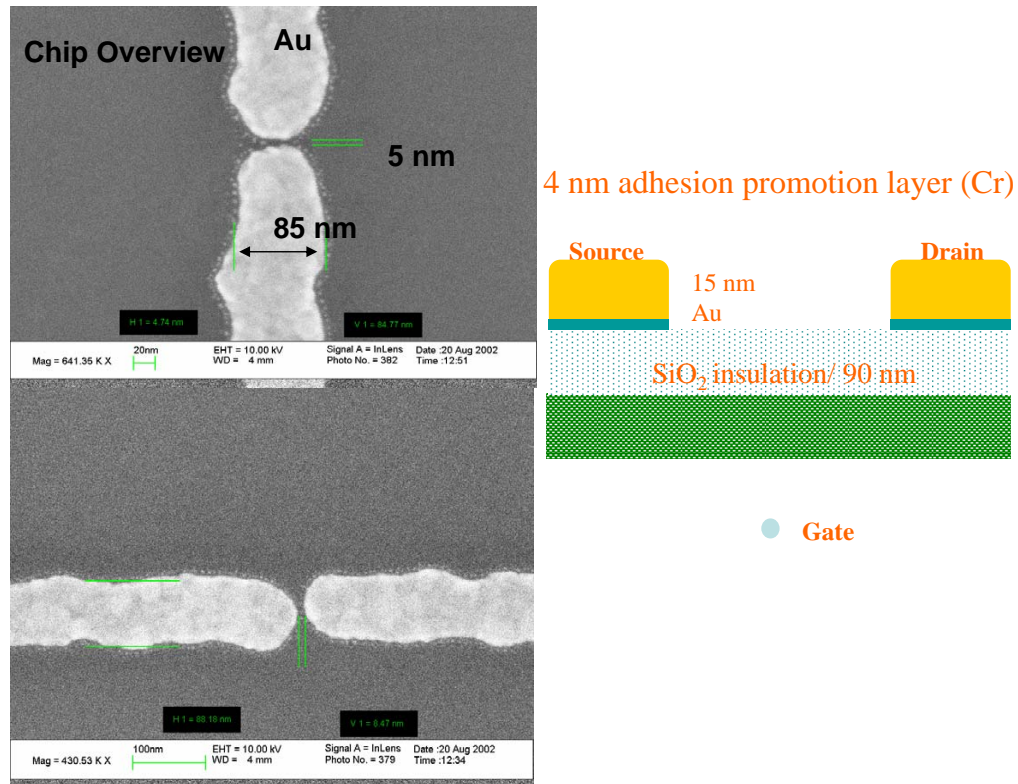
Figure 5.2: Scanning electron micro-graph for one of the best samples with Au electrodes of width = 85 nm, separated by a $\sim$ 5 nm gap. Small nanoparticles are visible along the edge of the electrodes. On the right: a cross-section of typical support structures.

developed the measuring system fully to be able to test sample performance under gate modulation. So it was hard to tell if the signal was from a molecule or just from an impurity.

The extremely low yield of interesting devices ($< 1\%$) have suggested that this approach was not applicable. Though the first trials were not successful, during them we have built the highly sensitive electronic platform for low temperature transport measurements starting from scratch, developed automatic computer controls using Labview programs and established the typical measurement protocols (Appendix A). The same support structures can also be used for gold-nanoparticles deposited by self-assembly and Langmuir-Blodgett technique.
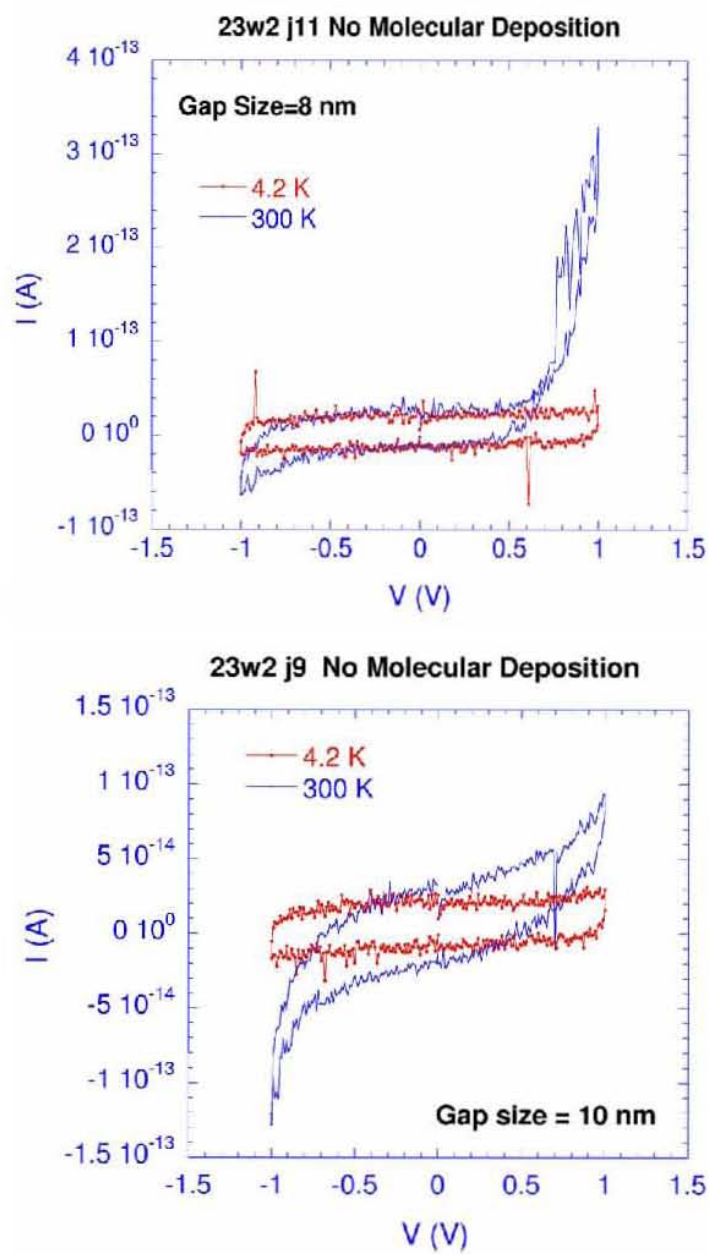
Figure 5.3: Electrical measurements of planar support structures at both room temperature and liquid helium temperatures.
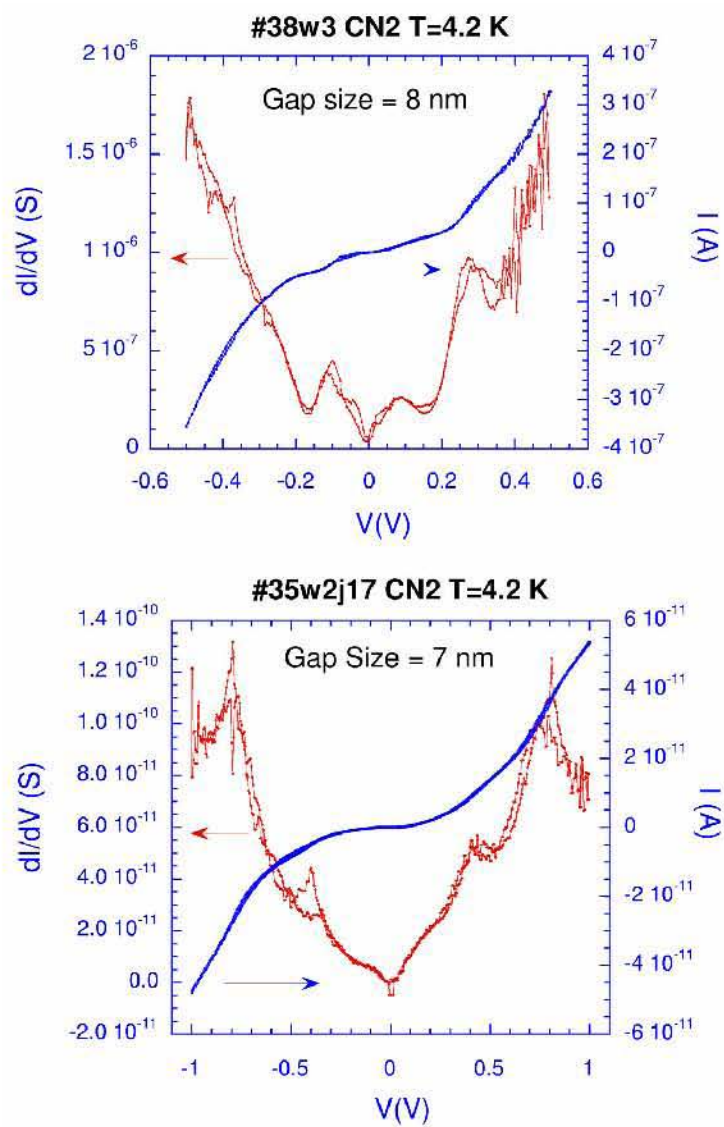
Figure 5.4: Electrical measurements of two nontrivial molecular junctions with gap sizes of 8 nm and 7 nm respectively. The origin of these data remains unknown due to the lack of further characterization techniques at the time.

Chapter 6

Molecular Junctions Formed by Electromigration

6.1 Introduction

Electromigration is the mass transport caused by gradual movement of the ions
in a conductor due to the momentum transfer between conducting electrons
and diffusing metal atoms. The process of electromigration is analogous to
the movement of small pebbles in a stream from one point to another as
a result of the water washing through the pebbles. This phenomenon has
been known for over decades as the major failure mode of interconnections
in microelectronic circuitry [157]. When a constriction area is developed in a
metal wire, the local current density is increased and the momenta of electrons
is transferred to nearby activated ions. This causes the ions to move away from
their original positions. When enough metal atoms had moved far away from
their original positions, a discontinuity or gap can be formed in the conducting
wire. Electromigration is enhanced under high current densities and the Joule
heating of the conductor, due to the temperature dependence of the atomic
drift. By carefully controlling the breaking environment consisted of current
density, temperature and circuitry, a nanometer sized gap can be developed in
the metal wire, which could be used to form single-molecule junctions.

The application of electromigration in fabricating interelectrode nanome-
ter gaps for electron transport measurement of a nanoscale system was first
demonstrated by Park *et al.* [158] in 1999. Two metallic electrodes with
nanometer separation were fabricated by passing a high electrical current
through a gold wire defined by electron-beam lithography and shadow evap-
oration, until the eventual breakage of the nanowire. The fabrication of
single-electron transistors was made from individual colloidal cadmium se-

lenide nanocrystals. Various research groups employed this method to make single-molecule transistors with different molecules to study various molecular electronic behaviors including Coulomb blockade, Kondo resonances, vibrational excitations and negative differential resistance. Other metal electrodes have been explored as well, including Au, Pt, Ni, *etc.* Table 6.1 summarizes the main experimental results to date on single molecular transistors using electromigration technique. As is obvious from this summary, different kinds of molecules have been intensively investigated, including conjugated organic molecules and molecules containing metal atoms.

In this chapter, we will first describe the fabrication procedure for continuous metal nanowires with gate electrodes. Each wire is used to form two electrodes with a nanometer-sized gap using the electromigration technique. The details of the electromigration process will be described in section 6.3. Two kinds of conjugated organic molecules are then studied: (i) simple oligo(phenylene ethylene) (OPE) chains (length = 2.2 nm), and (ii) OPE with a naphthalene diimide acceptor group (quasi-linear structures with a total length of 4.5 nm). Both molecules are capped with isocynide groups as the alligator clips to bind to the gold electrodes. Electrical measurements of these molecules will be discussed in section 6.4. The gate modulation and temperature dependence will be discussed at the end of this chapter.

6.2   Fabrication of Au-nanowire Junctions

The devices have been patterned on an oxidized silicon substrate using a combination of optical, electron-beam lithography and resist/lift-off process, as shown in Figure 6.1 a. Two types of gate oxides have been employed in our experiments: (1) a heavily doped silicon substrate as the gate electrode with a silicon oxide (hundreds of nanometers thick) as the gate oxide (wafer 8), and the gate voltage from -10 V to +10 V; (2) a thin layer of aluminum/aluminum oxide as the gate electrode/ gate oxide (wafers 10, 14, 17). The second configuration needs an additional step in its processing as follows: a 20 - 25 nm thick aluminum back gate has been deposited by dc-sputtering with a cryopumped vacuum system. The aluminum layer was then oxidized in 15 mTorr oxygen plasma for 10 - 15 minutes (see Figure 6.1 b). The thickness of the aluminum oxide is estimated to be 4 nm, which can withstand gate voltage up to 2.0 V with negligible leakage current in the pico-amp range. Table 6.2 summarizes the fabrication information of all the wafers fabricated for electromigration.

Two-layer resist PMMA/P(MMA-MAA) has been spun on the surface of silicon oxide or aluminum oxide and has been exposed to electron beam in the area that will later become nanowires, with a small discontinuous area

Molecule	Metal Electrode	Observation	References
C_{60}	Au	Vibrational excitations, including attachment modes, low temperature	[159]
C_{60}	Au	Kondo resonance, gateable; interplay between kondo and vibrational processes; NDR due to surface adsorbates	[165] [166]
C_{60}	Ni, Au	Kondo resonance in presence of ferromagnetic electrodes, not gateable	[167]
Co-terpyridal complexes	Au	Kondo resonance in strong coupling regime, no gating, low temperature	[160]
Divanadium compound	Au	Kondo resonance in strong coupling regime, gateable, low temperature	[161]
Rotaxane derivatives	Pt	Multiple accessible charge states, molecule-dependent conduction asymmetry, low temperature	[162]
C_{70}, C_{140}	Au	Internal vibrational modes	[163] [164]
Transition-metal complexes	Au	Inelastic cotunneling via vibrational levels (gate-modulated inelastic electron tunneling spectroscopy)	[168]
Ferrocene-oligophenylethynyl	Au	Resonant conduction approaching perfect transmission, low temperature, very limited gating	[169]
Oligo(phenylene-ethynylenes)	Au	Negative differential resistance, independent of molecule type, no gate dependence	[170]

Table 6.1: Summary of experimental results on single molecular transistors by electromigration methods [171].

Wafer	Planar Electrode	Gate	Gate Oxide	Au Etch
8	Au 15nm	Silicon	500 nm SiO_2	2∼4 sec
10	Au 15nm	Al 20nm	AlO_x 15mtorr×10min	2∼4 sec
14	Au 25nm	Al 20nm	AlO_x 15mtorr×15min	12 sec
17	Au 25nm	Al 20nm	AlO_x 15mtorr×10min	12 sec

Table 6.2: Summary of the fabrication information of all the wafers fabricated for electromigration.

in the middle (Figure 6.1 c). Due to the different dissolving speeds of the photo resists PMMA and P(MMA-MAA) during the development, we have a suspended PMMA layer with a hollow tunnel underneath in the MMA-MAA layer that will be used for a mask for subsequent angle evaporation.

First, the whole wafer has been tilted 15 degrees with respect to the direction of evaporation and 4 nm Cr has been evaporated under ultrahigh vacuum condition (see Figure 6.1 d) with deposition rate at 0.5 Å/sec. Cr is used to improve the adhesion between the gate oxide and gold nanowires. Then the wafer has been tilted 15 degrees in the opposite direction and 20 nm of Au was deposited without breaking the vacuum (see Figure 6.1 e) at $0.5 \sim 1.0$ Å/sec. Finally, the second gold layer (~ 60 nm) was evaporated at the same tilted angle as Cr ($+15^o$) on top of the first thin gold layer, forming a 100 nm constriction area for further breaking process at cryogenic temperature (Figure 6.1 f). The pressure during evaporation remains constant at $\sim 4 \times 10^{-7}$ torr. The three-step metal evaporation provides a clean interface between thin Au nanowires and aluminum or silicon gate oxide at the constriction area, which eliminates the possible complications caused by the adhesion layer since it is not known whether the adhesion layer will contribute to the inter-electrode conduction following the electromigration of Au nanowire.

The general deposition protocol was as follows. The device has been cleaned with acetone and isopropanol ultrasonically for $1 \sim 2$ minutes to remove any organic residues. Then the chip has been brought into an oxygen plasma cleaner for two minutes to further eliminate any organics left. The molecules were usually dissolved in toluene and deposited on to the wires right after the plasma cleaning. For molecular assembly, the chip has been soaked in dilute molecular solution (0.1 mg/mL of molecular compound in toluene) overnight. The sample has then been thoroughly rinsed with pure toluene, and completely dried under a steam of nitrogen flow. Other methods of molecular deposition have been also used, *e.g.*, putting a few droplets of dilute molecular solution on the substrate which was then gently dried in nitrogen flow. Both methods lead to similar break-junction results. The sample has been cooled
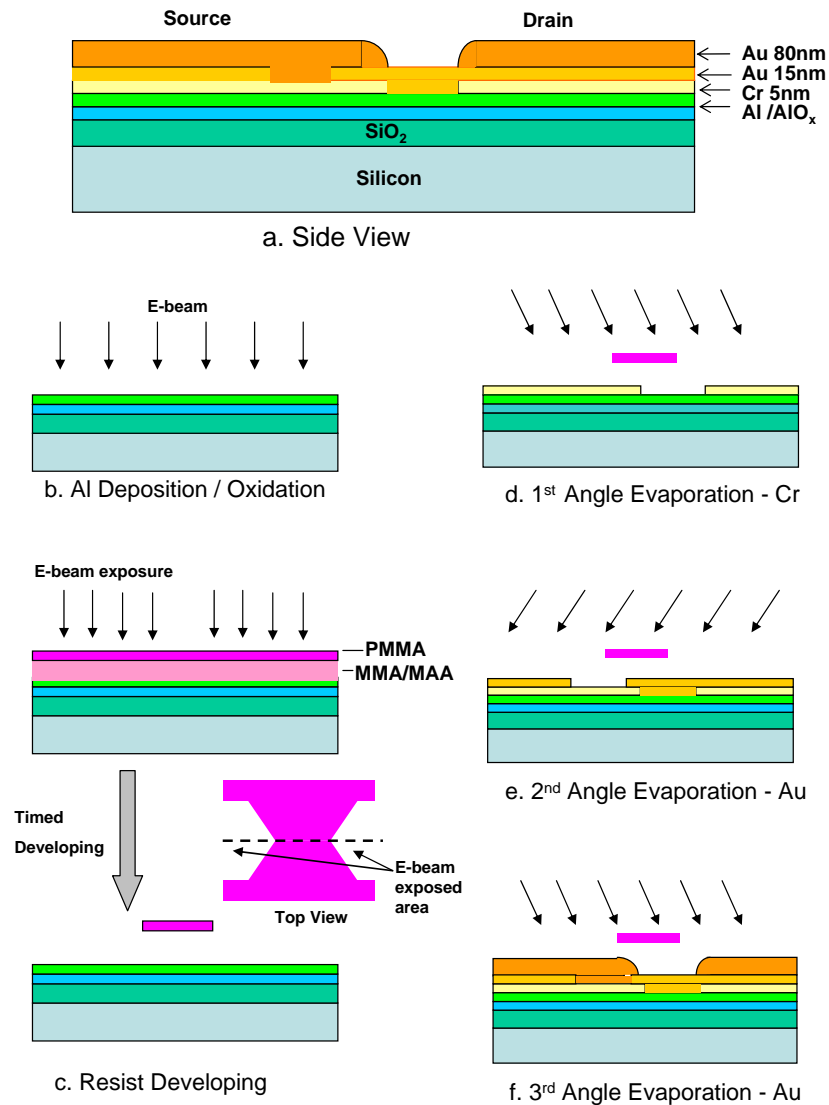
Figure 6.1: (a) Schematics of the cross-section of the gold nanowire junctions. The constriction area is about 100 nm wide and 15-20 nm thick, where nanometer gap will be formed after electromigration at 4.2K. (b) First deposition of aluminum layer of 20 nm and subsequent oxidation at room temperature. (c) Deposition and timed development of two-layer photo-resist PMMA/P(MMA/MAA). A suspended PMMA bridge will be used for a mask for subsequent angle evaporations. (d) $\sim$ (e) Three steps of angle evaporation of Cr, thin Au, and thick Au layers.

down to liquid helium temperature (4.2 K) and the gold nanowire has been broken via the electromigration process to create a nanometer-sized gap. For samples with heavily-doped silicon back-gate, 18 junctions are available on one chip (Figure 6.2 a). However, there are only 17 junctions available on the chip with aluminum back-gate. The additional pin is always connected to the aluminum gate, as shown in Figure 6.2 b.

6.3 Electromigration in Gold Nanowires

Usually the process of electromigration is performed under cryogenic conditions, by ramping up a dc voltage across the wire while monitoring the junction resistance. The breaking process is terminated when the resistance across the wires suddenly increases to very high values. By adjusting the concentration of molecular compound in the solution and carefully breaking the wire, one or a few molecules could be sitting right at the gap, bridging the two metallic electrodes to form a molecular junction. This is a rather statistical process and the yield of successful junctions is very important. Usually the yield of nanometer inter-electrode gaps is much lower for wire breaking at higher temperature than cryogenic temperature. There are two advantages for low temperature processes. First, the cryogenic temperature results in an effective ultrahigh vacuum environment, minimizing the risk of contamination of adsorbates on the electrode surface. Second, the configuration of the electrode surface is meta-stable immediately after breaking because of the limitation of surface reconstruction at low temperature. When the junctions are warmed up to room temperatures, the gap between the two electrode has been observed to change significantly, due to the rapid diffusion of gold atoms.

Figure 6.3 shows a representative current-time trace and the corresponding conductance of the gold nanowire during the breaking process, with the voltage ramping rate of 2 mV/s. The resistance of the device remains constant at about $40 \sim 50\ \Omega$ until the onset of breaking. This onset voltage V_b varies among different wafers, with values mostly grouped from 0.6 V to 0.8 V depending on individual fabrication condition. When voltage reaches above the onset or critical point at V_b, the conductance drops abruptly or through a few steps to the $\mu S \sim pS$ range. The electromigration process could be described through either two (1, 3) or three of the following steps (1 - 3) [172]: (1) at around 50 Ω, the mobility of gold atoms is increased by local heating by the passing high current density and start to migrate in the metallic neck; (2) in the intermediate resistance region close to the quantum value G_0 ($G_0 = 2e^2/h$), the conductance shows jumps and plateaus; (3) the nanogap is formed after the conductance is below G_0 where the tunneling regime is reached. For a
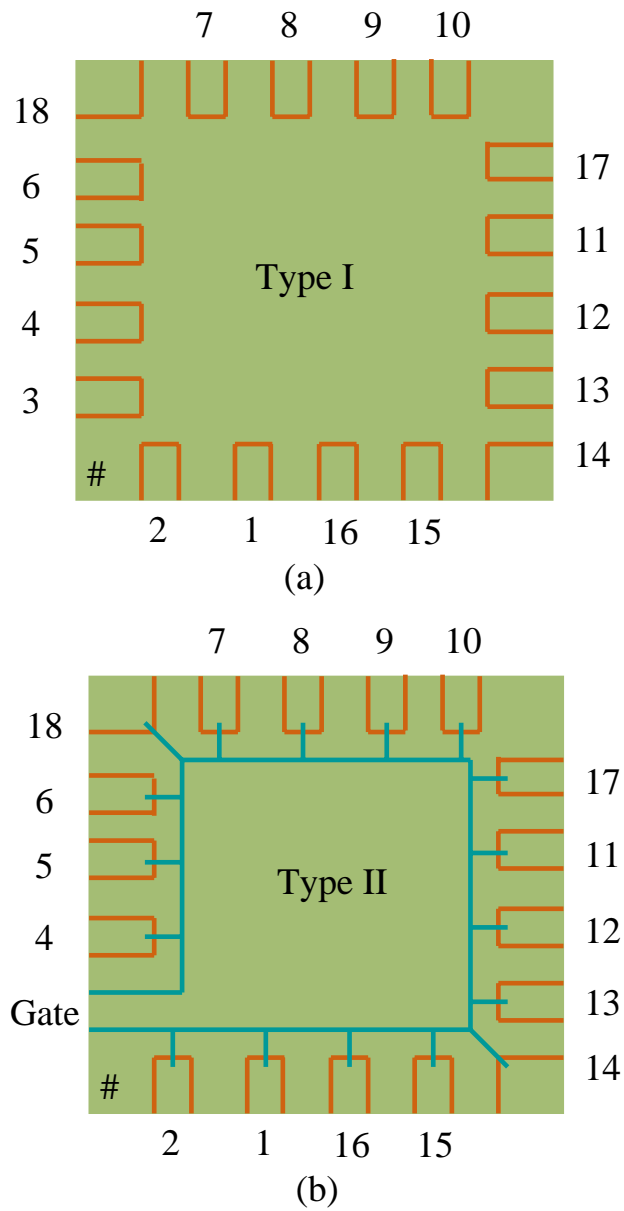
Figure 6.2: Schematics of wire pattern on a typical chip: (a). heavily doped silicon back gate (at the back of a chip) (b) thin aluminum as the back gate (blue line). Chip number is marked at the left bottom.
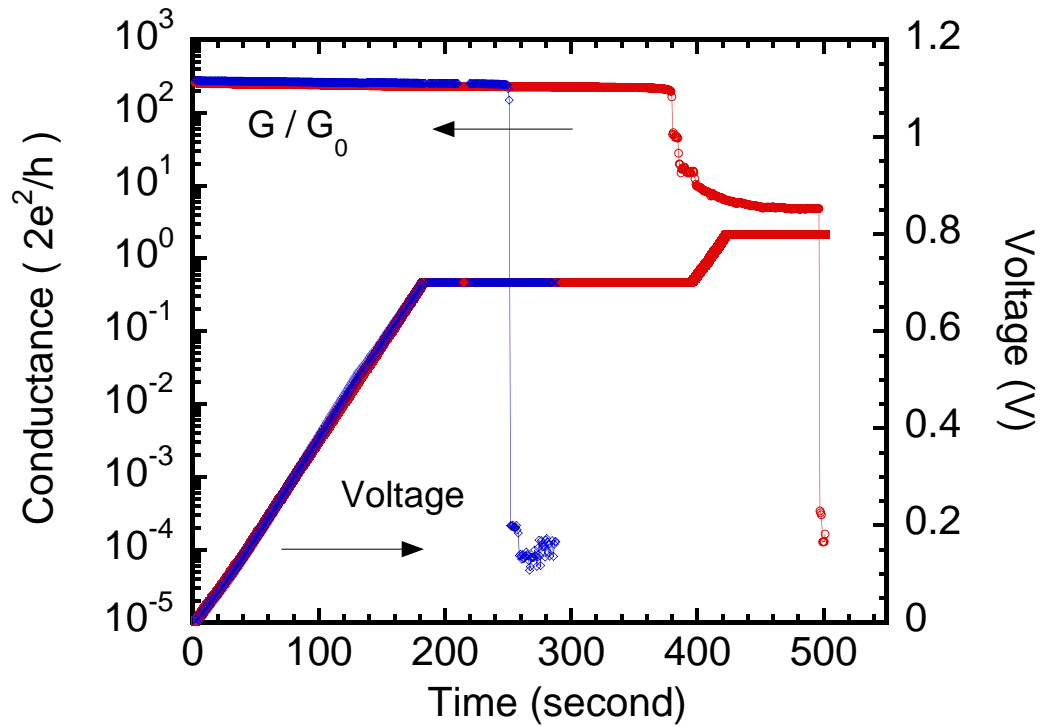
Figure 6.3: Two current/conductance - time traces are shown for a typical wire-breaking process. The voltage is ramped up slowly in steps of 2 mV/s. Trace 1 and 2 are selected from different junctions, representing two typical electromigration processes. The gap conductance between two gold electrode is much lower than G_0.

nanowire with length L and cross-section A, the relation between the breaking voltage and the critical current density j_b is as follows:

$$V_b = I_b R = j_b A * \rho L / A = j_b \rho L \qquad (6.1)$$

Here ρ is the resistivity of the nanowire material. Since the length of the nanowires is relatively constant, the breaking process in the nanowires is dominated by the current density. From the breaking current and the geometry of nanowires, we can estimate $j_b = I_b/A \sim 12$ mA/(15 nm $\times$ 150 nm) $\sim 5 \times 10^{12}$ A/m^2, which is similar to the value reported by Durkan *et al.* [176].

Figure 6.4 shows the scanning electron micrograph (SEM) of a metal electrode before and after electromigration. Both images were taken at room temperature, since we had no access to low-temperature atomic-scale imaging technique. Au is known to have large bulk and surface atomic diffusion and undergo annealing at room temperature. The SEM pictures cannot reveal the actual nanometer-scale gaps formed at 4.2 K because of the metal-surface reconstruction when the samples are warmed up to room temperature. The actual size of the gap formed at low temperature is expected to be substantially smaller than that of the "warm-up" gap. We have achieved ~ 5 nm separation at room temperature at best, estimated from the SEM images, not too much larger than the length of our molecules (2.2 nm and 4.5 nm). The picture shows that the location of the gap is not always in the middle of the wire.

6.4 Electrical Characterization

The electrical measurements have been carried out in situ right after electromigration at 4.2 K. Due to the stochastic nature of breaking process, every electrode pair breaks differently at atomic scale. The presence of the desired molecules at the size-matching nanogap is probabilistic and depends strongly on the initial surface coverage of the molecules. Ideally one or a few molecules with isocynide linker groups would bind with two electrodes and form a stable chemical bond between Au and -CN when the separation between two electrodes matches the length of the molecule. However, the coupling between the molecule and the metal electrodes are determined by the local environment of the junction region, which differs from sample to sample. It is very important to know whether the measured electrical properties belong to the molecule of interest or just artifacts from contaminates. We have used a statistical approach by measuring many samples to distinguish the features of single molecules from artifacts. Three types of samples have been investigated: (1) bare gold electrodes without any molecules; (2) junctions covered with long
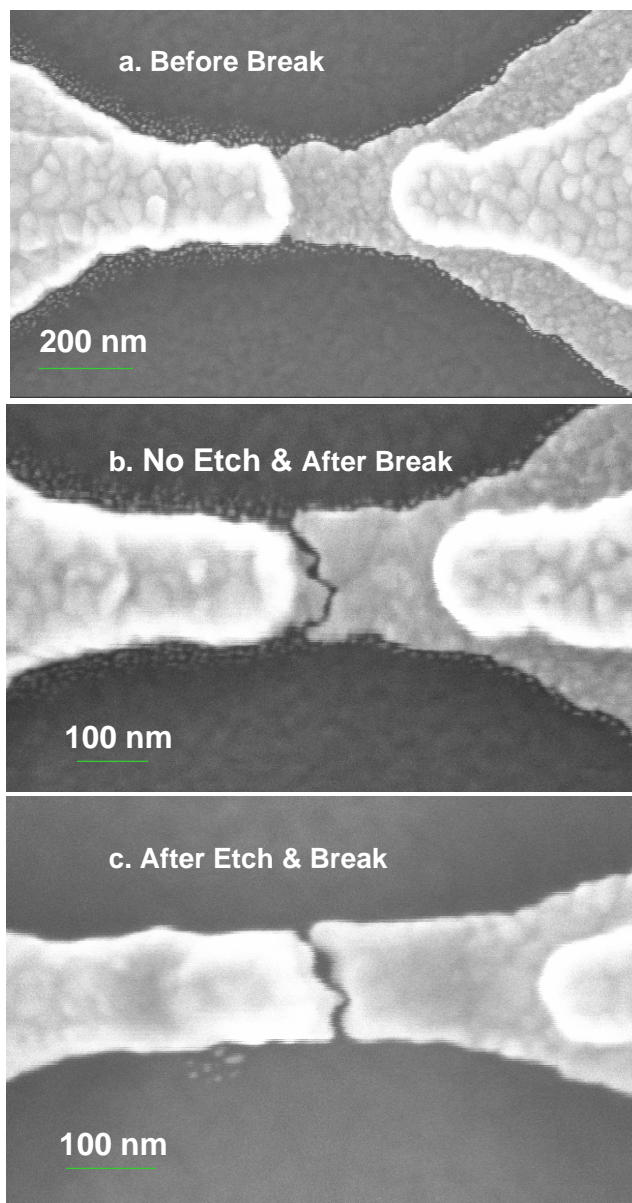
Figure 6.4: Scanning electron micrograph of a nanowire before and after the electromigration-induced breaking process. (a) Before the break: continuous Au wire of 100 nm wide. (b) After electromigration: small side Au particle are visible along the edge of a nanowire. (c) After electromigraion: small Au particles are removed by chemical etching. Both images taken at after the breaking clearly show a physical gap formed within the nanowires.

molecules with a naphthalene diimide acceptor group; (3) junctions covered with short molecules with OPE chain only.

6.4.1   Control Experiment - No Molecules

First we carried out the control experiments on bare Au electrodes without molecules. As Figure 6.4 shows, small gold grains of nanometer size are visible along the edges of gold electrodes. These are the by-products of the fabrication process. It is possible that these nanoparticles have been involved in the transport through the electromigrated junctions. For example, the Coulomb blockade effects have been observed even in the absence of the molecules [173], [174]. We have examined a total of 119 devices (wafer 8 & wafer 10) of such structures. As Figure 6.5 shows, 18% devices with high resistance within the range $G\Omega \sim 100$ $G\Omega$ show linear or tunneling-like current, suggesting nanometer-sized gap formed in gold nanowires. On the other end, there are 30% devices with high conductance close to G_0, indicating only a few atoms connecting the two metal electrodes. Most of the junctions in this range undergo the further breakage during the following $I-V$ sweeps. The resistance of 15% devices falls in the range of $M\Omega \sim 100$ $M\Omega$. Among them, we have observed two samples with Coulomb blockade features, probably due to the migration of small gold particles along the side of gold nanowires, or the unintentional formation of metal nanoparticles during the electromigration.

It was rather annoying to have small gold grains along the edge of the electrodes. To study the transport through molecules, we need a cleaner surface, *i.e.*, to get rid of these gold nanoparticles. One way to remove them is by wet etching. The gold etchant is made from the mixture of iodine, potassium iodide and deionized water. The concentration ratio was $I_2 : KI : DI - H_2O = 1 : 4 : 1000$. We first tried to soak the existing samples in the dilute gold etchant for a short time, from 2 seconds to 4 seconds. We have observed that as a result most of the wires have been broken even before the start of electromigration. The yield of continuous wires available for further electromigration after wet-etch was below 30%. There are three possible reasons for this low yield: (1) the etching time was too short to provide uniform etching; (2) the sample was broken by electrostatic discharge; (3) the first gold layer was too thin and could be partially etched away even in the mild gold etchant.

In order to increase the yield of good samples, of which the constriction area is both continuous and with no side gold nanoparticles, we have fabricated a thicker Au first layer of about 25 nm, which is 5 ~10 nm thicker than that of the older samples. The thickness of the second Au layer remains at 60 nm. By soaking the wafer in the dilute gold etchant for a longer time (*e.g.*, 12 seconds),

we have obtained samples with both continuous wire with no or little side-dots and a greatly improved high yield $> 80\%$ (Figure 6.4 c).

From the histogram of junction resistances(R_{br}) right after wire-breaking, we could see immediately the difference between the structures with and without the grains. For samples without post-etch treatment, which have been cleaned only under O_2 plasma, R_{br} is evenly distributed from KΩ all the way up to > 100 GΩ (Figure 6.5). However, for samples with post-etch treatment, the resistance of about 27% junctions falls into G$\Omega \sim 100$GΩ range and 60% junctions with > 100 GΩ resistance (Figure 6.6).

With the removal of side gold grains by mild chemical etching, we have obtained clean support structures for further investigation of interesting molecules. We first measured electrical current as a function of bias voltage through tunneling gap formed between bare gold nanowires. The current-voltage characteristics can be grouped into three categories according to the value of their resistance:

(1) R_{br} : K$\Omega \sim$ MΩ. Linear $I - V$ curves have been observed in most junctions at this range. $I - V$ characteristics is not stable during the voltage sweep for some samples and they are easily broken to higher resistance, especially at negative voltage (Figure 6.7 a. b.).

(2) R_{br} : G$\Omega \sim 100$ GΩ. Linear or near-linear $I - V$ curves have been observed for $\sim 25\%$ of junctions (Figure 6.7 c). This is probably due to tunneling through the vacuum gap between the two electrodes. The gap size is estimated to be below a few nanometers. Boomerang shaped $I - V$ has also been found in samples with junction resistance in this range, indicating local asymmetry after breaking (Figure 6.7 d). The gap is quite stable in liquid helium temperatures. However, two junctions still show the current-voltage characteristics resembling that of Coulomb blockade with suppressed conductance near zero voltages (Figure 6.7 e). This is another confirmation of our earlier assumption that metal nanoclusters do sometimes form between two gold electrodes during electromigration process.

(3) $R_{\mathrm{br}} > 100$ GΩ: The source-drain current is in the same order of magnitude for the leakage current below pA, suggesting the formed gap is too wide to be measured (Figure 6.7 f).

In conclusion, the junction quality has greatly been improved by successfully removing the small gold grains with the chemical-etching method, resulting in higher yield of nanometer sized gaps. The molecules of interest can then be added for further investigation.
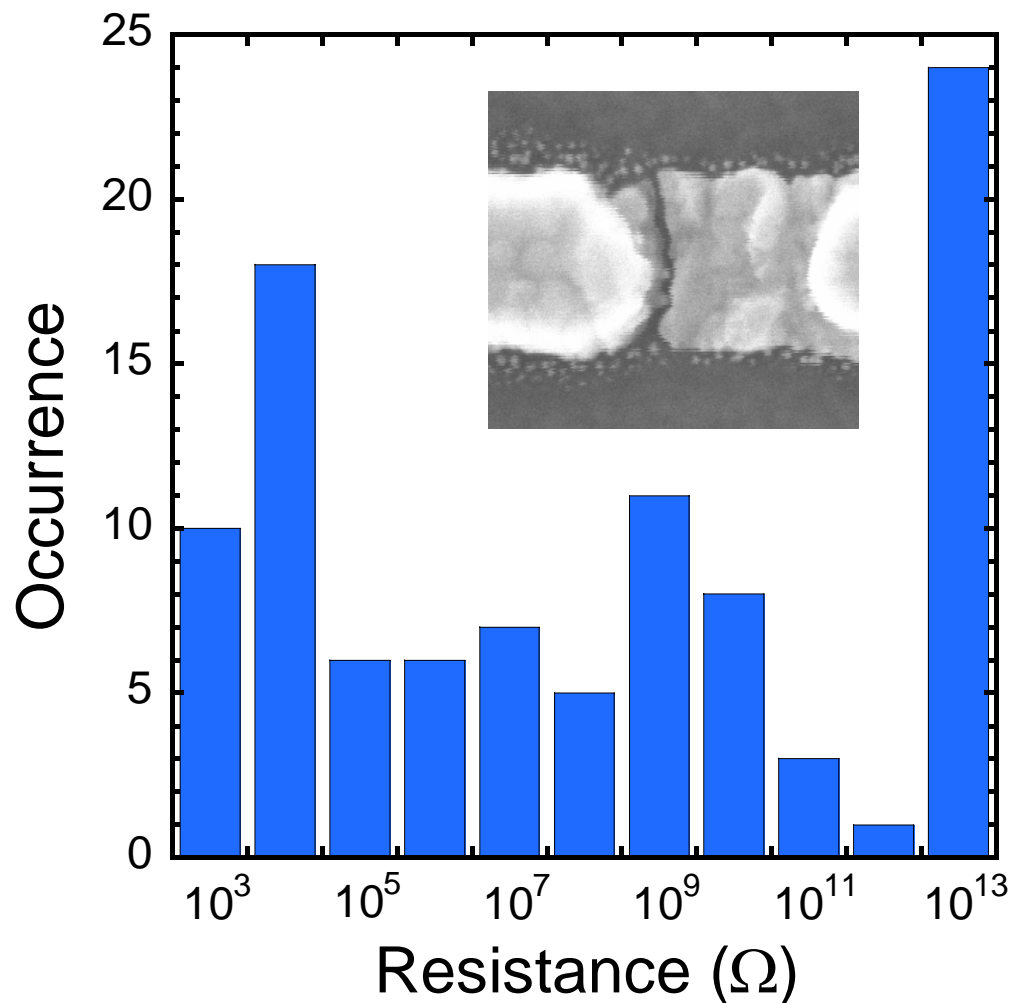
Figure 6.5: Histogram of resistance between the two metal electrodes right after the electromigraion. The samples are only cleaned under oxygen plasma for 2 minutes without any further treatment. The insertion shows the typical gap formed by this method. The gap size is about 5 nm, which is already close to the resolution of the scanning electron microscope (1 nm). Small gold grains are visible along the edges of the gold electrodes.
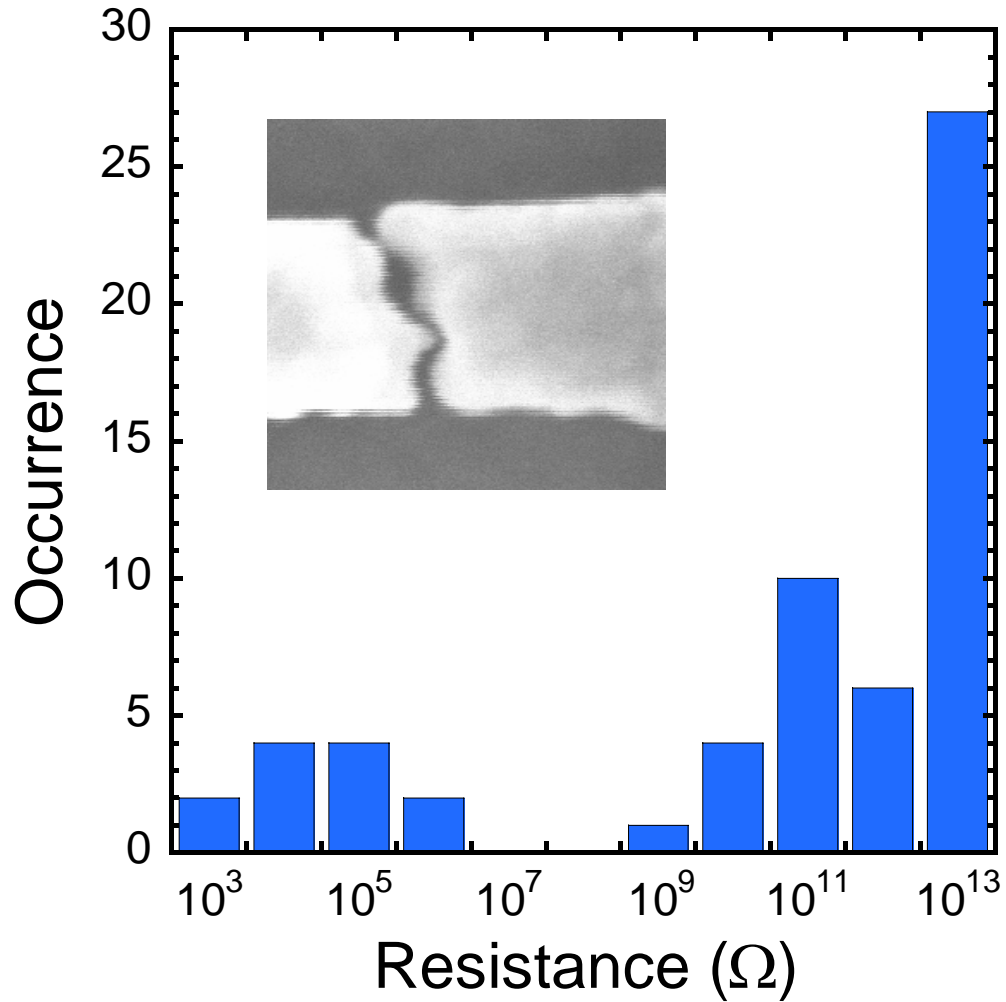
Figure 6.6: Histogram of resistances between the two metal electrodes right after the electromigration. The samples are cleaned in oxygen plasma for 2 minutes and chemically etched by very dilute gold etchant ($I_2 : KI : DI - H_2O = 1 : 4 : 1000$). The insertion shows the SEM picture of the formed nanometer gap. It is clearly seen that small gold grains which had used to sit on the edge of the gold electrodes have been removed.
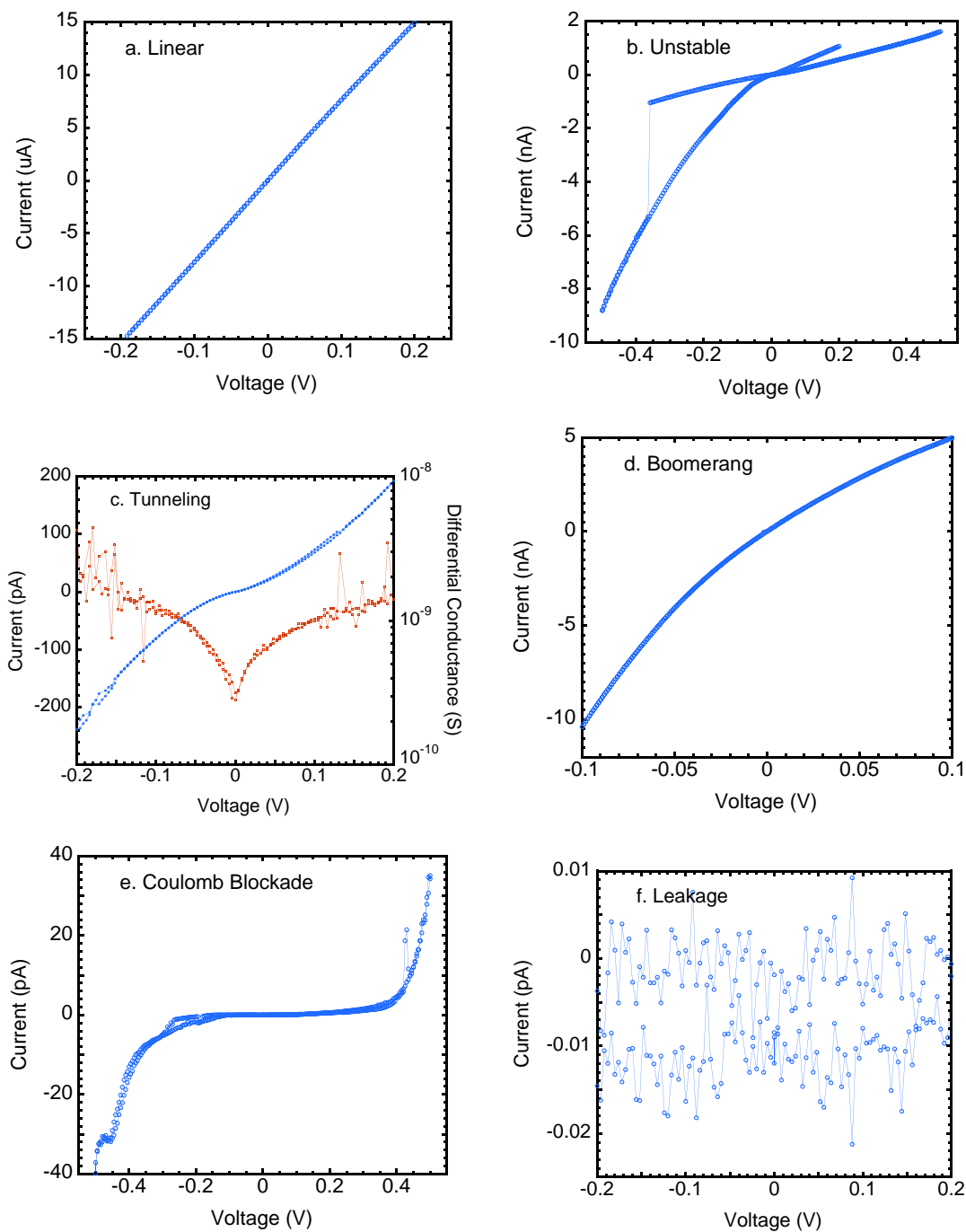
Figure 6.7: $I-V$ and $G-V$ plots of nanogaps formed after breaking are shown for control samples without molecules: a. linear; b. unstable; c. tunneling; d. asymmetric; e. Coulomb-blockade-like; f. negligible current (below 0.01 pA).

6.4.2 Oligo(phenylene-ehtynylene)s with Naphthalenedi- imide Group

We first investigated the single-electron-transistor like molecules with a naph- thalene diimide acceptor in the middle. Isocyanide groups were used as alliga- tor clips to bond with the gold electrodes. The schematics of the molecule is shown in Figure 4.4 II. The length of this molecule is about 4.5 nm, selected to match the size of possible gap created by electromigration. Molecules have been self-assembled on the gold wires before electromigration processing.

We have examined a total of 163 devices (15 chips) including 94 samples made of the older non-etched support structures (wafer 8) and 69 samples made of the post-etched support structures (wafer 10 & 14). The molecules have been either self-assembled for over 20 hours or deposited as a few droplets at room temperature with different concentrations (0.1 mg/mL & 1 mg/mL). The samples have been carried down to liquid helium immediately after the de- position for break-junction and electrical measurements. From the histogram of junction resistances right after breaking (Figure 6.8), we have observed that more than 60% of samples have low resistance KΩ and ∼ 20% devices show MΩ resistance. The distribution of the junction resistance is similar for both support structures (with & without post-etch) that most junctions sit in either low-R (KΩ ∼ MΩ) or very high-R (over 100 GΩ) regions. Since the current- voltage characteristics varied in all resistance range, we cannot simply classify them according to their resistance values (as in previous section). In general, we grouped the samples based on their $I - V$ shape into the following four categories.

(1) Linear or slightly non-linear $I - V$:

Figure 6.9a shows the typical $I - V$ with linear or slightly linear shape in 70 samples (including 45 samples from the old no-etch structures and 25 samples from the new etched structures.) Junction resistance varies from KΩ to GΩ while the majority of the samples have ∼ KΩ resistance. One explanation for the resulting low resistance of the devices would be that the thin constriction area has not been fully broken and was still connected by a few atoms (or metallic bridge). Due to the limitation of the current imaging technique at low temperature, we could not directly observe the formation of the nanometer gap. However, the above hypothesis could be partially checked by SEM imaging, which allowed us to probe the nanometer gap subjected to soft annealing at room temperature. The SEM pictures of some samples indeed shows the remaining bridge or particles connecting two gold electrodes (see insert inFigure 6.9a). By plotting the differential conductance of several devices together, we observe that they coincide with each other up to a small factor. Comparing to the control samples with no molecules, their $I - V$
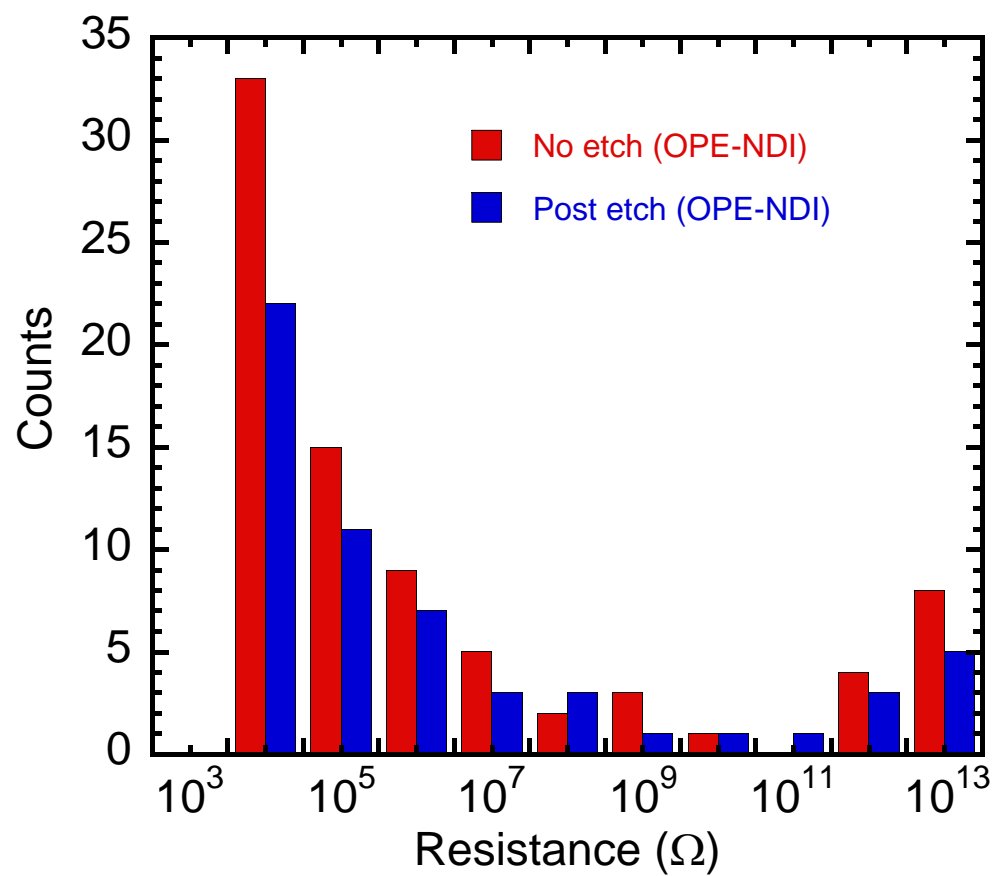
Figure 6.8: Histogram of R_{br} for OPE-NDI molecular devices. Red: structures without post-etch treatment. (The small gold particles are visible along the edge of nanowires); Blue: after post-etch treatment. (The small gold particles are removed by dilute chemical etchant.)

characteristics were also similar (Figure 6.9b). Both facts indicate that the resulting high conductance is partly due to incomplete electromigration.

For highly resistive devices, it is also possible that there were many molecules in parallel connecting to the metal electrodes, or they were just artifacts from the local environment. From current-voltage data at low temperature alone, it is not easy to tell which one is the case. To be simple, we generally discard devices in this class and no further investigation is pursued.

It is worth pointing out that there are 14 (additional) samples (5 - no etch, 9 - etched) which were unstable during the voltage ramp cycle (from -200 meV to 200 meV) and easily broken to higher resistance. This could be explained as the further migration of the few connecting atoms in the break-junction process. In order to eliminate the possibility of the remaining metallic bridge between the source and drain electrodes, it is important to break the junction fully beyond the quantum conductance regime.

(2) Nonlinear tunneling $I - V$:

We have observed 32 out of 163 samples with nonlinear tunneling-like $I - V$ with junction resistance varying from 10 K$\Omega \sim$ GΩ. The conductance of all the samples were obtained by numerically differentiating the current-voltage data. Figure 6.10 shows the typical $I - V$ shape in this category with or without the small resonance peaks near the zero-bias range. Simple tunneling model could be used to fit the data without small conductance peaks (24 samples). The natural interpretation is that no molecule of interest was located at the point of the closest interelectrode separation. The observed tunneling current originates from electrons tunneling through the vacuum gap between the two nanometer-separated gold electrodes. For the rest 8 samples, small conductance peaks around the zero voltages have been observed. It is hard to tell the origin of nonlinearities from the $I - V$ curves alone. It could be caused by desired molecules, unintended contaminants or adsorbates, or unintentional produced metal nanoparticles as mentioned earlier.

(3) Strongly nonlinear $I-V$ with suppressed zero conductance and current steps:

This group accounts for roughly 10% of the initial 163 devices. These are the devices of the most interest. Figure 6.11 shows the typical $I - V$ measured at liquid helium temperature. The current was suppressed near the zero voltage with threshold voltage between 30 mV to 200 mV. The threshold voltage depends on the initial charging condition of the molecular junctions. In order to distinguish between single molecular devices and artifacts, gate modulation (the third electrode) is essential. Gate potential could shift the molecular orbital level up or down and will change the current-voltage characteristics correspondingly. However, due to the unstable local environment and possible
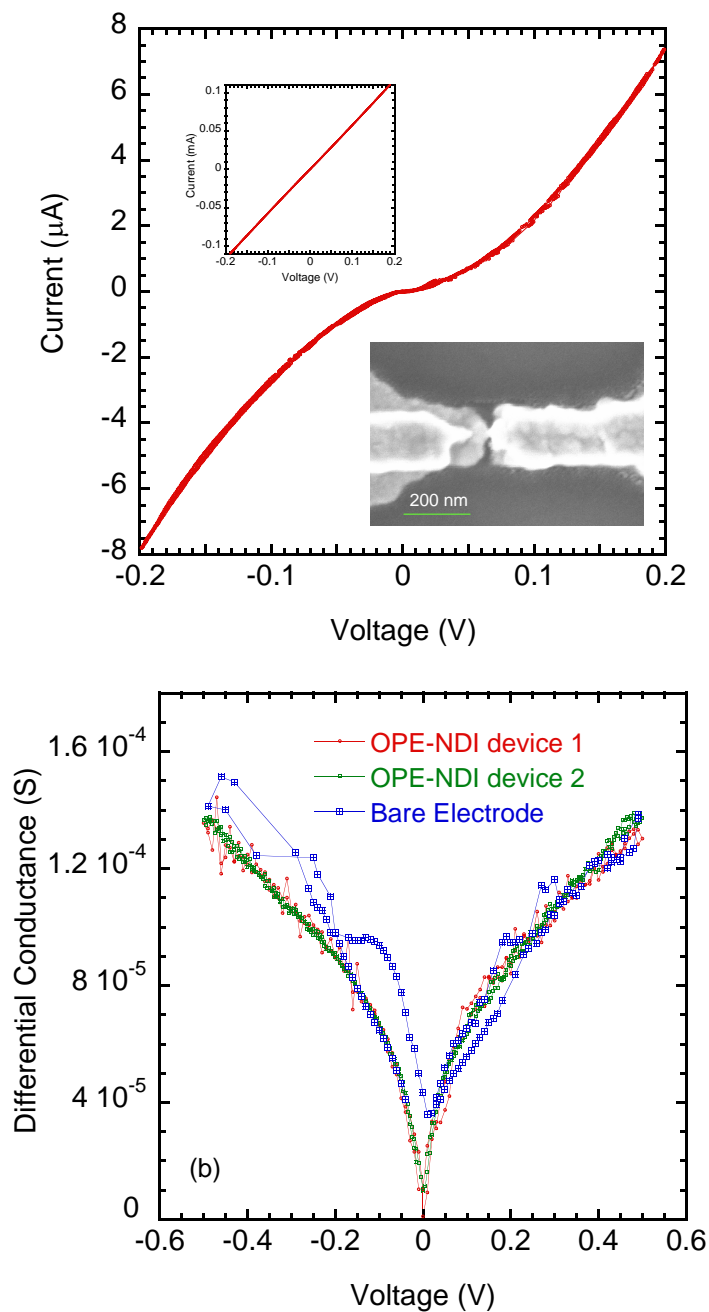
Figure 6.9: Linear-type $I-V$ curves: (a) two samples with different resistance ($M\Omega$ to $K\Omega$) have linear or slightly linear $I-V$ curves. Insert: an SEM image shows the two Au electrode are connected by a few gold atoms. (b) Differential conductance traces of three junctions (2 molecular devices and 1 control sample) virtually coincide.
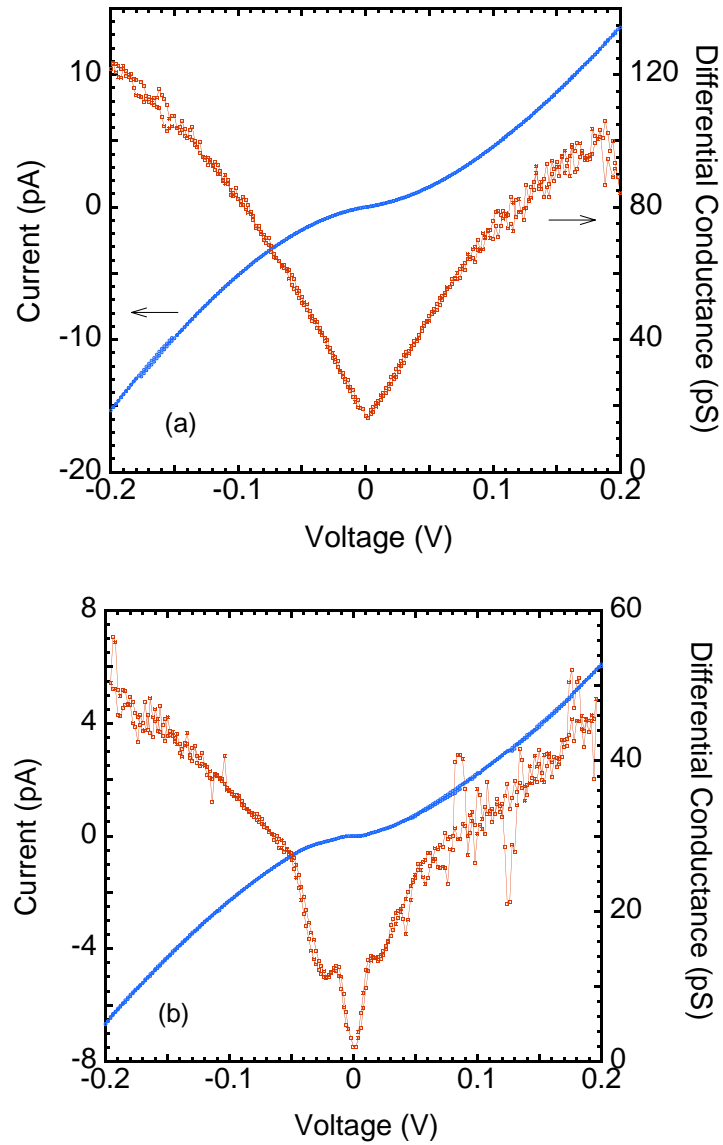
Figure 6.10: Nonlinear $I - V$ plots are shown for two typical junctions: (a) tunneling (b) small dI/dV peaks around the zero bias voltage

conformational change of molecules, the measured $I - V - V_G$ characteristics in our experiments was too noisy for these junctions to obtain any valuable information. Even under the same condition for the exactly same device, the $I - V$ traces changed from time to time. Since the tunneling properties of molecular junction not only depends on the molecules themselves, but also highly on the local contact environment, the molecules could sit in the middle of interelectrode gap, or be bonded to one or two Au electrodes. Thus the resulting $I - V$ characteristics could be symmetric or asymmetric.

At last, 15% of initial devices showed no measurable interelectrode conductance at voltage bias up to 0.5 V $\sim$ 1.0 V. These electrode sets have often been found to have wide gaps beyond the length of the molecules.

In summary, we have studied electromigrated samples with the complicated SET-like OPE-NDI molecules statistically and Coulomb-blockade-like $I - V$ curves have been observed for about 10% devices. However, the current trace is not stable. The molecules might be only weakly connected with the metal electrodes. Any tiny change of local charge environment would cause a big shift / change in the $I - V$ curves. Since the molecule is relatively long, possible conformational change, such as rotation or twisting, could affect the tunneling current too. In the next section, we will discuss how gate would affect the junction performance in detail. We should keep in mind that the plot of gate dependence could be very noisy as well.

6.4.3 Oligo(phenylene-ethynylene) Chains

We have investigated a simpler and shorter molecule with only oligo(phenylene ethynylene) bridges. The schematics of the molecule is shown in Figure 4.4I with $n = 1$. The molecular length is estimated to be 2.2 nm, selected to match the size of the electromigration formed nanogap. The OPE molecules have been widely studied for their possible usage as molecular wires, as well as active electronic components such as switches and memory elements (Chapter 4.4.2).

Similar to OPE-NDI molecules, we have examined a total of 114 devices (from 12 chips), all from wafer 14 & wafer 17 (new support structures after chemical etching treatments). Figure 6.12 shows the histogram of all the samples resistances right after breaking. Although about 50% of the initial devices showed no measurable current ($<$0.1 pA), a great number of junctions (more than 25%) have been broken into the GΩ range. In addition, only 6% devices showed linear or near-linear $I - V$. Compared to OPE-NDI devices, the yield of interesting devices has greatly been increased, partly due to the improvement of (the 3-step) electromigration procedures and the clean post-etched support structures. Table 6.3 summarizes the detailed information of $I - V$
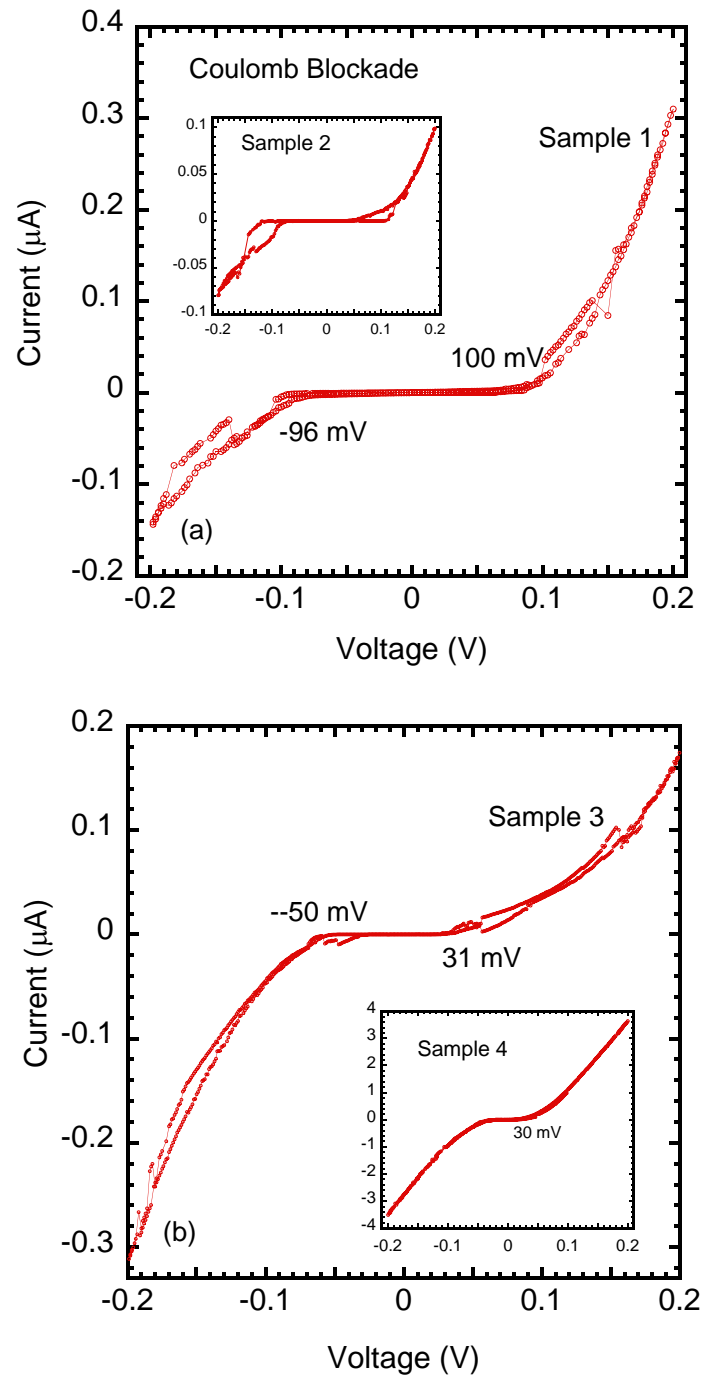
Figure 6.11: Strongly nonlinear $I - V$ plots are shown for four samples. The current is suppressed near the zero bias voltage for all devices. The threshold voltage varies from 30 mV to above 100 mV. Loops are observed at the onset of tunneling.
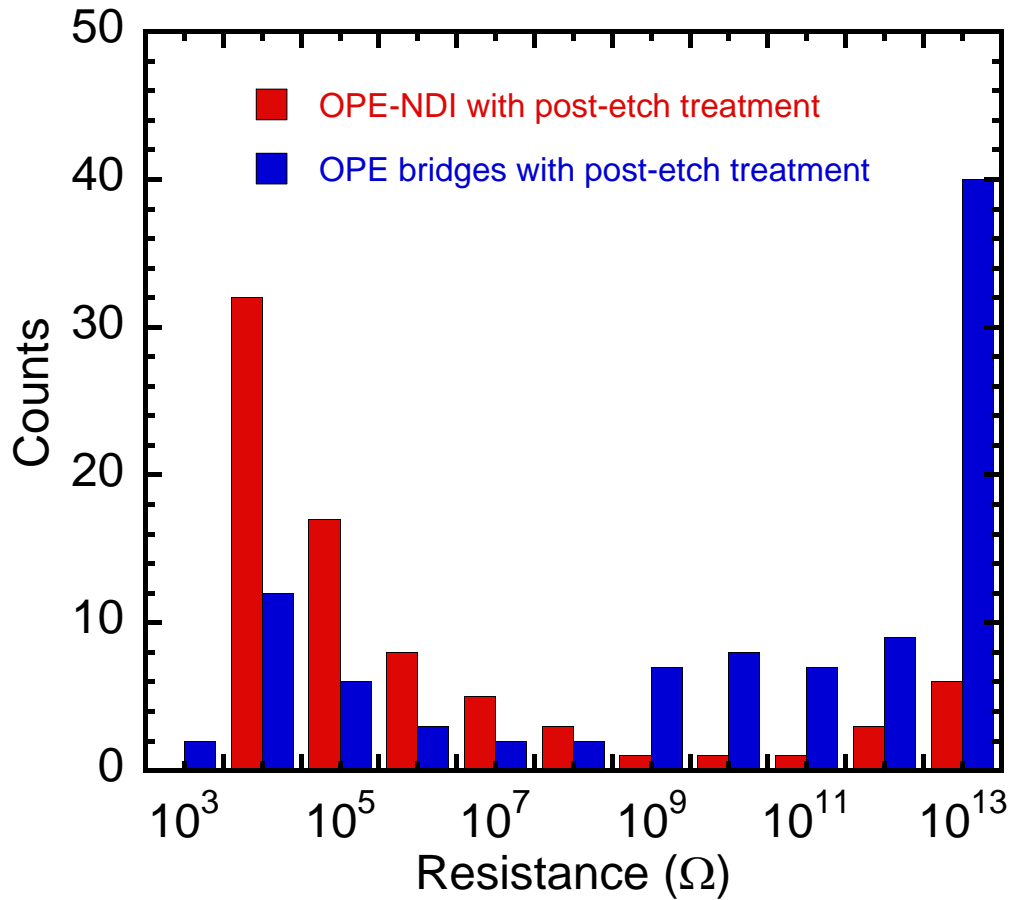
Figure 6.12: Histogram of R_{br} for OPE and OPE-NDI molecular devices are shown. We count only structures that undergo post chemical etching. A great number of OPE junctions have been broken into GΩ that are of most interest.

characteristics based on the classification described in the previous section.

We have discussed the current-voltage characteristics in class I, IV and V. Most of them are not related to the properties of molecules. Here we focus on samples particularly with nonlinear $I-V$ curves in class II and III: (i) strongly asymmetric $I-V$ with current steps, and (ii) strongly suppressed current near small voltages resembling the Coulomb blockade with additional current steps. Figure 6.13a shows the current I, differential conductance dI/dV as a function of the source-drain bias V for a typical OPE device ($R_{br} = 60$ MΩ) at liquid helium temperature. Several measurements at different time intervals (> 24 hours) were shown as an insert to track the possible conformational changes over this period. We have observed a diode-like current-voltage behavior for all

IV Characteristics		OPE-NDI			OPE n=1	
		No Etch	Etch	total %	Etch	%
I. Linear	Stable	45	25	44%	7	6%
	Unstable	5	9	9%	0	0
II. Nonlinear	no peak	17	7	15%	2	2%
	Small peak	4	4	5%	10	9%
III. Nontrival	CB	8	8	10%	19	16%
IV. Leakage	$I_{DS} \sim$ pA	12	12	15%	58	50%
V. Anormaly		2	2	2%	3	3%

Table 6.3: Summary of low-temperature $I - V$ characteristics of all electromigrated junctions. Each category of $I - V$ displays the number of junctions in this range, as well as the percentage rate.

the measurements taken at 4.2 K. However, its zero conductance was increased by about one order of magnitude from 2 pS to 24 pS, indicating minor changes in the local charge environment within the vicinity of the molecules. The current steps became more evident with strong differential conductance peaks at 63 mV, 104 mV and 170 mV, as well as two weak peaks at -65 mV and -125 mV respectively, with the period of about 60 mV. Since the OPE molecules are symmetric, the observed strong asymmetry could arise from the different local contact environments at each terminal of the molecule. When the molecules have been self-assembled onto the continuous gold electrodes, one isocynide group has strongly been attached to the gold electrodes by chemical bonding. After the device has been made by electromigration at liquid helium temperature, the other end of the molecule has been either weakly bonded or only physically attached to the gold electrode, resulting the diode-like current. Two other samples with similar asymmetric $I - V$ curves are shown below in Figure 6.13b, with one or more conductance peaks. Their break-resistance varies from 1 pS to 10 μS.

Figure 6.14 a. shows the current-voltage characteristics for one selected device whose behavior resembles the Coulomb Blockade with additional current steps. Different from previous samples, the current was quite symmetric on both positive and negative voltage ranges with conductance peaks at -530 mV, -290 mV, 180 mV, 430 mV and 520 mV. This is because the contact between the molecule and the electrodes is poor, resulting the formation of two tunnel barriers between the molecule and electrodes. Three other samples are also shown with resistances from MΩ to 10 GΩ and threshold voltages from 40 mV to 380 mV. For some devices, the current was suppressed at small voltages but very unstable at higher voltages with loops/hysterisis. Our experience
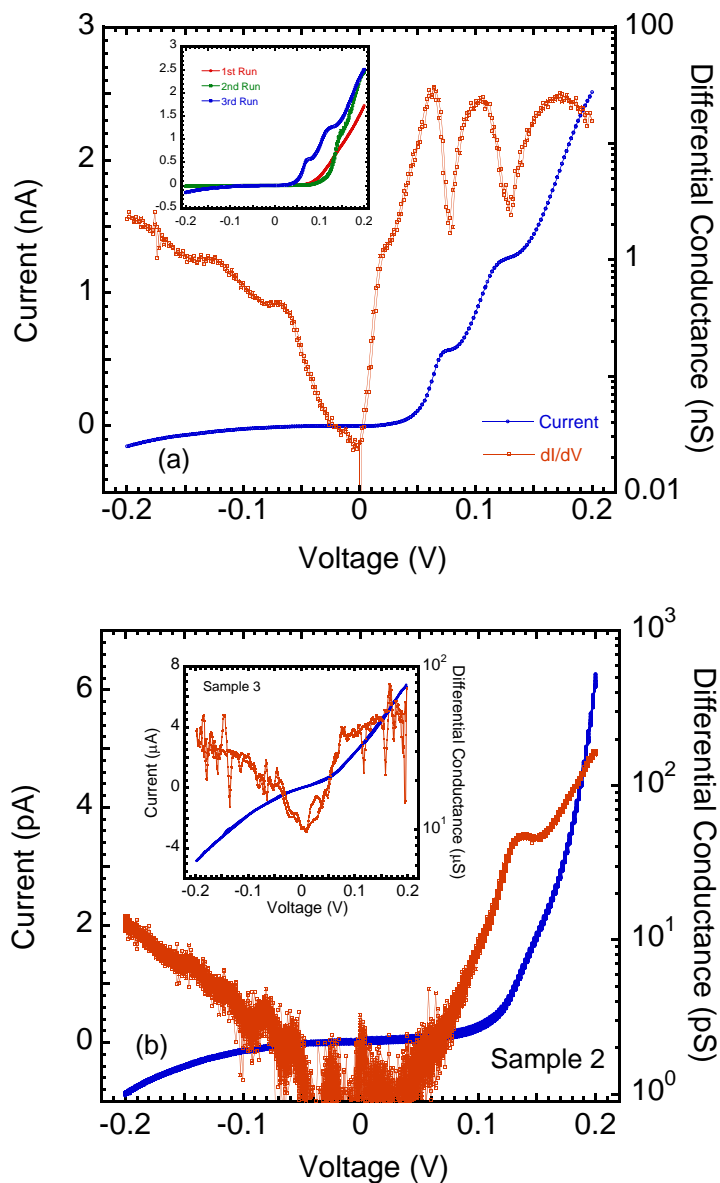
Figure 6.13: Strongly nonlinear $I-V$ plots are shown for three samples. (a) Strongly asymmetric $I-V$ curves with several differential conductance peaks. The insert shows several measurements for the same junction at different time intervals. (b) Two other samples with similar $I-V$ and $G-V$ characteristics.

shows that the application of high source-drain voltage (0.5 V to 1.0 V, which translates into an electric field of $\sim 10^6$ V/cm) often drastically changed the resistance of the system and occasionally destroyed the devices. The observed current steps are absent in tunnel $I - V$ of a simple tunnel junction with no molecules. Hence, these features indicate the incorporation of a molecule into the gap. By grouping all the voltage levels at the conductance peaks for all available devices, we have observed certain levels at an interval of approximately 60 mV as shown in Figure 6.15. The current steps are the result of the charging energy and discrete quantum levels of the OPE molecules.

It is interesting to notice that these device yields (among classes I to V described in Table 6.3 above) are essentially similar in our investigations for both molecules: SET-like and chain-like OPEs. They are also comparable to the results reported by other groups ([159] - [161], [163], [164], [167]). In contrast to the control samples that have been fabricated without molecules, the yield of strongly non-linear $I - V$ curves is much higher for molecular devices (1.6% vs. $> 10\%$). This suggests that a significant fraction of nonlinear $I - V$ curves, especially with current steps and gaps, that have been observed in molecular devices, are most possibly due to the presence of the molecules. The remaining non-linear $I - V$ signatures could be due to the existence of metal nano-particles or unintended adsorbates. It is very important to distinguish between the candidate single-molecule devices, and artifacts within the strongly non-linear $I - V$ groups.

6.5   Effect of Gate Modulation

Single-molecule transistor (SMT) has three electrodes: source(S), drain(D) and gate(G), while the molecules are connected with source and drain electrodes and separated by a thin gate oxide from the gate electrode. Control of molecular conductance by this third electrode is essential for a thorough study of transport in molecular junctions. The gate electrode allows us to modify the potential of the molecular orbitals electrostatically independent of bias voltages.

As described in the previous chapter, the extent to which the molecular levels can be shifted up and down is controlled by the gate coupling parameter. This parameter is related to the gain of the device which equals to the ratio of the gate capacitance to the total capacitance of the island (C_G/C). In an experiment, the gate coupling parameter needs to be as large as possible in order to access different charge states of the molecules. Factors that affect the gate coupling include the device geometry, the electrode separation (the length of the molecule) and the break-through of the gate oxide. Calculations
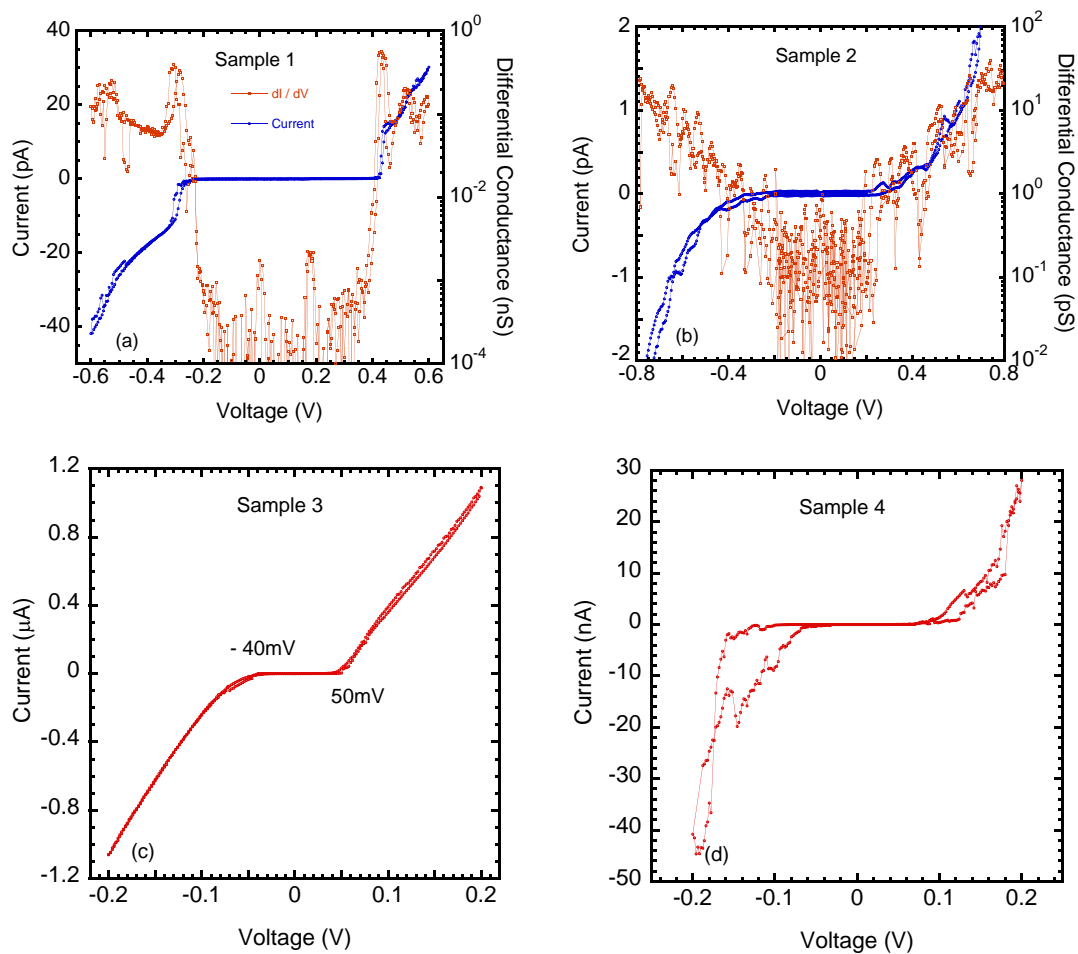
Figure 6.14: $I-V$ or $G-V$ plots of four OPE devices are shown. Current is strongly suppressed around zero bias voltage. The gap (V_{th}) varies from 40 mV to above 380 mV. The current steps have also been observed beyond the Coulomb blockade region, suggesting the presence of bridging molecules.
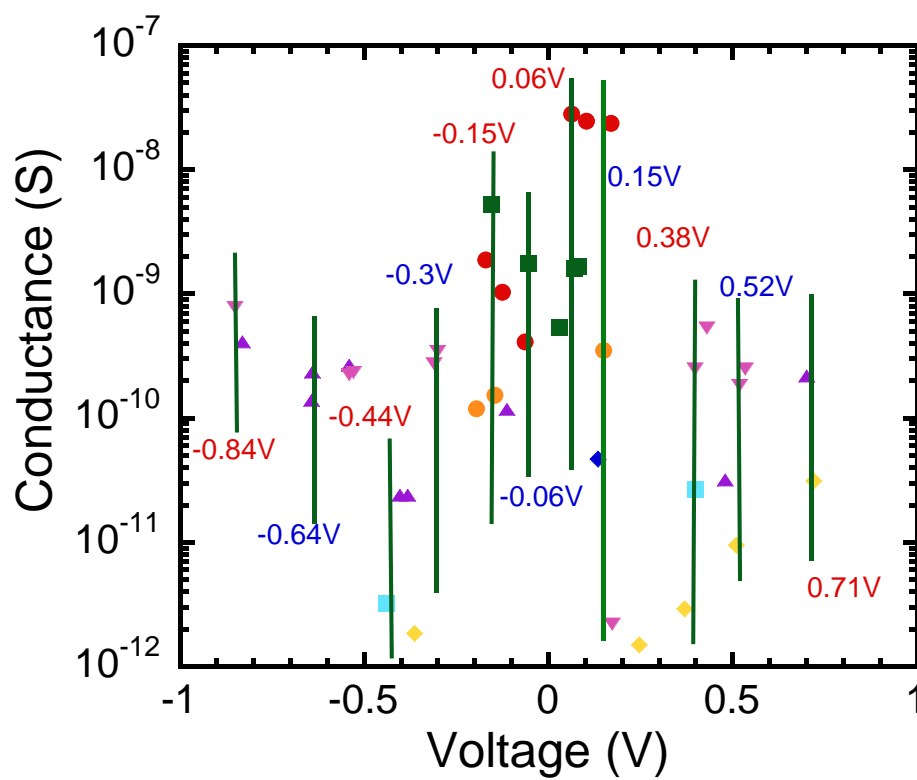
Figure 6.15: Plot of conductance peaks and their corresponding voltage levels for all available OPE-devices. Certain grouping levels are shown as vertical lines.

show that the gate-coupling factor is 100 times smaller for a silicon gate with thick oxide than that for an aluminum gate with thin oxide layers [175].

We have carried out current-voltage measurements for interesting devices under different gate voltages. The gate bias has been applied to the bottom aluminum layer underneath the gap. The leakage current through gate oxide is below pA up to 2.0 V. We usually limit the source-drain voltage to be below 0.5 V for device stability. Two methods of gate modulations have been used: (1) I is measured at fixed gate voltage V_G while changing V. (2) I is measured at fixed source-drain voltage V while varying the gate voltage V_G. Our experience tells that the two methods virtually gave the same result of gate effect. We will mainly focus on the first method.

We have carried out gate-dependent current measurements for bare electrodes, molecular junctions with OPE bridges and OPE-NDI units, especially focusing on samples with strong nonlinear $I - V$ curves. Gate voltages have been first set at the negative range, followed by the positive values up to 2.0 V or 10.0 V, depending on the back-gate metals (aluminum or heavily-doped silicon). The initial charge environment is essential in determining the corresponding $I - V$ characteristics. According to the shape of the commonly used $I - V - V_G$ diagram, we now discuss different behaviors of various junctions under gate modulation.

No or Weakly Gate Effect

Figure 6.16 shows a two-dimensional color plot of differential conductance as a function of source-drain bias and gate voltages for three different samples, selected from three types of devices: bare electrodes, OPE device and OPE-NDI device. Only straightly parallel lines have been observed with smooth edges or little perturbations along the edges. The $I - V$ characteristics stay almost the same under different gate voltages. One sample shows a clear change from limited gate coupling with unevenly distributed lines (-2.0 V $\sim$ +0.9 V) to completely no gate dependence with smooth color lines (0.9 V $\sim$ 2.0 V), as well as a decrease of the junction resistance. Such change is an indication of microscopic modification of the local charge environment or loss of the signal of possible molecules. Since no single-electron effect is observed, we consider there are no molecules trapped between the two Au electrodes.

Noisy Coulomb Blockade Diagram

In molecular devices with both OPE bridges and OPE-NDI SET-like molecules, we have observed a strong gate modulation on $I - V$ characteristics, however, accompanied with noisy background. Figure 6.14 presents representative current-voltage $(I - V)$ curves obtained at 4.2 K from an OPE device at different gate voltages V_G. The device exhibited strongly suppressed conductance near zero bias voltage and is noisy especially at high voltage.
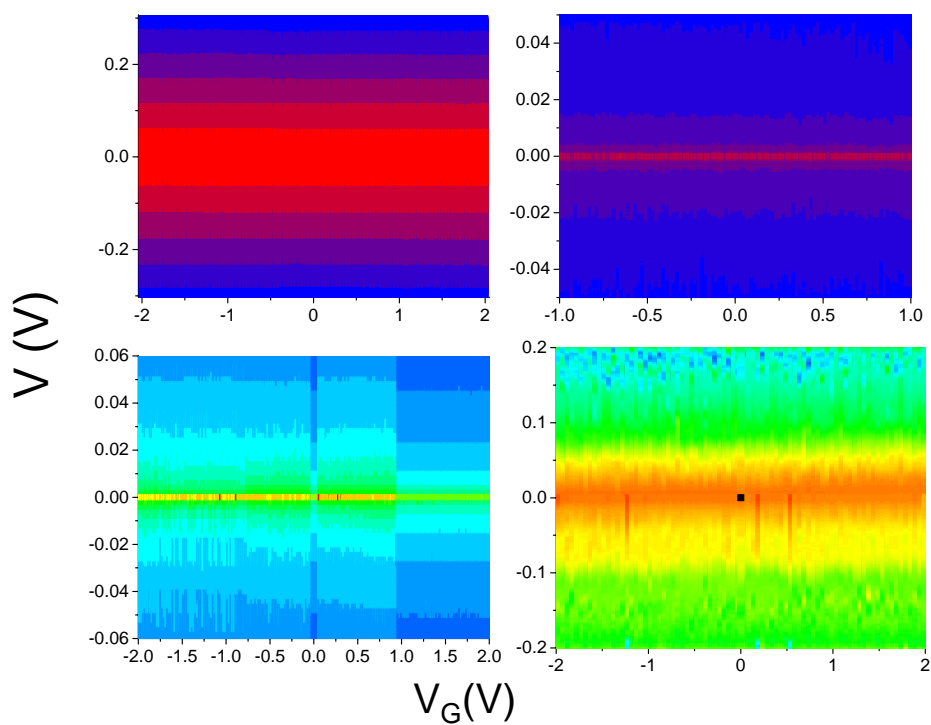
Figure 6.16: $I - V - V_G$ color plots are shown for 4 samples from (a) bare electrodes; (b) & (c) OPE-NDI molecules; (d) OPE molecules, with no or weakly gate dependence.

Since we plot differential conductance as a function of source-drain bias and gate voltages here, noisy two-dimensional $G - V - V_G$ plot is expected. We have used the adjacent averaging method to smooth the data set.

Figure 6.17 shows two-dimensional color plots of differential conductance (dI/dV) as a function of both source-drain bias V and gate voltage V_G for four different devices with OPE chains (c., d.) or OPE-NDI molecules (a., b.). Although the plots are noisy, we could still tell that the color shape resembles a partly completed Coulomb diamond diagram discussed in the previous chapter. As seen from Figure 6.17, the charge addition energy varies from 40 meV to 150 meV and the gate voltage V_c at which the conductance gap closed varies from device to device. Figure 6.17b shows abrupt changes at $V_G = -0.6$ V in the diagram, indicating sudden change of the local charge environment during the measurement. Figure 6.17c shows a more or less completed diamond plot with edges of different positive and negative slopes, suggesting the asymmetric contacts of molecules to both electrodes (different tunnel barriers at the contacts). The observed conductance gap is a consequence of the finite energy required to add or remove an electron to and from the molecule. The energy is a combination of single-electron charging and the quantized excitation spectrum of the system. The maximum observed gap in the experiments indicates that the charging energy of the molecule in this geometry can exceed 150 meV.

Peaks in dI/dV, which corresponds to the step-like features in current-voltage plot, are shown as lines in $G - V - V_G$ diagram. Figure 6.18 shows such a plot with two visible lines (*i.e.*, dI/dV peaks) outside the conductance gap for OPE chain molecules. The position of each dI/dV peak provides detailed information on the quantized excitations of the single OPE transistor system. The peaks appear when a new quantized excitation becomes energetically accessible to let electron tunnel between the molecule and the gold electrodes.

In summary, gate coupling is a very important consideration in single molecular devices. The electromigration process can result in molecules with little or no gate coupling. Two facts have to be taken into account: the screening properties of the source and drain electrodes, and the exact position of molecules that sit between these two electrodes. The V_G dependent features described above have not been observed in devices when no molecules were deposited. There are about 15% of more than 270 fabricated electrodes showing $I - V$ characteristics different from a single tunnel junction with no molecules and many devices have exhibited similar $I - V$ characteristics that are consistent with a single nanometer-sized object bridging two electrodes. Although we could not image directly the OPE or OPE-NDI molecules in these de-
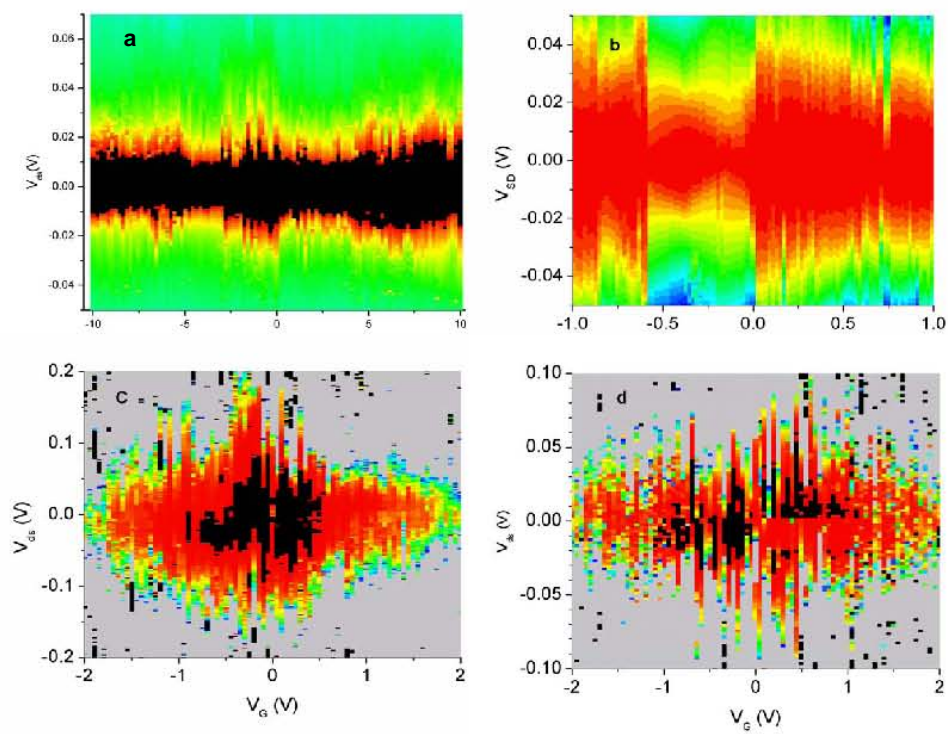
Figure 6.17: $G-V-V_G$ color plots are shown for 4 samples from (a) OPE-NDI molecules, and (b) OPE molecules, with noisy gate dependence.
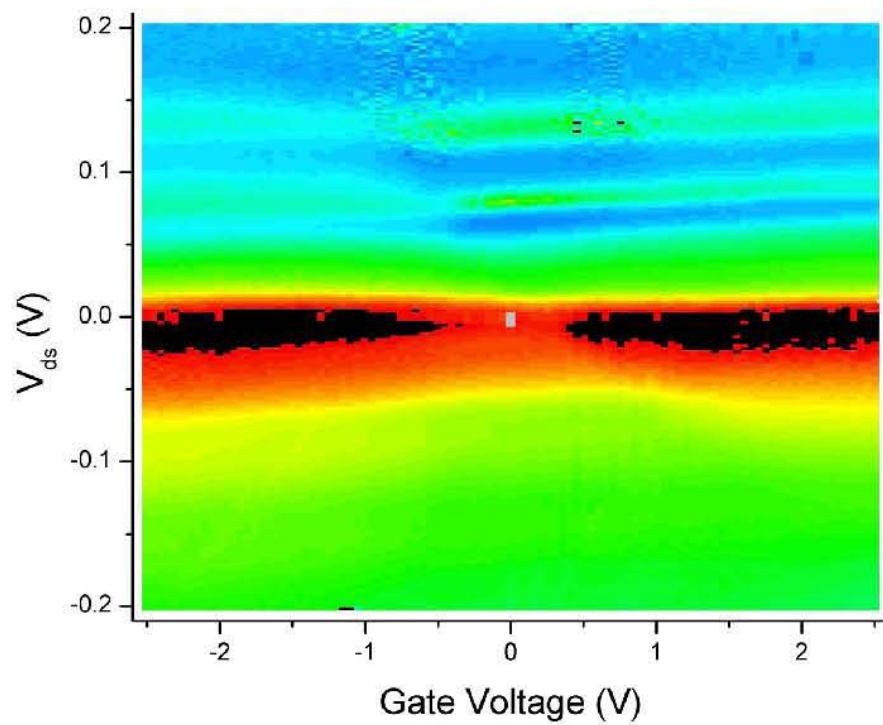
Figure 6.18: $G - V - V_G$ color plot is shown for an OPE device. The lines in the color diagram corresponds to the step-like features in current-voltage plot.

vices, these experimental observations indicate that individual molecules are responsible for the observed conductance features.

6.6 Temperature Effect

Temperature is another important factor that will affect the transport properties through molecular junctions. It has been suggested that the conduction through molecular bridges is controlled by two distinct mechanisms [177] - [182]. When the bridge energy and the Fermi level offset is greater than $\sim k_B T$, the molecular bridge is simply to mediate the electronic coupling between the two leads and charge tunnels between the two metal leads. When the bridge energy and the Fermi level are closer than $\sim k_B T$, hopping is expected to replace the coherent tunneling as the dominant transport mechanism. The transition between these two conduction regimes generally attributes to dephasing, disorder and relaxation, as well as temperature and molecular bridge length.

We have carried out temperature dependent $I-V$ measurements for interesting OPE devices, especially the ones that have survived the gate-modulation test. The probe has been lifted up to helium vapor phase for electrical measurements at various temperatures from 4.2 K to 290 K. Figure 6.19 shows the typical temperature dependent $I-V$ characteristics for two representative junctions. At room temperature, we have observed a linear $I-V$ region. As the temperature decreases, non-linear $I-V$ characteristics become more significant. The differential conductance in the gap is weakly dependent on temperature and essentially stays the same at temperature below 100 K. The fact that the increase of zero bias conductance with the increasing temperature, shows that a thermally activated conduction mechanism is dominant in the high temperature regime. An Arrhenius plot of the zero bias conductance is shown in Figure 6.20 and further demonstrates a clear transition between temperature independent regime and thermally activated transport regime. The observed thermally activated behavior is the result of transition from coherent tunneling to incoherent hopping transport mechanism. The activated zero conductance is proportional to $e^{-E_a/kT}$, where E_a is the activation energy for hopping. The slope in Figure 6.20 correspond to the energy barrier E_a. For our junctions, we have found E_a to be 36.5 meV and 32.2 meV for two OPE devices respectively. It has been suggested [182] that the barrier extracted from the Arrehenius plot is an intramolecular barrier for hopping between adjacent rings. For example, theoretical calculations of the rotational barriers in OPE rings are approximately $40 - 50$ meV.
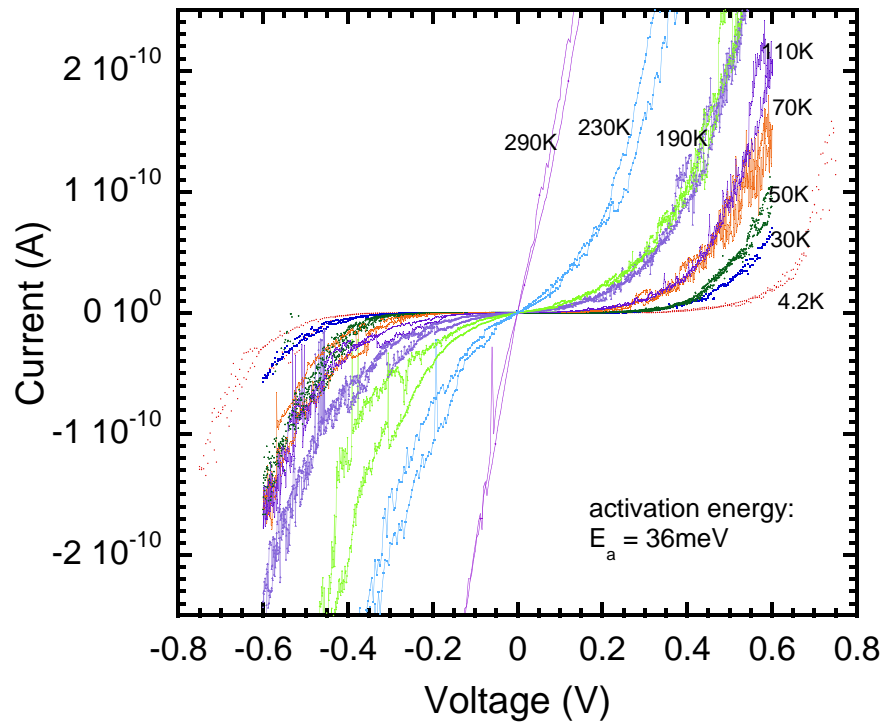
Figure 6.19: $I - V$ characteristics at various temperatures for a OPE device. Temperature varies from 4.2 K to 290 K.
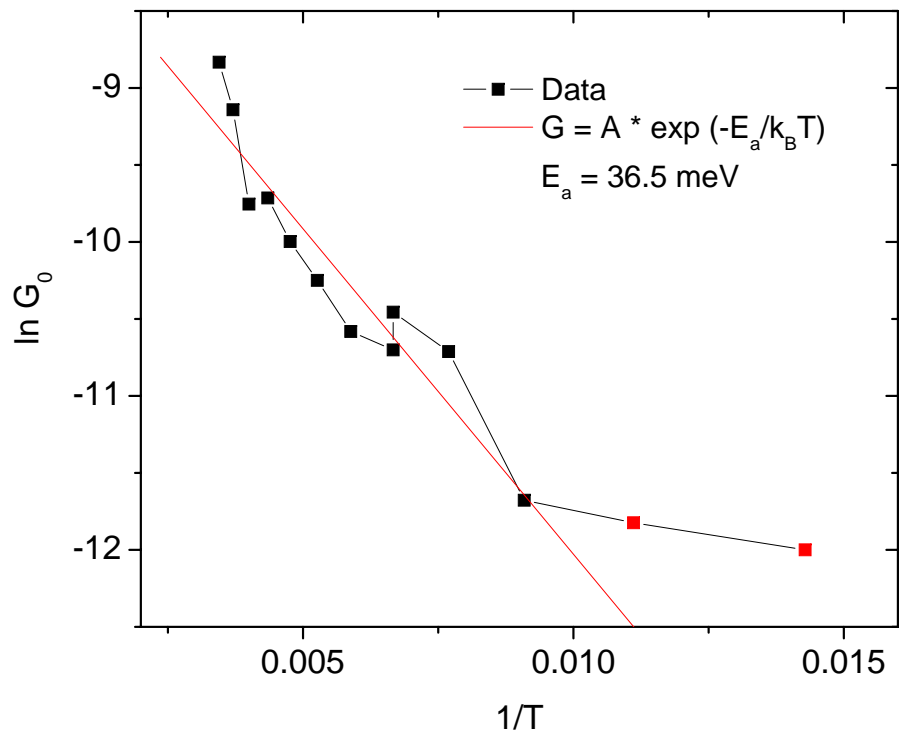
Figure 6.20: Arrhenius plot of zero bias conductance for an OPE device. For $T < 100$ K, G_0 stays the same. When $T > 100$ K, G_0 increases as temperature goes up. The activation energy is corresponding to the slope of the line, of about 36.5 meV.

6.7   Summary

In this chapter, we have shown our work on fabricating thin Au nanowires with nanometer separation gaps using electromigration technique. We have successfully removed the small gold nanoparticles from fabrication along the edge of the gold electrodes by selective chemical etching. We have also provided effective gate coupling through thin aluminum oxide underneath the junctions. We have measured the electrical properties of both OPE and OPE-NDI molecules with gate and temperature modulations. Electrical measurements after the breaking show simple tunnel $I - V$ curves or the Coulomb blockade, depending on whether a molecule is located in the gap. Statistics shows that there are at least 15% devices showing strongly nonlinear $I - V$ curves with current steps and visible gate dependence. The discrete current steps may be due to electron transport through one or a few molecules trapped between Au electrodes. Some samples show an activation current at high temperatures, indicating the transition from coherent tunneling regime toward the thermally activated hopping regime.

Chapter 7

Cross-point Junctions

In this chapter, we introduce the process of fabrication of the metal-nanowire-based crosspoint structures for self-assembled molecular junctions. The gap between the electrodes is only a few nanometers wide and is defined by the aluminum oxide layer thickness. This geometry is suitable for crossbar-based molecular electronic circuits, including their CMOL variety. The fabrication process is compatible with the conventional IC production techniques. Two kinds of conjugated molecules have been studied: (i) simple oligo(phenylene etylene) chain with two rings in the middle (length = 2.9 nm); (ii) OPE chains with a naphthalene diimide group in the middle (working as an acceptor) with length = 4.5 nm. These molecules are within the size range of the vertical gaps and are expected to be self-assembled between two nanowires. The detailed electrical characterization of these molecules will be discussed, together with studies of their temperature dependence.

7.1 Device Fabrication and Sample Preparation

Standard IC processing steps have been used to fabricate metal nanowires. Two perpendicular metallic nanowires have been separated by a thin insulation layer at their crosspoint area. The top electrode consist of Pt/Au layers and the bottom electrode is made of Pt. The nanogap width is determined by the thickness of thermally grown aluminum oxide, which could be controlled over a wide range of values. Wet-etch has been used at last to remove part of the insulation layers, in order to form the necessary undercut for the molecular self-assembly, as illustrated in Figure 7.1 [185].
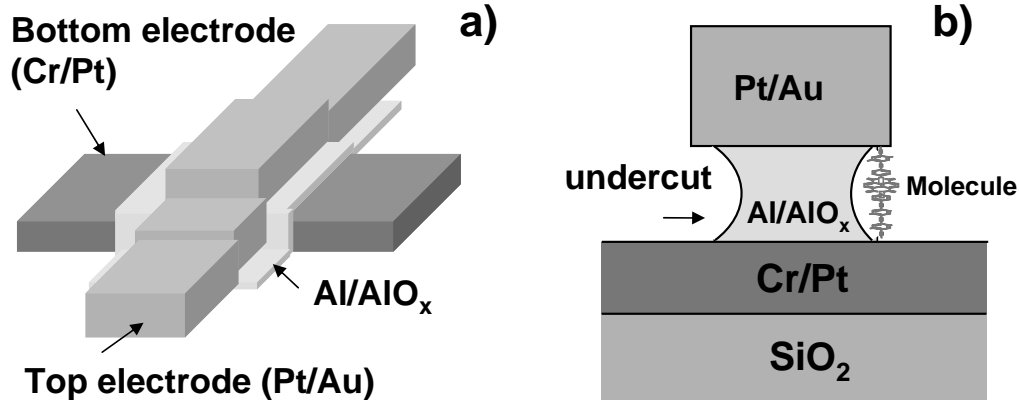
Figure 7.1: Geometry of our cross-point devices: (a) 3D view, and (b) cross-sectional view (both schematically).

7.1.1 Fabrication of $Pt/Al/AlO_x/Pt/Au$ Cross-point Structures

Our structures have been fabricated on 2-inch (50 mm) oxidized Si wafers. First, a 10-nm-thick Pt layer has been deposited on top of 4-nm-thick Cr sub-layer by electron beam evaporation, as the bottom electrode. The Pt layer is 100 nm wide. Direct electron-beam lithography and double-layer resist polymethylmethacrylate/poly(methylmethacrylate / methacrylic acid) (PMMA/P(MMA/MAA)) have been used for patterning and lift-off masks. The Cr layer is used to improve the adhesion of Pt to the Si substrate.

Secondly, a resist mask made by electron beam lithography, has been aligned to the bottom Pt nanowires for lifting-off the insulating layer (Al/AlO_x). The wafer has been loaded into the deposition chamber and sputter-cleaned in Ar plasma for 1 minute (200 W, 9 mT). The chamber has then been pumped down to base pressure 2×10^{-7} Pa. We have removed a very thin (~ 4 nm) top part of the Pt layer by Ar plasma sputtering. Without breaking the vacuum, the chamber has been pumped down to base pressure and a thin aluminum layer has been deposited on the fresh surface by dc sputtering. The sputtering condition listed in Table 7.1 below is used to obtain a 3-nm thick aluminum layer.

After the aluminum layer deposition, the vacuum chamber has been pumped down to the base pressure again and filled with pure oxygen to prepare for aluminum oxidation. The deposited aluminum has then been oxidized at 200 Torr for 15 hours at room temperature. The thickness of the insulation layer

Gas	Pressure	Power	Voltage	Current	Time
Ar	5 mT	150 W	309 V	0.46 A	6 s

Table 7.1: Aluminum sputtering conditions.

Wafer	Bottom Electrode	Al	AlO$_x$	Top Electrode
12	10 nm Au	4-8 nm Al	PO 15 mTorr ×10 min	60 nm Au
20	10 nm Pt	4-6 nm Al	PO 15 mTorr ×10 min	10 nm Pt + 60 nm Au
23	10 nm Pt	3-5 nm Al	TO 200Torr × 15 hours	10 nm Pt + 60 nm Au

Table 7.2: Wafer fabrication information.

is chosen to match the length of the molecules under study. By adjusting the thickness of the aluminum layer, we could precisely control aluminum oxide layer thickness, thus the gap size.

Next, a top bilayer of 10-nm-thick Pt plus 60-nm Au has been deposited on the Al/AlO$_x$ layer by electron-beam evaporation. E-beam lithography and lift-off have been used for patterning to form the cross-point geometry. Figure 7.2a shows a scanning electron microscopy (SEM) of a structure after the top nanowire patterning. The Al/AlO$_x$ patch is visible as a dark field around the cross-point area. We have 18 pre-fabricated supporting crosspoint structures on one chip. Table 7.2 lists fabrication information for all wafers.

7.1.2 Sample Preparation

The sample has been cleaned in acetone and isopropyl alcohol (IPA) with ultrasonic agitation for two minutes and further cleaned in O$_2$ rf-plasma (50 W, 1 Torr) for 30 seconds. Then the Al/AlO$_x$ layer has been partially etched away with 15% phosphoric acid (diluted in deionized water) at 50ºC to form the necessary undercut. By varying the etching time and temperature, we could reasonably control the etching rate. Figure 7.2b and 7.2c show the SEM pictures of our structures under different etching time. We could see that after 60 seconds of soaking in the etchant, almost all aluminum oxide has been removed from the surface. The dark field around the cross-point area is almost invisible after proper etch. In this case, an undercut is formed between the cross-wires and ready for the assembly of organic molecules. If the sample has been etched for a shorter time (40 seconds), we could still see the remains of the dark field, indicating that some Al/AlO$_x$ residues still remain on the
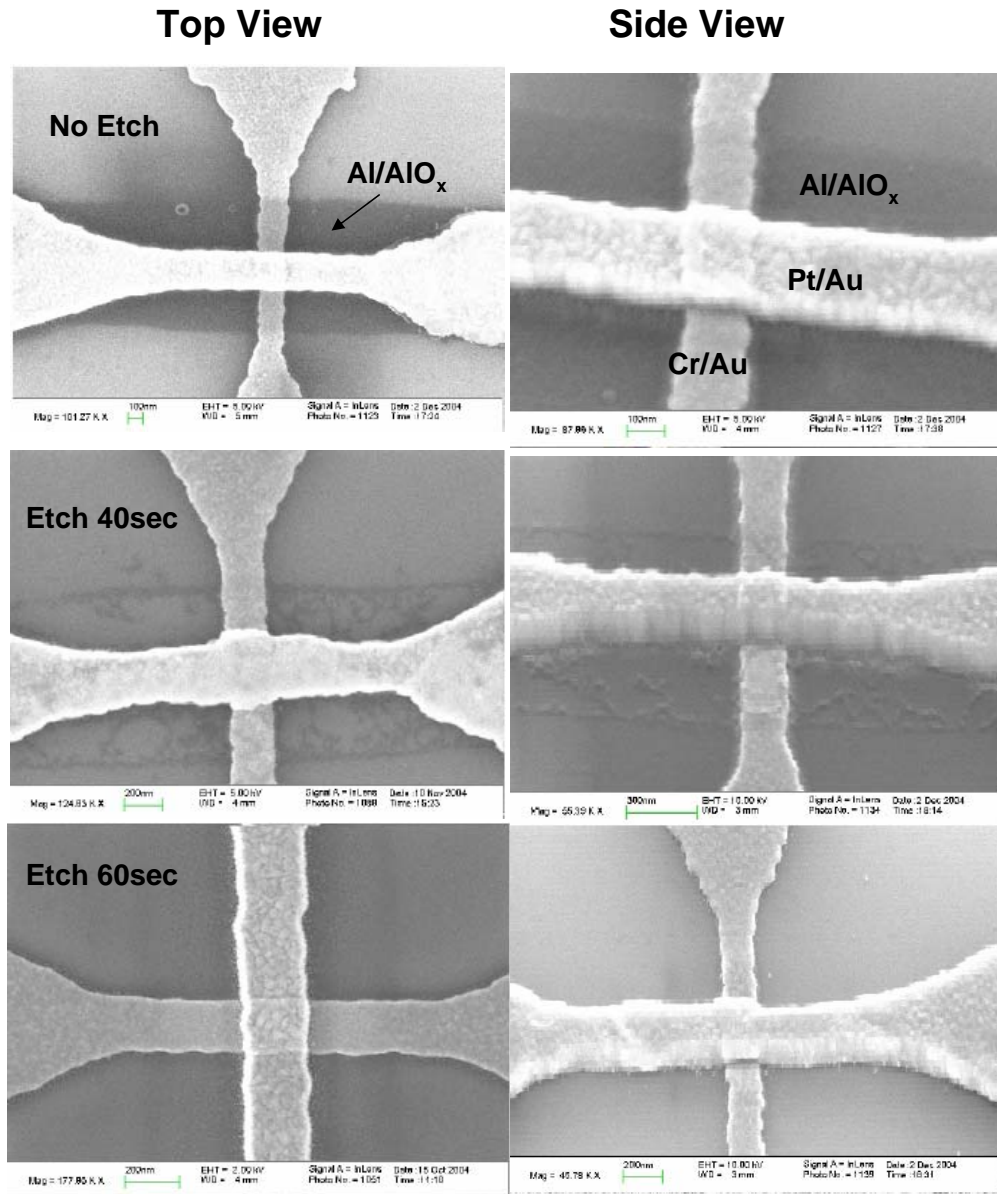
Top View　　　　**Side View**

Figure 7.2: SEM micrographs of a typical structure for both top-view and tilted-view: (a) before the Al/AlOx etch, (b) after the etch for 40 seconds , and (c) after the etch for 60 seconds.

surface, thus preventing the attachment of molecules. The side view is also showed for comparison. It is crucial to find appropriate etching conditions for the formation of cross-point junctions. As a standard, we always perform the etching at 50ºC for 50 seconds in dilute phosphoric acid.

After the removal of aluminum oxide, the structure was immediately rinsed with deionized water and isopropyl alcohol (IPA) for 30 seconds. To reduce the surface tension, the samples have been cleaned in ethanol with ul-traonic agitation for 2 minutes, followed by a flow dry in nitrogen. A brief and quick check of junction resistance has been done at room temperature prior to the assembly to assure the presence of an open gap with low leakage current through the junction. Then, the device was immediately transferred to toluene solution (5 ml) with various molecular compounds (1.0 mg). Af-ter soaking for over 24 hours, the sample was removed from the solution and thoroughly rinsed with toluene for 30 seconds and dried in nitrogen flow. We have prepared the molecular devices for further electrical characterization.

7.2 TEM and AFM Characterization of Pt and Pt/Al Interface

Before we started to use Pt film as the base electrode, we began with Au film in the very first trials. After the initial characterization, we have observed a great amount of junctions showing large leakage current. For some junctions (without molecular deposition), we have even observed the Coulomb blockade like $I - V$ curves, which could be attributed to small Au grains distributed along the nanowire. Another concern is that Au and Al are known to form alloy easily. We might not be able to etch away all Al/AlO_x to form the necessary undercut. The quality of aluminum oxide is unknown and it is not clear if molecules can be self-assembled on the mixed surface.

Instead of Au, we choose Pt film as the base electrode for fabrication of cross-point structures. It is found that surface roughness of the Pt film plays an important role in determining the quality of the insulating layer. To characterize the Pt film, we have performed atomic force microscopy at room temperature. The estimated roughness of the Pt surface is about 0.6 nm (Figure 7.3).

We have also fabricated test structures to study the Pt/Al interface, in which (instead of the Pt/Au top layer used in real devices) a protection layer of about 100 nm Nb has been deposited in-situ immediately after the aluminum oxidation. Figure 7.4 shows high-resolution TEM images of the cross-section of the test structures. One can see that the Pt/Al interface is indeed smooth
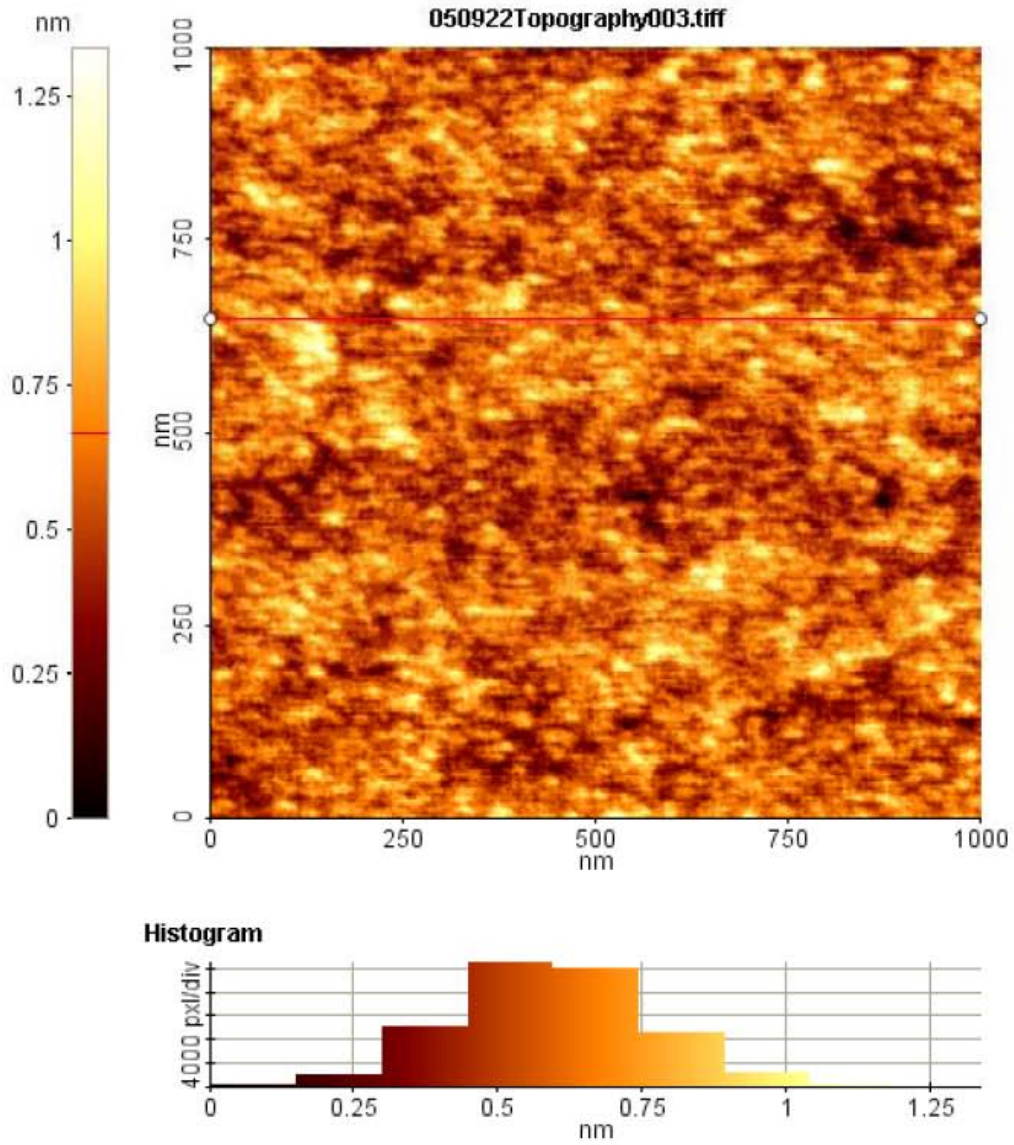
Figure 7.3: AFM image of the 10-nm thick Pt on top of 4-nm Cr layer, and its thickness histogram. r.m.s. roughness of the film is about 0.6 nm.

and clear, and the Al layer is almost completely oxidized and quite uniform.

7.3 Electrical Measurement of OPE chains

The completed support structures have been characterized at both room and low (liquid helium) temperatures. Before any chemical etching treatment, electrical measurements have shown that for most devices the room-temperature leakage resistance of a $\sim 200 \times 200$ nm^2 cross-point junction is typically around 10^{12} Ω (Figure 7.5a). The measured leakage current of the order of pA for a typical junction is shown as an insert.

After the Al/AlO$_x$ etch, the junctions become somewhat more leaky but over 70% of the junctions still show a very high resistance ($\sim 10^{11}$ Ω) (7.5b). The yield is much higher than our other test structures. For example, in experiments with electromigration-formed structures, only 40% of the junctions showed similarly low leakage current when no molecules had been deposited.

We have carried out the preliminary testing of a self-assembly of specially synthesized molecules on our support structures. The core of these molecules is an oligo(phenylene-ethynylene) (OPE) chain of length n, which plays the role of tunnel barrier in the planned molecular single-electron latching switches [186]. For our experiments, the chains have been terminated with isocyanide groups on both ends [187]. In order to match the size of the vertical gap (or thickness of Al/AlO$_x$), we have chosen molecules with $n = 2$ (2.9 nm). Apparently molecules with $n = 1$ (2.2 nm) are too short for this application. Our preliminary tests also shows that the devices have comparable $I-V$ curves with or without the short molecules ($n = 1$).

We have examined a total of 72 devices (all from wafer 23) with OPE-bridges ($n = 2$). Immediately after soaking and drying, the sample has been transfered to our measurement set-up for preliminary resistance check-up at room temperature. Then the sample has been carried down to liquid helium for further electrical characterization. From the histogram of junction resistances after molecular deposition (Figure 7.5c), we have observed that the molecular self-assembly has led to a considerable and stable decrease of resistance (from $\sim 10^{11}$ Ω to $\sim 10^9$ Ω), .

7.3.1 Low Temperature $I - V$ Characteristics

As seen from the histogram of resistances(Figure 7.5), some junctions exhibited large leakage current, even before the deposition of molecules. Though we have kept the chemical etching condition almost the same every time, the actual chip-to-chip or junction-to-junction variance is expected. To avoid the
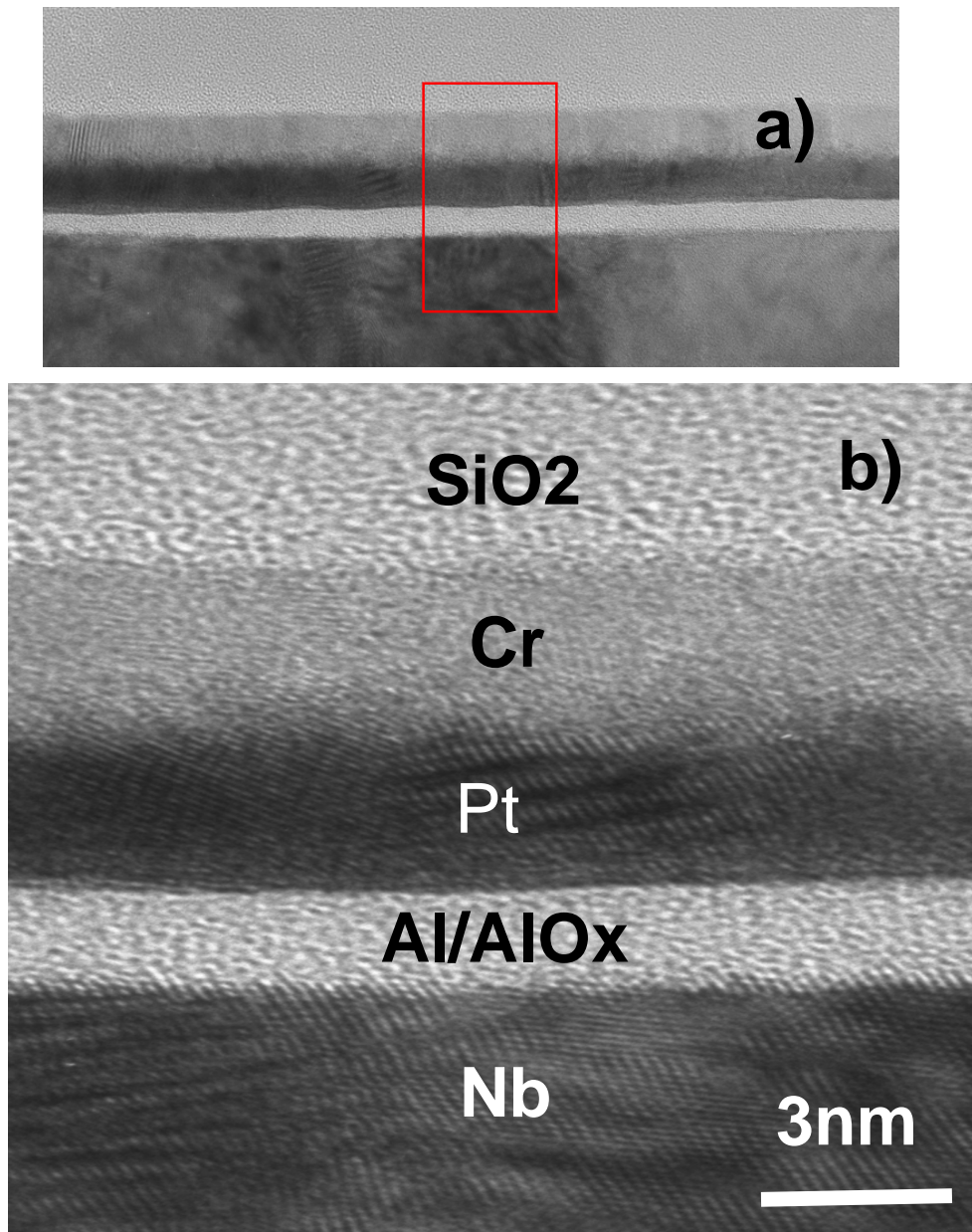
Figure 7.4: High-resolution TEM images of one of the test structures at: a) low and b) high magnification, with $SiO_2/Cr/Pt/Al/AlO_x/Nb$ structure. The interface between Pt and Al is very smooth.

Figure 7.5: Histograms of the support structure leakage resistance at 50 mV bias voltage, measured at room temperature: (a) before and (b) after the Al/AlO$_x$ etch, (c) after deposition of OPE molecules. Insets show typical $I - V$ curves; the hysteresis is related to the voltage sweep speed.

complication, only the support structures with low leakage current (< 10 pA) undergo further electrical measurements at liquid helium temperature after the deposition of molecules.

There are 23 samples which have showed interesting Coulomb-blockade or Coulomb staircase $I - V$ characteristics. Among them, the measured currents of 19 samples are in the range of 1 pA $\sim$ 100 pA, with corresponding resistance from G$\Omega \sim$ 10 GΩ. 4 samples showed higher current (1 nA $\sim$ 10 nA) with 10 M$\Omega \sim$ 100 MΩ resistance. The values of current measured at ± 1 V are comparable to those of our electromigrated devices and other single molecule junctions with similar molecular structures. By plotting the histogram of resistance from these 23 samples (Figure 7.6), we could clearly see a stable decrease of junction resistance after the molecular self-assembly.

Figure 7.7 shows a family of dc $I - V$ and their differential conductance curves typical for four samples with resistances in the range $10^9 - 10^{10}$ Ω measured at 4.2 K. We have observed strongly suppressed current at small voltages resembling Coulomb blockade with additional current steps. The threshold voltages vary from around 100 mV to 500 mV, which are much higher than what we have observed in electromigrated junctions. We believe that there are just one or a few molecules assembled on the support structure. The high-resistance plateau near the origin may be interpreted as the result of the virtual absence of electron transport for conditions when the Fermi levels of both electrodes are located within the LUMO-HOMO gap. The current steps, especially sharp at low temperatures, are probably due to the alignment of the Fermi levels (separated by the product of the electron charge and the applied voltage) with one of the effective single-particle levels [188] of the molecule. This interpretation is consistent with the picture of sequential single-electron tunneling with the molecule playing the role of a single-electron island with a discrete energy spectrum [188], [189]. This picture, as well as the few-pA scale of the current steps, imply that isocyanide groups are separated from the metallic electrodes with 1-nm-scale tunnel barriers whose origin still has to be identified.

7.3.2   Temperature Dependence

The device yield of crosspoint structures is significantly higher (30%) than our previous test bed using electromigrated-break junction technique (15%). It is very important to distinguish between the candidate single-molecule devices and artifacts. As mentioned earlier, the usual method is to incorporate the third electrode as a gate to change the energy levels inside the molecules, thus changing the transport properties. However, the current device does not allow for effective gate control so far. Fortunately, temperature is another knob
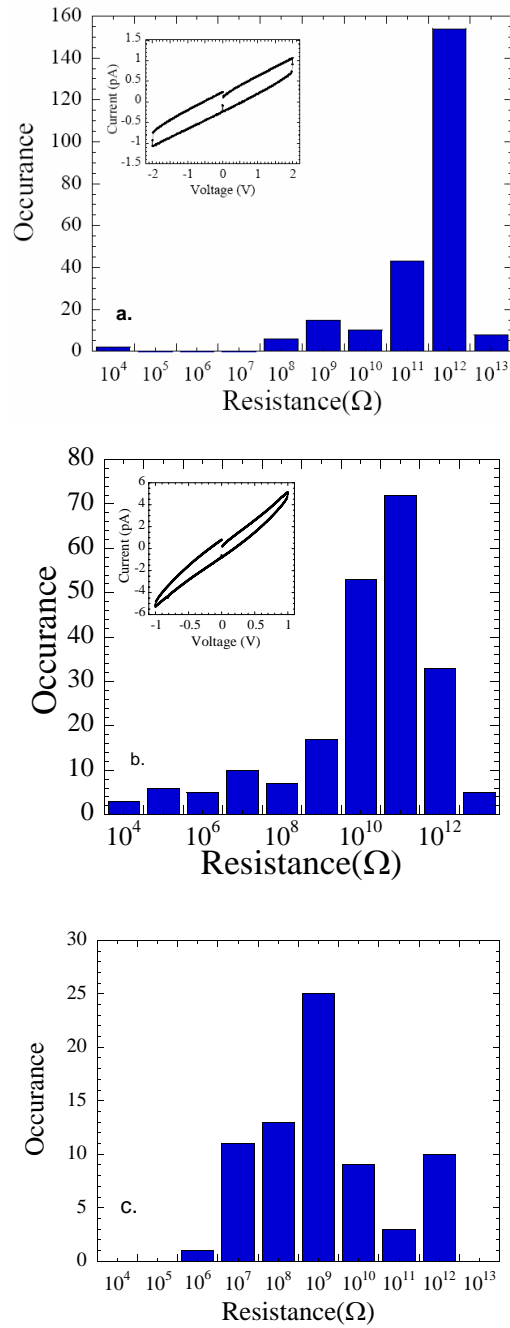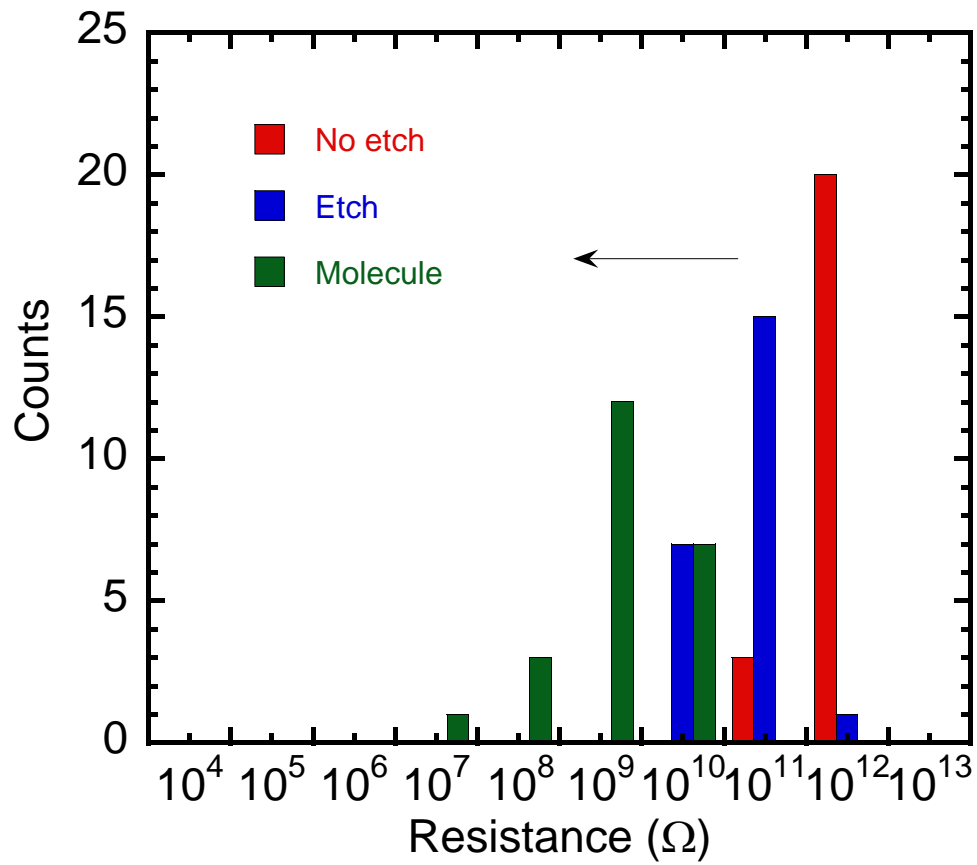
Figure 7.6: Histograms of the support structure leakage resistance at 50 mV bias voltage, measured at room temperature especially for devices showing interesting $I - V$ characterization: (a) before and (b) after the Al/AlO$_x$ etch, (c) after the deposition of OPE molecules.

Figure 7.7: DC-IV curves for 4 selected high resistance junctions at 4.2 K. The differential conductance $G(V) = dI/dV$ is also plotted.

available that can be used to identify the transport mechanism.

We have carried out temperature dependent $I - V$ measurements for all interesting OPE devices. The probe has been lifted up to helium vapor phase for electrical measurements at various temperatures from 20 K to 200 K. We have limited our measurements to a ± 1 V window since voltages exceeding this range typically cause degradation of the junction, which is probably due to the excessive heat dissipation, especially at high temperatures.

Figure 7.8 shows the typical temperature dependent $I - V$ characteristics for two representative junctions. At low temperature, we have observed a strongly non-linear $I - V$ curve with suppressed current and threshold voltage in the range of 100 mV to 500 mV. As the temperature increases, we have observed an overall increase in current and a decrease of the threshold voltage, which suggests that a thermally activated conduction mechanism operates in parallel with the tunneling mechanism.

The differential conductance dI/dV of a typical junction as a function of bias voltage V and temperature T is shown in Figure 7.9. As the temperature increasdes from 4.2 K to 130 K, the resonance conductance peaks still remain the same or with a slight shift to lower voltage range. At temperature higher than 160 K, the peak feature disappears and the $I - V$ curve becomes noisy at higher voltage end, which indicates the degradation of junction quality.

The differential conductance is weakly dependent on temperature and essentially has the same value below 100 K. At higher temperatures, the differential conductance increases, which means that a thermally activated conduction mechanism dominates transport in the high temperature regime. An Arrhenius plot of the zero bias conductance for 4 different devices is shown in Figure 7.10. The transition between two conduction mechanisms (from coherent tunneling to incoherent hopping) is more evident. Based on $G_0 \propto e^{-E_a/kT}$ (E_a is the activation energy for hopping), the slope in Figure 7.10 should correspond to the activation energy barrier E_a. The calculated activation energy for the four devices are rather spread at 29 meV, 44 meV, 53 meV, 89 meV repectively, which are still small when compared to previous calculations that suggest the HOMO-LUMO gap of this molecule should be greater than 2 eV [184], [188]. Since experimental data does not yet exist regarding the size of the HOMO-LUMO gap or the relative position of the Fermi level in this system, it has been suggested that the barrier extracted from the Arrehenius plot is actually an intramolecular level for hopping between adjacent rings [182].
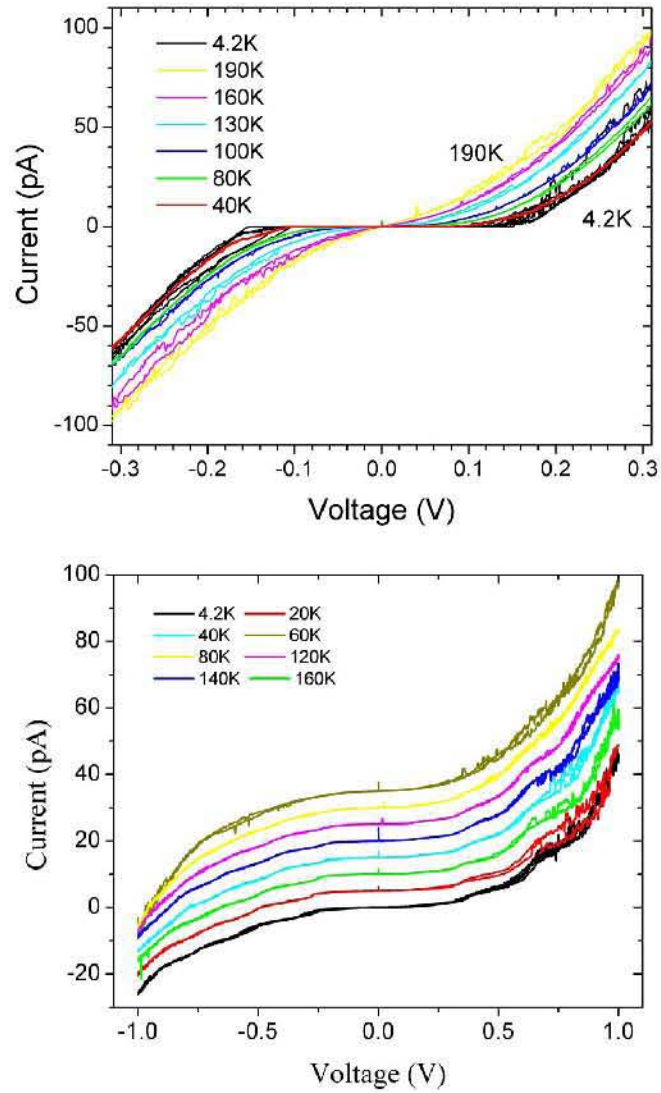
Figure 7.8: DC-IV curves for two selected high resistance junctions at various temperature. For one junction, the curves are offset for clarity.
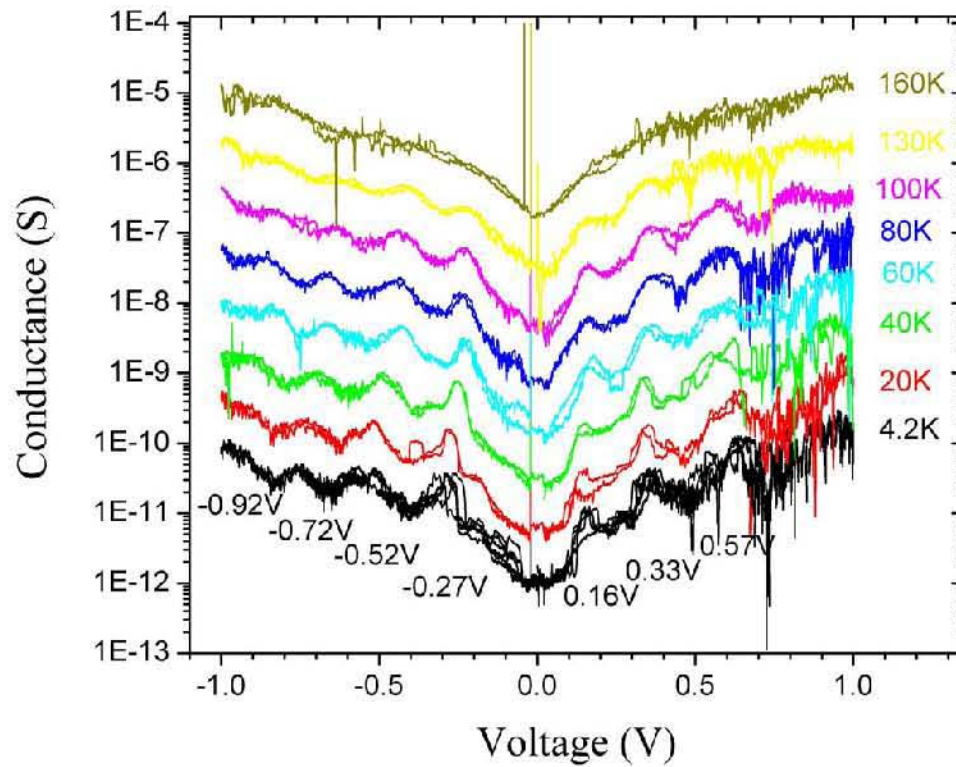
Figure 7.9: Differential conductance as a function of bias voltage and temperature T. The curves are offset for clarity.
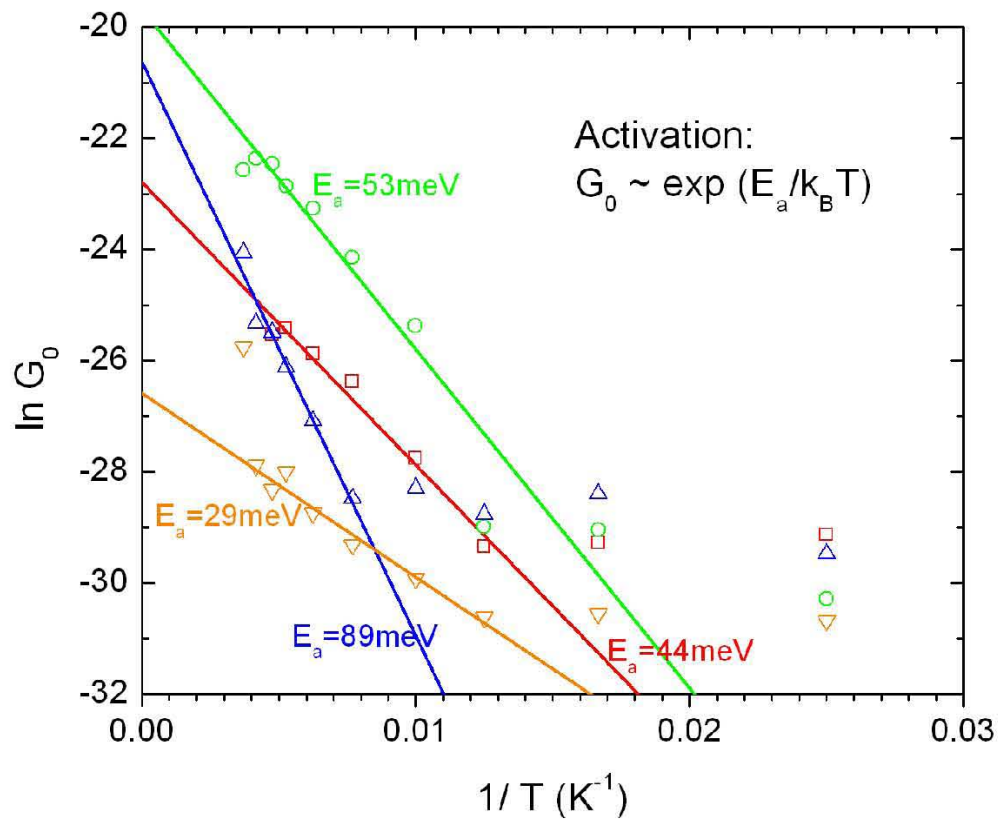
Figure 7.10: Arrhenius plot of the zero bias conductance for four different OPE-devices.

7.4 Electrical Measurement of OPE-NDI Molecules

The SET-like molecules with oligo(phenylene ethynylene)s containing central naphthalenediimide group have been investigated in electromigrated structures. With $n = 1$, the length of the molecule is 4.5 nm, comparable to the gap size of the cross-point structures (3 - 5 nm). Following the same cleaning and deposition procedures as for the short OPE chains, we have examined 5 chips (each containing 18 junctions) in this category.

While we have always kept the same etching condition, the support structures tend to have larger leakage current than before, probably due to the slight different distribution of aluminum oxide on the whole wafer. For relatively thinner aluminum oxide (*e.g.*, 3 nm), we could have etched away too much of aluminum oxide, leading to a big leakage current of the order of nA. Since we have used the same dilute phosphoric acid as an etchant, the solution could undergo certain degradation after a number of usages. The predetermined etching rate will be different from now.

After molecular deposition, we have observed an increase of junction resistance for some leaky samples (after etching treatment). In this case, it is not clear whether the measured signal is from the molecule itself, or some artifacts or impurities from the solvent, although some of them show nonlinear $I - V$ curves with Coulomb steps. Due to a lot of complications, we will not consider devices in this class as genuine molecular devices.

There are still a number of devices showing an increased conductance after the deposition of the molecules. Figure 7.11 shows the typical dc $I - V$ curves and their differential conductance for two representative junctions. The conductance is strongly suppressed around the zero bias voltage with a threshold from 200 mV to 300 mV. The current steps outside the suppressed regions correspond to the resonance peaks in conductance plots. The magnitude of the current is similar to that of the OPE rings, in the range of pA $\sim$ 10 pA. The current steps are the result of the charging energy and discrete quantum energy levels of the molecules.

The average observed threshold voltage is between 100 mV to 300 mV. Let us define the Coulomb gap size to be the difference between the positive and negative threshold voltages ($V_{\mathrm{gap}} = V_{+,\mathrm{th}} - V_{-,\mathrm{th}}$). Figure 7.12 shows the zero-bias conductance distribution with the Coulomb gap size for devices (1) without molecule, (2) with OPE ($n = 2$) molecules, and (3) with OPE-NDI ($n = 1$) molecules. It is clearly seen from the plot that the majority of junctions have 200 mV to 600 mV range (the shaded area). It is known that V_{th} depends much on the local charge environment. We still lack of good gating method at this stage. Figure 7.12 indicates that the maximum observed gap of these OPE-based molecules can exceed 500 mV.
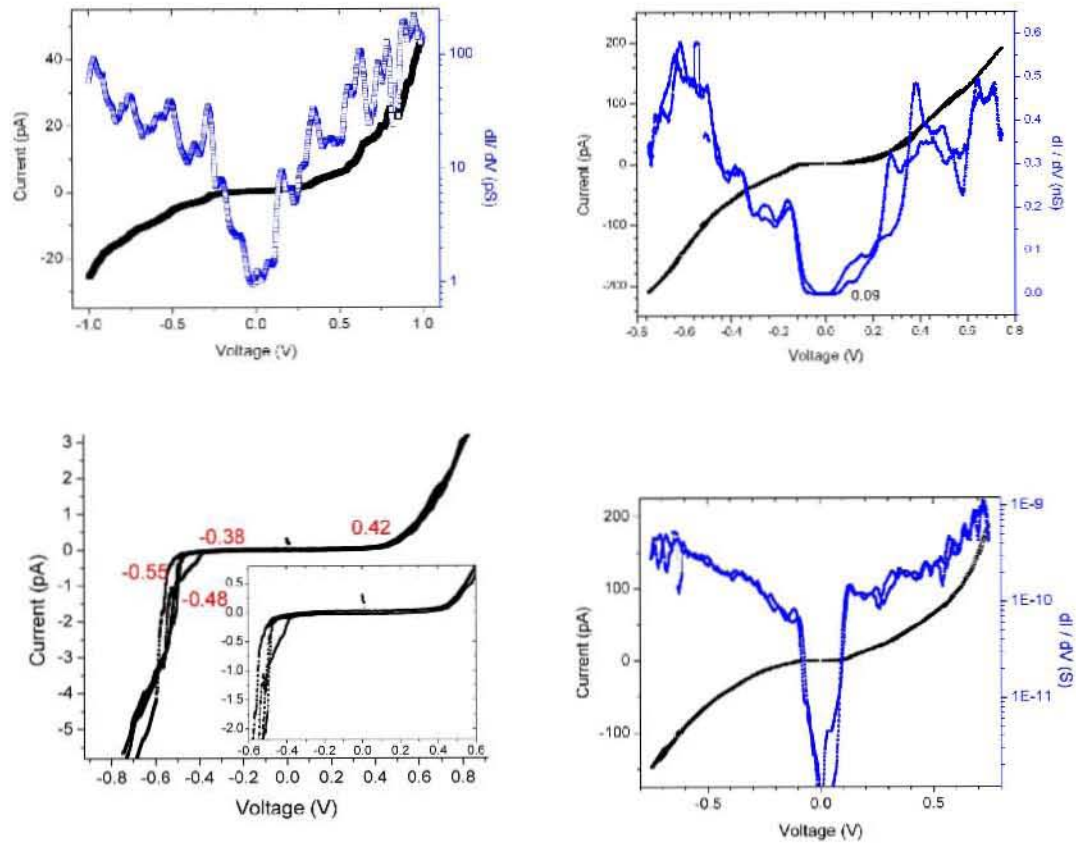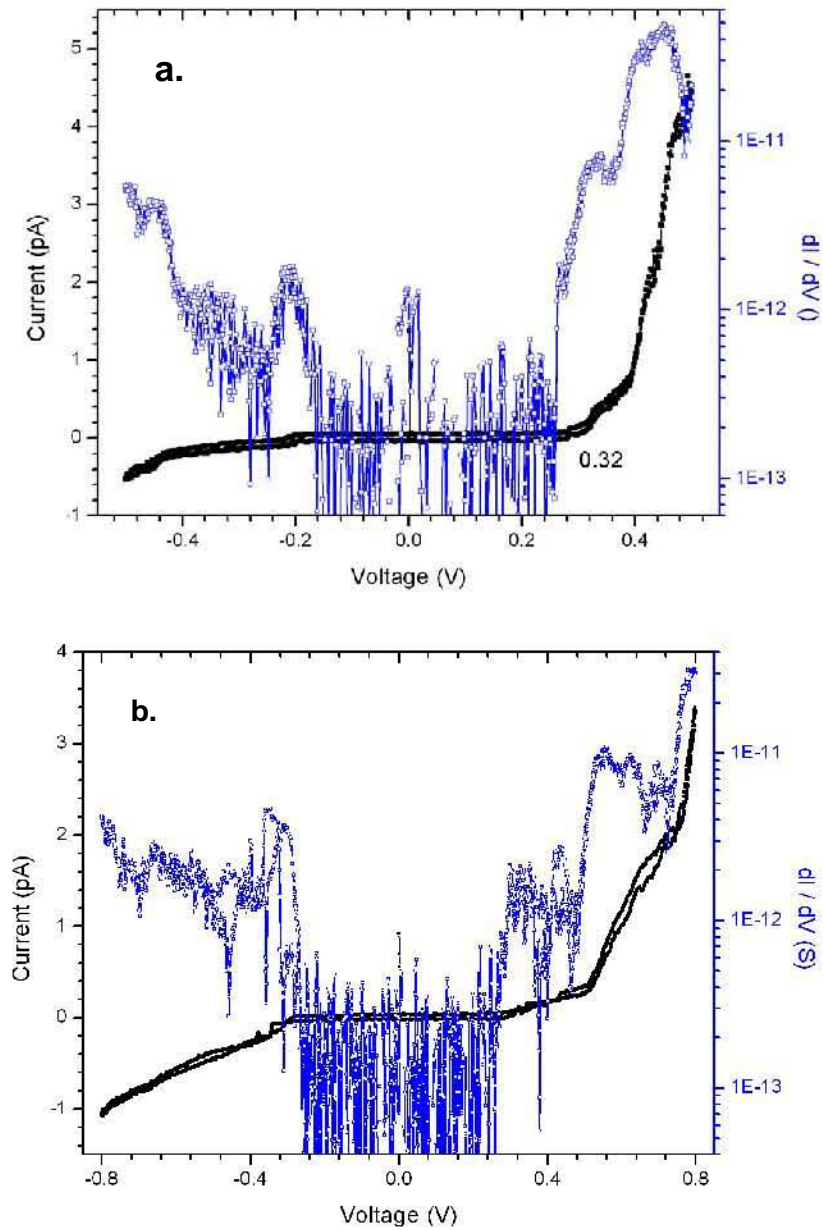
Figure 7.11: DC-*IV* curves for two selected high resistance junctions (OPE-NDI) at 4.2 K. The differential conductance $G(V) = dI/dV$ is also plotted.
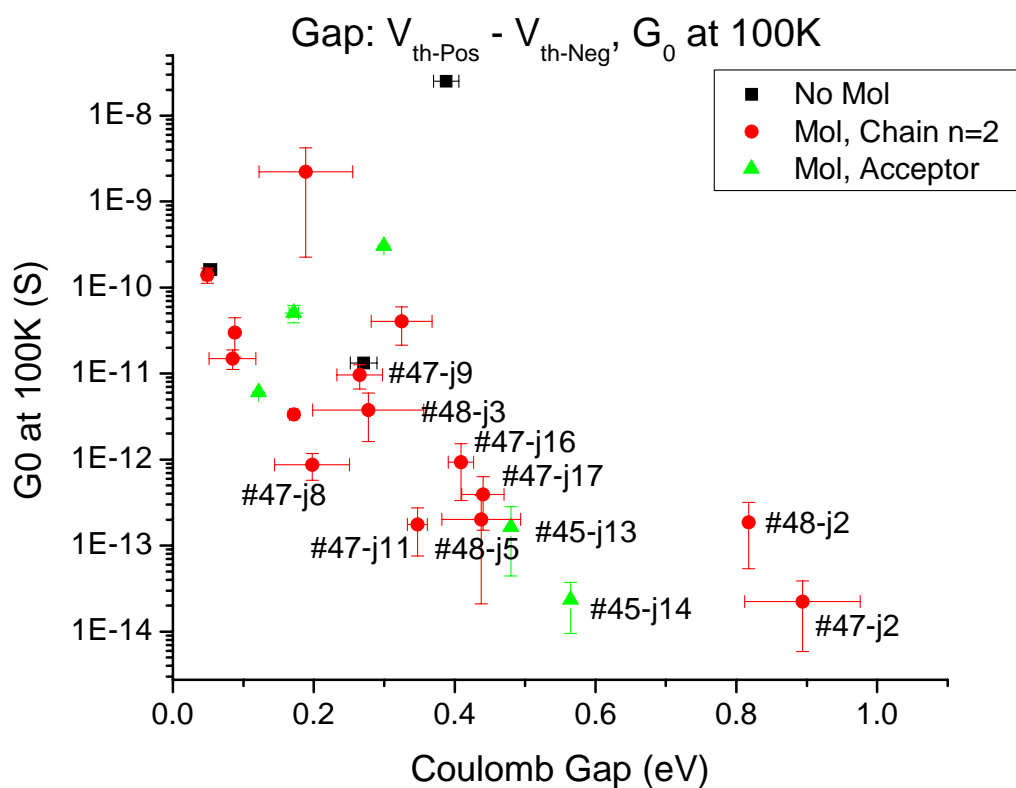
Figure 7.12: Coulomb gap distribution with zero-bias conductance for (1) bare support structures; (2) OPE chain molecular devices; (3) OPE-NDI molecular devices.

7.5   Conclusion

To summarize, we have fabricated a new type of support structure for subsequent molecular self-assembly, whose geometry is very suitable for crossbar-based molecular electronic circuits (including the CMOL variety). The structures feature few-nm vacuum/air gaps between metallic electrodes, which may be adjusted with sub-nm accuracy to match the length of the molecules for higher assembly yield. Room-temperature leakage conductance of a $\sim$ 200×200 nm^2 structure is typically around 10^{12} Ω. In most samples, the molecular self-assembly leads to a considerable and stable increase of conductance, with typical nonlinear $I-V$ curves. Coulomb blockade and conductance peaks have been observed for both types of molecules with single-electron addition energy above 100 mV. We have performed detailed electrical measurements at various temperatures from 4.2 K to 300 K. The observed thermal activation indicates a transition of transport mechanism from the tunneling regime to the hopping regime. These structures with various molecules, are very interesting candidates for building hybrid CMOS/nanodevice integrated circuits.

Chapter 8

Conclusion

As the conventional semiconductor technology is reaching the scaling limits, new technologies are needed to further increase the density and performance of integrated circuits. In this work, we have investigated two types of potential systems: aluminum based crested tunnel barriers and single-molecule transistors.

8.1 Summary of the Crested Barriers Studies

With the idea of using layered tunnel barriers in standard nonvolatile memory devices (*e.g.*, flash memory) (chapter 2), we have studied aluminum oxide grown either thermally or by plasma under different oxygen exposure conditions. Similar wafers fabricated at both SBU and Hypres, Inc. showed high reproducibility. Such aluminum oxide is very stable and can be stored at ambient condition for years without degradation. Most samples have been subjected to rapid thermal annealing treatments from 300ºC to 650ºC. We have measured the $I - V$ curves at both room and liquid helium temperatures. The temperature independence suggests the dominant transport mechanism is by direct tunneling. We have fit our data based on the joint solution of Schrödinger equation and Poisson equation with hot-electron relaxation approximation.

For thermally grown aluminum oxide, higher oxygen exposure leads to the increase of both barrier height and thickness. As the post annealing temperature increases, the junction conductance drops dramatically with an increase of hard breakdown voltage from 1.0 V to almost 4.0 V. By fitting the data with either one layer or multi-layer models, we have observed that the tunnel barrier height increases dramatically from 1.8 eV to $2.5 \sim 2.9$ eV, while the effective barrier thickness increase from 0.8 nm to $2.2 \sim 2.5$ nm, with above 60% increase in the breakdown electric field.

For plasma grown aluminum oxide, higher oxygen exposure does not affect the tunnel barrier as much as the thermal oxide. It has been sexpected that the adsorption of oxygen has reached its saturation level in the first few minutes. However, the rf-plasma power is an important factor. For standard rf power of 50 W, the tunnel barrier height stays almost the same at ~ 2.0 V within a broad range of RTA temperatures. The effective barrier thickness increases from 2.3 nm to 3.5 nm. For a low rf-plasma power of 10 W, we have observed a high zero conductance (~ 6.0 S/m^2), about 3 orders of magnitude higher than that of 50 W sample. As the post-annealing temperature increase, the zero conductance also drops in the same fashion as that of thermal oxide.

The fact that the thermal and 50 W-rf plasma show different annealing behavior, offers the possibility to use them in layered barriers. We have fabricated 6 wafers with double-layered aluminum oxides; however, none of them showed desired $I-V$ performance due to the complex interface chemistry and possible charge trapping. However, we have found that 10 W-rf-plamsa oxide exhibit very high endurance to electric fields (> 10 MV/cm) and extremely high values of charge-to-breakdown ($\sim 10^6$ C/cm^2) with post-annealing. These properties may be acceptable in floating gate RAM applications. Our future plan is to continue the optimization of fabrication parameters (in particular, oxygen pressure and rf plasma power) in order to further increase the write/erase cycles.

8.2   Summary of the Molecular Junction Work

Chapters 5 to 7 describe three methods we have used to build molecular devices. We have started with the most straight forward idea - to put individual molecules directly between the gap of two metal electrodes, assuming the length of the molecule will match the size of the nanogap. In order to match the 8 - 9 nm gap defined by e-beam lithography (this is also the fabrication limit), we have used relatively long molecules OPE-NDI (9 nm). After more than one year of repeated experiments, we have found only 2 devices with non-linear $I-V$ with conductance peaks. This extremely low yield of interesting devices has suggested that this method is a dead end.

With this in mind, we are more interested in shorter molecules, such as OPE ($n = 1, 2$) or OPE-NDI ($n = 1$). They are about 2 to 5 nm long. However, this scale is beyond the e-beam lithography limit. Among the various available techniques, electromigraion is of the most interest, since it provides easy way to fabricate 1 nm gap at liquid helium temperature. The drawback is also obvious. Due to the stochastic nature of the process, every junction differs at atomic scale. This method relies on statistical analysis of many samples.

We successfully removed the tiny gold nanoparticles induced from fabrication along the edge of the gold electrode by selective chemical etching and provided effective gate coupling through thin aluminum oxide underneath the junctions. More than 30% junctions showed $G\Omega$-scale resistance after breaking with tunneling $I-V$ characteristics, indicating that a few nm gaps were successfully created at low temperatures. We have investigated both types (wire-like and SET-like) of pre-assembled molecules and observed nonlinear $I-V$ curves for more than 40% the devices. About 10% devices showed discrete current steps, apparently due to electron transport through one or a few molecules, especially for wire-like molecules.

Although we have greatly improved the yield of molecular devices by electromigration, it is not compatible with conventional VLSI circuits production. This is why we have developed a novel cross-point structure, whose geometry is suitable for crossbar-based molecular electronic circuits (including the CMOL variety). Molecules have been self-asseblemed between two metallic electrodes separated by an insulation layer with adjustable thickness matching the length of the molecules. Chemical etching has been used to remove parts of oxide layer to form the necessary undercut under appropriate conditions. We have achieved a relatively high yield of high-quality support structures (leakage current < 1 pA). In most samples, the molecular self-assembly leads to a considerable and stable increase of conductance, with typical nonlinear $I-V$ curves. Coulomb-blockade and conductance peaks have been observed for both types of molecules with single-electron addition energy above 100 mV. We have performed detailed electrical measurements at various temperatures from 4.2 K to 300 K. Some samples show an activation current at high temperatures, indicating the transition from coherent tunneling regime toward the thermally activated hopping regime, with activation energy varying from 29 meV to 89 meV. Although this structure provides better electrical characterization of the molecular device than electromigration method, it is limited by wet-etching, and the actual etching environment differs from one chip to another. Further, better imaging tools are needed to physically check the extent of undercut of the spacers (aluminum oxide).

For the second and third configurations, single molecular devices from both chain-like OPE molecules and SET-like OPE-NDI molecules exhibited several common behaviors. The current magnitude is in the same range from pA to nA. The Coulomb blockade was observed at liquid helium temperature (4.2 K), because single molecules in our device form quantum dots due to a large charging energy and the energy level quantization. The overall conductance of a single molecule device is dominated by the properties of the contacts between the molecule and the electrodes and is significantly lower

than the conductance quantum e^2/h. In a large number of devices, we could resolve additional dI/dV peaks outside Coulomb blockade area. These additional peaks may correspond to quantum excitation of phonons in the devices. The future work of this project includes the implementation of the third gate electrode for cross-point structures.

In summary, the conductance of the molecule depends not only on the intrinsic properties of the molecule, but also on the electrode materials. The conductance is also sensitive to the atomic level details of the molecule-electrode contact and the local environment of the molecule. To measure the single-molecule conductivity has been difficult owing to lack of a technique that can provide reliable and well-defined molecule-electrode contacts. Creating identical contact geometries has been a challenging experimental problem, and the lack of atomic-level structural information of the contacts makes it hard to compare calculations with measurements. In order to achieve reproducible molecular devices, SAMs with specially designed molecules may be considered an alternative way to go, since the molecules are typically immobilized on one electrode surface. Both self-assembly and Langmuir-Blodgett methods provide ordered molecular films that are highly desired. In this type of devices, we need to place a second electrode on top of the molecular film. Usually the deposition of the top electrode is often the most difficult part of the process, since one must make sure that energetic metal atoms do not damage the molecular film and does not penetrate into the molecular film via defect sites. The recent work by Akkerman *et al.* [190] might open a realistic way to minimize the top-metal deposition problem. Instead of directly evaporating a metal layer, a conducting polymer layer is put onto the molecular film first. Our future plans are to reproduce such devices and to implement a more complex molecule, specially designed with desired functionality.

Appendix A

Electrical Measurement Setup

All transport measurements have been performed with a standard transport measurement setup with switches to suit for both crested barriers and molecular junctions. For a dc $I - V$ measurement, we apply a bias voltage V to the device and then measure the current flowing through the circuit using a low-noise, high sensitive sub-femtoamp remote SourceMeter (Model: 6430) from Keityley Instrument Inc. A computer controlled data acquisition GPIB card is used to transfer data to and from the sourcemeter. The applied bias is directly recorded to the computer and the current can be simultaneously read from the preamp. For molecular devices, a high resolution multifunction board (National Instruments NI-PIC-6030E) has been used to provide gate voltages with maximum output voltage of ± 10 V and a resolution of 1.5 mV. The temperature measurements are provided with a Cryogenic Temperature Controller (Model 22) from Cryogenic Control Systems Inc.

Figure A.1 shows the actual view of the whole measurement setup including the device wiring and measurement circuit, metallic probe and sample holder, liquid helium dewar. The metallic probe is made of three components: the electronic box, the 1-inch-diameter tube and the sample holder with metallic shielding. All external electric signals can be applied to or red from the electronic box, and transported to a 5 mm $\times$ 5 mm chip through cable-wirings in the tube and sample holder. Figure A.2 shows the schematic diagram of main electronic wiring circuits in the metallic box. The external electronic signals are coming from the Keithley 6430 source meter ("High", "Low", and "Guard"), the GPIB card (to control 18 relays, corresponding to 18 devices), the DAC card (to provide gate voltage) and the temperature controller. Based on the sample configuration, we can measure both crested-barrier chips and molecular devices just by changing the positions of various switches and an easy step of soldering or detaching one or two wires. When a device is selected, its two terminals are connected to the "High" and "Low" pins of the
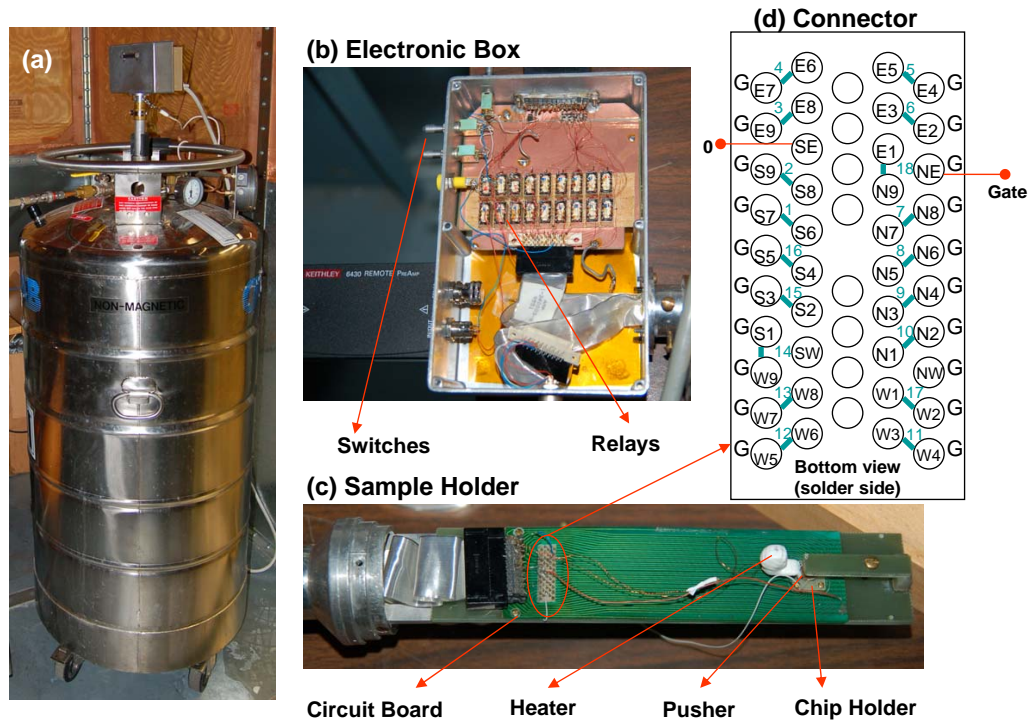
Figure A.1: The actual view of the measurement setup: (a) the liquid helium dewar with an inserted probe, (b) the electronic box which is connected to all external electronic signals, (c) the sample holder which is immersed in the liquid helium, and (d) the bottom view of the connector (solder side) with 40 pins, grouped into 18 junctions (green number). Every other pin is connected to "Guard", marked as "G" at the side. Pin "SE" is connected to ground and pin "NE" is connected to the gate signal. Each pin connects one metallic wire along the circuit board to be contacted with the chip.
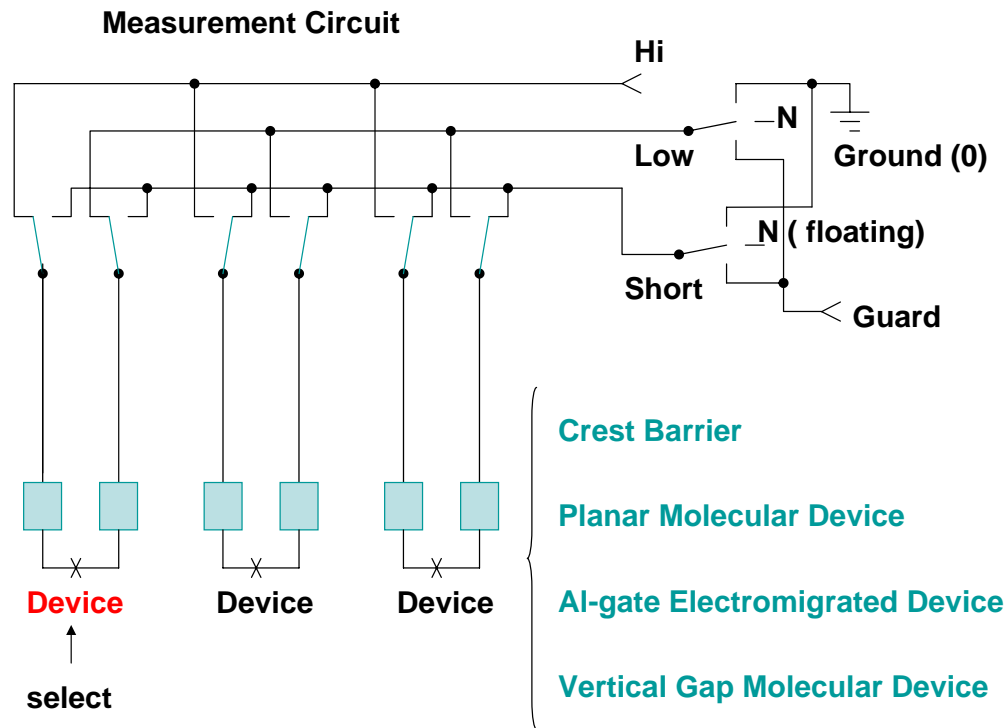
Figure A.2: The schematic diagram of electronic wiring circuit for measurement of crested barrier and molecular junctions.

sourcemeter, where the voltage will be applied to. All the other devices are connected to the third pin "Guard" for protection. This configuration ensures only one device can be measured each time while all the other devices are kept untouched.

The circuit board on the sample holder is made of high resistive material - fiber glass (FR4). To ensure the low leakage current of our setup in the range of 0.01 pA - 0.1 pA, several procedures have to be taken care of. From the circuit design point of view, the wires that provides electronic signals have to be properly shielded to prevent leakage between adjacent parallel wires. In this case, two wires are screened from each other by placing a third wire in between, which is connected to "Guard". Secondly, proper cleaning is needed to ensure extremely low leakage current. Usually we clean the circuit board during the regular maintenance every three months. We use a Q-tips cotton swap or a Kimwipe paper with a few drops of acetone to clean the connector and pins with great care (not to bend or break the pins). Then the board is
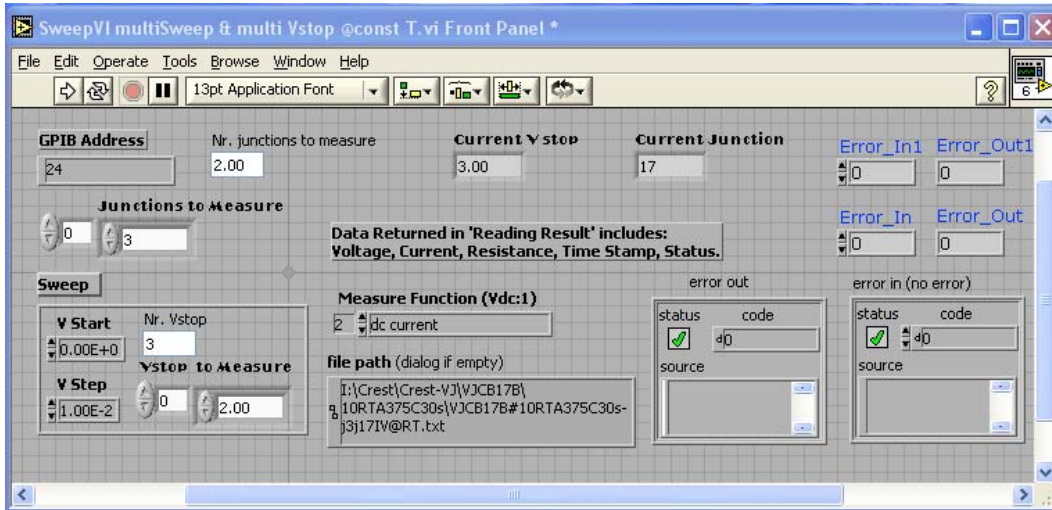
Figure A.3: The front panel of a typical labview program for data acquisition. This program can select any device and perform $I - V$ measurements for any maximum voltages. It can also record temperature.

thoroughly rinsed with IPA (isopropanol), followed by the blow-dry in air or drying with a heater.

All the data have been taken using a custom designed program in the National Instruments LabView programming environment. Figure A.3 shows a typical interface including the real-time monitoring of current, voltage, time and temperature. The automated program can select any desired device and control two voltage outputs: (1) source-drain bias, and (2) the gate bias. It also controls the temperature by automatically adjusting the heating power. It is a very versatile program and has many usefully functions and a large room for further development. All the measurements are automatically controlled by computer. The general sequence of the programs consist of card initiation, selection of junctions, $I - V$ measurements with either applied gate bias or certain target temperature, data acquisition and file input/output.

The general measurement protocol is described as follows for different sample configurations:

Aluminum Oxide Barriers
a. Setup and switches:

For all crested barrier samples, the ground is provided through the southeast corner pin. The white wire from the back of the holder, which connects to this pin, has to be connected to the chassis (*i.e.*, ground). The gate wire

needs to be disconnected from pin 3 (or, "E8", as shows in Figure A.1d) and the pusher. The switch positions on the side of electronic box are listed below: "Low" → nothing (middle position), "Short" → nothing (middle position), and "Gate" → nothing (middle position).

b. Chip cleaning procedures:

The chip is soaked ultrasonically in acetone for 30 seconds to 1 minute, → rinsed with IPA, → soaked in IPA and stay ultrasonically for 30 seconds, → flow-dried in air.

c. General IV measurement procedures:

i. Check junction resistance at room temperature (usually at 50 mV), → to measure IV at room temperature for a few junctions, → break one or a few junctions at room temperature.

ii. Check junction resistance at liquid helium temperature (at 50 mV), → to measure one typical junction (from each area) until hard breakdown, → to measure all the other junctions.

Molecular Devices - Planar Electrodes:

a. Setup and switches:

This type of chips use the chip back (heavily doped silicon) as the gate, so we have to connect the gate wire (white) to the aluminum pusher and disconnect pin 3 (blue wire). The ground wire (white) from the back of the holder is always kept disconnected. The switch positions are listed as follows: "Low" → 0 (*i.e.*, ground), "Short" → nothing or 0, and "Gate" → nothing when we only measure the $I - V$ curves, or "Gate" → "DAC" when we check the gate dependence.

b. Chip cleaning and molecular deposition:

All the chips have been cleaned in the cleanroom. Generally the chip is soaked in acetone and stay ultrasonically for 30 seconds to 1 minute, → rinsed with IPA, → soaked in IPA and stay ultrasonically for 30 seconds to 1 minute, → dried in a stream of N_2, → plasma cleaning for 2 minutes. Then, the chip is immediately transferred to molecular solution and covered with aluminum wrap for self-assembly. The concentration of the molecules is usually set to 1 mg compound in 10 ml toluene. The soaking time varies from 1 hour to 24 hours. After the chip is taken out of the solution, it is rinsed thoroughly with pure toluene and dried in N_2 flow.

c. General $I - V$ measurement procedures:

i. Cool the probe down to the liquid helium and check $I - V$ at 4.2 K.

ii. Check $I - V$ at different gate voltages V_G.

iii. Check $I - V_G$ at different source-drain voltages V.

iv. Lift up the probe and check $I - V$ at different temperatures up to 295

K inside the helium dewar.

Molecular Devices - Electromigration
a. Setup:

If the chip uses its back (silicon) as the gate, please follow the same setup configuration as the planar electrodes. If the chip uses aluminum as the back-gate, the blue wire that is connected to pin 3 has to be soldered to the gate pin. The white wire that connects to the pusher has to be left disconnected. Also, the ground wire to the chassis from the back of the sample holder is always kept disconnected. The chip cleaning procedures are similar to that of the planar electrodes (see Chapter 6 for details).

b. General IV measurement procedures & switch positions:

i. Cool the probe down to 4.2 K.

ii. Check the aluminum oxide quality (gate oxide): "Low" $\rightarrow$ nothing, "short" $\rightarrow$ ground, and "Gate" $\rightarrow$ nothing. Select device 3 to check for overall oxide quality. If device 3 shows a low resistance (*e.g.,* $K\,\Omega$), measure the gate oxide resistance of every junction.

iii. Check the junction resistance at 4.2 K and break junction: "Low" $\rightarrow$ 0, short $\rightarrow$ 0, "Gate" $\rightarrow$ nothing. All junction resistances have been measured at 50 mV. If the resistance of device 3 is about 200 Ω, the aluminum gate wire is considered to be continuous. Before electromigration, the junction resistance is about 30 to 50 Ω. Then, the bias voltage is ramped slowly up at a speed of 1 mV/sec until the breakage of the junction. We usually run IV measurements right after breaking. After breaking all available devices, the IV measurements are repeated for all interesting junctions.

iv. Gate dependence: Based on the IV curves, we select good junctions with strong nonlinear $I - V$ for further gate testing. Here the switch positions are "Low" $\rightarrow$ 0, "Short" $\rightarrow$ nothing, and "Gate" $\rightarrow$ "DAC". We could either run $I - V$ at fixed gate voltage V_G (-2.0 V to +2.0 V), or run $I - V_G$ at fixed source drain V.

v. Check reproducibility: After the gate measurement, we always measure $I - V$ again for interesting devices. The switch positions are: "Low" $\rightarrow$ 0, "Short" $\rightarrow$ 0 and "Gate" $\rightarrow$ nothing.

vi. If the chip survives all above characterizations, we could lift up the probe out of the liquid helium and stay in the helium vapor. The $I - V$ curves are then measured at various temperatures.

Molecular Devices - Crosspoint Structures
a. Setup:

The current setup is the same as the one used for electromigration except

that there is no aluminum gate oxide available. Generally, we disconnect pin 3 from the gate pin, and disconnect the ground wire at the back of the sample holder. We could still use the back of the chip as the gate (silicon, not very effective however) by connecting the white wire to the gate pin, where the white wire is always wired to the aluminum pusher. The cleaning procedures are described in details in Chapter 7.

b. Switch positions:

For $I - V$ measurements, we usually put "Low" $\rightarrow$ 0, "Short" $\rightarrow$ 0 or nothing, and "Gate" $\rightarrow$ nothing. For gate dependent IV measurements , we just change the "Gate" pin to "DAC" position.

c. General IV measurement procedures:

i. Check leakage current for all junctions before wet-etch at room temperature.

ii. After the aluminum oxide is etched in phosphorous acid, we check the leakage current again at room temperature.

iii. After molecular deposition, We check $I - V$ at liquid helium temperature first. Then, the probe is lifted up to the helium vapor phase and $I - V$ is measured at various temperatures.

Appendix B

Ellipsometry Measurement for Self-assembled Molecules

Ellipsometry provides a nondestructive method for measuring both thickness and refractive index of transparent films. It is very useful for thin films for accurate measurement of film thickness. We have performed ellipsometry measurements for self-assembled monolayers (SAMs) of oligo(phenylene-ethynylene) bridges (with both $n = 1$ and $n = 2$ [187]) on Pt substrate. To prepare for SAMs, we soaked the fresh grown Pt substrate in molecular solution at room temperature for periods of 20 hours under ambient conditions. We always kept the Pt substrate in oxygen-free environment for storage. For not-fresh grown Pt substrate, it has always been subjected to a few steps of cleaning procedures: first it was ultrasonically rinsed by acetone and IPA, then it was transferred to plasma chamber for further cleaning for 2 minutes, followed by a through rinse with ethanol for 10 minutes and dried in a flow of nitrogen and ready for molecular self-assembly.

The substrate was measured by the ellipsometor before the deposition of molecules, in order to determine the average refractive index n_s and extinction coefficient k_s. We use a dual-mode automatic ellipsometer with He-Ne laser light of wavelength 632.8 nm at a 70° incident angle. The thickness of the SAMs was measured based on a refractive index of $n_f = 1.5$, $k_f = 0$. Table B.1 summarize the measurement results for OPE bridges. We could see that longer molecules ($n = 2$) tend to lay down on the metal surface instead of standing up. By modifying one CN- terminal of the OPEs bridge by a hydrophilic group, the molecule is not symmetric any more (figure B.1). Such molecules can be used for Langmuir-blodgett films, which is constructed by transferring mono-layers floating on water surface to a solid substrate. Such molecules have also used for self-assembly for comparison. They both show reasonable thickness, comparable to the expected or calculated molecular length.
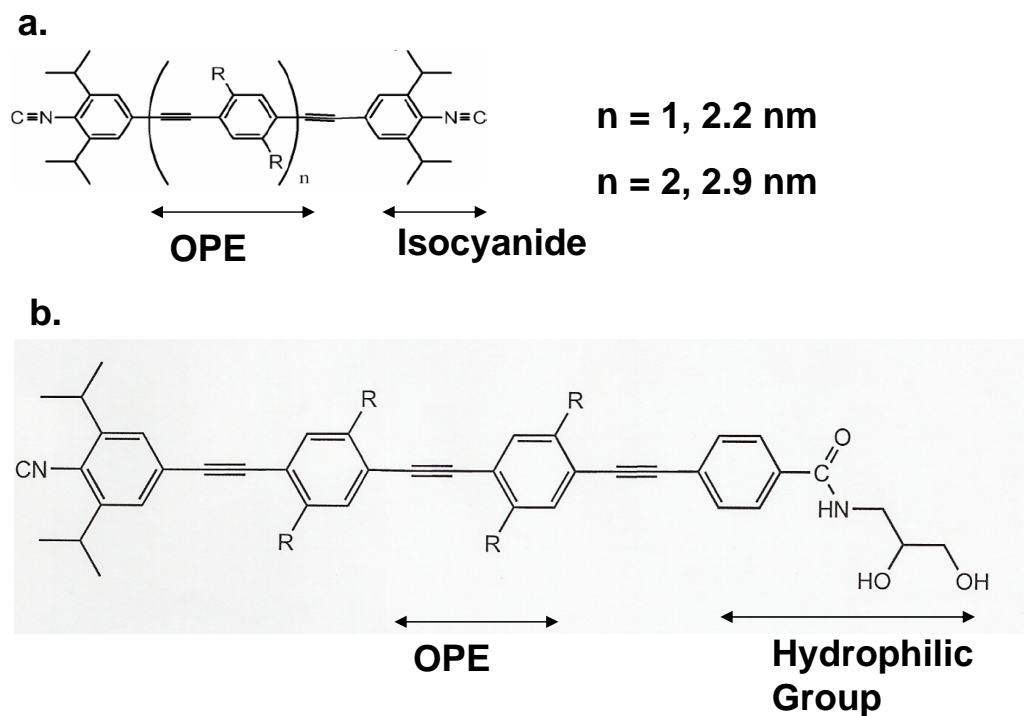
Figure B.1: Two type of OPE molecules for ellipsometry measurements: a. symmetric OPE molecule with n = 1, or 2; b. asymmetric OPE molecule with one hydrophilic terminal groups.

OPE rings	Terminal Groups	Method	Calculated Length (nm)	Measured Thickness (nm)
n = 1	Both CN	SAM	2.2	1.72 ± 0.13
n = 2	Both CN	SAM	2.9	1.2 ± 0.1
n = 2	CN + OH groups	SAM	2.9 +2	3.57 ± 0.30
n = 2	CN + OH groups	LB	2.9 +2	3.45 ± 0.26

Table B.1: Ellipsometry measurement of OPE SAMs.

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