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**PROCESS DEVELOPMENT FOR  
HIGH SPEED SUPERCONDUCTOR  
MICROELECTRONICS FOR  
DIGITAL AND MIXED SIGNAL  
APPLICATIONS**

A Dissertation Presented

by

**Daniel T. Yohannes**

to

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in Partial Fulfillment of the Requirements

for the Degree of

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in

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Abstract of the Dissertation

**PROCESS DEVELOPMENT FOR HIGH  
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2008

After half a century of enormous successes and complete dominance, semiconductor electronics based on silicon Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) is fast approaching its limits for high-end applications in telecommunications, computing and routing. Digital superconductor electronics (SCE) based on the Rapid Single Flux Quantum Logic (RSFQ) is considered a viable low risk alternative to Si CMOS circuits, due to its potential for ultra-high operating frequency and ultra-low power dissipation. The most developed and reliable superconductor electronics fabrication technology is based on the externally shunted  $Nb/Al/AlO_x/Nb$  Josephson tunnel junctions (JJ). The technology level is characterized by the  $Nb/Al/AlO_x/Nb$  trilayer critical current density,  $j_c$ , and the minimum junction size,  $a$ . The maximum clock frequency of the RSFQ-based SCE circuits scales as square root of  $j_c$  and inversely proportional to  $a$ . The main goals of the

thesis work is: first, to research the physical limitations of the existing methods of making SCE and restrictions on the circuit complexity and speed; second, to develop a reliable and scalable SCE fabrication process that is capable of making high-speed complex circuits for digital and mixed signal applications; and third to implement the results at a commercial SCE foundry at HYPRES Inc. To this end, an advanced fabrication process with  $4.5 \text{ kA/cm}^2$  critical current density JJ has been developed. The process is based on an enhanced lithography and thin film processes and incorporates an additional anodization step for JJ protection. A simple approach for scaling of the existing circuit designs to newer higher  $j_c$  processes has been proposed and implemented. A great number of complex digital circuits  $> 10^4 \text{ JJ}$  operating at clock frequencies in excess of 30 GHz has been fabricated for the first time as well as less complex (about 500 JJs) circuits operating above 40 GHz and simple circuits with about 20 JJs operating to about 400 GHz. The maximum operating frequency as well as the complexity of SCE circuits has been doubled with respect to the previous state-of-the-art as a result of this work.

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# Publications

The following are list of publications that I have authored, co-authored, presented and co-presented:

1. Sergey K. Tolpygo, Denis Amparo, Alex Kirichenko and Daniel Yohannes, "Plasma process-induced damage to Josephson tunnel junctions in superconducting integrated circuits," *Supercond. Sci. Technol.*, vol 20, No 11, pp. s341 - s349, November 2007.
2. Daniel T. Yohannes and Sergey K. Tolpygo, "Resolution enhancement technique for advanced superconductor microelectronic circuits with sub micron Josephson junctions", *International Superconductive Electronic Conference: Extended Abstracts*, pp. P-T05, June 2007.
3. D. Yohannes, A.F. Kirichenko, S. Sarwana, and S.K. Tolpygo, "Parametric testing of HYPRES superconducting integrated circuit fabrication process," *IEEE Trans. Appl. Supercond.*, vol. 17, No. 2, pp. 181-186, June 2007.
4. S. K. Tolpygo, D. A. Donnelly, R. T. Hunt, J.A. Vivalda, D. Yohannes, D. Amparo, A.F. Kirichenko. "20.0  $kA/cm^2$  process development for superconductor integrated circuits with 80 GHz clock frequency," *IEEE Trans. Appl. Supercond.*, vol. 17, No. 2, pp. 946-951, June 2007.
5. D. Yohannes, S. Sarwana, S.K. Tolpygo, A. Sahu, Yu.A. Polyakov, and V.K. Semenov, "Characterization of HYPRES' 4.5  $kA/cm^2$  and 8.0  $kA/cm^2$  Nb/AlOx/Nb fabrication process," *IEEE Trans. Appl. Supercond.*, vol. 15, No. 2, pp. 90-93, June 2005.
6. A. F. Kirichenko, S. Sarwana, D. Gupta, and D. Yohannes, "Superconductor digital receiver components," *IEEE Trans. Appl. Supercond.*, vol. 15, No. 2, pp. 249-254, June 2005.
7. S. K. Tolpygo, D. A. Donnelly, R. T. Hunt, J.A. Vivalda, D. Yohannes. "HYPRES' advanced fabrication processes for superconducting high speed

digital electronics and quantum computing,” presented at Applied Superconductivity Conference, August 2004, Jacksonville, FL, USA, unpublished.

8. W. Chen, V. Patel, S. K. Tolpygo, D. Yohannes, S. Pottorf, and J. E. Lukens, ”Development toward high-speed integrated circuits and SQUID Qubits with  $Nb/Al/AlO_x/Nb$  Josephson junctions,” *IEEE Trans Appl. Supercond.*, vol. 13, pp. 103-106, June 2003.

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1. Igor V. Vernik, Dmitri E. Kirichenko, Vladimir V. Dotsenko, Robert Miller, Robert J Webber, Pavel Shevchenko, Andrei Talalaevskii, Deepnarayan Gupta and Oleg A. Mukhanov, ”Cryocooled wideband digital channelizing radio-frequency receiver based on low-pass ADC,” *Supercond. Sci. Technol.*, vol 20, No 11, pp. s323 -s327, November 2007
2. Deepnarayan Gupta, et.al., ”Digital Channelizing Radio Frequency Receiver,” *IEEE Trans. Appl. Supercond.*, vol. 17, No. 2, pp. 430-437, June 2007.
3. Igor V. Vernik, et al., ”Superconducting High-Resolution Low-Pass Analog-to-Digital Converters ,” *IEEE Trans. Appl. Supercond.*, vol. 17, No. 2, pp. 442-445, June 2007.
4. Alex Kirichenko, Deepnarayan Gupta, and Saad Sarwana, ”RSFQ Asynchronous Switch Matrix,” *IEEE Trans. Appl. Supercond.*, vol. 17, No. 2, pp. 505-507, June 2007.

# Chapter 1

## MOTIVATION

### 1.1 Extended abstract

After half a century of enormous successes and complete dominance, semiconductor electronics based on Si Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) is fast approaching its limits for high end applications in telecommunications, computing and routing. Although the semiconductor industry continues to find more and more sophisticated, elaborate and creative ways of increasing the speed of CMOS circuits by shrinking the size and packing more and more transistors on chips, other semiconductor materials, physical concepts, and viable technologies are being developed to replace or supplement the Si-based industry in the most critical and demanding applications. Among the most frequently cited are compound semiconductors for non-classical CMOS (SiGe, GaAs, GaN, InP, etc.), nanotechnology (carbon nano-tubes), molecular electronics, and superconductor electronics.

Superconductor digital electronics based on the Rapid Single Flux Quantum Logic - RSFQ [14] has been considered a low risk alternative to Si CMOS circuits [15, 16] due to its potential for ultra-high operation frequency and ultra-low power dissipation. At the heart of RSFQ logic is the Josephson junction, the main switching element, which is as essential to superconductor electronics as the transistor is to semiconductor electronics. The most developed and reliable superconductor electronics fabrication technology is based on externally shunted  $Nb/Al/AlO_x/Nb$  Josephson tunnel junctions [17–19]. The maximum clock frequency of RSFQ-based circuits scales basically as square root of  $j_c$  or  $1/a$ , where  $j_c$  is the Josephson critical current density and  $a$  is the typical size of the junctions. Therefore, the technology level can be characterized by the  $Nb/Al/AlO_x/Nb$  tri-layer critical current density and the minimum junction size. At the beginning of this thesis work, aside from the

university labs, e.g. [20], there existed three main fabrication facilities for superconductor digital circuits each using  $Nb/Al/AlO_x/Nb$  junctions and their own proprietary process:

1. HYPRES, Inc. (Elmsford, New York) process with  $1.0 \text{ kA/cm}^2$  critical current density and  $3.5 \text{ }\mu\text{m}$  minimum Josephson junction size.
2. TRW and then Northrop-Grumman Space Technology (NGST) (Redondo Beach, CA) process with  $2.0 \text{ kA/cm}^2$  and  $2.5 \text{ }\mu\text{m}$  junction diameter [3]. The NGST facility has not been operational since the end of 2004.
3. NEC and later SRL ISTECH (Tsukuba, Japan) process with  $2.5 \text{ kA/cm}^2$  and  $2.2 \text{ }\mu\text{m}$  junctions [21].

At the beginning of the thesis work, the state-of-the-art in the superconductor electronics industry was considered to be digital circuits containing about 6000 Josephson junctions (JJs) and capable of operating at a clock frequency of about  $19.6 \text{ GHz}$  with a minimum junction size about  $3.5 \text{ }\mu\text{m}$ , such as Analog-to-Digital Converters [22, 23]. The ultimate potential of superconductor electronics circuit speed was demonstrated by SUNY-Stony Brook researchers by using very simple circuits, static-frequency dividers containing around 10 JJs operating at frequencies up to  $770 \text{ GHz}$  [4, 5]. For complex circuits this may translate into about  $100 - 120 \text{ GHz}$  clock frequencies. The fabrication technology used [24, 25], however, employed electron-beam lithography for Josephson junction definition and only two superconducting layers, and therefore could not be readily extended or adapted for a large scale superconductor integrated circuit fabrication. The main goals of the thesis work has been **a)** to research the physical limitations of the existing methods of making superconducting electronics circuits and restrictions on the circuit complexity and speed, **b)** to develop a reliable and scalable superconducting electronics fabrication process that would enable doubling the circuit complexity and speed with respect to the state-of-the-art, i.e. to develop a process capable of making complex digital circuits operating at  $40 \text{ GHz}$  and above for digital and mixed signal applications, and **c)** implement the results at a commercial superconductor electronics foundry at HYPRES Inc.

The ultimate goal of superconductor microelectronic fabrication technology based on  $Nb/Al/AlO_x/Nb$  junction technology is to make complex superconducting chips operating up to about  $120 \text{ GHz}$ . There are at least two ways to achieve this. First, one can start with the highest practical critical current density and the smallest possible JJ size by using the most advanced lithography available such as e-beam lithography. Such a technology would initially

allow fabrication of very simple circuits containing just less than 50 JJs as was demonstrated in SUNY-Stony Brook. Then, one can start increasing the circuit complexity level by designing more complex circuits, adding extra layers of metals and dielectrics, improving lithography and chemical mechanical planarization, etc. The problem with this approach is that the integration level required to make really useful digital circuits (which would justify the cost of this technology development) starts at greater than 5000 JJs and needs at least four superconducting layers, making the gap technologically challenging to close.

The second approach is to start with already demonstrated complex chips currently having low operation frequencies (and large JJs) and sequentially develop processes with ever increasing Josephson critical current density and, correspondingly decreasing JJ size. For instance, take the existing process at HYPRES capable of making about 6000 JJs with  $1.0 \text{ kA/cm}^2$  critical current density and increase the operating frequency by increasing the  $j_c$ . Then the number of JJs can be increased in order to reach the next level of the circuit's functionality and so on. This approach has been chosen for this thesis work. From the technology development standpoint, this set of goals requires that the tri-layer critical current density increased at least by a factor of four and the junction size scaled down by a factor of two. Also, many other process modifications, which will be discussed in detail later, needed to be made. As a result, a  $4.5 \text{ kA/cm}^2$  critical current density process with a minimum junction radius of  $0.94 \text{ }\mu\text{m}$  has been developed and standardized, and is accepted as the advanced process at HYPRES Inc., while a  $20.0 \text{ kA/cm}^2$  critical current density with a minimum junction radius of  $0.5 \text{ }\mu\text{m}$  is under development. A list below summarizes the main results and accomplishments of this work:

1. It was found that the minimum JJ size and, hence, the maximum operating frequency of the digital circuits in the technology that was available at the beginning of the thesis work (that will be referred to as HYPRES "old process") are limited by the diffraction effects in the optical lithography system and by the poor choice of the JJ shape (square) [26].
2. It was found that the maximum integration level of superconducting digital circuits in the HYPRES "old process" was limited by random structural defects, micro-shorts between the superconducting layers, and poor control over the line-width of superconducting strips forming circuit inductances. The last two were found to be a result of a particular choice of the layer process sequence and a reaction between an Al layer, a part of  $Nb/Al/AlO_x/Nb$  tri-layer, and processing chemicals [1].
3. An enhanced optical lithography process for JJ definition has been devel-

oped that uses a shorter wavelength for optical lithography and circular-shaped junctions in order to minimize diffraction-induced distortions of the junction shape and area. Electric and SEM characterization of JJ has been made [26].

4. A resolution enhancement technique (RET) was developed for defining square and rectangular junctions. The RET is based on the double-exposure of mutually orthogonal lines [27].
5. The minimum JJ size was reduced from about  $3.5 \mu\text{m}$  square JJ to  $1.2 \mu\text{m}$  circular JJ and to  $0.8 \mu\text{m}$  for the RET-defined square JJs[28].
6. A  $1\sigma$  ( $\sigma$  is the standard deviation) spread of the critical currents of Josephson junctions of 1.2% has been achieved in arrays of 100 Josephson junctions; and a 2.4% spread across  $5 \times 5 \text{ mm}$  chip [26].
7. An advanced fabrication process with  $4.5 \text{ kA}/\text{cm}^2$  critical current density has been developed. The process is based on the advanced lithography process and incorporates an additional anodization step for JJ protection. The new process is immune to the problems of the HYPRES "old process" listed in (2) above [26].
8. A simple approach for scaling the existing circuit designs to newer higher  $j_c$  processes has been proposed and implemented. It allows for fast and low cost improvements in the circuit speed [7, 28]
9. Fabrication process control and monitoring has been developed and implemented to control the Josephson junction quality and uniformity across 150-mm wafers as well as thin film resistors, inductors, and other circuit parameters [28].
10. A great number of complex digital circuits with greater than  $10^4$  JJ operating at clock frequencies in excess of  $30 \text{ GHz}$  have been fabricated for the first time [6, 29] as well as less complex about 500 JJs circuits operating above  $40 \text{ GHz}$  [7] and simple circuits with about 20 JJs operating at around  $400 \text{ GHz}$  [1]. As the result of this thesis work, both the maximum operating frequency of superconducting integrated circuits and their complexity has been doubled with respect to the previous state-of-the-art.

## 1.2 Thesis outline

The thesis is organized as follows: first the subject matter and the physics behind the thesis work will be introduced by very briefly going through the series of experimental discoveries, theoretical explanations and predictions starting from the discovery superconductivity in 1911 to the prediction of Josephson effect in 1961. Then details of the Josephson junction dynamics will be presented setting the physics background to the RSFQ technology; concluding that the technology level and hence the maximum operating frequency of devices is defined by the critical current density of the Josephson junction. The maximum operating frequency scales as the square root of the critical current density and hence inversely proportional to the junction size.

The third chapter introduces the preferred fabrication technology for superconductor micro-electronics ( $Nb/Al/AlO_x/Nb$ ) tri-layer based junctions together with its integration to multi-layer process, which is one of the main requirements for making functional digital circuits. Then we will introduce the existing state of the art fabrication technology at the beginning of this thesis work referred as "old" fabrication process and its shortcomings for scaling it to the next level from for higher critical current density processes. The limitations include: scaling the shunted junctions (critical current density and sheet resistance), the size and shape of the junctions, control of inductances, limited integration level due to the above factors compounded by inter-layer shorts caused by poor inter-layer dielectric deposition. Then we will go through the solutions to these limitations: changing the junction shape, improving lithography, using anodization for junction passivation, inverting layer process sequence and using PECVD for the inter-layer dielectric. Next the details of the process flow for the proposed new fabrication process will be discussed. This is followed by an explanation of the unit fabrication process consisting of thin film deposition, photolithography, etching and wet-chemical process. The chapter ends with a summary of the re-targeting approach will be given for re-designing circuits from the low to the high critical current density process.

The fourth chapter introduces the parameters for the building blocks of RSFQ circuits, i.e., the Josephson junctions, resistors, inductors and interconnects. Emphasis is given to the experimental evaluation of fabrication and design parameters and process control. The fifth chapter covers the implementations of the new process for digital and mixed signal applications starting from the simple 20 JJs digital frequency divider operating up to 400  $GHz$  to the most complex All Digital RF-receiver with more than 10,000 JJs operating up to 34  $GHz$  and its components with more than 500 JJ operating up to 44  $GHz$ . The sixth chapter will discuss the main results on fabrication, process monitor control; and digital and mixed signal applications.

# Chapter 2

## INTRODUCTION

### 2.1 Historical overview

The remarkable physical phenomenon of superconductivity was discovered by Kamerlingh Onnes in 1911 by observing electric resistance of mercury dropping to zero below a certain critical temperature  $T_c$  at about 4.2 K [30]. In about a year he reported that sufficient electric current and magnetic field could restore the resistive nature of the sample. Zero resistance is a fundamental property of all superconductors. Another fundamental property is the expulsion of magnetic flux from a conventional superconductor in its superconducting state - ideal diamagnetism. It was discovered experimentally by Meissner and Ochsenfeld in 1933 and commonly referred as the Meissner effect [31]. In 1935 two brothers F. and H. London introduced a phenomenological theory to describe the microscopic (local) electric and magnetic fields in superconductors. It turns out that in the Meissner effect, magnetic fields do not penetrate the superconductor to some depth called the magnetic penetration depth (the London penetration depth  $\lambda_L$ ) and is expelled completely from the bulk. Above a certain temperature dependent critical magnetic field  $H_c$  the superconducting state is destroyed. The group of superconductors that are described by a single critical magnetic field are called type-I. Discovered by L. V. Shubnikov in 1937, type-II superconductors on the other hand are characterized by two critical fields  $H_{c1}$  and  $H_{c2}$ . Below  $H_{c1}$  they behave like Type-I. As the magnetic field is increased above  $H_{c1}$  it starts to penetrate the bulk of the superconductor in the form of Abrikosov vortices predicted by A.A. Abrikosov in 1957 and experimentally discovered soon after. The number of vortices grows with the magnetic field until superconductivity is destroyed above  $H_{c2}$ . Bulk pure niobium, being a type-II superconductor, has the highest critical field (about 0.2 T) as well as the highest critical temperature about



9.2 K among elemental superconductors, as was discovered in 1930. Coupled with the fact that it is a refractory metal makes it the superconductor of choice for many low temperature superconducting microelectronic applications. E. Maxwell and C. A. Reynolds study of different superconducting isotopes of Mercury established a relationship between the critical temperature  $T_c$  and the isotope mass  $M$ :  $T_c M^{1/2} = Constant$  [32]. This was a follow up to the proposal in 1950 by H. Frochlich that the effect of vibrating atoms on superconductivity could be investigated by the isotope effect which would establish whether or not lattice vibrations play a role in the interaction responsible for the superconductivity. The prediction and observation of the isotope effect paved the way to the microscopic theory of superconductivity. In 1956 Leon Cooper showed that, in the presence of a very weak electron-phonon (lattice) interaction, two conducting electrons are capable of forming a stable paired state in "momentum space". After the discovery of the isotope effect this was the second and the last breakthrough leading to the microscopic theory of superconductivity. Indeed a year later in 1957 the microscopic theory of superconductivity in metals was formulated by J. Bardeen, L. Cooper and R. Schrieffer - BCS theory [33, 34]. The central concept of the BCS theory is a weak electron-phonon interaction, which leads to the appearance of an attractive potential between pairs of electrons with opposite momenta and spin [35]. These paired electrons are now referred to as the Cooper pairs. Cooper pairs obey the Bose-Einstein statistics and condense to the lowest energy levels at low temperatures. Quantum-mechanical tunneling of Cooper pairs through a thin insulating barrier of the order of a few nanometers between two superconductors was theoretically predicted by B. D. Josephson in 1962 [36]. This effect - known as Josephson effect- is the frame work for superconductor electronics. The rest of the introduction is dedicated to describing the physics and dynamics of the device called the Josephson junction.

## 2.2 Josephson junction dynamics

Consider two superconductors separated by an insulator of thickness  $\delta x$ . If  $\delta x$  is larger than about  $100\text{\AA}$  the two superconductors are uncoupled [37–39],

$$i\hbar \frac{d}{dt} \psi_1(t) = E_1 \psi_1(t) \quad (2.1)$$

$$i\hbar \frac{d}{dt} \psi_2(t) = E_2 \psi_2(t) \quad (2.2)$$

$E_1$  and  $E_2$  are energies of the Cooper pair condensate. If a potential is maintained across the insulator  $E_1$  will be different from  $E_2$  by  $2eV$ :

$$E_1 - E_2 = 2eV \quad (2.3)$$

When the two superconductors are brought in to a close contact but separated by a weak link such as about  $10 \text{ \AA}$  of dielectric a junction called "Josephson junction" is formed. Josephson tunneling can occur and the two wave functions are correlated:

$$i\hbar \frac{d}{dt} \psi_1(t) = E_1 \psi_1(t) + K \psi_2 \quad (2.4)$$

$$i\hbar \frac{d}{dt} \psi_2(t) = E_2 \psi_2(t) + K \psi_1 \quad (2.5)$$

where  $K$  is real coupling constant. Since the wavelength characterizing the Cooper pairs is much bigger than the junction width  $\delta x$ . The phase of the quasi-wave function does not change much when  $x$  is of the order of  $\delta x$  making it possible to assume that each superconductor has a position independent phase

$$\psi_j(t) = \sqrt{n_j(t)} \exp i\theta_j \quad (2.6)$$

where  $n_j$  is the Cooper-pair density of superconductors, and is position-independent for each superconductor. Substituting equation 2.6 into equations 2.4 and 2.5 respectively, and equating real and imaginary parts we get:

$$\hbar \dot{n}_1 = K \sqrt{n_2 n_1} \sin(\phi), \quad \hbar \dot{n}_2 = -K \sqrt{n_1 n_2} \sin(\phi) \quad (2.7)$$

$$\hbar \dot{\theta}_1 = E_1 + K \frac{n_2}{n_1} \cos(\phi), \quad \hbar \dot{\theta}_2 = E_2 + K \frac{n_1}{n_2} \cos(\phi) \quad (2.8)$$

where  $\phi = \theta_2 - \theta_1$  is the gauge invariant phase difference of the electrode wave functions. For steady state condition, i.e.,  $n_1 = n_2 = n_0$  the rate of change of Cooper pair density will be:

$$I \propto \dot{n}_1 = -\dot{n}_2 = \frac{K}{\hbar} n_0 \sin(\theta) \quad (2.9)$$

The proportionality constant depends on the charge ( $2e$ ) of the Cooper pairs:

$$I = I_c \sin(\theta) \quad (2.10)$$

Where  $I_c = 2en_0/\hbar$  is the maximum super-current which the weak link can support and is linear in Cooper pair density  $n_0$  and in the junction energy constant  $K$ . Taking the difference of the two equations in equation 2.8 and making use equation 2.3 of we get the time evolution of the phase difference :

$$\dot{\phi} = \frac{2e}{\hbar}V \quad (2.11)$$

Equations 2.10 and 2.11 are commonly referred to us the DC and AC Josephson effects respectively after their first prediction by B. D. Josephson in 1962 [36]. Later experimentally confirmed by P. W. Anderson [40] of the fact that a weak link between two superconducting electrodes maintains superconducting current with no energy loss and is a function of the phase difference between the electrodes. Besides the cooper-pair tunneling described by equations 2.10 and 2.11, there is conduction due to quasi-particle tunneling given by [41]:

$$I_{qp} = \int \frac{|E|}{\sqrt{|E^2 - \Delta^2|}} \frac{|E + eV|}{\sqrt{|(E + eV)^2 - \Delta^2|}} [f(E) - f(E - eV)] dE \quad (2.12)$$

where  $\Delta$  is the superconducting gap in the electrodes,  $f(E)$  is the Fermi distribution, and the constant of proportionality is related to the tunneling matrix element. A typical IV characteristic of an unshunted  $Nb/AlO_x/Nb$  Josephson junction depicting the superconducting and quasi-particle branches the conduction is shown in figure 2.1 [25, 42].

## 2.3 RCSJ model

For superconducting microelectronic applications the Josephson junction is modeled by the Resistively Capacitively Shunted Junction (RCSJ) model as shown in figure 2.2. The total current is the sum of the Josephson tunnel current equation 2.10, the quasi-particle current equation 2.12, the displacement current through the junction capacitance  $C$  and the current through the external shunt resistor (if there is one):[43]

$$I = I_c \sin \phi + I_{qp} + C \frac{dV}{dt} + I_R \quad (2.13)$$

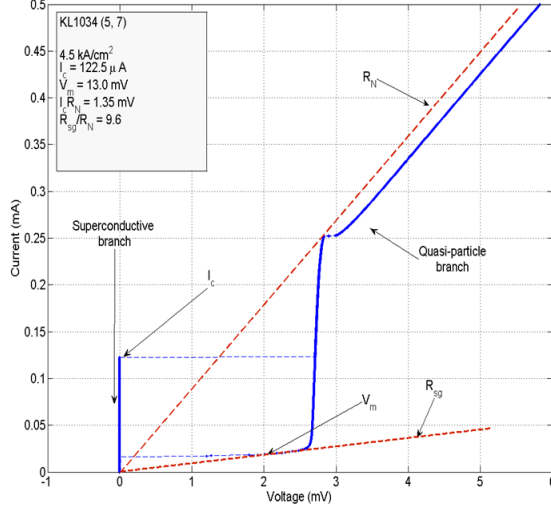


Figure 2.1: Typical IV characteristic measured for unshunted Josephson junctions, showing two branches: the superconducting branch and the quasi-particle branch.

Representing the effective resistance  $R_{eff}$  as the parallel combination of quasi-particle current resistance

$$R(V) = \begin{cases} R_N, & \text{for } V > V_g \\ R_{sg}, & \text{for } V < V_g \end{cases}$$

and the external shunt resistance. Where  $R_N$  is normal resistance to the tunneling electrons and  $R_{sg}$  is the quasi-particle resistance. Making use of equation 2.11, equation 2.13 can be rewritten as

$$\frac{1}{\omega_p^2} \frac{d^2 \phi}{dt^2} + \frac{1}{\omega_c} \frac{d\phi}{dt} + \sin \phi = i \quad (2.14)$$

Where

$$\omega_c = \frac{2e}{\hbar} R_{eff} I_c \equiv \frac{2\pi}{\phi_0} I_c R_{eff} \quad (2.15)$$

is the characteristic frequency of the junction and

$$\omega_p = \sqrt{\frac{2e I_c}{\hbar C}} \equiv \sqrt{\frac{1}{L_J C}} \quad (2.16)$$

is the plasma frequency of oscillation. and  $L_J$  is the Josephson inductance

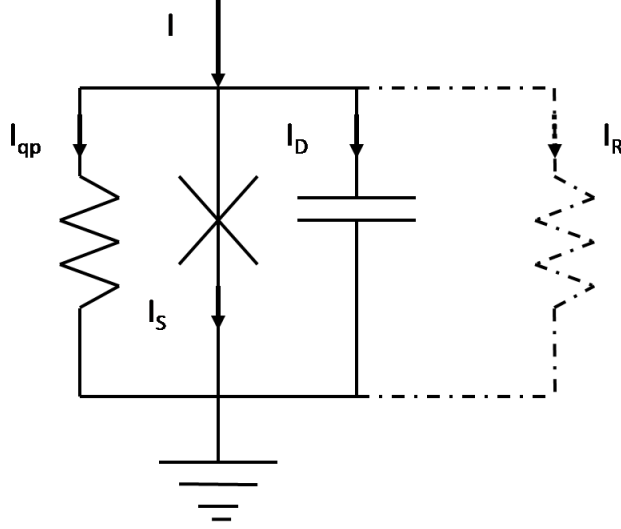


Figure 2.2: Equivalent circuit of a Josephson junction, showing resistively and capacitively shunted junction (RCSJ-model) with a current bias. The total current is divided into four branches: The super-current ( $I_S$ ), the quasi-particle current ( $I_{qp}$ ) through the sub-gap resistance ( $R_{sg}$ ), the displacement current ( $I_D$ ) across the junction capacitance and the current through the external shunt resistance ( $I_R$ )

given by:

$$L_J \equiv \frac{\phi_0}{2\pi I_c} \quad (2.17)$$

Equation 2.16 shows that the plasma frequency is independent of the junction area as both the critical current and the junction capacitance are proportional to the area. Since the critical current depends exponentially on the barrier thickness while the specific capacitance scales inversely proportional to it, the plasma oscillation frequency roughly scales proportional to the square root of the critical current density. More discussion of this argument is given in the next section.

Damping is described by the McCumber-Stewart parameter [44, 45] which is given by the ratio of the characteristic frequency to the plasma frequency squared:

$$\beta_c = \frac{2\pi}{\phi_0} I_c R_{eff}^2 C \quad (2.18)$$

For unshunted junctions  $\beta_c \gg 1$ , to critically damp the junctions a  $\beta_c = 1$  is required. Thus the value of the shunt resistance is chosen such that the plasma oscillation frequency is equal to the characteristic frequency. The value of the shunt which would be much smaller than the sub-gap resistance is calculated from:

$$R_{shunt} = \left[ \frac{1}{A} \left( \sqrt{\frac{2\pi}{\phi_0} j_c C_S} - \frac{j_c}{V_m} \right) \right]^{-1} \quad (2.19)$$

where  $V_m = R_{sg} I_c$  is the measure of the junction quality, and  $A$  is the area of the junction. Equation 2.19 shows that  $R_{shunt}$  scales inversely proportional to the square-root of the critical current density.

## 2.4 Rapid Single Flux Quantum (RSFQ) logic

In 1985 Likharev, Mukhanov, and Semenov [46] proposed, the use of picosecond voltage pulses generated by shunted Josephson junctions  $V(t)$  (SFQ pulses) with quantized area of

$$\int V(t) dt = \phi_0 \sim 2.07 \text{ mV} \times \text{ps} \quad (2.20)$$

to represent logic instead of using voltage state logic [47]. This proposal opened the way for fast and scalable superconducting microelectronic integrated circuits. The fact that elementary circuits comprising an appropriately shunted Josephson junction can be easily used to "generate" from DC, "store" in the form of flux and "convert" back to DC and governed by the simple but elegant Josephson relations described by equation 2.11 and equation 2.12 makes the approach novel. Soon, a complete RSFQ logic / memory family was developed [14]. The generation of SFQ pulses can be well understood by considering a simple circuit with just one Josephson junction - a device commonly called a SQUID (Superconducting QUantum Interference Device) illustrated in figure 2.3 [48]:

The total magnetic flux through the loop is the difference between the external applied flux and flux generated in the loop by the circulating current.

$$\Phi = \Phi_{ext} - LI \quad (2.21)$$

This flux is related to the phase difference across the Josephson junction (Faraday's induction law) as:

$$\frac{d\Phi}{dt} = V \equiv \frac{\phi_0}{2\pi} \frac{d\phi}{dt} \quad (2.22)$$

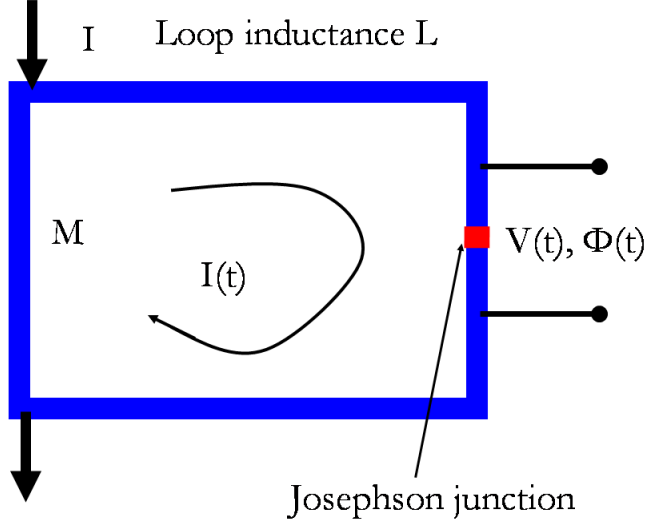


Figure 2.3: Simplest SFQ pulse generator circuit (SQUID).

Hence equation 2.21 can be rewritten by making use of equations 2.22, 2.10 and 2.13 as

$$\phi + \frac{L}{L_J} \sin \phi = \phi_{ext} \quad (2.23)$$

where  $\phi_{ext} = \phi_0/2\pi\Phi_{ext}$ , equation 2.23 has unique solution as a function of  $\phi$  if  $L/L_J$  is less than one, which means that a Josephson junction with small critical current suppresses the quantization effect of the superconducting loop. However if  $L/L_J$  is large enough, equation 2.23 has several stationary stable states for the same external field, implying that insertion of a Josephson junction with large critical current retains the flux quantization effect. The Josephson junction, however, limits the number of stable flux states to  $N \cong L/(\pi L_J)$ . In particular for a typical RSFQ circuit  $L \cong 2\pi L_J$  allowing for only two stable flux states. Switching between the two states may be achieved by changing the external flux (via changing the external current). The switching can be interpreted as the junction exceeding its critical current; the excess current being carried by the normal current. This develops a voltage across the junctions, and according to the Josephson AC relation equation 2.11 the phase difference will start to evolve moving beyond its critical value. This will further decrease  $I_c$  leading to the growth of  $I_N$  and  $V$  and the rate of phase difference. This positive-feedback leads to exponential growth of the phase stopping only when the phase has come close to its initial value plus  $2\pi$ , i.e.;

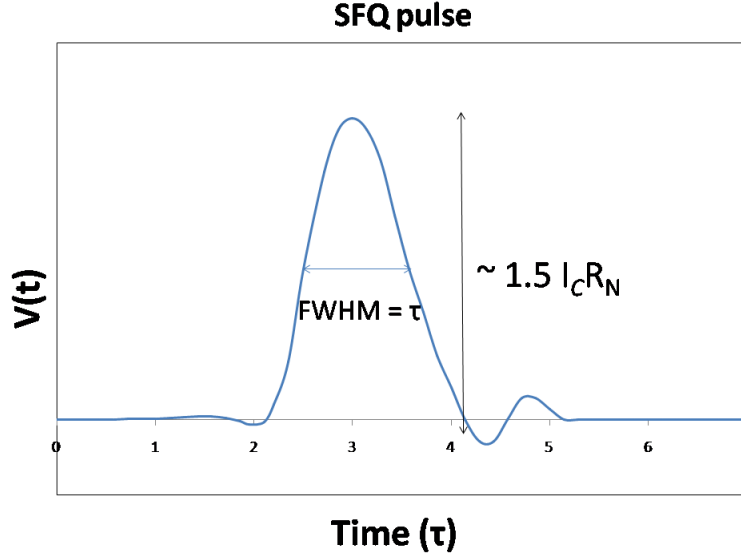


Figure 2.4: An SFQ pulse with quantized area of  $\phi_0$ , pulse height is  $\sim 1.5 I_c R$  and the FWHM is the ratio of quantized area to the pulse height equation 2.24

when a  $2\pi$  leap in phase has been performed. The building block of any RSFQ circuits is a shunted Josephson junction. During switching of a flux state, a short voltage pulse is developed across the junction in the superconducting loop. This voltage pulse has a quantized area equal to the flux quanta  $\phi_0$ . The SFQ pulse width limits the speed of the RSFQ circuits. Its pulse height is approximated by  $1.5I_cR$ . Thus the FWHM of the SFQ pulse as illustrated in figure 2.4 is:

$$\tau \approx 1.5 \frac{\phi_0}{I_c R} \quad (2.24)$$

The energy loss during switching:

$$\Delta E = \int IV dt \approx I_c \phi_0 \quad (2.25)$$

However  $I_c$  cannot be set to arbitrary low value where thermal fluctuations cause improper switching:

$$I_c \gg I_T \equiv \frac{2\pi}{\phi_0} k_B T \quad (2.26)$$

For liquid helium temperature operation of niobium-based circuits (temperatures around 4.2 K), It is about  $0.2\mu A$ . To get a reasonable bit error rate



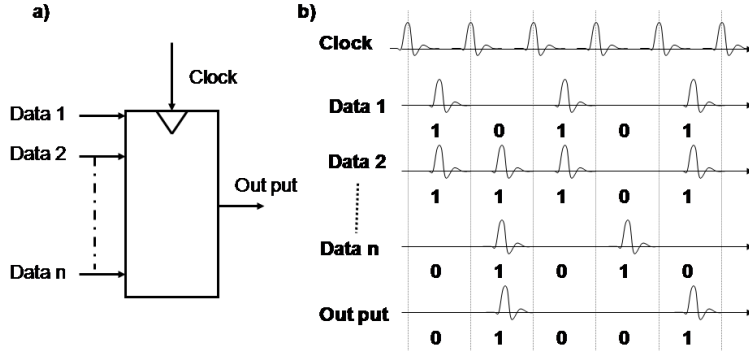


Figure 2.5: a) General scheme of RSFQ circuits, with  $n$ -Data lines and an Output all synchronized with a Clock signal. b) Signal sequence of RSFQ circuits, the arrival of an SFQ Data or Output pulse between consecutive Clock SFQ pulses represents a binary "1" and "0" otherwise.

a proportionality constant of about 625 is chosen for equation 2.26 leading to the choice of the smallest junction with critical current of  $I_u = 125 \mu A$ . This corresponds to energy dissipation per switching event of  $2 \times 10^{-19} J$ . Critical current of junctions are normalized to  $I_u$  for circuit simulation in PSCAN [49, 50]. Given the minimum junction area  $A_{min}$  that can be comfortably defined, the technology level defined by the critical current density will be:

$$j_c = \frac{I_u}{A_{min}} \quad (2.27)$$

Logic is defined by the presence or absence of data SFQ pulse between two consecutive SFQ clock pulses. Binary "1" is the presence of SFQ pulse and "0" is the absence of SFQ pulse between respective clock pulses, the general scheme of an RSFQ circuits is given in figure 2.5-a and a signal sequence of RSFQ circuits is shown in figure 2.5-b.

The maximum frequency of operations scales proportional to the characteristic frequency of the Josephson junctions equation 2.15 up to the plasma frequency, equation 2.16, above which Josephson oscillations become progressively shorted by the junction capacitance. If the junctions are critically damped ( $\beta_c = 1$ ), then

$$f_c = f_p = \sqrt{\frac{1}{2\pi\phi_0} \frac{j_c}{C_s}} \quad (2.28)$$

In the simplest model,  $j_c$  decays exponentially whereas capacitance decreases inversely with the tunnel barrier thickness. This leads to an expres-

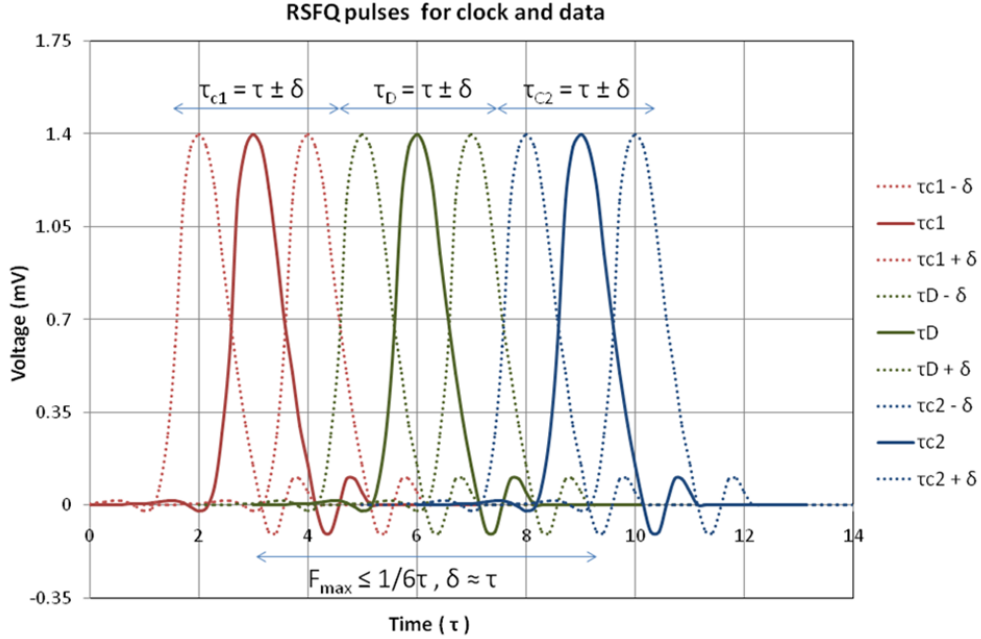


Figure 2.6: Maximum operating frequency of an RSFQ circuit, showing a clock cycle and a data with their respective jitter of the SFQ pulses. The maximum operating frequency of complex circuits is limited by the jitter and delays in the circuit.

sion  $1/C_s = P_1 - P_2 \times \log j_c$ . Fitting to the  $C_s$  data obtained from SQUID LC resonances and plasma resonance measurements for  $Nb/Al/AlO_x/Nb$  [51] gives  $P_1 = 1.72 \times 10^{-2}$  and  $P_2 = 4.3 \times 10^{-3}$  where  $j_c$  is in units of  $kA/cm^2$  and  $C_s$  is in  $fF/\mu m^2$ . Substituting this into equation 2.28 we get:

$$f_{max} = 115.06 \sqrt{j_c (1 - 0.25 \log j_c)} \quad (2.29)$$

Operating frequency scaling for circuits containing tens of Josephson junctions is well described by using equation 2.29. But as the complexities of the circuits are increased, the maximum operating frequency scaling is limited by other factors such as data and clock SFQ pulse jitter [52], commutative delay between clock and data [52, 53] etc. A hand waving analysis introducing a jitter of approximately one SFQ pulse to the Clock and Data pulse streams suggests that the maximum operating frequency of complex circuits to be one sixth of the  $f_{max}$  as illustrated in figure 2.6. So far, experimentally the

maximum operating frequency of most complex circuits has been found to be  $f_{max}/7$ .

## 2.5 Conclusion

The technology level of SCE circuits based on RSFQ is defined by the critical current density ( $j_c$ ) of Josephson junctions and the circuit integration. The maximum operating speed of the circuits scales as the square root of  $j_c$ . In order to make the next generation of complex circuits, one needs to increase the  $j_c$  while proportionally decreasing the junction size. Circuit integration is a function of the number of Josephson junctions, resistors, inductors and interconnects used to make a functional circuit. For the proposed two fold increase in speed and complexity the  $j_c$  needs to be increased by a factor of four and the size reduced by a factor of two.

# Chapter 3

## FABRICATION PROCESSES FOR SUPERCONDUCTOR MICROELECTRONICS

### 3.1 Introduction

Among the more than 20 metallic elements known to be superconductors niobium has been the material of choice for low temperature SCE applications. Soft metallic elements such as Al, Sn, Pb and In were commonly used to fabricate the first tunnel junctions in the 1960s because they can easily be evaporated in simple vacuum systems due to their low melting points and because the tunnel barrier can easily be formed by exposing the base electrode to oxygen or oxygen plasma [54]. However, such junctions were unstable when thermally recycled repeatedly and they corrode easily. On the other hand, Nb is a refractory material is therefore very resilient to thermal recycling. Nb also have other parameters suitable for SCE applications such as a high critical temperature, a large superconducting energy gap, a long superconducting coherence length, and a short penetration depth of the electrode material. Ideally one would prefer to use a material with even higher critical temperature, wider gap, longer coherence length and shorter penetration depth. The higher the energy gap the faster the circuits work. For JJs the gap fully develops above  $2/3T_c$  of the bulk material, so the preferred material would be a metal with highest critical temperature. The energy gap and the critical temperature of the Josephson junction could be lower than that of the bulk material because the material within the coherence length from the barrier determines it. So a longer coherence length is desirable in order minimize the effect of surface irregularities of the superconductor/insulator

interface on device performance. The penetration depth should be shorter in order to be able to conveniently realize the inductance for the circuits and to minimize the effect of flux trapping on device performance. Bulk elemental niobium has the highest critical temperature as well as critical field among elemental superconductors. For the material used as a barrier in the junctions the main parameters that determine its properties are its barrier height, thickness, uniformity and the junction specific capacitance. Sub-gap leakage current characterizes the quality of junctions used in SCE applications and is a result of none superconducting micro-shorts and / or existence of localized electron states in the barrier. The critical current of the junction depends exponentially on the barrier width while the normal state resistance is proportional to the barrier height and thickness. Lower barrier height allows one to use thicker barrier that may be desirable for a better control of junction critical current. The first barrier material that comes to mind for a Nb based technology is its own native oxide  $Nb_2O_5$  and had been a subject of study in the late 1970s [55, 56]. But the junction quality suffered by micro-shorts resulting from the formation of NbO (metallic) and  $NbO_2$  (semiconducting) phases when the top electrode is deposited. The barrier material quest was then geared towards finding an artificial barrier. The first successful research towards making an artificial refractory barrier was done on  $AlO_x$ . First it was found out that a thin layer of aluminum was enough to completely cover a clean niobium surface [57]. Then junctions of high quality were soon made by a 'trilayer' process first introduced in the early 80s at Bell Labs [17–19]. The trilayer process is now the most developed and reliable process for making high quality Josephson junctions for superconductor electronics. In this process the  $Nb/AlO_x/Nb$  sandwich is made in the same run and chamber- in situ process. In the thesis work trilayers were made first by depositing about 1500 Å Nb base electrode. Then about 80 Å of Al is deposited in the same chamber and oxidized by exposing the Al to oxygen for some time by maintaining the chamber under certain pressure depending on the thickness of the oxide barrier required [58, 59]. The product of the oxygen pressure and time commonly known as exposure determines the thickness of the  $AlO_x$  grown and hence the barrier properties. Finally, the top counter electrode is deposited to complete the process. The result is clean and uniform Josephson junctions with predictable critical current densities [60, 61]. The fact that the trilayer is made of all refractory materials and the excellent adhesion of niobium to both Al and  $AlO_x$  to Nb makes the resulting junctions robust and resilient to thermal recycling.

The main focus of the thesis work towards developing higher critical current density process was finding an optimal process flow that could support

Table 3.1: List of layers used in making of SCE circuits.

Layer	Material	Description
M0	niobium	used as a ground, most of ground current flows through it.
I0	$SiO_2$	first dielectric layer between M0 and M1.
M1	niobium	junction base electrode, interconnection, inductor.
Barrier	$Al/AlO_x$	junction dielectric.
I1A/*I1C	niobium	niobium junction counter electrode.
*A1	$Al_2O_3/Nb_2O_5$	junction passivation (by anodization).
I1B1	$SiO_2$	The first part of second dielectric layer between R2 and I1A/M1.
R2	molybdenum	For shunting junctions and making bias resistors.
I1B2	$SiO_2$	The second part of second dielectric layer between M2 and R2.
M2/*M2-A	niobium	niobium interconnect, inductor.
I2	$SiO_2$	The third dielectric layer between M3 and M2.
M3	niobium	niobium interconnect, ground.
R3	Ti/Pd/Au	Contact pads.

Layers marked with \* are layers introduced during the course of the thesis work - The NEW Fabrication process

it. The proposed approach was to keep the same basic circuit layout optimized in  $1.0 \text{ kA/cm}^2$  Josephson junction critical current density i.e., keep the same junction critical currents, bias currents and inductance values. This was implemented by adapting the following methodology: First reduce the junction size by  $1/\sqrt{J_c}$  to get the same junction critical currents, second increase the sheet resistance by a factor proportional to  $\sqrt{J_c}$  which will preserve shunt resistor value and hence the value of  $\beta_c$  and third compensate the value of the bias resistor. The existing fabrication process at the start of the thesis work - "Old" fabrication process uses 10 layers with 40 process steps. The "old" fabrication process had critical limitations that made it impossible to implement the proposed  $4.5 \text{ kA/cm}^2$  Josephson junction critical current density process. In the new process one additional layer is added increasing the number of layers to 11 listed in Table 1 and process steps to 44. Each layer is subjected to unit fabrication processes with four steps: thin film deposition, lithography, etch, and wet chemical processes. Before going to the details of the "New" fabrication process the limitations of the "old" fabrication process and implemented solutions will be presented.

## 3.2 "Old" fabrication process and its limitations

"Old" fabrication process is a fabrication process for superconducting integrated circuits that had been in use at HYPRES Inc. at the beginning of the thesis work. It was a 10-layer process with 40 processing steps. The cross section of the layers is shown in figure 3.1 and includes four superconducting (M0, M1, M2, and M3) layers, two resistive (R2 and R3) layers and insulating layers in between. The process was implemented on  $Nb/Al/AlO_x/Nb$  trilayers with  $1 \text{ kA/cm}^2$  critical current density with square junctions of minimum size  $3.5 \mu\text{m}$ . The most advanced digital and mixed signal circuit demonstrated with this fabrication technology was an Analog-to-Digital Converter (ADC), a circuit containing about  $6 \times 10^3$  Josephson junctions (JJs) and capable of operating at a clock frequency of about  $19.6 \text{ GHz}$  [23].

In this section the physical limitation of the old fabrication process will be presented. Four main limitations has been identified and corrected during the course of the thesis work. These are: 1) The Josephson junction shape. The old fabrication process implements square junctions which are sensitive to the diffraction limited lithography. 2) Josephson junction size and shunt resistance. The minimum junction size was limited by the minimum size of the contact hole to and the alignment tolerance. 3) Poor line width control of

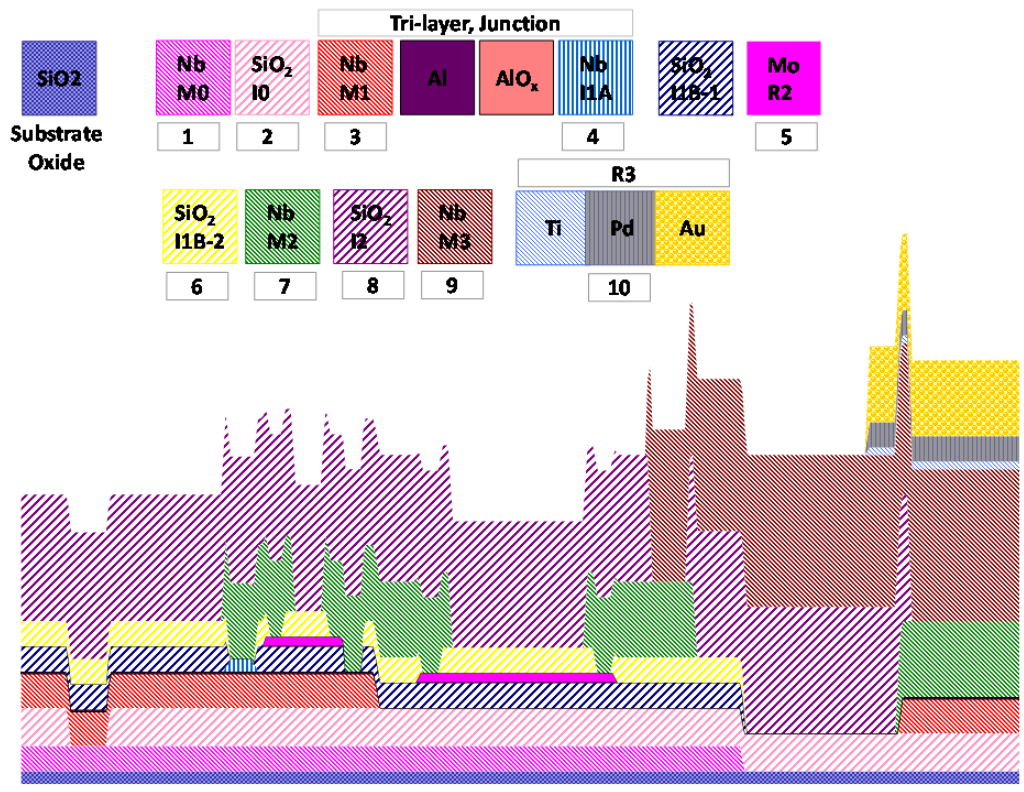


Figure 3.1: "Old" fabrication process layer cross-section. It was a ten layer process with four superconducting niobium layers (M0, M1, M2, and M3) deposited by magnetron sputtering, two resistive layers (R2 deposited by magnetron sputtered molybdenum and R3 evaporated titanium/palladium/gold), and three ion-beam-deposited  $SiO_2$  dielectric layers.



junction base electrode. The use of the barrier material ( $Al/AlO_x$ ) as an etch stop when etching the counter electrode results in poor line width control as the Al is prone to chemical attacks during lithography. 4) Interlayer dielectric. The use of the ion beam deposited  $SiO_2$  was prone to contamination and heating resulting in interlayer shorts limiting the integration level of circuits. Detail of each physical limitation follows.

### 3.2.1 Josephson junction size and shunt resistance

Scaling of the technology from the "old" fabrication process with  $j_c = 1 \text{ kA/cm}^2$  to the proposed "new" fabrication process of with  $j_c = 4.5 \text{ kA/cm}^2$  was limited by the minimum junction size; which in turn was limited by the minimum size of a contact hole to the junction and the contact hole alignment tolerance. With the available lithography tool (Perkin-Elmer full 150-mm wafer projection aligner) this size is about  $2 \text{ }\mu\text{m}$ . This restriction put the intended "new" fabrication process of  $4.5 \text{ kA/cm}^2$  (requiring a  $1.7 \text{ }\mu\text{m}$ ) out of the limit of the projection lithography. The solution to the problem are then either upgrade to higher resolution and better alignment tolerance lithography or formulate a process with no alignment tolerance restriction. As the cost of implementing the first solution was found to be prohibitive. The second solution was pursued by implementing an anodization step right after the junction definition step. Superconducting electronics circuits based on RSFQ technology uses critically damped Josephson junction. Damping is achieved by external thin film shunt resistor made of molybdenum. For the "new" process, the sheet resistance was scaled from  $1.0 \text{ }\Omega/\square$  for the  $1.0 \text{ kA/cm}^2$  to  $2.1 \text{ }\Omega/\square$  for  $4.5 \text{ kA/cm}^2$ , according to  $\sqrt{j_c}$  scaling in order to preserve the same junction damping factor  $\beta_c$  [26]. This required thinning of the resistor layer while still maintaining uniformity across 150-mm wafers. To insure uniformity of sheet resistance across 150-mm wafer, the deposition rate uniformity was verified over  $300 \times 300 \text{ mm}$  area of the pallet. At room temperature the average sheet resistance was  $1.92 \pm 0.08 \text{ }\Omega/\square$  and the average thickness was  $755 \pm 22 \text{ \AA}$  as shown in figure 3.2. This gives very uniform sheet resistance of  $1.0 \pm 0.1 \text{ }\Omega/\square$  at 4.2 K for the "old" process no matter where the wafer is placed on the pallet, enabling even two wafers to be processed at the same time. For the new process with  $j_c = 4.5 \text{ kA/cm}^2$ , the sheet resistance at room temperature has to be around  $3.85 \text{ }\Omega/\square$  with an average thickness of around  $430 \text{ \AA}$ . To get the same level of uniformity the most uniform part of the pallet was chosen, which happens to be the center of the pallet. Thus for the new process wafers had to be processed one at a time, placed at the center of the pallet.

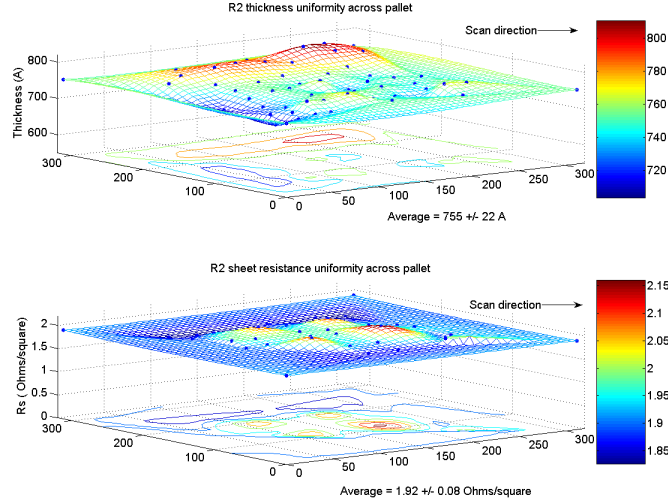


Figure 3.2: Thickness and sheet resistance uniformity across 300 x 300 mm pallet, average thickness ( $755 \pm 22 \text{ \AA}$ ) and average sheet resistance  $1.92 \pm 0.08 \text{ } \Omega/\square$

### 3.2.2 Junction geometry

The "old" fabrication process had predominantly been using square Josephson junctions with minimum size of  $3.5 \text{ } \mu\text{m}$ . At the end of junction definition, i.e., after lithography and etching, these square junctions remained a square-shaped with some corner rounding, resulting in the so-called missing area  $ds$ . For the "new" process the size needed to be reduced to a minimum  $1.7 \text{ } \mu\text{m}$  square junctions, the diffraction-induced rounding became dominating, and the junction shape had to be optimized in order to minimize the missing area. Three types of junctions had been designed and tested to find one with minimum area loss (bias) - square, Manhattan-shaped and circular junctions, each having its own advantages and disadvantages. For instance, square shapes are easy to design and implement even on larger grid ( $> 0.25 \text{ } \mu\text{m}$ ) photo-masks. Circular shape on the other hand can only be implemented with smaller grid ( $0.1 \text{ } \mu\text{m}$ ), and thus more expensive, photo-masks. The advantage is that after the processing they remain circular junctions with some missing radius  $dr$ . Manhattan shape was designed to emulate circular shape on the  $0.25\text{--}\mu\text{m}$ -grid masks.

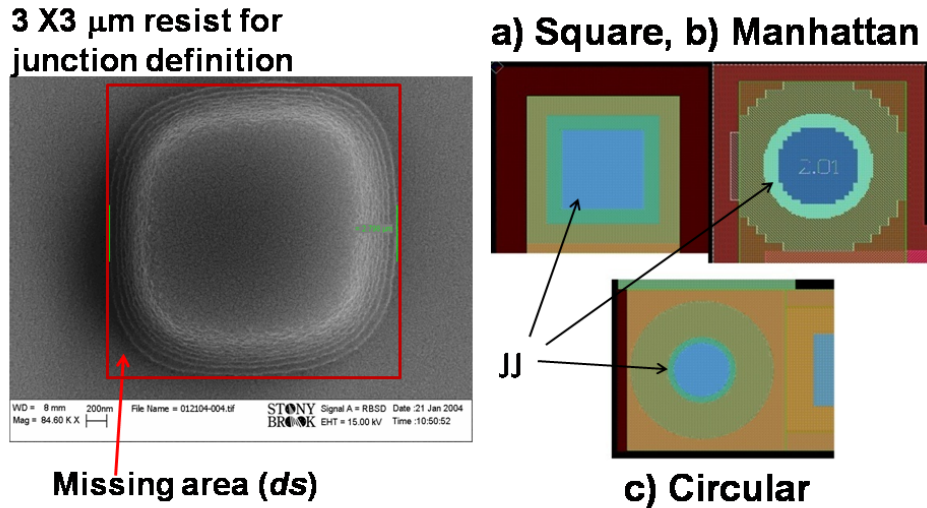


Figure 3.3: SEM of of  $3 \times 3 \mu m$  junction definition photoresist depicting the diffraction induced corner rounding. Layout of studied junction geometries: square, Manhattan and circular shapes. The three concentric structures respectively are: via to the junction (I1B), the junction (I1A/I1C) and the anodization ring (A1).

### 3.2.3 Line width control of junction counter electrode

In the "old" fabrication process the junction area definition (layer I1A) was done after the base electrode (layer M1) has been defined partially by removing the top counter electrode, the  $Al/AlO_x$  barrier and part of the base electrode by ion beam milling. This exposes on the edges the  $Al/AlO_x$  barrier material to environment, particularly Al has been found to be prone to chemical attacks from developer used for photolithography [62]. Since the junction definition step uses the aluminum under-layer for an etch stop; part of the base electrode not protected by the  $Al/AlO_x$  over-layer is removed. This makes the M1 critical dimension control unpredictable caused by the chemical attack of the  $Al/AlO_x$  barrier material. Figure 3.4 show a typical observation from processing wafer KL753.

### 3.2.4 Level of integration and circuit complexity

The level of integration and hence the circuit complexity has been limited by the interlayer shorts mainly because of the poor step coverage of interlayer dielectric [63, 64]. The main problem being the ion beam deposited  $SiO_2$

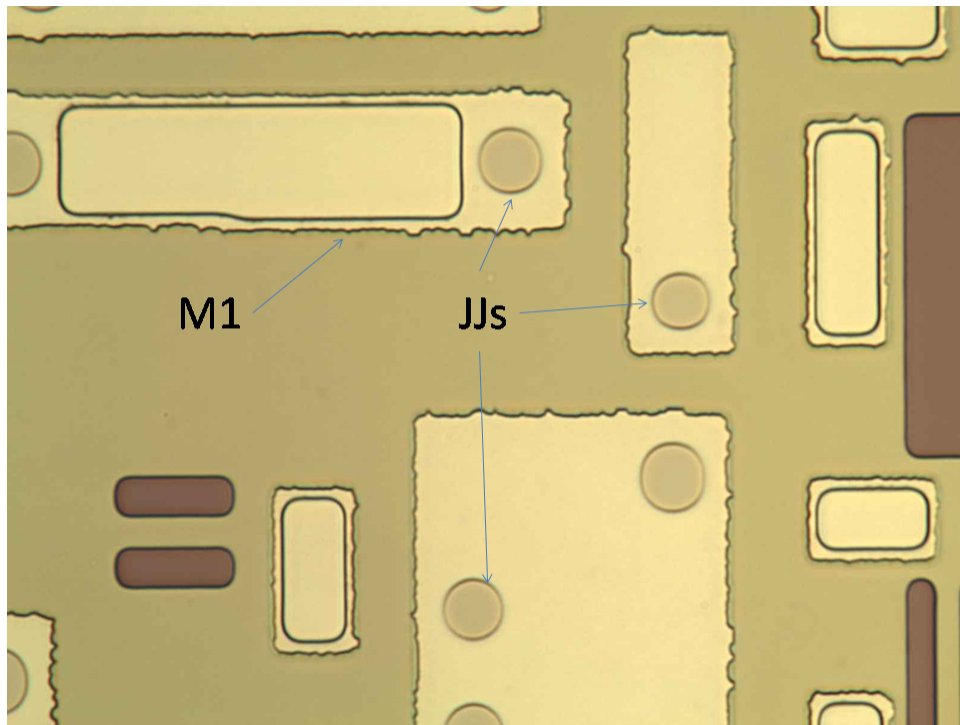


Figure 3.4: Micrograph of circuit elements after the junction definition step. The M1 features (bright yellow rectangles) suffered great undercut because the etch stop Al has been attacked by chemicals during photolithography.

material contamination, and slow deposition rate. The  $SiO_2$  gets deposited everywhere in the chamber and it tends to flake off increasing material contamination when it gets too thick. The fact that the deposition rate is low makes the wafer to heat up and the process to be slow with low through-put as long as 8 hours to process a single layer.

### 3.3 Implemented solutions to alleviate the limitations of "old" fabrication process

RSFQ based SCE circuits implement critically shunted Josephson junction, inductors, resistors (for shunting, biasing and impedance matching), interconnects to manufacture integrated circuits. Scaling from one technology level to the next is thus achieved by making process adjustments to all of the critical elements. In the previous section the limitations of the "old" fabrication process has been identified as: poor choice of junction geometry for the diffraction limited projection photolithography; size being limited by the via to the junction rather than the junction itself; effect of junction definition step to the base electrode which is mainly used to define circuit inductances and interconnection - rendering the inductance control to be poor; interlayer dielectric deposition being slow and prone to contamination leading to interlayer shorts and hence promoting lower integration level. The next four subsections describe the implemented solutions to address the limitations.

#### 3.3.1 Optimum junction shape

From the three junction geometries considered, circular junctions were found to be optimum junction shapes for making Josephson junctions especially smaller than  $2.0 \mu m$ . As a matter of fact the circular junction has been adopted as standard junction shape for  $1.0 kA/cm^2$  and  $4.5 kA/cm^2$  critical current densities. SEM pictures of Josephson junctions were used to measure the spread in size and check the shape of the junctions after lithography and etching. figure 3.5 shows one of such comparisons for square and circular junctions of size  $1.5 \mu m$  and less. Square junction of size  $1.5 \mu m$  and  $1.0 \mu m$  came out as circular with big missing area of  $0.6 \mu m^2$  on average, whereas circular-shaped junctions still remained circular with a missing radius of  $0.15 \mu m$ .

#### 3.3.2 Enhanced photolithography process

A 24% increase in resolution of the projection photolithography was achieved by upgrading the exposure source from a broad-band exposure (340 - 440 nm

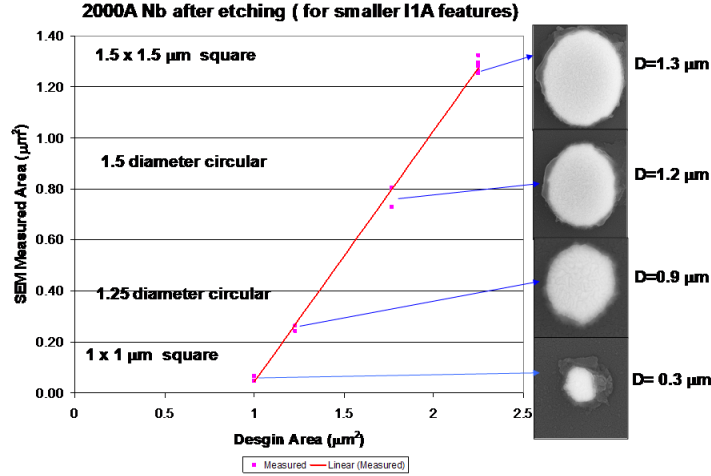


Figure 3.5: SEM measured area vs. design area for square and circular junctions of designed size of  $1.5 \mu\text{m}$  and less defined by projection lithography.

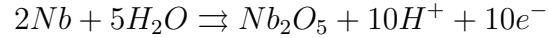
wavelength) to UV3 band (290 - 340 nm wavelength) by introducing appropriate filter in the aligner optics. Even though enhancement of the exposure source reduced the focus depth by about 23% the resolution was maintained by rigorously monitoring the focus,  $90^\circ$  and  $45^\circ$  astigmatism, skewness, x and y magnifications of the projection lithography machine. Besides the standard procedures that are used to control state of the lithography machine, photolithography monitoring structures were included on every mask release and all layers. These structures are included on four corners next to the alignment marks and contain an array of circular features of size (2, 1.5 and  $1.0 \mu\text{m}$  in diameter), equal lines and spaces and isolated line of size (2.0, 1.5, 1.0,  $0.8 \mu\text{m}$  wide) placed vertical and horizontal, and (4.0, 2.0  $1.0 \mu\text{m}$  wide) lines for measuring critical dimension optically using a  $150 \times$  magnifying objective of an optical microscope (total magnification  $\times 1500$ ) shown in figure 3.6. The included structures provide excellent visual information from which one can decide whether to correct the respective problems. For example, if the circular features as well as isolated lines suffer significant size reduction from their design value this is most likely due to focus problem; if there is a difference in size between the horizontal and vertical lines and/or the circular features have an oval shape the most likely cause is astigmatism; if the machine is focused but the array of lines and spaces are not of equal size the most likely cause is over/under exposure, etc.



Figure 3.6: A micrograph of photolithography monitoring structure containing an array of circular features, lines and spaces and CD bars placed on all layers, providing the visual clue and control mechanism.

### 3.3.3 Anodization for junction definition

The restriction to the junction size due to contact hole alignment tolerance to the I1B-via was alleviated by anodizing an area around the junction. This allowed the definition of junction size to be independent of contact hole size i.e., the junction can now be smaller or bigger than the contact hole. Anodization short for anodic oxidation is a process of oxidizing a metal by electrolysis [65–68]. The metal to be oxidized is the only one connected to the anode electrode which is immersed in an electrolyte. A niobium film surface can be anodized to form a uniform dense and stable oxide ( $Nb_2O_5$ ) [69–76]. For cathode, metals like platinum and molybdenum are commonly used. During electrolysis the following electrochemical reaction occur at the anode and cathode respectively:



and



The anodization solution is a mixture of 156 g ammonium pentaborate, 1120 ml ethylene glycol and 760 ml  $H_2O$ . A molybdenum cathode is used

and niobium is the only anodic conductor exposed to the electrolyte. As the oxide growth the electric field developed between the electrodes proportionally decreases for a given applied voltage between the electrodes. Current density on the other hand is reduced exponentially until an equilibrium thickness is reached. Since the anodic surface is an equi-potential surface regardless of the surface geometry the oxide that grows is very uniform and well controlled by the applied voltage. We have estimated that each volt across produces 23 Å of  $Nb_2O_5$  from about 9 Å of Nb. Anodization process integration is summarized in figures 3.7 and 3.8. After the *in situ* trilayer deposition of  $Nb/Al/AlO_x/Nb$  I1A or I1C mask set is used to define junction area as usual except the photoresist is hard baked for 5:00 min at 110 °C after development. This makes the photoresist stronger and usable for the next two processing steps i.e., counter electrode etch by RIE and anodization. After RIE of the counter electrode the wafer is then anodized by applying a constant voltage of about 28 V and 700 mA initial current forming a double protecting layer of  $Al_2O_3$  and  $Nb_2O_5$  as shown in figures 3.7. The current exponentially decays about 15 mA in 2:00 min when a dense oxide has formed.

Then the resist is stripped by a wet chemical process involving acetone, methanol and isopropanol and is ready for the anodization definition step (layer A1). A1 photolithography covers the junctions and areas around the junctions by photoresist mask. The rest of the wafer area is milled removing the  $Al_2O_3$  and  $Nb_2O_5$  and some part of the base electrode. Stripping the photoresist results in a wafer populated by junctions well passivated by anodization protecting them from any further process induced chemical attack. The process flow for anodization junction definition is illustrated in figure 3.8.

Scanning electron microscope (SEM) pictures of an anodized array of Josephson junction is shown in the figure 3.9. Via to the junction is bigger than the junction the square shaped traces around the junctions are the anodization bi-layer encapsulating the junction.

### 3.3.4 Inverted process of junction definition

The introduction of the anodization process enables the junction to be defined and protected from damage in subsequent processes. The base electrode can now be easily and more accurately defined by RIE without the need to use aluminum as an etch stop which is very susceptible to various chemical attacks described in the previous section.



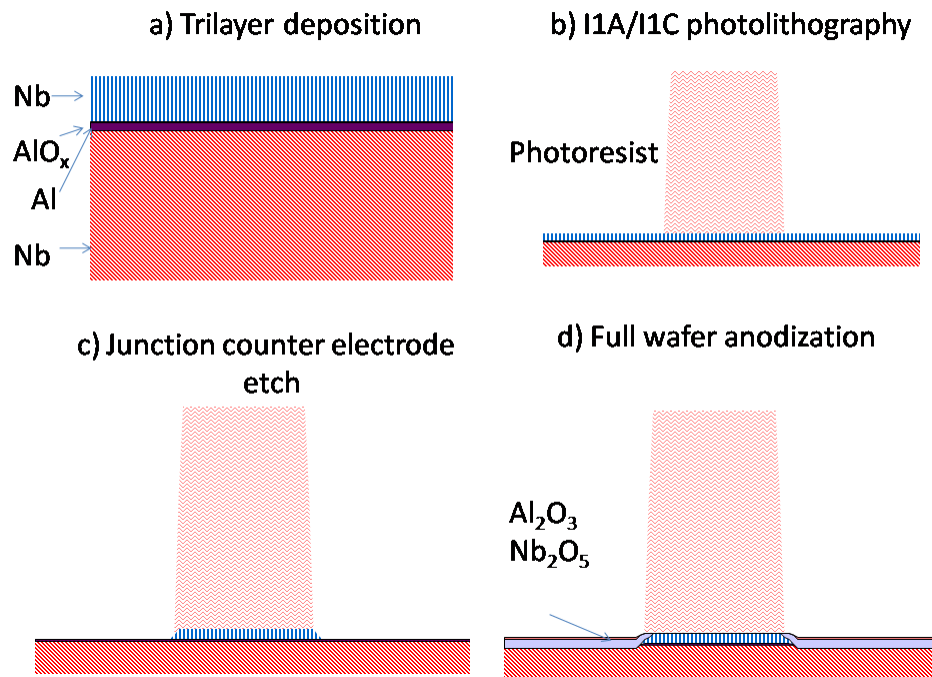


Figure 3.7: Anodization step process integration - junction definition step: **a)** after the *in situ* trilayer deposition of  $Nb/Al/AlO_x/Nb$ ; **b)** the junction definition photolithography is done; **c)** then junction counter electrode is etched by RIE; **d)** the wafer is then anodized by applying about 28 V and 700 mA current forming a double protecting layer of  $Al_2O_3$  and  $Nb_2O_5$ .

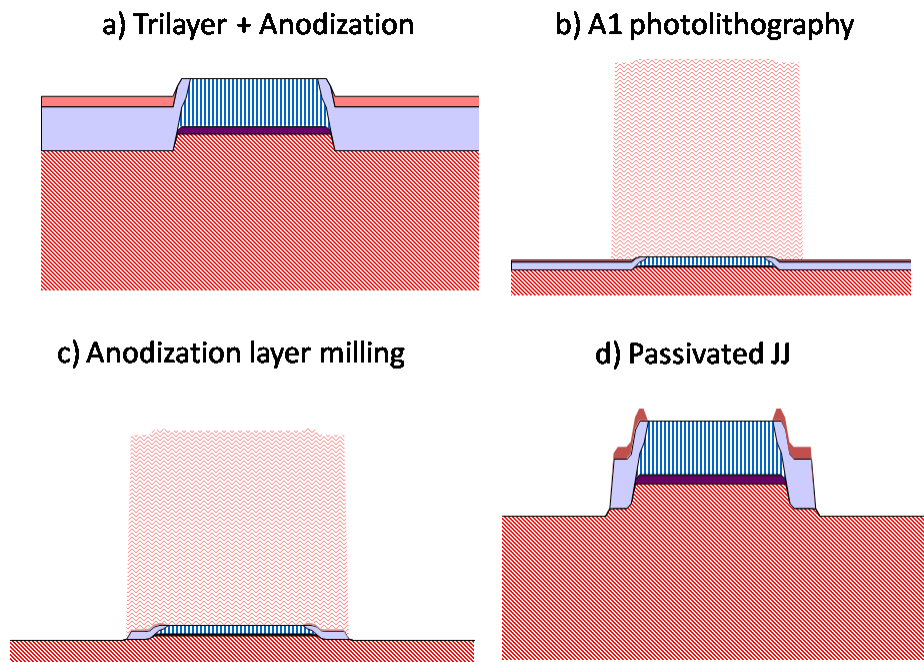


Figure 3.8: Anodization step process integration - ring anodization definition step: **a)** after I1A/I1C definition photoresist striped **b)** the anodization ring definition photolithography (A1) is done; **c)** then the wafer is milled removing anodized  $Al_2O_3$  and  $Nb_2O_5$  except around the junction. **d)** The result is a wafer with well passivated junctions ready for the next process steps.

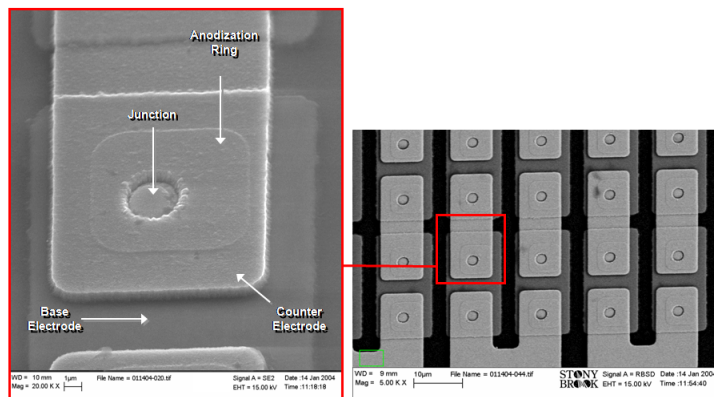


Figure 3.9: SEM picture of anodized Josephson junctions in an array.

### 3.3.5 PECVD deposited $SiO_2$

To overcome the drawbacks of ion beam deposition a Plasma Enhanced Chemical Vapor Deposition (PECVD) system was implemented to deposit dielectric at low temperatures (  $150\text{ }^\circ\text{C}$  both lower and upper electrodes) from a tetra-ethoxysilane (TEOS) source at 12 sccm TEOS and 400 sccm  $O_2$  flow and chamber pressure of 40 Pa, and 200 W RF power. Step coverage was examined during process development using SEM on cross-sections of chips as shown in figure 3.10 and was found to be superior to the previously used ion-beam-sputtered  $SiO_2$ . The resulting  $SiO_2$  dielectric film is very similar to what is deposited using an electron cyclotron resonance (ECR) PECVD in [77–79].

A combination of chemical and plasma cleaning is used for surface preparation to avoid pin-hole formation between and after dielectric layer deposition. For the "old" fabrication step this was very important as it was used to remove any protruding metals by spin scrubbing the surface.

### 3.3.6 Resolution enhancement technique

The latest important development which exploited the implemented solutions to greater extent has been the current process development for  $20\text{ kA/cm}^2$  process. An advanced process for fabricating SICs operating at  $80\text{ GHz}$  clock frequency requires Josephson junctions (JJs) with  $20\text{ kA/cm}^2$  critical current

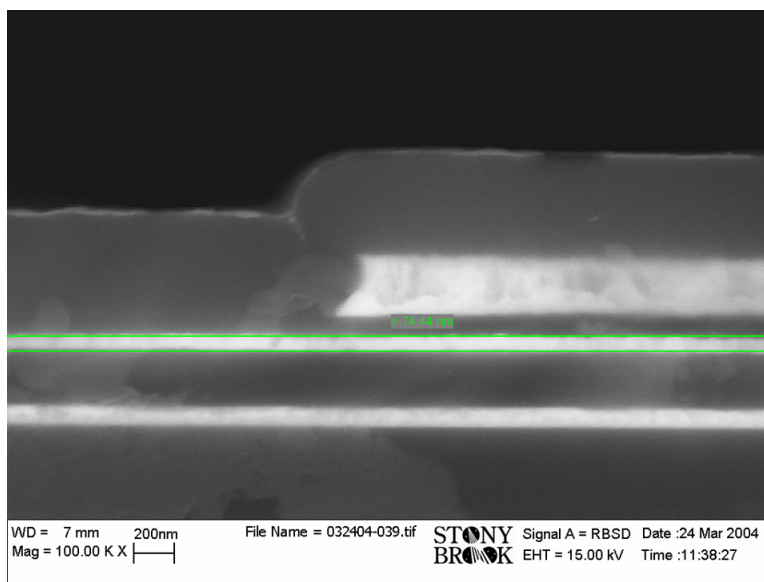


Figure 3.10: Picture showing excellent step coverage of  $SiO_2$  deposited by PECVD between metal layers (bright white).

density and the smallest area of  $0.5 \mu m^2$  corresponding to a circular junction of 800 nm in diameter. This critical dimension (CD) must be controlled within  $\pm 40$  nm in order to have JJ critical current uniformity within  $\pm 10\%$  that is believed to be sufficient for yielding SICs with  $10^4$  JJs. To minimize run-to-run variation, corner rounding, and CD loss a powerful resolution enhancement technique (RET) has been developed and implemented [27]. The RET takes advantage of the fact that the projection aligner could resolve as small as  $0.7 \mu m$  single isolated lines when properly focused. Two mutually perpendicular single lines can then be used to produce submicron junctions with improved area control on the same tool. We believe RET can also be used for defining deep submicron square (rectangular) junctions on any of the more advanced lithography tools when a tight area control is required.

In the implemented RET the JJ area is defined by using two photolithographic steps and two photo masks, each containing a set of lines of a given width that are mutually orthogonal to the corresponding lines on the other mask. First, a set of, e.g., horizontal lines is exposed and then the second mask is used to expose the vertical set. The junction area is defined by the overlap of two mutually orthogonal lines. This double exposure technique allows for much better resolution, better area and corner definition, etc. Also standard RETs and phase shifting techniques can be added to enhance the resolution of the single lines at each exposure [80].

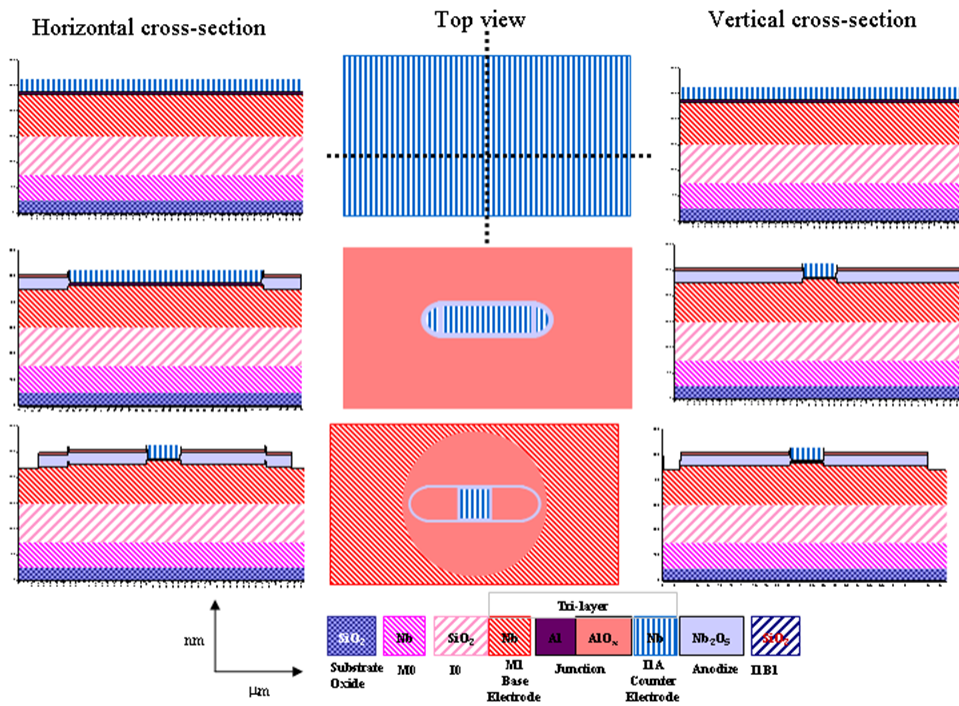


Figure 3.11: Dual-Step Anodized Junctions (*DSAJs*) definition. The first row shows  $Nb/Al/AlO_x/Nb$  trilayer. The second and third rows show the first and the second lithography/etch/anodization junction definition steps. The fourth row shows the resulting square (rectangular) Josephson junction

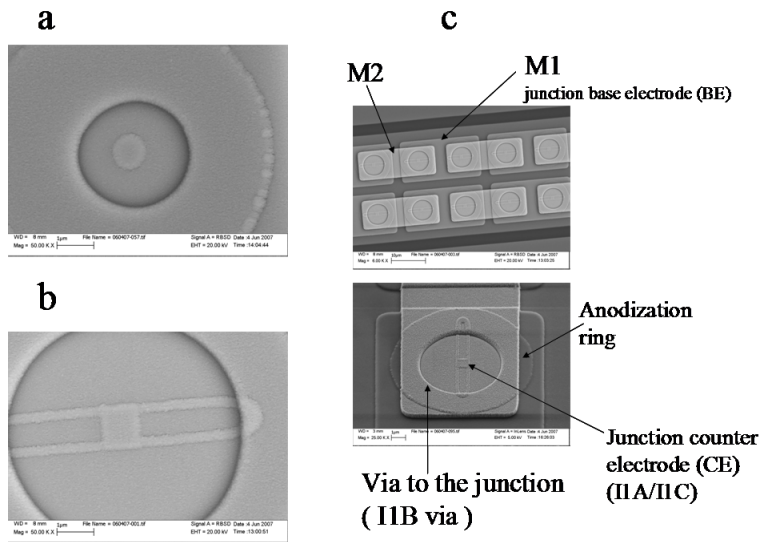


Figure 3.12: (a) An SEM picture of a circular junction defined in the second step of DSAJ definition; designed radius  $0.60 \mu\text{m}$ , measured radius  $0.35 \mu\text{m}$  with a  $0.19 \mu\text{m}$  wide  $\text{Nb}_2\text{O}_5$  ring. The significant bias on radius is partly due to over-exposure (b) An SEM picture of a junction defined by dual Step. Design size  $0.75 \times 0.75 \mu\text{m}$ , measured size  $0.76 \times 0.85 \mu\text{m}$  with a  $0.19 \mu\text{m}$  wide  $\text{Nb}_2\text{O}_5$  ring. (c) An array of junctions with description of different layers around the junction.

Two practical implementations of the described method have been pursued. In the first, the resist pattern after each exposure is directly transferred onto the counter electrode (CE). That is, the first lithography step is followed by CE etching and immediate anodization of the exposed barrier area with the photoresist as an anodization mask protecting the top surface of the formed rectangular line in the CE. The resist is then stripped, and the whole process is repeated with the second mask as shown in figure 3.11. The second method is to transfer the photoresist patterns after each exposure onto an extra masking layer, e.g., an overlay of  $SiO_2$  deposited on top of the CE. After each exposure selective etching of  $SiO_2$  is done stopping at (or slightly etching in to) the CE. Two exposures and two etches define the desired JJ shapes in the  $SiO_2$  over layer. After that the pattern is transferred onto the CE by etching the CE and doing a single anodization, the  $SiO_2$  mask serves both as an etch and anodization mask. The convenient  $SiO_2$  over layer thickness is in the range of 50 to 100 nm. The second method can be more useful for processes utilizing photoresist having poor adhesion to Nb (but much better adhesion to  $SiO_2$ ) and having difficulties surviving the anodization step such as deep UV resists. An SEM picture of a junction defined by DSAJ is shown in figure 3.12.

### 3.4 New fabrication process flow

The main features of the new fabrication process are:

1. Circular Josephson junctions for both  $1\text{ kA/cm}^2$  and  $4.5\text{ kA/cm}^2$  processes, defined by I1A and I1C masks, respectively. The I1C mask is the new mask added.
2. New mask for patterning the anodization layer protecting the junctions, called A1.
3. Inverted junction definition process: counter electrode is defined before the base electrode contrary to the "Old process" where the base electrode was defined first.
4. The use of the same resistor material (molybdenum) for both  $1.0\text{ kA/cm}^2$  and  $4.5\text{ kA/cm}^2$  processes. Scaling the sheet resistance from  $1.0\ \Omega/\square$  to  $2.1\ \Omega/\square$  respectively.
5. The use of PECVD for depositing interlayer dielectrics.
6. Separate M2 masks for  $1\text{ kA/cm}^2$  (called M2) and  $4.5\text{ kA/cm}^2$  (called M2-A, new) processes.

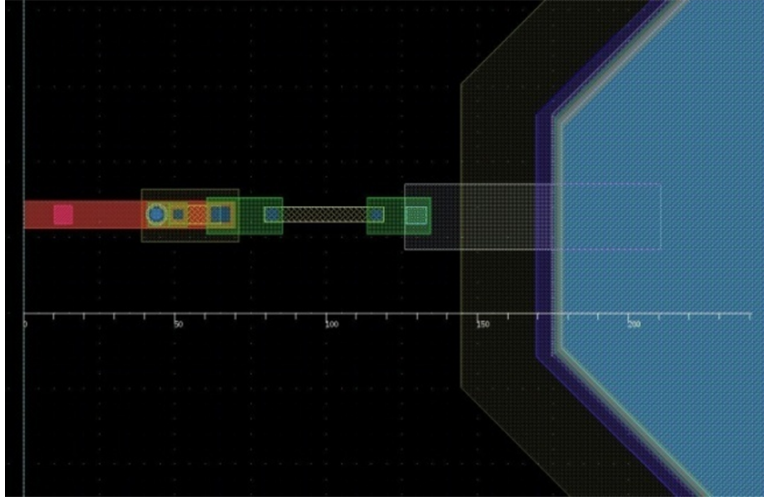


Figure 3.13: Layout of a shunted junction connected to bias pad with a bias resistor and grounded through the base electrode of the junction.

#### 7. Lift-off process for patterning R3 layer of evaporated Ti/Pd/Au.

The details of the process flow will be described by following the cross-section of a structure of shunted Josephson junction connected to the contact pad through bias resistor and superconducting interconnects in M2 and M3 layers. The layout of structure implemented is shown in figure 3.13.

The process starts with a bare 150 mm diameter oxidized silicon wafer by deposition the first Nb metal layer (M0). The deposition is done in a cryo-pumped chamber to a pressure of about  $10^{-7}$  Torr. Magnetron sputtering is used for deposition where the wafer is scanned under the target at constant speed. Both the scan speed and the chamber pressure are adjusted to get the required film thickness growing without stress. At 3 kW power the wafer is scanned at 20 cm/sec to make a film of thickness  $1000\text{\AA}$  for M0 at stress free chamber pressure of 17 mTorr. After deposition the Nb thin film is patterned using M0-mask, a dark field mask and a positive photoresist AZ5214-E IR. Pattern is transferred to the thin film after etching it in end-point-detected  $SF_6$  plasma RIE. Following etching the resist and etch by-products are stripped and cleared by wet processing. The four steps needed to complete the making of the any layer are described in the next section together with the means and method of characterization. The final cross section after the completion of the first layer is given in figure 3.14 First layer - M0, sputter deposited, dark field mask lithography,  $SF_6$  RIE etched, chemically striped. Figure 3.14, it is done



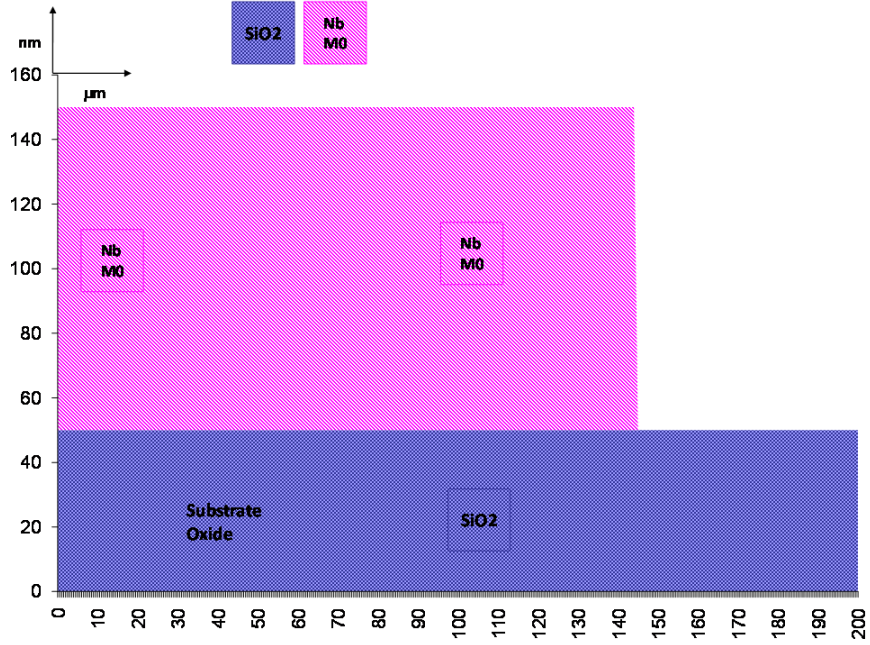


Figure 3.14: First layer - M0, sputter deposited, dark field mask lithography,  $SF_6$  RIE etched, chemically stripped.

to scale with nano-meter scale on the Y-axis and micro-meter scale on the X-axis. Layer description the 11 layers of the new fabrication process follow:

1) M0 is the first Niobium superconductor layer shown in figure 3.14. It is grown to a thickness of  $1000 \text{ \AA} \pm 10\%$  and the film's sheet resistance at room temperature is  $1.90 \pm 0.2 \Omega/\square$ . In a circuit this layer is used as grounding and most of the return current flow through it. To reduce the effect of ground current induced magnetic field interference to the operation of the circuit a number of holes and motes are included in this layer. Holes and motes can have a minimum size of  $2 \times 2 \mu m$  and a bias  $(0.25 \pm 0.25) \mu m$  and a minimum spacing of  $3 \mu m$  between them. Figure 3.14.

2) I0 - interlayer dielectric between M0 and M1 layer shown in figure 3.15. It was PECVD deposited  $SiO_2$  insulator of thickness  $1500 \text{ \AA} \pm 10\%$  with a specific capacitance of  $0.277 \text{ fF}/\mu m^2 \pm 20\%$ . Contact to M0 is through I0 vias with a minimum size of  $2 \times 2 \mu m$  and a bias  $(0.30 \pm 0.25) \mu m$ . The alignment tolerance of I0 to M0 is  $\pm 0.25 \mu m$

3) I1C - Niobium superconductor counter electrode of the tri-layer layer shown in figure 3.16. It is deposited by magnetron sputtering in a load locked, cryo-pumped chamber with a base pressure of  $1 \times 10^{-9} T$ . It is grown to a thickness of  $500 \text{ \AA} \pm 10\%$ . Junctions are defined in this layer by using a clear

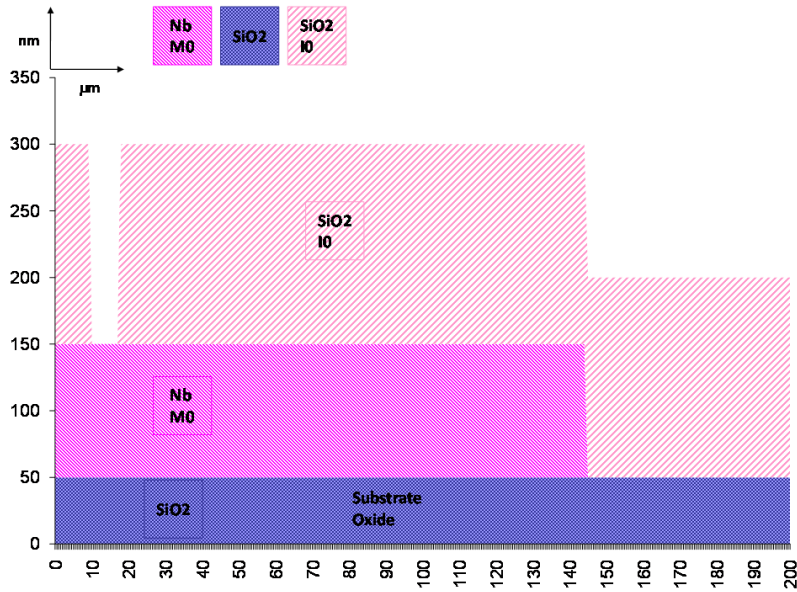


Figure 3.15: Second layer I0 - ion beam deposited, dark field mask lithography defining vias between M1 and M0, etched in  $CHF_3 + O_2$  mixture, chemically stripped.

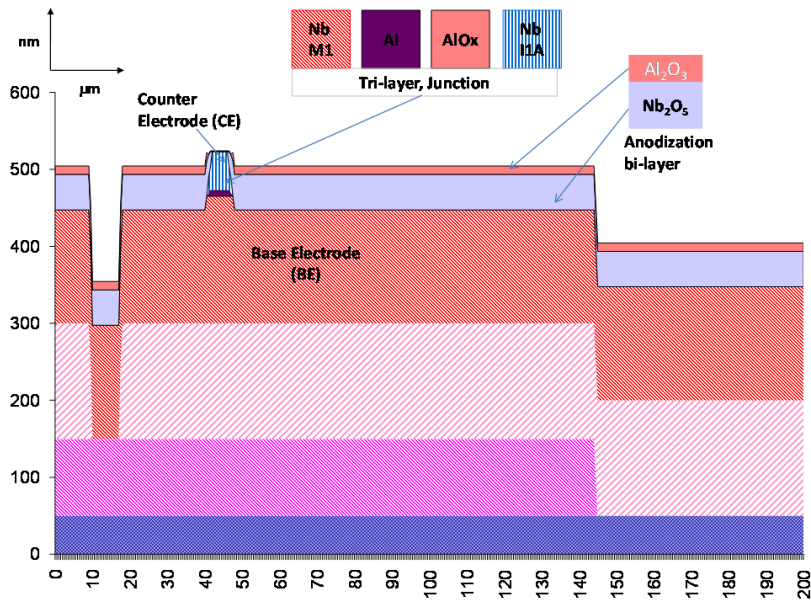


Figure 3.16: Third layer - Tri-layer *insitu* sputter deposited  $Nb/Al/AlO_x/Nb$ , I1C clear field mask lithography defining junctions hard baked photoresist, Anodization, chemically stripped.

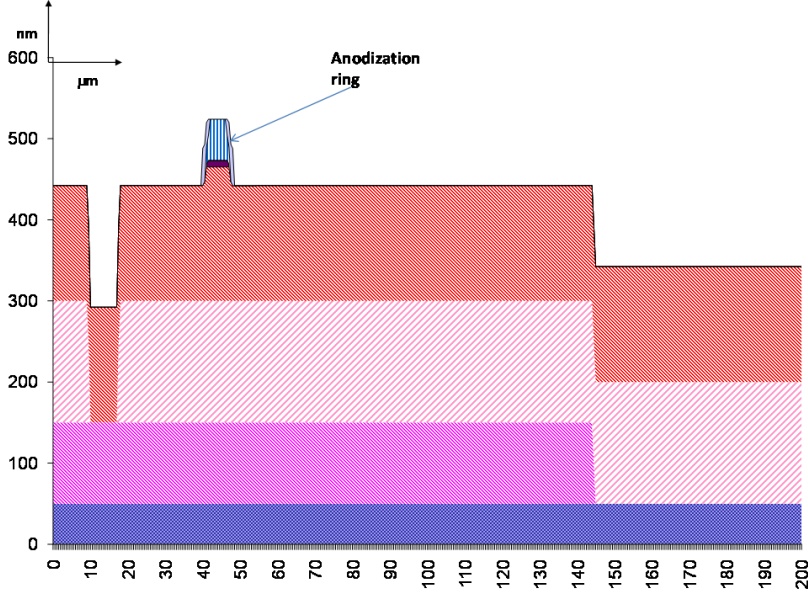


Figure 3.17: Layer - A1, anodization ring definition, A1 clear field mask lithography defining Josephson junctions, ion beam milled, chemically stripped. Detail in section 3.3.3.

field mask I1C. The alignment tolerance of I1C to M0 and/or I0 is  $\pm 0.25 \mu m$ . After the counter electrode is etched in  $SF_6$  plasma, the wafer is anodized as described in section 3.3.3.

4) A1 -  $Al_2O_3/Nb_2O_5$  double layer layer shown in figure 3.17. It is grown by anodization after RIE of the base electrode by applying a constant voltage of about 28 V and 700 mA initial current forming a double protecting layer of  $Al_2O_3$  and  $Nb_2O_5$ . The thickness of the bi-layer is about  $560 \text{ \AA} \pm 10\%$ . After A1 definition the remaining bi-layer surrounds the Josephson junctions by about  $0.5 \mu m$ . A1 is aligned to I1C with an alignment tolerance of  $\pm 0.25 \mu m$ .

5) M1 - Niobium superconductor counter electrode of the tri-layer layer shown in figure 3.18. It is deposited by magnetron sputtering in a load locked, cryo-pumped chamber with a base pressure of  $1 \times 10^{-9} T$ . It is grown to a thickness of  $1500 \text{ \AA} \pm 10\%$  and the film's sheet resistance at room temperature is  $1.70 \pm 0.2 \Omega/\square$ . Most of circuit inductances are defined in this layer by microstrip lines with M0 as ground plane and M3 for double ground plane. A specific inductance of M1 over M0 ground plane is  $0.487 \pm 0.007 pH$  with a fringing factor of  $0.54 \pm 0.13 \mu m$ . Minimum line width  $2 \mu m$  and a bias ( $-0.30 \pm 0.25$ )  $\mu m$ . The alignment tolerance of M1 to M0 and/or I0 is  $\pm 0.25 \mu m$ .

6) R2 - Molybdenum resistor material layer shown in figure 3.19. It is deposited by magnetron sputtering in a load locked; cryo-pumped chamber

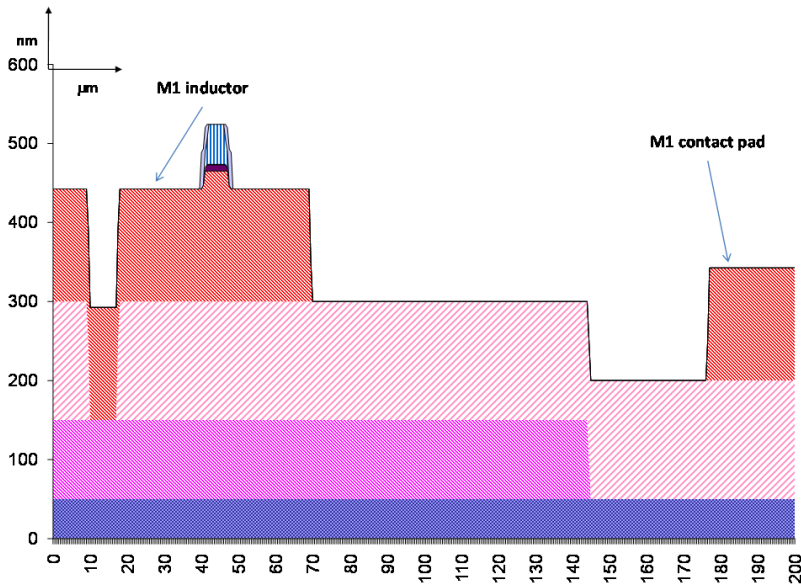


Figure 3.18: Layer- M1, base electrode of the tri-layer. M1 clear field mask lithography defining inductances and interconnects by RIE, chemically stripped.

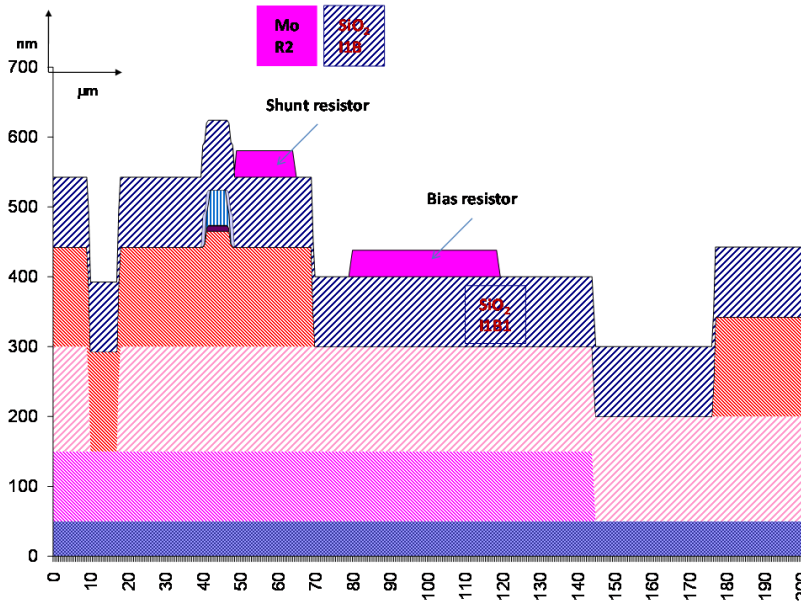


Figure 3.19: The sixth layer R2, sputter deposited molybdenum, clear field mask lithography defining the shunt and bias resistors of the circuit,  $SF_6$  plasma etched, chemically stripped.

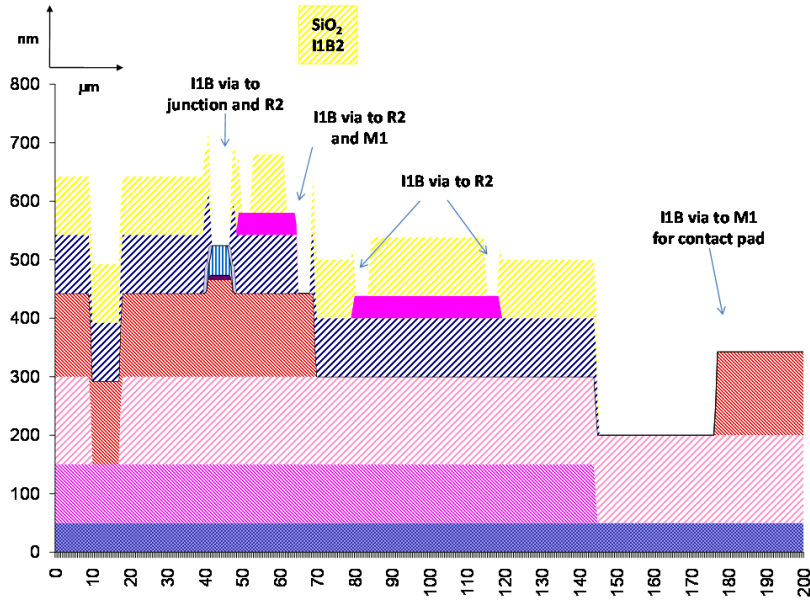


Figure 3.20: The seventh layer I1B-1 and I1B-2 - PECVD deposited, I1B lithography dark field mask defining vias to junction, resistors and contact pads, etched in  $CHF_3 + O_2$  mixture, chemically stripped.

with a base pressure of  $1 \times 10^{-7} T$  right after the first part of the I1B1 dielectric is deposited. It is grown to a thickness of  $750 \text{ \AA} \pm 10\%$  for  $1kA/cm^2$  process and  $480 \text{ \AA} \pm 10\%$  for  $4.5kA/cm^2$  processes, respectively. This gives the film's sheet resistance at room temperature of  $1.95 \pm 0.1 \Omega/\square$  and  $3.85 \pm 0.1 \Omega/\square$ , respectively, and  $1.0 \pm 0.1 \Omega/\square$  and  $2.0 \pm 0.1 \Omega/\square$  at 4.2 K. The minimum line width allowed is  $2 \mu m$  wide a bias  $(-0.2 \pm 0.25) \mu m$ . This bias is corrected on the mask. The shunt and bias resistors are defined in this layer. The alignment tolerance of R2 to I1A is  $\pm 0.25 \mu m$ .

7) I1B - interlayer dielectric between tri-layer and R2 - I1B1; tri-layer and M2 - I1B2 layer shown in figure 3.20. I1B1 and I1B2 are PECVD deposited  $SiO_2$  insulator of thickness  $2000 \text{ \AA} \pm 20\%$  with a specific capacitance of  $0.416 fF/\mu m^2 \pm 20\%$ . Contact to M1 and I1A is through I1B vias with a minimum size of  $2 \mu m$  wide and a bias of  $(0.20 \pm 0.25) \mu m$ . The alignment tolerance of I1B to I1A is  $\pm 0.1 \mu m$ .

8) M2 - Niobium superconductor material layer shown in figure 3.21. It is deposited by magnetron sputtering in a load locked, cryo-pumped chamber with a base pressure of  $1 \times 10^{-7} T$ . It is grown to a thickness of  $3000 \text{ \AA} \pm 10\%$  and the film's sheet resistance at room temperature is  $0.60 \Omega/\square \pm 10\%$ . The minimum line width is  $2 \mu m$  and the minimum gap between lines is  $2.5 \mu m$

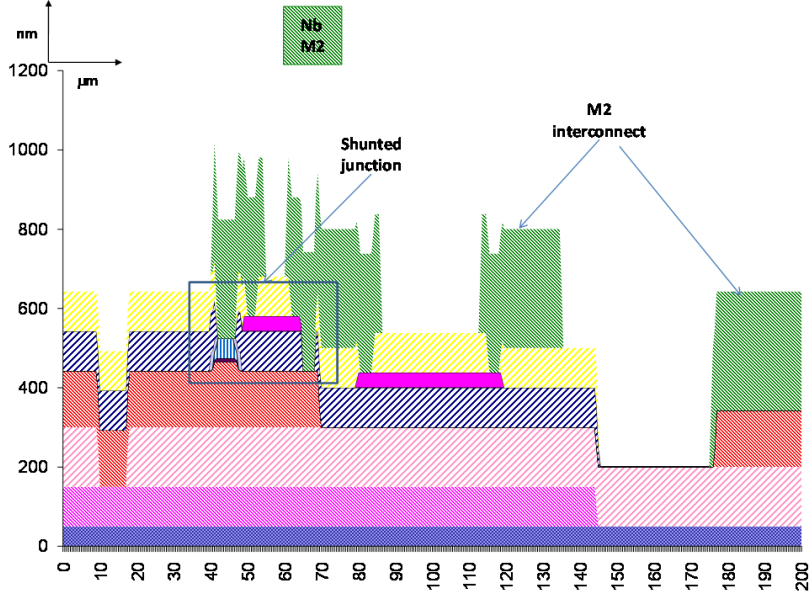


Figure 3.21: The eighth layer - M2, sputter deposited niobium, clear field mask lithography defining M2 inductors and interconnects,  $SF_6$  RIE etched, chemically stripped.

with a bias of  $(-0.5 \pm 0.25) \mu m$ . The alignment tolerance of M2 to I1B is  $\pm 0.25 \mu m$ . This layer is mainly used for wiring, as an inductor with M0 as a ground plane and M3 for a double ground plane. M2 layer over M0 ground plane has a specific inductance of  $0.67 \pm 0.01 pH/\square$  and a fringing factor of  $0.98 \pm 0.19 \mu m$ .

9) I2 - interlayer dielectric between M2 and M3 layer shown in figure 3.22. It is PECVD deposited  $SiO_2$  insulator of thickness  $5000 \text{ \AA} \pm 10\%$  with a specific capacitance of  $0.08 fF/\mu m^2 \pm 20\%$ . Contact to M2 is through I2 vias with a minimum size of  $2 \times 2 \mu m$  and a bias of  $(0.20 \pm 0.25) \mu m$ . The alignment tolerance of I2 to M2 is  $\pm 0.25 \mu m$ .

10) M3 - Niobium superconductor material layer shown in figure 3.23. It is deposited by magnetron sputtering in a load locked, cryo-pumped chamber with a base pressure of  $1 \times 10^{-7} T$ . It is grown to a thickness of  $6000 \text{ \AA} \pm 10\%$  and the film's sheet resistance at room temperature is  $0.30 \Omega/\square \pm 10\%$ . The minimum line width  $2 \mu m$  and a minimum gap between lines of  $2.5 \mu m$  with a bias of  $(-0.75 \pm 0.25) \mu m$ . The alignment tolerance of M3 to I2 is  $\pm 0.5 \mu m$ . This layer is mainly used for wiring and as an inductor with M0 as a ground plane. M3 layer over M0 ground plane has a specific inductance of  $1.26 \pm 0.02 pH/\square$  and a fringing factor of  $1.9 \pm 0.1 \mu m$ .

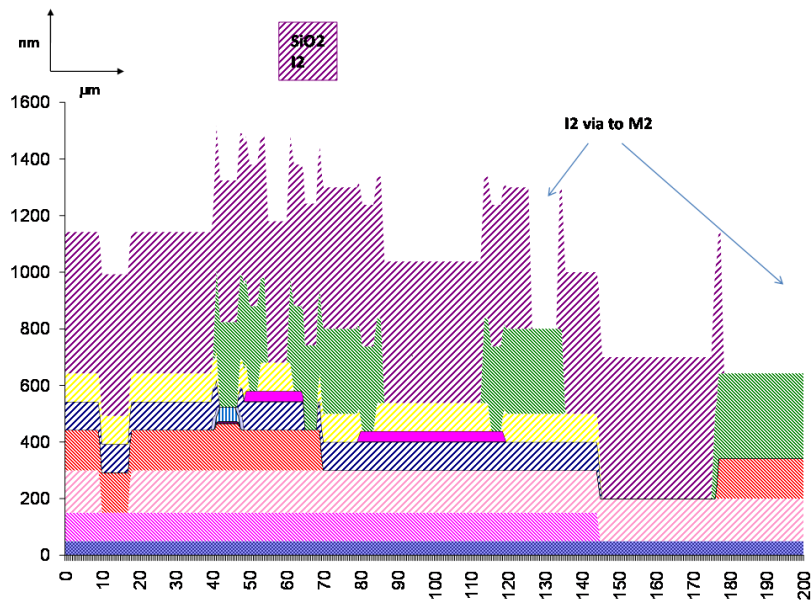


Figure 3.22: The ninth layer I2 - PECVD deposited, dark field mask lithography defining vias to contact pad and M2 wiring, etched in  $CHF_3 + O_2$  mixture, chemically stripped.

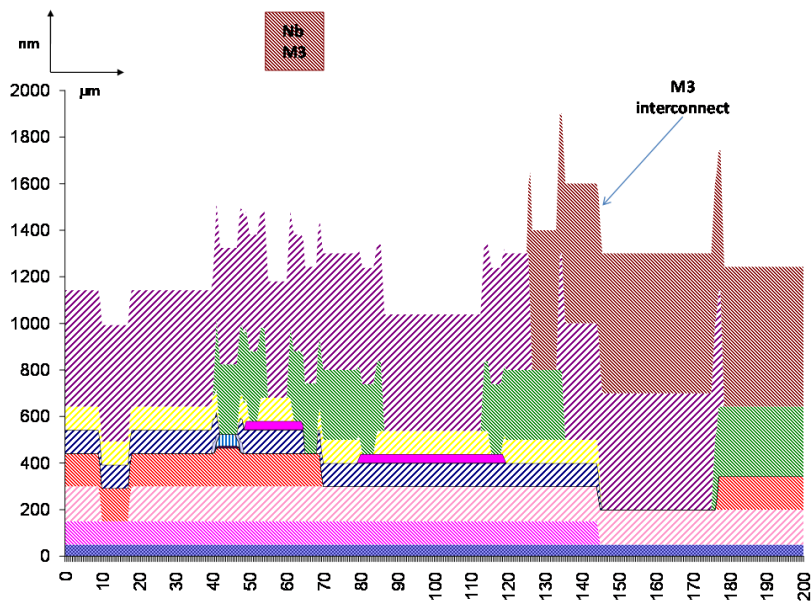


Figure 3.23: The tenth layer - M3, sputter deposited niobium, clear field mask lithography defining M3 interconnects,  $SF_6$  RIE etched, chemically stripped.

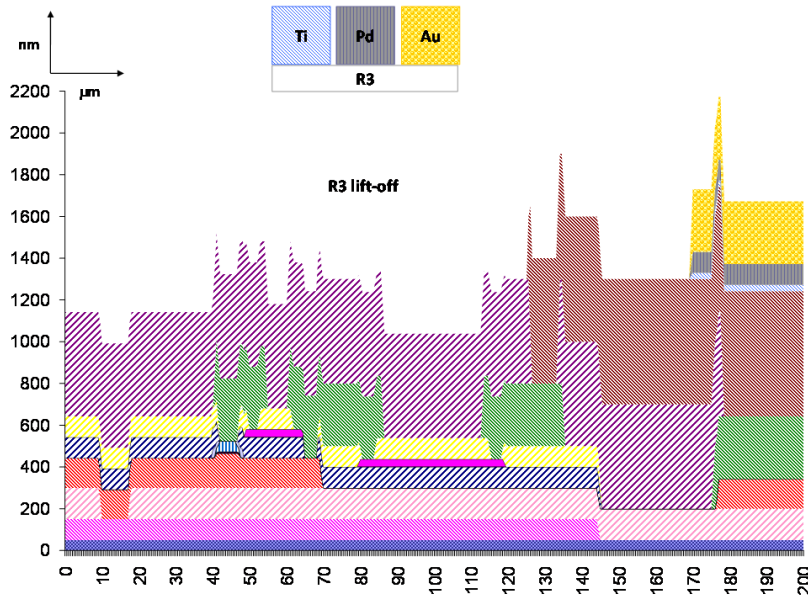


Figure 3.24: The eleventh layer - R3, image reversal lithography using clear field mask defining R3, electron beam evaporated Ti/Pd/Au, Lift-off, chemically cleaned.

11) R3 - Titanium/Palladium/Gold (Ti/Pd/Au) resistor material layer shown in figure 3.24. It is deposited by electron beam evaporation in a vacuum chamber with a base pressure of  $1 \times 10^{-7} T$ . It is grown to a thickness of  $(300/1000/2000 \text{ \AA}) \pm 10\%$  and the film's sheet resistance at room temperature is  $0.23 \pm 0.05 \Omega/\square$  and  $0.15 \pm 0.05 \Omega/\square$  at 4.2 K. The minimum line width  $2 \mu m$ . Contact pads are defined in this layer. The alignment tolerance of R3 to M3 is  $\pm 0.5 \mu m$ .

### 3.5 Unit Process: method and characterization

Each layer is subjected to four steps: thin film deposition, lithography, etch and wet chemical processes as illustrated in figure 3.25. The rest of the section is dedicated to the method and characterization of the unit processes.

#### 3.5.1 Thin film deposition

Two separate systems are used for metal deposition by magnetron sputtering. The first system is dedicated for superconducting metal (Nb) intercon-



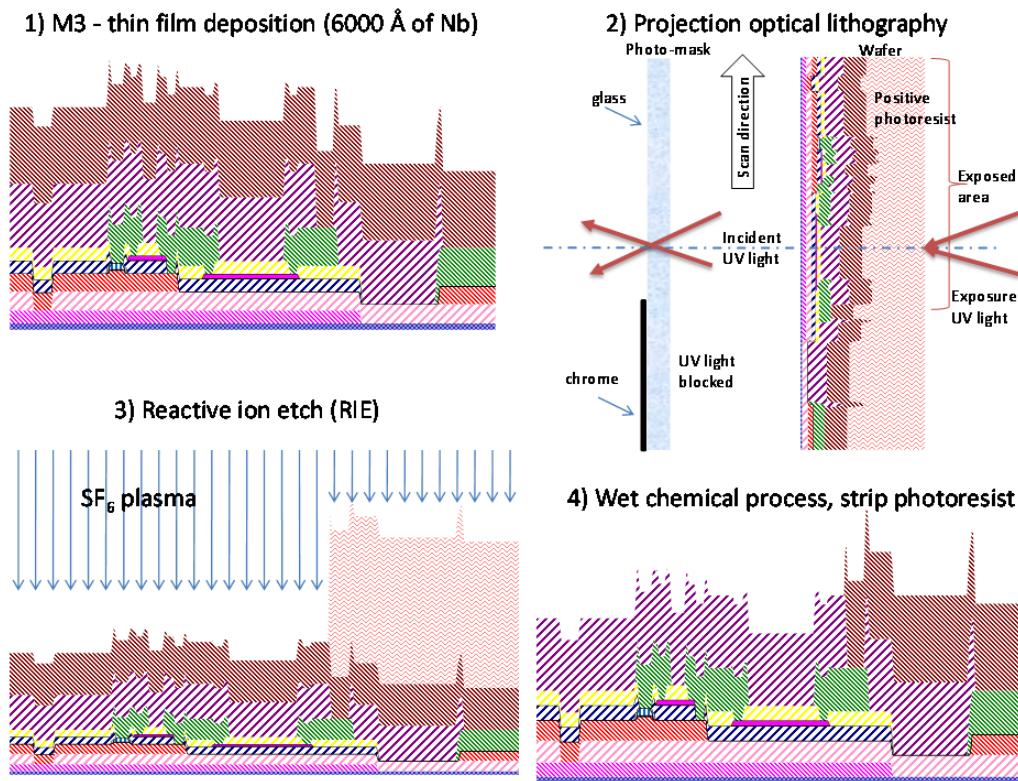


Figure 3.25: The four unit process steps executed on the last superconducting layer (M3). First, the superconductor metal niobium of 6000 Å is deposited by sputtering. Second, photolithography is done on a projection lithography system with a clear field mask using a positive photoresist. Third, the thin film is etched by Reactive Ion Etching (RIE) in  $SF_6$  plasma. Finally, the photoresist is removed and the wafer cleaned using a wet process.

nects (M0, M2 and M3) as well as the resistor layer (R2). The second system is dedicated for an *in situ* deposition of the tri-layer ( $Nb/Al, AlO_x/Nb$ ). Dielectric deposition is done on a PECVD system. Steps for metal and dielectric depositions are given by the process flow diagrams in figure 3.26:

Al deposition is performed in the same run as Nb during the trilayer deposition. The process starts with deposition of about 1500 Å of Nb base electrode followed by 80 Å of aluminum followed by an oxidation to form about 10 Å of  $AlO_x$  barrier. Then the top counter electrode of about 500 Å Nb is deposited completing the tri-layer. Film characterization includes thickness, sheet resistance measurements and insuring stress free deposition conditions. Film thickness and stress are measured by a *Tencor P-10 profiler* with an accuracy of about 20 Å. The profiler characterizes surfaces by scanning it with a diamond stylus. The vertical motion of the stylus and hence the thickness is detected by a capacitive sensor. Sheet resistance is measured using a 4-point probe to measure resistance of an equally spaced leads and converted to sheet resistance with the standard Van Der Pauw relation given by equation 3.2 [81] shown in figure 3.27:

$$\exp\left(\frac{-\pi R_1}{R_s}\right) + \exp\left(\frac{-\pi R_2}{R_s}\right) = 1 \quad (3.1)$$

For symmetric structure  $R_1 = R_2 = R$  Thus:

$$R = \frac{\pi}{\ln 2} \times R_s \quad (3.2)$$

Details of implementation of the Van Der Pauw structures for determining sheet resistance of metal layers is described in the Process Control Monitor (PCM) section. One of the parameters that need to be monitored for thin film deposition is stress in the film which develops during the deposition. There are two components of stress; one is caused by a thermal expansion mismatch of the thin film with the substrate and the second is an intrinsic stress which can depend on variables such as the substrate temperature, deposition rate, and film thickness [82]. Stress is commonly measured using the change in the bow of the wafer before and after film deposition as illustrated in figure 3.28:

$$\sigma = \frac{1}{6R} \xi \frac{t_s^2}{t_f} \quad (3.3)$$

Where  $t_s$  is the substrate thickness,  $t_f$  is the film thickness,  $R$  is the radius of curvature and,  $\epsilon_0$  is the substrate elastic constant  $= 1.805 \times 10^{11} Pa$  for the silicon wafer used in the process. For a chord length much larger than the bow  $R = L^2/8\delta$  where  $\delta$  is the maximum bow, and  $L$  is chord scan length [83]. Film thickness for the interlayer dielectric is measured by Gaertner Sciences

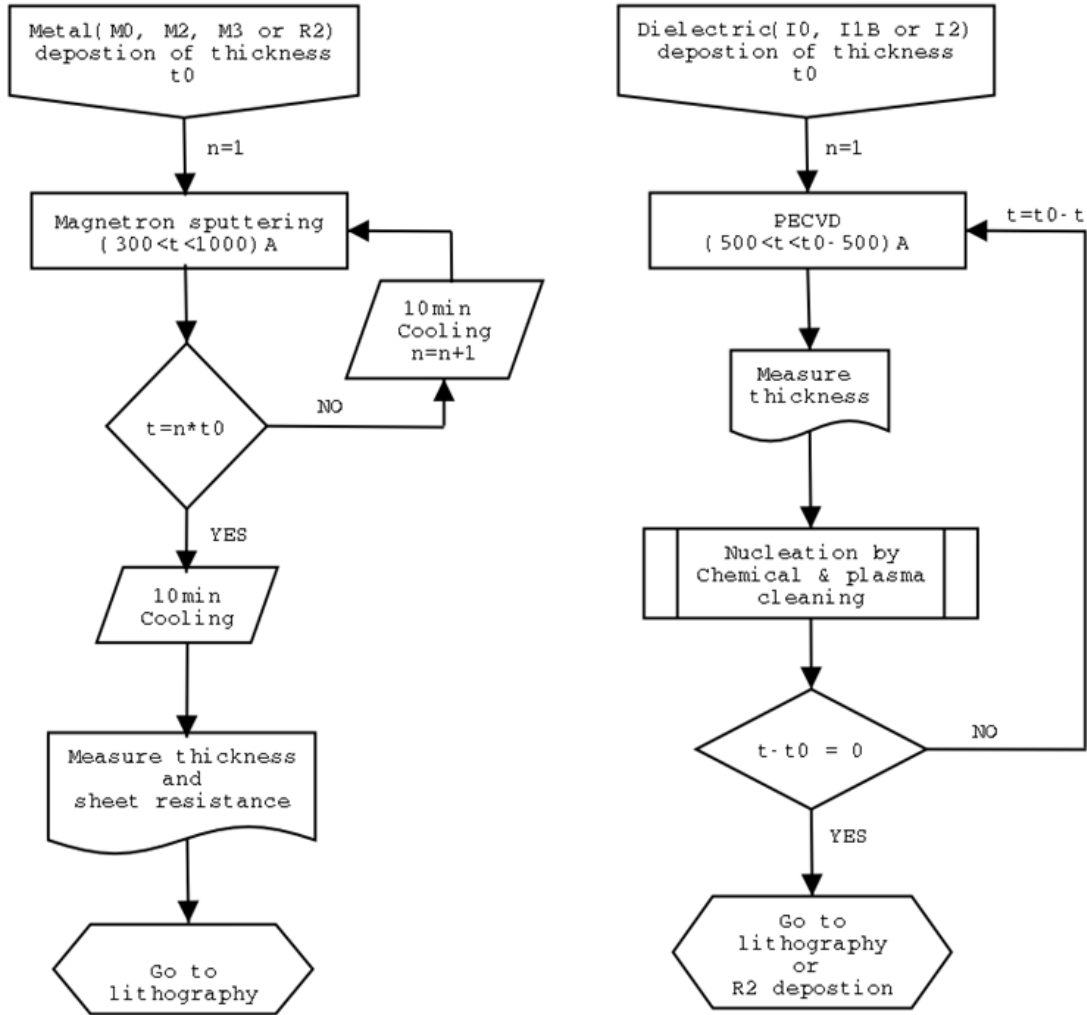


Figure 3.26: Typical process flows for thin film metal and dielectric depositions.  $t$  is the thickness during deposition,  $n$  is the number of depositions and it varies from 1 for M0 and R2 to 6 for M3 deposition. The dielectric thin film process flow is illustrated for the New fabrication process.

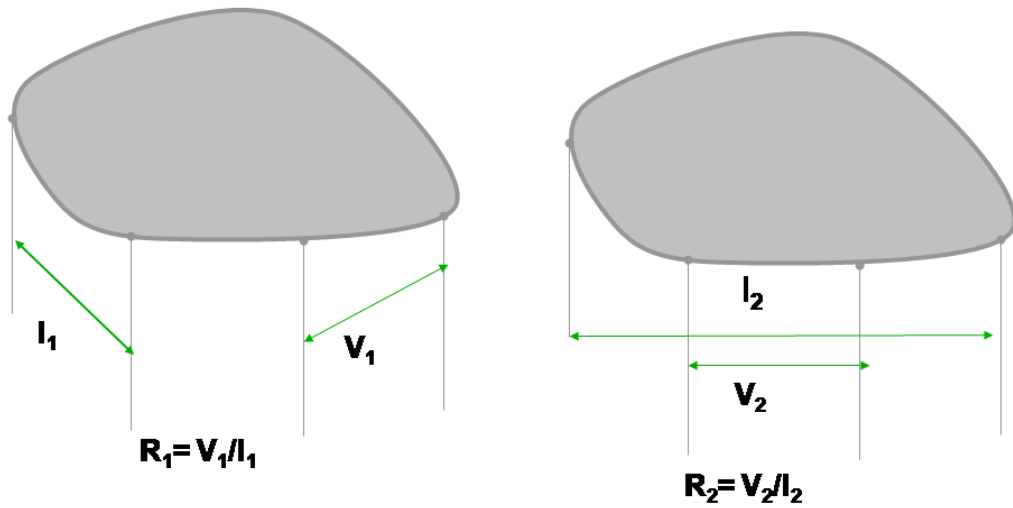


Figure 3.27: Determining sheet resistance of a thin film by Van Der Pauw method.

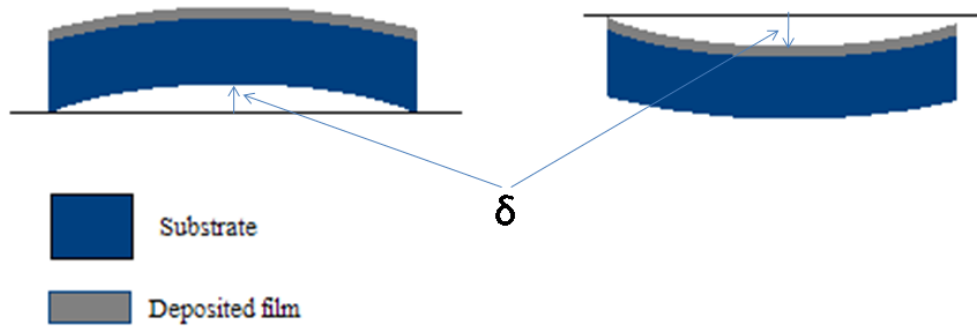


Figure 3.28: Compressive and tensile stress on substrate after depositing a film where  $\delta$  is the change in the deflection in the center of the wafer.

variable angle Stokes ellipsometer *L116S300*. Ellipsometric measurements involve illuminating the surface of a sample with light of a known wavelength and polarization (a low power helium-neon laser light source of wavelength 632.8 nm) and then analyzing the polarization of the reflected light. The ellipsometer has provisions for precise settings of the angle of incidence from 30° to 90° in increments of 5°. After setting the detector angle to be equal to the light source angle the sample table is raised or lowered so that the intersection of the incidence and reflective optical axes occurs on the sample surface. The reflected light with its polarization altered by the optical properties of the sample is detected by the four detectors of the Stokes meter.

### 3.5.2 Photolithography

In HYPRES' conventional  $1.0 \text{ kA/cm}^2$  process, the minimum junction size was limited by the minimum size of a contact hole to the junction and the contact hole alignment tolerance. With the existing photolithography tool (*Perkin-Elmer full 150 - mm - wafer projection aligner*) this size is about  $2 \mu\text{m}$ . This restriction was alleviated by implementing an anodization step right after the junction counter electrode definition by reactive ion etching, enabling the contact hole to be larger than the junction. The lithography tool uses reflective spherical mirror surfaces to project images of the mask into the wafer substrate. The illuminating radiation generated from a high-pressure mercury lamp passes through the condenser and a slit of a few millimeters in width. A set of spherical mirrors are used to generate a narrow, ring-shaped aberration-free arc of light. Wafers are scanned with this arc to produce an image as the mask is moved synchronously in the object plane. One of the outstanding features of projection lithography is its flexibility. The mirror lens system configuration has essentially no chromatic aberration. The exposure wavelength can be simply varied by imposing the appropriate transmission filter between condenser system and the mask. The mercury lamp that is used as light source has high output in the near-UV region (340-450 nm) called UV4; in the mid-UV region (300 - 340 nm) called UV3 and the lower output in the deep-UV region (200-300 nm). For the old fabrication process the UV4 was used while for the new fabrication process UV3 light is being used. The process control during the photolithography includes a critical dimension (CD) measurement on  $1 \mu\text{m} - 4 \mu\text{m}$  bars using a  $15000\times$  objective optical system. The exposure dose is controlled by monitoring lines and spaces of size from  $1 \mu\text{m}$  to  $2 \mu\text{m}$ . The tool is equipped with Automatic Fine Alignment (AFA) providing  $3\sigma$  alignment tolerance of  $0.25 \mu\text{m}$ . Scanning electron microscopy was also used for controlling the photo resist profile and CD during the process development phase. The photolithographic process flow is given in figure 3.29.

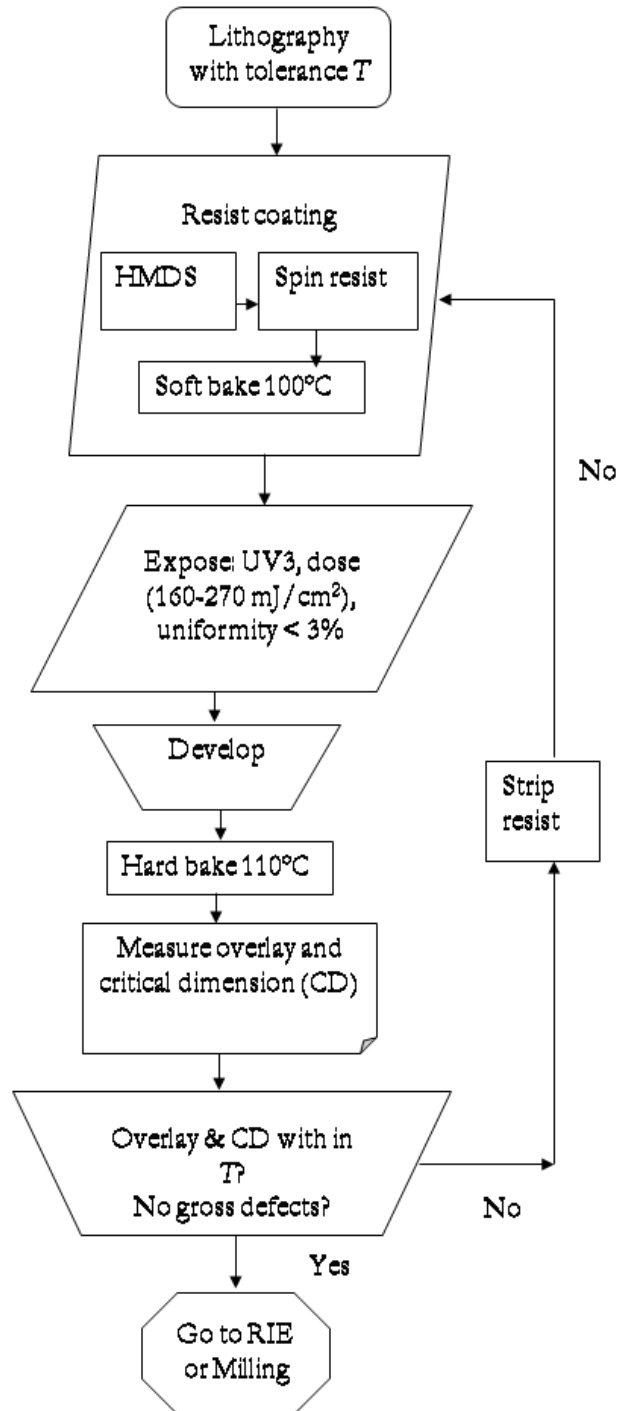


Figure 3.29: Photolithography process flow, typical lithographic tolerances  $0.25 \mu\text{m}$  alignment tolerance, and a CD measured optically on a  $4 \mu\text{m}$  line to be within 10%

### 3.5.3 Thin film etching

Etching of metal and dielectric is done in two Reactive Ion Etching (RIE) systems. The first system is an RIE system with fluorine based chemistries ( $SF_6$ ,  $CHF_3$ ,  $CF_4$ ) and the second one is an inductively-coupled plasma (ICP) etch system equipped with both fluorine and chlorine-based chemistries ( $Cl_2$ ,  $BCl_3$ ). RIE is a preferred method of etching as it is very anisotropic with high selectivity. For niobium etching the most commonly used plasmas are fluorine-based, e.g.,  $SF_6$  plasma. The typical etch parameter consists of an  $SF_6$  gas flowing at 20 sccm in a chamber pressurized to 2 Pascal with the plasma sustained using an RF power of 45 W. All dielectric layers are etched in a  $CHF_3$  and  $O_2$  plasma, 8 sccm of  $O_2$  and 45 sccm of  $CHF_3$  is flown in to the chamber held at a pressure of 13.33 Pa. Etching is done at 150 W RF power while the temperature on the back of the wafer is kept controlled by a chiller set to about  $11^\circ C$ . The bi-layer anodization material of  $Al_2O_3/Nb_2O_5$  has been removed using ion milling. This is done in a chamber pumped down to  $2 \times 10^{-4}$  T with an argon gas flow of 16 sccm, a beam voltage of 500 V with 200 mA beam current giving a milling rate and uniformity for an A1 mill of about  $80 \text{ \AA}/min$  with  $\pm 10$  % uniformity. In the old process the top gold layer (R3) was also milled with the same mill conditions and the rate and uniformity measured was  $326 \text{ \AA}/min$  and  $\pm 10$  % respectively [84]. A *Verity SD1024 spectrometer* is used for end-point detection, with a spectral range of 200 - 800 nm wavelength in 0.5 nm increments. For end point detection the strong fluorine spectra line of 703 nm is monitored for fluorine based chemistries.

### 3.5.4 Wet chemical processes

Wet processing is used to remove the photoresist in acetone, methanol and isopropanol chemical bathes right after etching. Wafers are usually soaked in an ultrasonic acetone bath from 30:00 min to few hours depending on the conditions the photoresist was subjected to. Then they are transferred to a second fresh acetone bath, scrubbed with a queue tip thoroughly and subjected to a half hour or more of ultrasonic while in the same bath. Then it is transferred to a methanol bath after vigorously sprayed with acetone, with an ultrasonic bath for half an hour or more. Then it is transferred to the third and final ultrasonic - isopropanol bath after vigorously spraying with methanol. After half hour or more it gets removed from the bath is vigorously sprayed with isopropanol, and is blown dry with a clean nitrogen gas. After the last common steps described above are performed, one of the following three things is done. If the layer being cleaned is a dielectric it is further scrubbed on a wafer scrubber equipped with a rotating brush, megasonic DI water scrubbing,

vigorous DI + acetone spraying and dried by rotating at much higher speed after being sprayed with methanol. If the layer being cleaned is a metal, then it gets further treatment in an ozone plasma asher. Such sequences of steps are necessary to insure the removal of the photoresist as well as any polymers that may have formed during the RIE etch or ion mill processes. The result is a very clean wafer without any photoresist or polymer. An optical microscope is used for inspection defects and critical dimension measurement.

### 3.6 Re-designing circuits for the new process

A significant part of the cost of establishing any new fabrication process is the cost of conversion of IC designs (and process diagnostics) from an old process to the new one and associated cost of new photomasks. In order to minimize these costs and design labor [51], the following approach was implemented. For transition from a process with the critical current density  $j_c^{old}$  (e.g.,  $1.0 \text{ kA/cm}^2$ ) to a new process with a higher critical current density  $j_c^{new}$  (e.g.,  $4.5 \text{ kA/cm}^2$  or  $20 \text{ kA/cm}^2$ ), the critical currents of the junctions,  $I_c^i$  are kept the same in order to preserve the same inductances in the logic cells. Therefore, the junction areas scale as  $A_i^{new} = A_i^{old} \times (j_c^{old}/j_c^{new})$ . Next, in order to preserve the proper shunting of the junctions  $\beta_c^i \sim 1$ , (where  $\beta_c^i = 2\pi I_c^i (R_s^i)^2 C^i / \phi_0$  and  $R_s^i$  and  $C^i$  are the shunt resistance and capacitance of the  $i^{th}$  junction,  $\phi_0$  is the flux quantum) and preserve the full shunt resistor design including the location of contact holes, the sheet resistance of the resistive layer in the new process is scaled, accordingly, as  $R_{sq}^{new} = R_{sq}^{old} \times (j_c^{new}/j_c^{old})^{1/2} \times (C_s^{old}/C_s^{new})^{1/2}$ , where  $C_s$  is the junction specific capacitance. For example, for the transition from the HYPRES'  $1 \text{ kA/cm}^2$  critical current density process to  $4.5 \text{ kA/cm}^2$  critical current density process, the  $R_{sq}$  of molybdenum resistors was increased from 1 to  $2.1 \text{ } \Omega/\square$ . When this approach is adopted, only two new photo masks are required - one for the junction counter electrode (CE) layer (I1A) and another one for the wiring layer to the junctions CE (M2). (This one is needed only to adjust the length of the bias resistors and, hence, preserve the original circuit bias voltages.) The remaining 9 photolithography layers can be kept unchanged. Another advantage of this approach is that any circuit on the single set of photomasks can be fabricated by either the old or new process or both and hence the performance increase can be easily evaluated. Design conversion errors can also be minimized. The disadvantage of the above approach is that the circuit density remains unchanged. Also the parasitic capacitance of wiring layers increases with respect to the junction capacitance. We believe that the advantages of our approach on the research and development stages of superconductor microelec-



tronics outweigh the disadvantages. Some circuits re-optimization involving other layers (e.g., M2) may be required in the future commercialization stages.

### **3.7 Conclusion**

The "old" fabrication process for  $1.0 \text{ kA/cm}^2$  critical current density has been successfully overhauled and optimized for the new fabrication process with  $4.5 \text{ kA/cm}^2$  critical current density and the potential has been verified up to  $20 \text{ kA/cm}^2$  critical current density with the resolution enhanced lithography technique. This has been achieved by first indentifying and resolving the main limitations of the "old" process, refining the process flow and then proposing and implementing a retargeting approach to migrate designs from the "old" to the new process.

## Chapter 4

# EXPERIMENTAL EVALUATION OF PROCESS AND DESIGN PARAMETERS AND PROCESS CONTROL

Despite the unparalleled advantages of superconducting digital electronics in clock frequency and power consumption, the integration level of superconducting integrated circuits is still very low in comparison with semiconductor integrated circuits. In order to maintain the advantages, the integration level of SICs and the clock frequency need to keep growing. This brings to the forefront the issues of yield, manufacturability, and process control and monitoring as it has been long recognized by the semiconductor counterpart. Both design and fabrication parameters have to be monitored and controlled to insure a stable process. Similar to VLSI circuit fabrication in semiconductor industry, this has been achieved by implementing process control monitors (PCMs). Since superconducting IC fabrication in many respects is similar to semiconductor IC manufacturing as far as the tools and process are concerned, the design of PCMs can use many elements and test structures similar to those implemented in the semiconductor industry except for a few new structures peculiar to superconductors. This section describes the implemented test structures together with the parameters under control.

## 4.1 Description of process and circuit design parameters and test structures

Digital superconducting electronics implements Josephson junctions (JJs), resistors, inductors, and interconnects as circuit elements. A typical 150 mm process wafer contains well more than half a million Josephson junctions and can be populated by a little more than 500 chips of 5 mm x 5 mm die size. In order to meet the increasing demand in complexity of chips some part of the wafer is devoted for a 10 mm x 10 mm die size. Compared to the start of the thesis work, there has been a three-fold increase in the number of 10 mm die chips. This is a direct result of the upgrades in fabrication facilities, equipment and fabrication processes. A set of Process Monitor Control (PMC) chips are included in every mask release to monitor both fabrication as well as design parameters. This section is dedicated to the details of these PCM chips and the parameters which are extracted from them.

### 4.1.1 Josephson junctions

The minimum set of parameters required for circuit design and characterization of Josephson junctions include: critical current ( $I_c$ ), physical area ( $A$ ), normal state resistance ( $R_N$ ), resistance at 2 mV (sub-gap resistance -  $R_{sg}$ ), specific capacitance ( $C_s$ ), gap voltage ( $V_g$ ); and secondary parameters such as the  $I_c R_N$  product, characteristic voltage ( $V_m = I_c R_{sg}$ ) and the ratio of  $R_{sg}/R_N$ . These parameters are extracted using arrays of twenty unshunted circular junctions of various sizes ranging from 0.6  $\mu m$  to 4.0  $\mu m$  in radius.

Figure 4.1 shows the micrograph of test structures used to characterize Josephson junctions. The critical current density and the size bias (missing radius  $dr$ ) are extracted by fitting the data to equation 4.1 [85]. For circular junctions one can relate the critical current,  $I_c$  of a junction with design radius  $r$ , and missing radius  $dr$  to the current density  $j_c$  by:

$$I_c = j_c \times \pi(r - dr)^2 \quad (4.1)$$

Since the critical (switching) current of small-unshunted junctions can be affected by thermal and external noise, 100-junction arrays of critically damped ( $\beta_c = 1$ ), shunted junctions of various sizes were also implemented for complementary extraction of  $j_c$  and  $dr$ . A room temperature electric test of the junction normal resistance was also done by measuring the difference of the resistance of a 100-junction array and the resistance of the same array structure without junctions (only the base electrode, wiring, and contact holes remaining). Arrays of different JJ sizes were used. A good proportionality

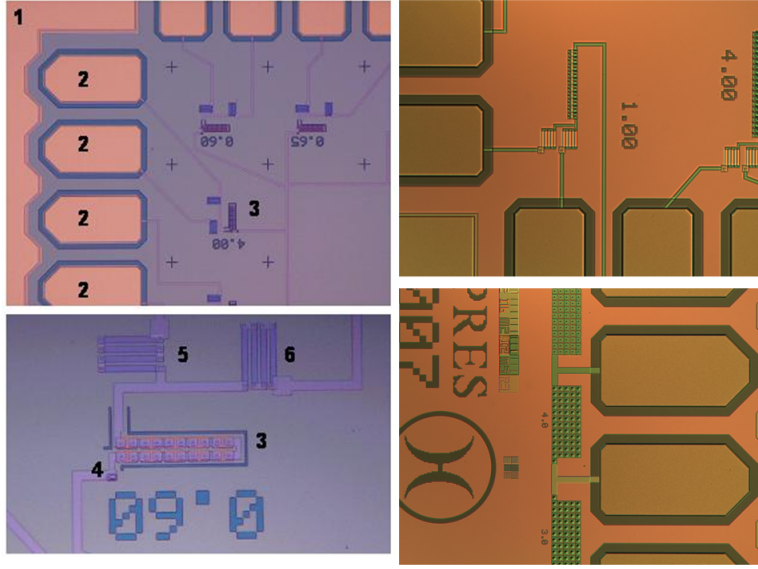


Figure 4.1: Micrograph of test structures used to characterize Josephson junctions: arrays of 20 shunted and unshunted JJs measured at 4.2 K, and array of 100 unshunted JJs for room temperature characterization of junction conductance.

between the junction normal conductance ( $G_N$ ) at room temperature and the Josephson critical current density at 4.2 K was found as expected from the Ambegaokar-Baratoff relationship for  $I_c R_N$  [50]. The experimentally determined  $j_c/G_N$  ratio was used for a quick screening of wafers from these room temperature measurements. junction capacitance can be expressed by a plane-condenser capacitance:  $C = \epsilon_0 \epsilon_r A/d_I$ , where  $\epsilon_0 \approx 8.85 \times 10^{-12} F/m$  and  $\epsilon_r$  is the relative dielectric constant of the interlayer dielectric,  $d_I$ , is the barrier thickness, and  $A$  is the junction area. To determine junctions specific capacitance  $C_s = C/A$ , a simple circuit shown in figure 4.2 was designed. It consists of a small junction (active junction) shunted by a bigger junction (passive junction) and a resistor [86, 87].

The passive junction acts as a parallel  $L_J RC$  resonator where  $L_J$  is the Josephson inductance given by equation 2.17. The active junction generates an AC current that circulates in the loop formed by the active Josephson junction, the passive  $RL_J C$  resonator and the shunt. Resonance happens at Josephson plasma frequency given by equation 2.16. The voltage at which resonance happens is then given by:

$$V_r \equiv \frac{\phi_0}{2\pi} \omega_p \quad (4.2)$$

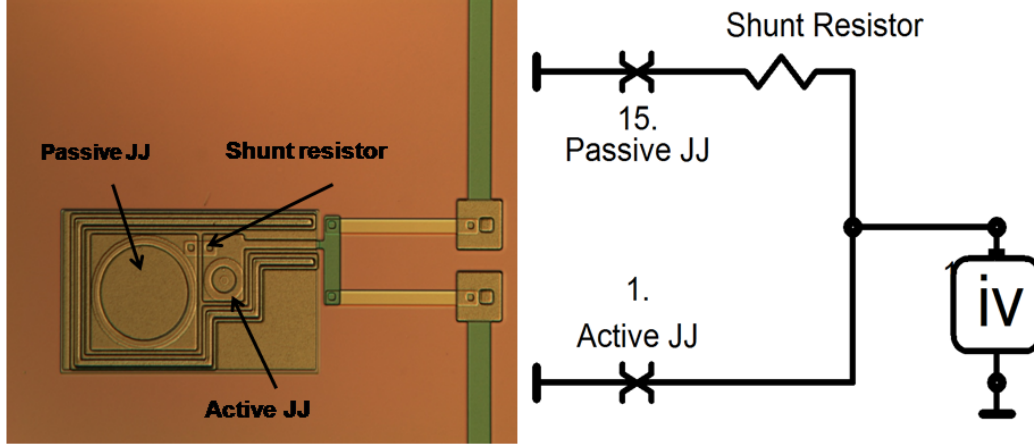


Figure 4.2: Test structure used for extraction of junction capacitance and the respective circuit diagram used for simulation, critical current of JJs  $1 \times I_u$  and  $15 \times I_u$  ( $I_u = 125 \mu A$ ) for the active and passive junctions respectively.

The junction capacitance for a given  $j_c$  is then calculated from:

$$C_s = \frac{\phi_0 j_c}{2\pi V_r^2} \quad (4.3)$$

#### 4.1.2 Thin film resistors

Resistors are needed for shunting JJ, circuit biasing and impedance matching. On average, resistors cover about 1.5% area of the wafer. For thin-film resistors,  $R = R_{sq} N_{sq}$ , where  $R_{sq} = \rho/d$  is the sheet resistance (resistance per square) and  $d$  is the film thickness.  $N_{sq}$  is the effective number of squares that includes the geometric factor  $l/(w + dw)$ , the contribution of corners, and spreading resistance associated with contact holes. Here,  $l$  and  $w$  are the resistor length and width, respectively;  $dw$  is the deviation of the resistor linewidth from the design value (bias) due to lithography and etch processes. All these parameters were extracted from four-probe strip configurations ( $l \gg w$ ) of different widths and meander-shaped resistors. An additional large-size square or cross-type geometry was used to check  $R_{sq}$  independently from Van der Pauw-type measurements [81] as shown in the figure 4.3.

#### 4.1.3 Inductors

The four niobium superconducting layers can be configured in five practical configurations to be used as inductors (micro-strip line) in a superconducting

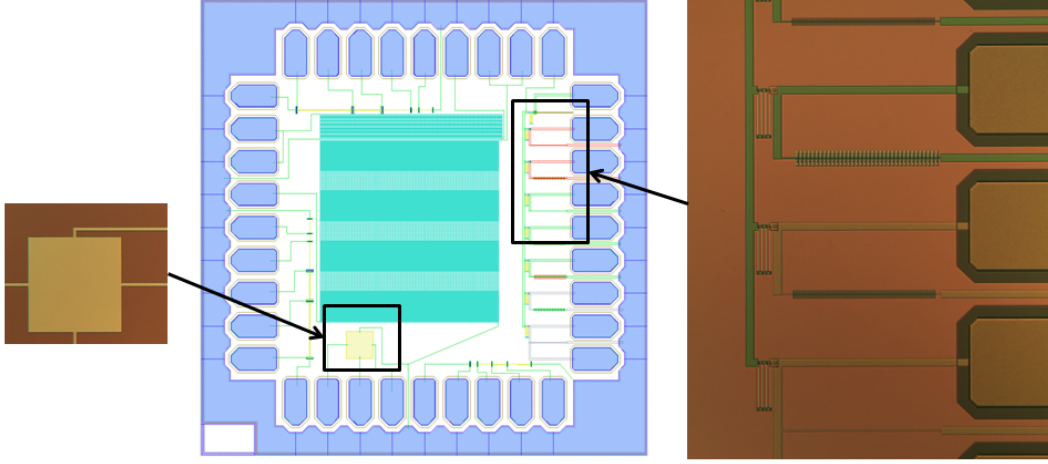


Figure 4.3: Test structure for characterization of circuit resistors and superconducting current carrying capacity of superconducting strips. The parameters extracted were sheet resistance and one side over-etches.

integrated circuit. These configurations are: M1 over M0 ground plane, M1 sandwiched between M0 and M3 ground planes, M2 over M0 ground plane, M2 sandwiched between M0 and M3 ground planes, M3 over M0 ground plane. For a superconducting micro strip, the inductance  $L$  can be written in the form:

$$L = L_{sq} \times \frac{l}{(w + b)} \quad (4.4)$$

Where:  $L_{sq}$  is the inductance per unit square of the micro strip line,  $l$  is the micro strip length, and  $w$  is its width and  $b$  is a combination of the width bias (from lithography and etch) and its fringing factor that characterizes the edge effect of the magnetic field at the sides of the strip line. Superconducting Quantum Interference Devices (SQUIDs) are used to measure the inductance of micro-strip lines, shown in figure 4.4. The structure has three taps in which currents can be applied and voltages measured. Such a configuration allows one to do three independent measurement namely  $L_1$ ,  $L_2$ , and their sum ( $L_1 + L_2$ ). Each measurement contains the parasitic inductance  $L_p$ . By design the length of  $L_1$  is two times that of  $L_2$ . Measurement of an individual configuration is done by applying a current  $I + I_b + i$  on the first lead connected to the inductor, and a  $-I$  currents on the other lead connected to the same inductor.  $I_b$  is set to 70% of the critical current of the junctions ( $I_c$ ), and the SQUID modulation is achieved by sweeping the current  $i$  from 0 to about 50%  $I_c$ . The output voltage  $V$  is then sensed on the third lead.

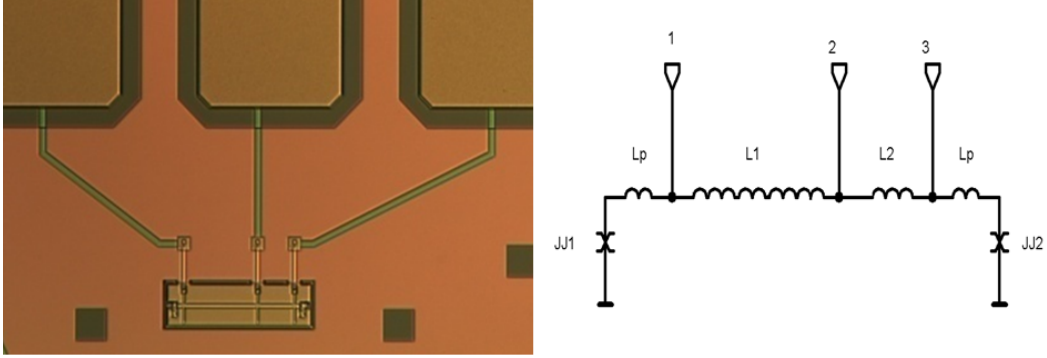


Figure 4.4: Micrograph of a test structure used to extract inductance values of microstrip lines included as part of a SQUID (left) with the corresponding circuit diagram (right).

A simulation of a typical output voltage ( $V$ ) as a function of modulation current ( $I$ ) is shown in figure 4.5. The product of the inductance of the inductor, including its parasitic and the period of the modulation current is equal to the flux quanta ( $\phi_0$ ). The inductance per unit length for a given width is determined after subtracting the parasitic inductance. Each test chip, for the five inductance configurations, is populated with the test structure described above with widths varying from 3.0 to 20.0  $\mu m$ . The sheet inductance and the fringing factor are then extracted by fitting the results to equation 4.4.

The effective sheet inductance ( $L_{sq}$ ) and the width bias ( $dw$ ) are extracted from the inverse of the inductance per unit length measurements as a function of the width of the microstrip lines using a linear regression. The x-axis intercept corresponds to an effective width offset  $dw$ , due to a combination of over-etch and edge-field - fringing factor. The reciprocal of the slope is the effective sheet inductance  $L_{sq}$  figure 4.6.

#### 4.1.4 Interconnects and interlayer dielectric

Niobium thin film wires are used for interconnecting circuit elements; The interconnections can be formed in any of the four superconducting layers. The following parameters are monitored for the superconducting layers: critical temperature  $T_c$ , critical current per unit width of the wire, and the line-width bias extracted from electric measurements in the normal state. The critical current of wires depends on the layer surface topography and reduces if the wire crosses over edges of underlying structures. Resistance measurements on meander- and comb-type structures are used to monitor the lithography and etch processes at the minimum allowed line spacing as well as particulate

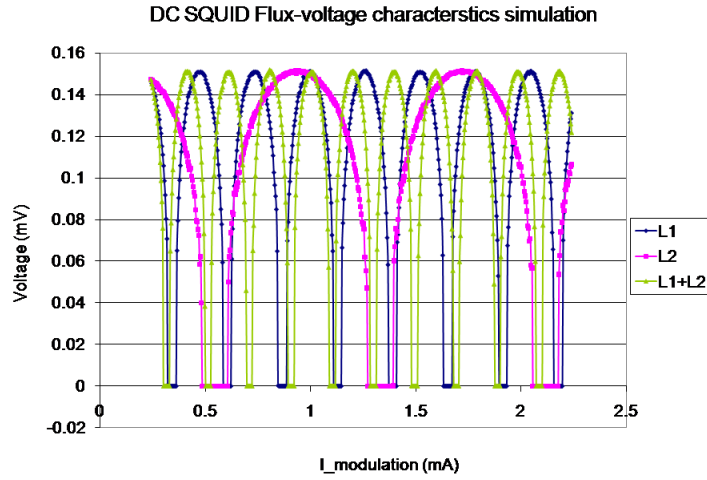


Figure 4.5: Simulation output of SQUID flux-voltage characteristics with  $I_c = 2$ ,  $L_1 = 1$ ,  $L_2 = 2$  (all in PSCAN units [71]). The product of the inductance and the period of I modulation is equal to the flux quantum ( $\phi_0$ )

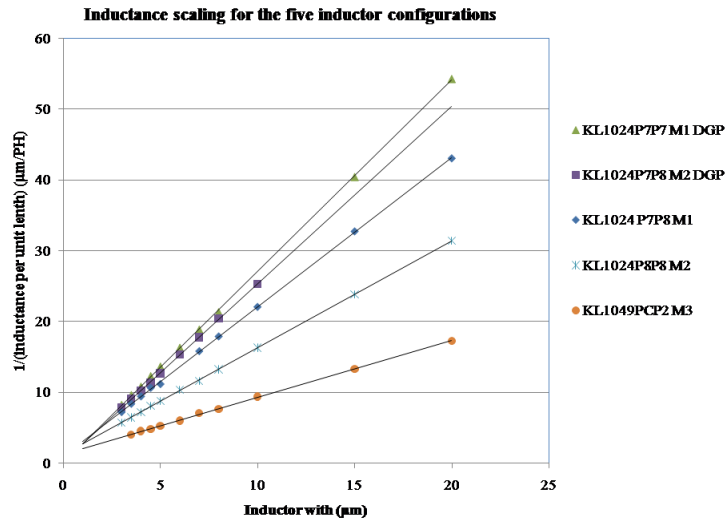


Figure 4.6: Reciprocal inductance per unit length as a function of microstrip line width for the five inductor configurations. The x-axis intercept gives an effective offset of the width  $dw$ , The reciprocal of the slope gives the sheet inductance ( $L_{sq}$ ).



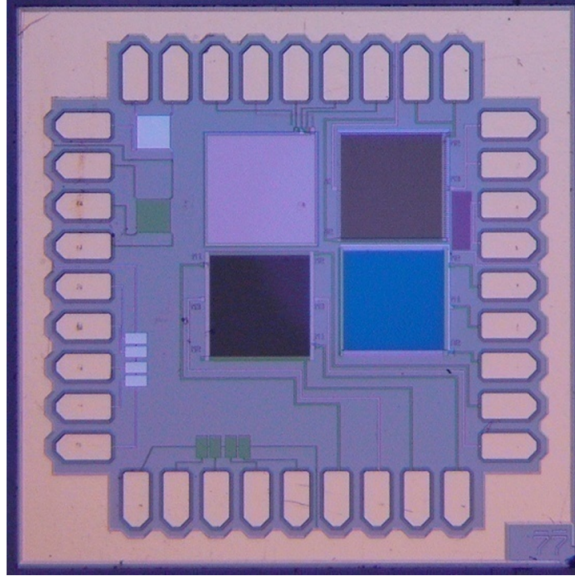


Figure 4.7: PCM chip for characterizing interconnect and interlayer dielectric.

defects causing shorts between the lines [88]. Different layers are connected to each other by using contact holes. There are three types of contact holes between the four superconducting layers, labeled as I0 (between layers M1 and M0), I1B (between M1 and M2, between resistor layer R2 and M2; and between junction counter electrode layer I1A and M2), and I2 (between layers M2 and M3). The largest HYPRES circuits contain about  $6 \times 10^4$  I1B contact holes. Contacts between nonadjacent layers (e.g., M2 to M0) are formed using vias presenting several contact holes placed on top of each other (e.g., I1B over I0). Patches of corresponding intermediate metal layers are needed (e.g., M1 in the example above) to achieve high superconducting critical currents of vias. The critical current of all types of the contact holes and vias of the minimum size allowed by the Hypres Inc., Design Rules were monitored using arrays of 10,000 contact holes for I0 and I2, and 30,000 I1B contact holes. A quick characterization of the lithography contact holes and etch processes was also done by room temperature resistance measurements. Silicon dioxide deposited by low temperature Plasma Enhanced Chemical Vapor Deposition (PECVD) is used as an interlayer dielectric (ILD). Four  $SiO_2$  layers are needed to insulate five metal layers. The main parameters that are monitored are the ILD thickness and specific capacitance. The thickness was measured using a *Tencore P-10 profilometer* and a *Gartner ellipsometer*. Plane capacitors between various metal layers were used for specific capacitance measurements. Another parameter of the prime importance is the ILD integrity and step

coverage. It was monitored by checking for electric shorts between wires in different layers placed over different topographies such as a meander over a plane, a meander in one metal layer crossing over meanders in one or several different metal layers, a meander in one metal layer going along the edge of a meander in a different metal layer shown in figure 4.7.

## 4.2 Electrical measurements and extraction of parameters

All the measurements that have been performed to extract parameters for junctions, resistors, inductors, and interconnect were dc I-V type. A typical 5 x 5 mm chip has 36 pads to which the different test structures are connected. Up to four chips can be loaded on a 4x-probe and pushed against probe-fingers by applying a predetermined torque on the screws. The probe is equipped with a removable RC low pass filter so that external noise due to electromagnetic interference and the equipment itself could be blocked. Once loaded on the probe, the room temperature resistance of the contact pads is measured to insure that all the pads including the ground are connected to the respective channels of the measurement setup. A three layer  $\mu$ -metal magnetic shield is secured on the probe. Then it is time to cool by slowly lowering the probe inside the shielded Dewar to the liquid helium level, cooling it from room temperature to 4.2 K. Automated testing of superconducting circuits requires a system that can do a set of operations including but not limited to: simultaneously supply of regulated of DC-power, provide a means to extract the resistance values of all the pads of the chip connected to the circuits, measurement of IV characteristics, generation of digital test patterns, analysis of digital responses, and search for multi-dimensional parameter bias margins of circuits. A setup that can do all the above stated functions and more has been developed and implemented in the RSFQ laboratory at Stony Brook University (OCTOPUX) [89]. Electrical testing of all PCM chips and digital low frequency measurements were done using OCTOPUX, figure 4.8.

### 4.2.1 Measurement setup

Low speed electrical measurements were all performed using OCTOPUX - multifunctional test system figure 4.8, which is capable of performing exhaustive tests of large digital and analog circuits. OCTOPUX features 64 regular I/O channels, 32 auxiliary read-only channels, high-accuracy voltage measurements using a precise Keithley 2001 multi-meter or fast measurement using the

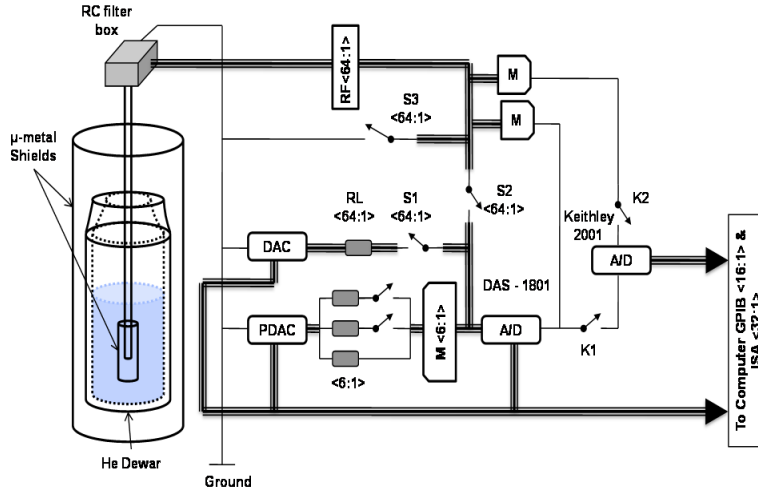


Figure 4.8: OCTOPUX: an advanced automated setup for testing superconductor circuits.

DAS-1801 board. The data acquisition rates is 400 Hz and an effective RMS noise of  $0.15 \mu V$ . There are 70 16-bit D/A converters with output currents up to  $\pm 5 mA$  on a loading resistor  $R_L = 2 k\Omega$ . Six independent high power current sources can provide output current in three different ranges depending on the load resistor selected :  $\pm 30 mA$  for  $R_L = 9.1 \Omega$ ,  $\pm 200 mA$  for  $R_L = 52 \Omega$ ,  $\pm 1 mA$  for  $R_L = 302 k\Omega$ . These power sources are interfaced to any regular channels using the relay multiplexers  $M1 - M6$ . It has 64-bit digital pattern generation with programmable output levels. Basic measurements are done by independently commuting channels, connecting regular current sources to the channels, upon switching the  $S_1$  relays on, and disconnected using relay switch  $S_2$ . Relay switch  $S_3$  is used to short-circuit all the pads of the chip to the ground, which is useful when connecting and disconnecting the setup to the probe and when cooling down the circuit. This directs any current that may be flowing in the circuits to the ground thus avoiding the possibility of flux trapping.

## 4.2.2 Parameter extraction

Diagnostic test chips have been designed in such a way that both the fabrication and the design parameters can be extracted and controlled. Ten  $5 \times 5$  mm PCM chips with test structures covering all the parameters described in section 4.1 were used. They were placed in five representative locations

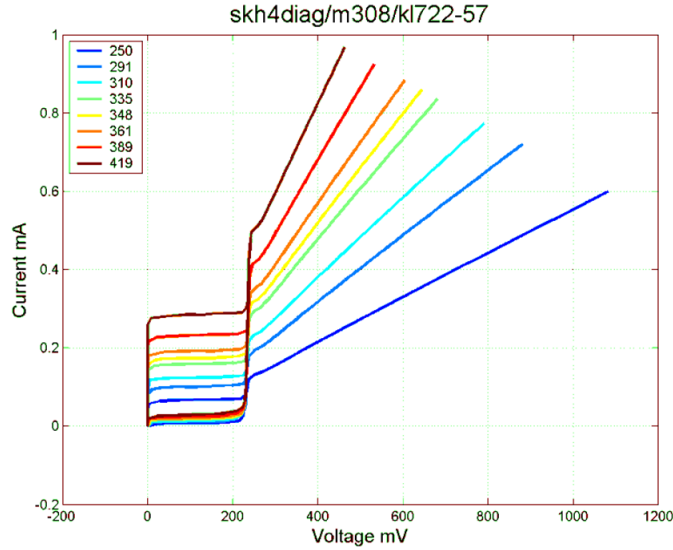


Figure 4.9: Typical IV curves of 100-junction arrays of circular junctions with diameter ranging from 1.5 to 3.5  $\mu m$ .

on the wafer: in the center and in the middle of the four quadrants, labeled as (+,+), (-,+), (-,-), and (+,-). For over a year now, these locations have been kept the same in order to monitor the uniformity of parameters across the wafers and run-to-run reproducibility. All electrical measurements were done entirely by OCTOPUX in a shielded room as described in the previous section. Upon cooling the 4x probe to liquid He temperature, all the chips were measured sequentially. This allowed us to reduce significantly the time wasted during probe cool down and warm up. Test algorithms have been developed for all of the diagnostic chips such that a single command could automatically measure, collect, and log the data. A database system with a web-based interface easily accessible from the intranet has been developed to automate the display of results and to do trend analysis and correlation. Figure 4.9 shows the typical IV measurements of arrays of 100 circular Josephson junction of on chip diameter ranging from 1.5  $\mu m$  to 3.5  $\mu m$  in diameter.

The critical current density spread on the 5 x 5 mm chip is best visualized by normalizing the curves with their normal resistance  $R_N$  because the junctions of different sizes can be easily compared as shown in figure 4.9. This gives the total 1  $\sigma$  spread across a 5 mm chip of 2.4%, whereas spread inside individual arrays is less than 1.2%. However, the above given spreads of critical currents includes both the thermal noise and the "fabrication" noise figure 4.10. Subtracting the thermal noise from the measured spreads of crit-

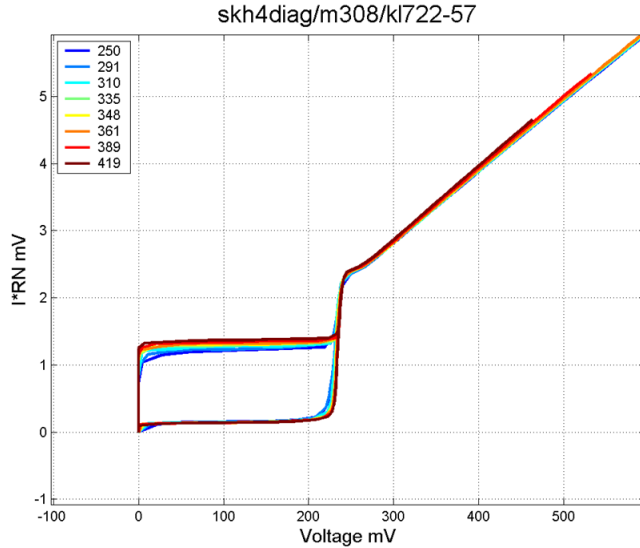


Figure 4.10: Normalized IV curves show the critical current spread across the chip of about 2.4% as compared to the spread within individual arrays with less than 1.2%

ical currents would result in yet lower fabrication spreads. One of the main parameters is the junction critical current spreads. Our goal was to achieve 1  $\sigma$  spread of less than 3%. This was done both by choosing the right anodization method and by optimizing anodization and etching parameters.

For unshunted junctions a four-point measurement was done on each array. The automated algorithm is centered on finding a median switching current that is defined as a current at which 50% of the junctions in the array switch. The data were fit to a parabolic function equation 3.2 to extract the critical current density ( $j_c$ ) and the "missing" radius ( $dr$ ), figure 4.11. One of the most important parameters for VLSI superconducting circuit fabrication is the on-chip uniformity of JJ critical currents. Along with defect density it determines the complexity of yieldable circuits.

For all JJ sizes used in the circuits, the  $I_c$  uniformity was measured on 20-junction arrays of unshunted junctions as shown in Fig. 2. Also, 30 and 100 junction arrays were used to measure the  $I_c$  spreads for two representative values: the smallest  $I_c$  and the most frequent  $I_c$  used in the circuits. Details of the  $I_c$  deviations and the effect on largest yieldable circuit is given in chapter five. The full range of spread (the difference between the largest and the smallest current in the array) was used to estimate the standard deviation  $\delta I$  by assuming normal distribution.

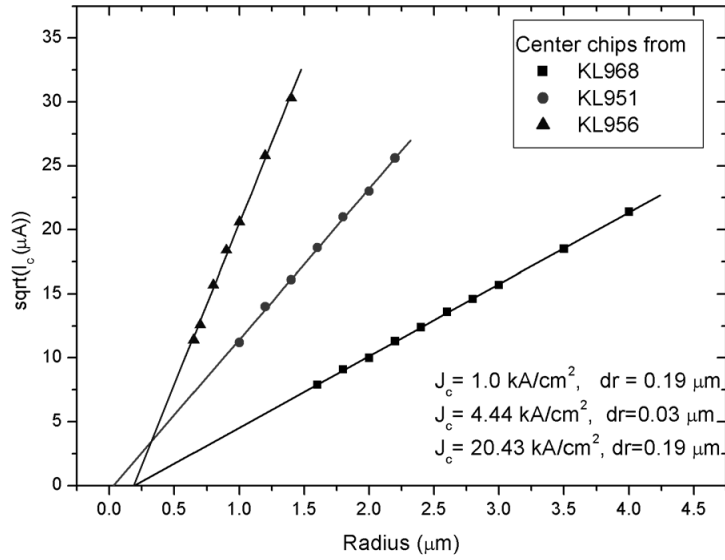


Figure 4.11: Critical currents of 20-junction arrays of circular unshunted JJs of different sizes for the three current density processes. Fit to  $I_c = j_c \times (r - dr)^2$  is shown by straight lines. The data are from PCMs located at the wafer center.

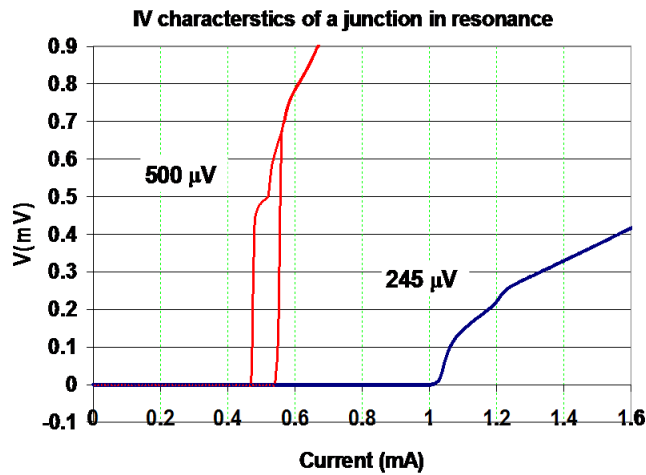


Figure 4.12: I-V characteristic of junctions of capacitance measurement. The respective resonance steps for both  $1 \text{ kA/cm}^2$  and  $4.5 \text{ kA/cm}^2$  process are  $245 \text{ } \mu\text{V}$  and  $500 \text{ } \mu\text{V}$  respectively. This corresponds to junction's specific capacitance of  $5$  and  $6 \text{ } \mu\text{F/cm}^2$  respectively.

Table 4.1: Summary of average inductance measurements.

Inductor configuration	Normalized sheet inductance, $L_{sq}/L_0(L_0 = 2.63 \text{ pH})$	Fringing factor (m)
M0-M1	$0.18 \pm 0.01$	$0.48 \pm 0.32$
M0-M1-M3	$0.15 \pm 0.01$	$0.34 \pm 0.12$
M0-M2	$0.27 \pm 0.02$	$1.15 \pm 0.1$
M0-M2-M3	$0.16 \pm 0.01$	$0.31 \pm 0.15$
M0-M3	$0.52 \pm 0.03$	$2.52 \pm 0.3$

Figure 4.12 is a typical I-V measurement done on a test structure for determining junction capacitance. The  $1 \text{ kA/cm}^2$  test structure was properly shunted and it is easy to see the resonance steps, which was about  $245 \text{ } \mu\text{V}$  which corresponds to a specific capacitance of about  $5.5 \text{ } \mu\text{F/cm}^2$ . However the  $4.5 \text{ kA/cm}^2$  test structure was under-shunted making the I-V curve hysteretic. The resonance voltage of  $500 \text{ } \mu\text{V}$  is still readable on the back-trace. This corresponds to  $6.0 \text{ } \mu\text{F/cm}^2$  specific capacitance. The junction specific capacitance was extracted from an I-V curve of a small junction RF-coupled to a large junction, similar [86]. A pronounced step on the I-V curve was observed, corresponding to the plasma resonance in the large junction equation 4.2 and equation 4.3. The specific capacitance data obtained in this way for  $1.0 \text{ kA/cm}^2$  process are:  $C_s = (55.9 \pm 3.2) \text{ fF}/\mu\text{m}^2$ , averaged over 9 wafers. For the  $4.5 \text{ kA/cm}^2$  process, only four test structures were measured from three wafers, giving  $C_s = (63.4 \pm 1.0) \text{ fF}/\mu\text{m}^2$ . A summary of the resulting sheet inductance and the fringing factor measurements is shown in table 4.1 for the five-inductor configurations.

The cells of the HYPRES design library are optimized in such a way that any cell can tolerate simultaneous deviation of all inductances up to  $\pm 40\%$ , and of any single inductance up to  $\pm 40\%$ . The minimum line-width of inductors currently implemented in HYPRES circuits is  $4 \text{ } \mu\text{m}$ . At this minimum line-width, the inductance was found to be the easiest of all parameters to control. Show in figure 4.13 inductance trend chart of the data collected from six wafers fabricated in the last six months. None of the five inductor configurations deviated more than  $\pm 10\%$  from the designed value.

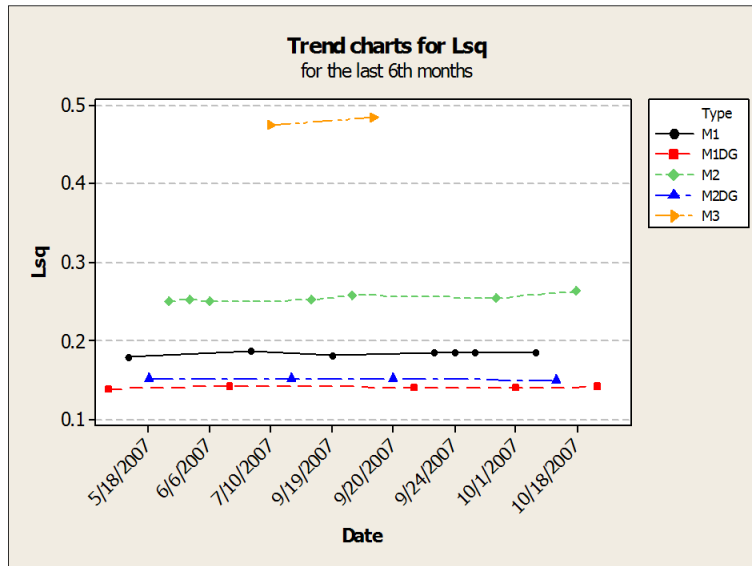


Figure 4.13: Inductance trend chart of the data collected from six wafers fabricated in the last six months.

### 4.3 Conclusion

A set of diagnostic chips has been developed for monitoring the superconducting IC fabrication process and extracting all the design and fabrication parameters. An automated test setup, OCTOPUX has been used to test the parameters for junctions, resistors, inductors and interconnects. Junction critical current spread from wafer to wafer as well as chip-to-chip has been found to be hard to control limiting the complexity level of circuits. Parameters for inductance and resistance have been within the design specification of  $\pm 10\%$ .



# Chapter 5

## DIGITAL AND MIXED SIGNAL APPLICATIONS

### 5.1 High speed benchmark test

It became a custom to characterize the maximum operating speed of superconducting circuits using the maximum frequency of the divide by two operation of the static frequency divider based on the TFF gate [4, 5], [3],[2]. The implemented test circuit contains 20 JJs, the layout of which is shown in the figure 5.1. The analog testing was based on comparing the input voltage and twice the output voltage (both related to the input and output frequency by the Josephson relation ( $hf = 2eV$ )), and is similar to that reported in [4, 5], [3], [2]. The maximum input voltage (frequency) was measured as a function of the circuit bias current using an automated test set-up OCTOPUX. Contrary to the experimental procedures in [4, 5] where 4 independent current sources were used to bias a total of 8 Josephson junctions in the circuit, a single main bias was used in this work for the JTL and TFF as it is more appropriate for a digital process.

A second current source was used to control the DC/SFQ converter and vary the input frequency. The typical dependence of the input frequency applied to the divider (converted from the input voltage using  $hf = 2eV$ ) and the output frequency of the divider as a function of the bias current of the DC/SFQ converter are shown in figure 5.2. Different curves correspond to the different main biases applied to the circuit. The frequency where  $2 \times f_{out}$  starts to deviate from  $f_{in}$  is the maximum operating speed,  $f_{max}$  at a given bias. This maximum frequency is shown in Fig. 4. It can be seen that the margins of the circuit operation are very wide. For instance, at 325 GHz input frequency, the margins on the main bias current are  $\pm 13\%$ . The margins shrink to zero

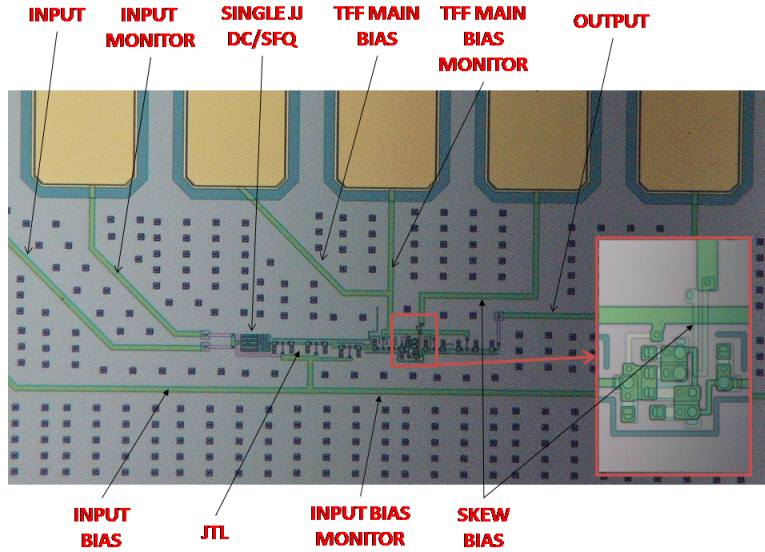


Figure 5.1: Layout of digital frequency divider circuit with a single stage static divider implemented for maximum frequency test.

at  $400\text{ GHz}$ . Please note that at this point the circuit is still not limited by the TFF speed but rather by the generation in the JTL. We conducted an additional experiment where the extra current source was used to separately bias the JTL between the DC/SFQ and the TFF. In this case the maximum operating frequency was found to be about  $500\text{ GHz}$ .

Information about the highest frequencies of operation can also be extracted by measuring the operating margins of a skew bias, figure 5.3. The skew bias acts as a gate - by changing the current flowing through the coil the inductance of the quantizing loop of the TFF is varied by inductive coupling. The vertical axis is depicting the deviation of the input frequency from twice the output frequency.

Table 5.1 summarizes the operating frequency as well as the margins on the skew bias. The maximum operating frequency is the frequency at which the skew bias margin goes to zero and is obtained by extrapolating. This frequency is about  $227.9\text{ GHz}$  for the new process measured on the latest release of wafers for  $4.5\text{ kA/cm}^2$

## 5.2 Typical circuit implementations

One of the highly pursued and successful applications of SCE is to directly digitize radio frequency (RF) signals right from the antenna (Digital-RF).

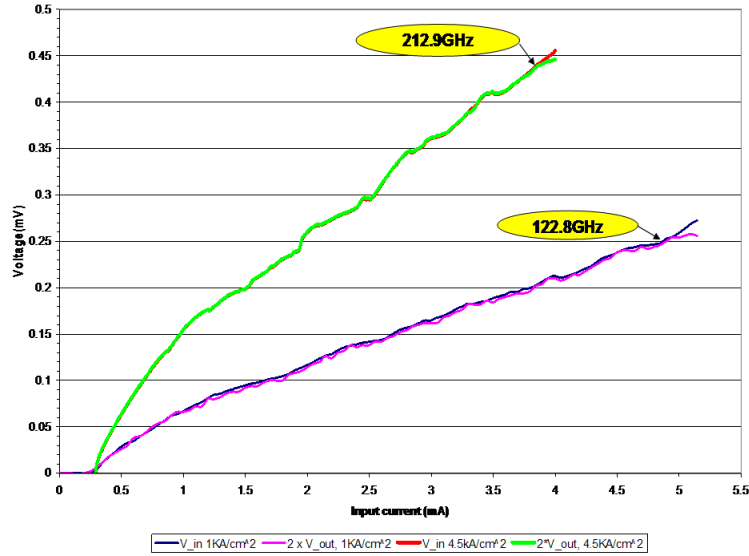


Figure 5.2: Typical input output characteristic measurements done on a digital frequency divider for high frequency test with  $V_{in}$  and  $2 * V_{out}$  as a function of input current, for  $1.0 \text{ kA/cm}^2$  and  $4.5 \text{ kA/cm}^2$  processes.

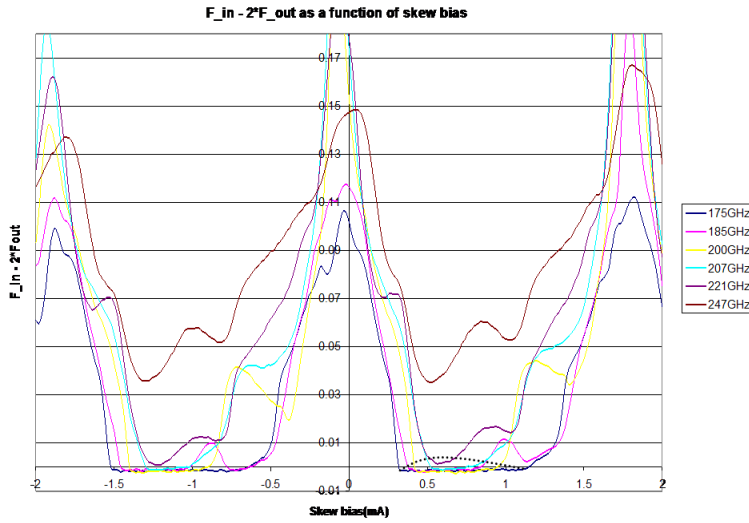


Figure 5.3:  $F_{in} - 2 * F_{out}$  as a function of Skew bias for different input frequencies, the skew bias is used to change the inductance of the quantizing loop and hence is a direct manifestation of the margins of operation of the T flip-flop for the given frequency.

Table 5.1: Skew bias margins for T-flip flop operating at different frequencies.

Frequency of operation (GHz)	skew bias	
	mA	%
175	$0.74 \pm 0.42$	$\pm 56.7$
185	$0.74 \pm 0.36$	$\pm 48.6$
200	$0.69 \pm 0.25$	$\pm 36.2$
207	$0.67 \pm 0.17$	$\pm 25.4$
221	$0.60 \pm 0.06$	$\pm 10$
227.9	$0.47 \pm 0.0$	$\pm 0.0$

The last value is an extrapolation to zero bias margin

The success of digital-RF stems from the fact that the conventional analog-RF technology fails in many respects to meet the current and future demands of military and commercial RF applications. Some of the pressing demands include better utilization of the RF-spectrum, moving towards the higher frequency, wider bandwidth and, greater flexibility in interfacing to input and output. Digital-RF application would extend the digital processing to the analog domain, a concept commonly referred to as software radio [90]. Such an application would make it possible to replace the single band, single mode traditional RF radios with software-programmable digital hardware avoiding the frequency and protocol specific hardware. Direct conversion between analog and digital domains at several  $GHz$  frequencies can be achieved using mixed-signal RSFQ [91]. The analog-to-digital conversion takes advantages of high speed, low power, quantum accuracy, high sensitivity and low noise inherent to RSFQ technology. [92, 93]. HYPRES has developed a multi-band, multi-channel digital RF transceiver architecture to harness the opportunities presented [94]. In this section some of the successful implementations of parts of the transceiver architecture in the new process will be presented. The receiver side has already been developed to an integrated-system level and delivered to customers as cryo-packaged wideband single channel RF receiver using a low pass analog-to-digital converters (LP ADC)s and a band-pass(BP) ADC [29, 95]. The All Digital Receiver (ADR) chips used for the systems have a front end and a channelizing unit. The front end is some form of ADC modulator (Low Pass Phase Modulation Demodulation (LP-PMD) or a Band Pass BP) and a clock source (internal or external) which takes the analog RF input and produces a digitized single bit data stream as an output digitizing the RF signal. The digital RF output together with the clock is fed to the channelizing unit for further processing. The digital channelizer accepts the

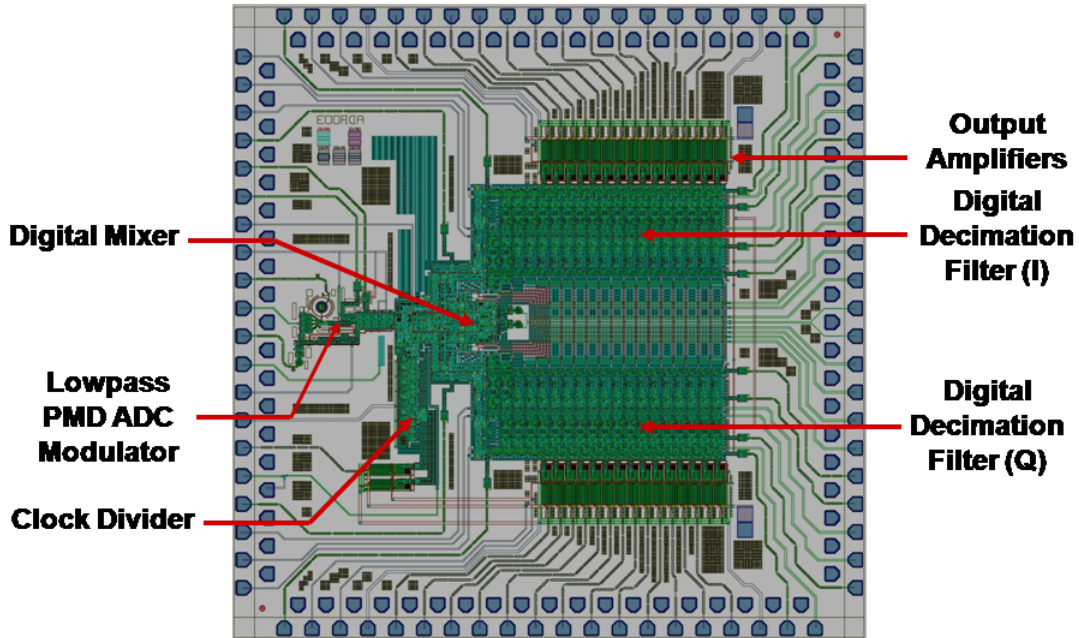


Figure 5.4: Layout of an All Digital Receiver (ADR) with a Low Pass Phase Modulation-Demodulation Analog-to-Digital Converter (LP-PMD ADC) and a Digital Channelizer.

single-bit oversampled data from the front end and produces the in-phase ( $I$ ) and quadrature ( $Q$ ) digital outputs of the signal. The main components of the channelizer are a single bit  $I/Q$ -mixer, local oscillator, digital decimation filters, and output amplifiers. The low pass all-digital receiver (LP ADR) chip is assembled on a 1 cm x 1 cm die and contains about 10,500 JJs and operated up to 24.32 GHz clock frequency on the cryo-cooler and up to 28.16 GHz in liquid helium [96]. The micro-graph of the chip is presented in figure 5.4.

In the present design, the output data from digital filters are delivered to the room temperature interface electronics by using a parallel output scheme. This requires a large number of contact pads on the chip and output leads in the cryo-package. One of the possible modifications that is currently under development is to replace a parallel output by a serialized data output. This improvement would be an essential step towards realization of a cryo-cooled

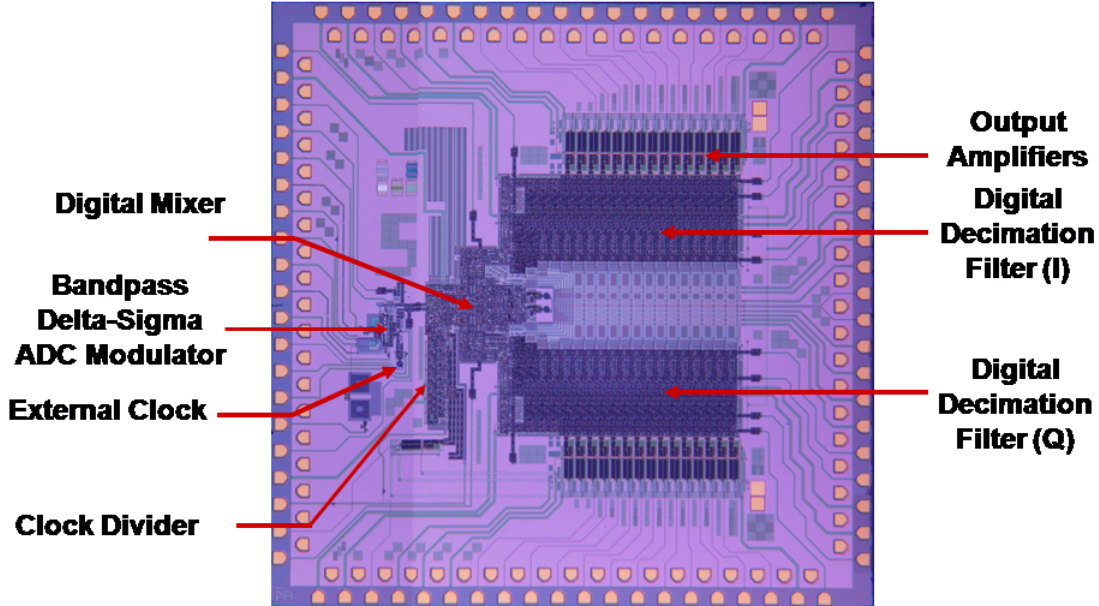


Figure 5.5: Fabricated Band-pass ADR.

multi-channel digital-RF receiver. This approach was validated by designing and testing a LP ADC chip (front-end + one decimation filter) with serialized outputs in liquid helium. The ADC employs two 8-bit parallel-to-serial converters. The chip was found to be operational up to  $34\text{ GHz}$  clock [6]. The second delivered system was based on Band Pass ADR and is designed to work at  $30\text{ GHz}$  frequency. The micro-graph of the chip is presented in figure 5.5. The chip was tested and found to be operational at the design frequency of  $30.72\text{ GHz}$  in liquid helium. Direct reception of X-band satellite communication signal was demonstrated in the field [95].

The digital I/Q-mixer [97] and 4 slices of the digital decimation filter [98] have been used as test vehicles for low and high frequency digital characterization of the new process. An important component of the digital receiver being developed at HYPRES is a digital I/Q mixer for converting narrow-band ( $5\text{ MHz}$ ) signals down from a few- $\text{GHz}$ . To achieve this goal with maximum efficiency a circuit similar in principle to the Gilbert quadrature mixer [99]

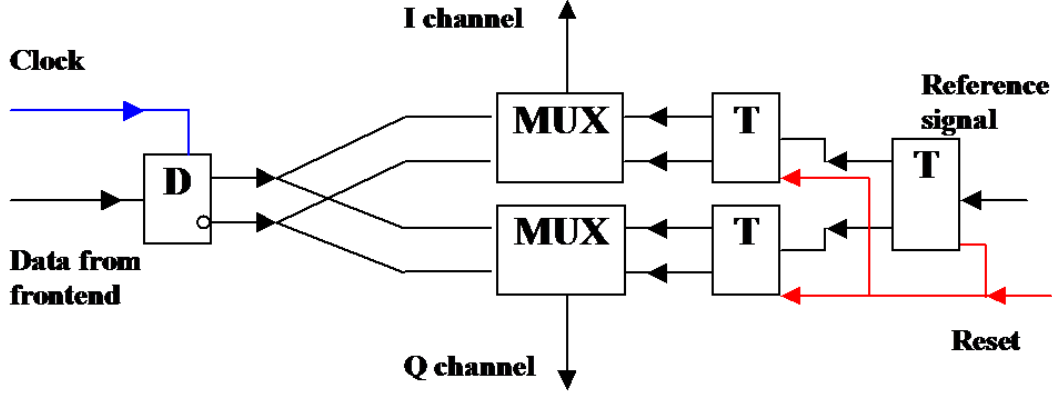


Figure 5.6: Block diagram of a novel I/Q mixer for square wave. Where D is a D-flip-flop, MUX is a multiplexer unit, and T are T flip-flops.

was chosen, shown in figure 5.6. The basic idea of this mixer is to use square waves as a local oscillator signal instead of sine waves. The mathematical representation of square wave is  $G(t) = \text{sign}[\sin(\omega_{LO}t)]$ , where  $\omega_{LO}$  is a local oscillator frequency. The digital version of such a mixer is comparably easy to implement in RSFQ for the case of single-bit coding, e.g. output of a delta-sigma modulator [94].

Figure 5.6 is a block diagram of one of the mixer designs which makes use of single-bit-stream XOR multiplication. It exploits the fact that  $A \otimes 0 = A$  and  $A \otimes 1 = \bar{A}$ . After the modulated signal passes through a D flip-flop with complementary outputs (DFFC) [100], it becomes asynchronous. Multiplexing a direct and inverted data outputs to the proper channel effectively results in digital I/Q signal down-conversion. Multiplexing is done by a binary tree of resettable T flip-flops which create two (I and Q) local oscillator signals with  $90^\circ$  relative phase shift between the I and Q channels (figure 5.7).

In order to determine the initial functionality of the digital I/Q mixer, low speed functionality tests have been performed (figure 5.8). The most critical test conditions occur at the two extreme cases: maximum negative signal, when the modulator output is zero; and the maximum positive signal, when the modulator output is all "ones". In the first case, all input SFQ pulses go to inverted output of the D flip-flop only; in the second case, only to the direct one. In both cases, the I and Q outputs of the mixer produced the correctly ( $90^\circ$ ) phase shifted I and Q outputs. The mixer was operational within  $\pm 20\%$  DC bias margins.

Moreover random modulator input signal as shown in figure 5.9 were used to check the bit error rate test (BERT) of the mixer at low speed. The rate was found to be well below  $10^{-3}$ .



Figure 5.7: Micrograph of streaming I/Q mixer implemented in  $4.5 \text{ kA/cm}^2$ .

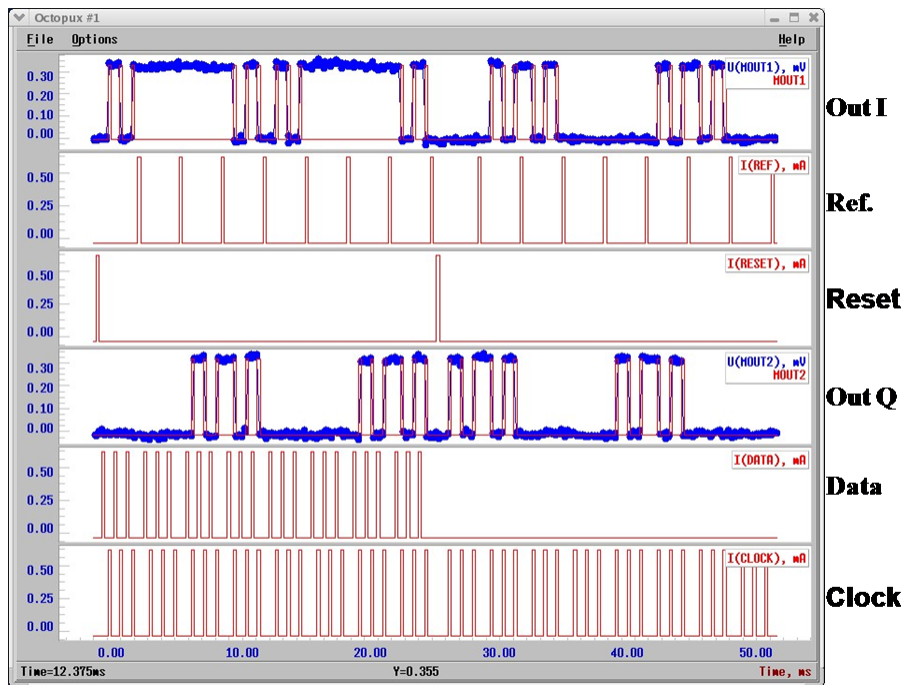


Figure 5.8: Low frequency functionality test for an I/Q mixer with and without Data. Margins of operation was  $\pm 20\%$ .



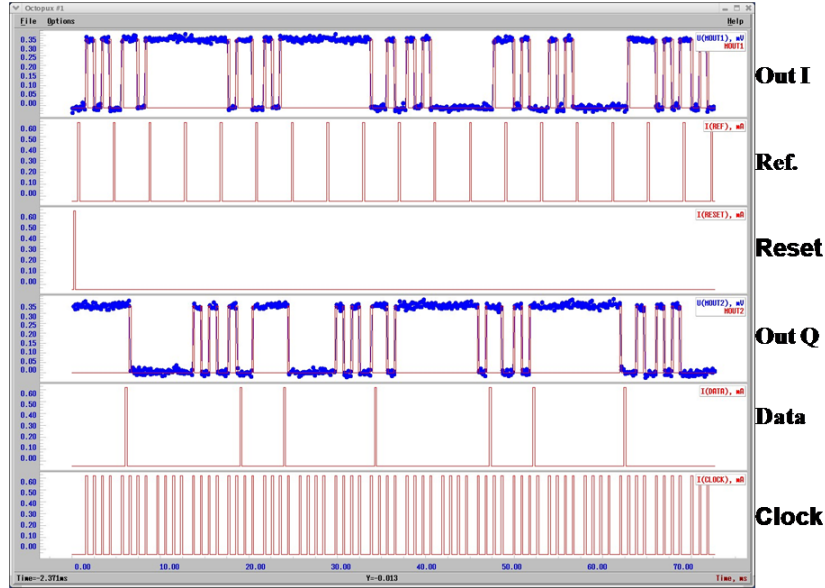


Figure 5.9: Random data was used to check the bit error rate at low frequency, it was confirmed that the rate is well below  $10^{-3}$ .

For high-speed testing of the mixer, high-speed data together with a low-speed reference signal was applied. The I and Q outputs were monitored on the oscilloscope (figures 5.10 a and b). The output is in the form of an eye-diagram for I and Q which are synchronized to the reference signal. First clock signal was applied separately to emulate a trail of zeros from the modulator. The output voltage of I and Q monitors (upper two traces of figure 5.10-a) formed eye diagrams shifted by  $90^\circ$  in accordance with the reference signal monitor (lower trace of figure 5.10-a). The output signals were monitored with toggling SFQ-to-DC converters with a DC voltage swing  $0.4$  mV. Because of this, the absence of output signal leaves a double line on the oscilloscope (0 and  $0.4$  mV), and the high-speed output leaves a single line at average voltage  $0.2$  mV. The clear "eyes" in figure 5.10 indicate very low error rate of the operation at the clock frequency up to  $44$  GHz within 6% DC bias current margins. To verify high-speed operation, when the output from the modulator is not "all-zeros", a signal of  $1/4$  of the clock frequency ( $f_{data} = f_{clk}/4$ ) was applied to the data input of the mixer. To study possible malfunctioning due to simultaneous arrival of Clock and Data SFQ pulses, which is forbidden in RSFQ, beat-frequency test was performed, i.e. a slow phase creep between Data and Clock ( $f_{data} = 0.25f_{clk} + f_{ref}$ ). Now, the output from the modulator is a one to three mix of "ones" and "zeroes". It causes both channels to generate  $HF$

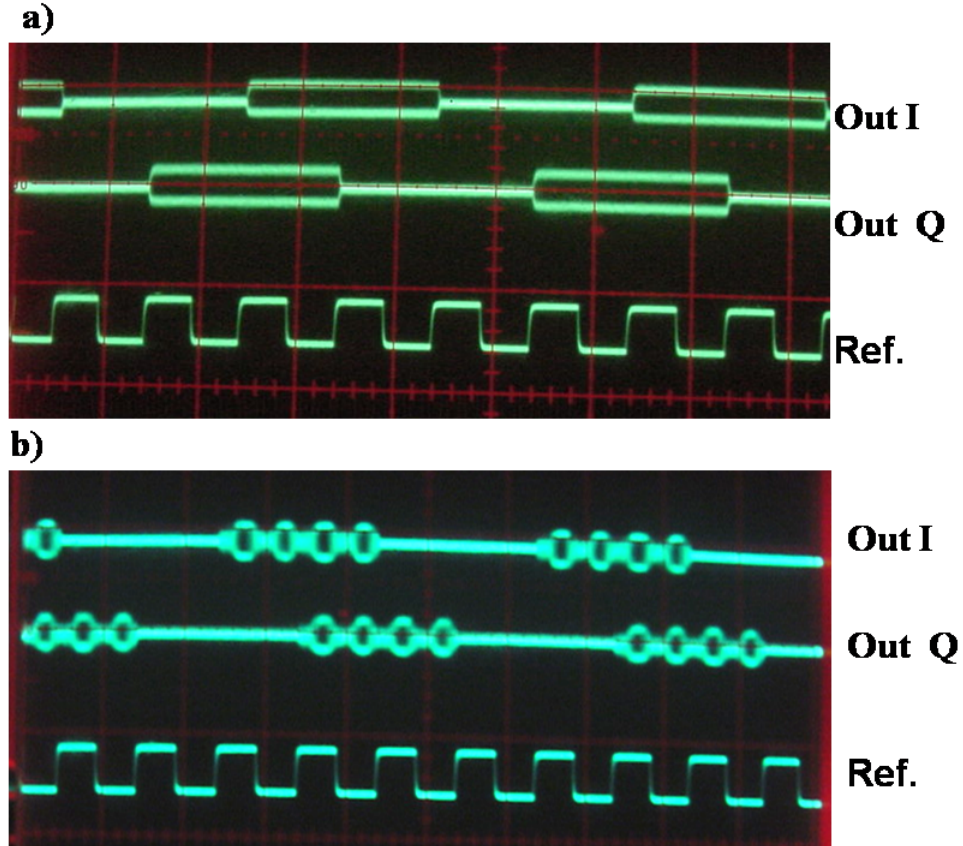


Figure 5.10: a) High speed test of the digital I/Q mixer Clock  $44\text{ GHz}$ , Reference -  $20\text{ kHz}$ , b) High-speed test of the I/Q mixer. Clock  $40\text{ GHz}$ , Data -  $10.00002\text{ GHz}$ , Reference -  $10\text{ GHz}$ .

output, and therefore, there should be no "eyes" on the oscilloscope screen at the proper operation. Increasing the clock signal frequency (and proportionally the data signal frequency), results in a malfunction signaled by the appearance of an eye diagram (figure 5.10-b). It has occurred at the  $40\text{ GHz}$  clock and  $10.00002\text{ GHz}$  data.

The ideal filter for integration with superconductor ADCs is the cascade integrator comb (CIC) filter, introduced by Hogenauer [101] over two decades ago. The simplest CIC filter is in the class of a moving average (or running sum filter) that has a rectangular time-domain impulse response, and therefore, has a sinc ( $\text{sinc}(x)$ ) function frequency response. Such a filter response is ideal for superconductor ADCs as the CIC filter requires no multipliers and is therefore, the fastest. Since the ADCs are sampled at very high speed, the filter must also operate at the same high speed ( $20\text{-}40\text{ GHz}$ ) [102]. Low speed

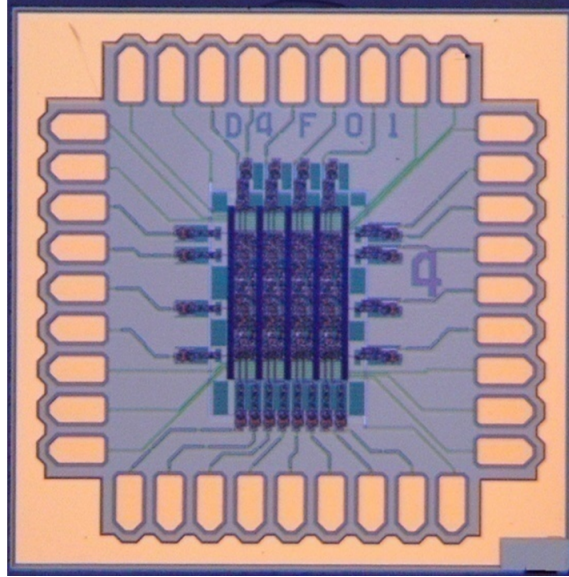


Figure 5.11: Four slices of digital filter for functionality test at low speed.

functionality tests have been performed on Single as well as four slice digital filters in Octopux.

Four slices of digital filter (figure 5.11) has about 600 Josephson junctions and is characterized to greater than  $\pm 25\%$  bias margins. Besides Digital-RF, RSFQ is also a viable alternative to CMOS for high performance computers [103–106] designs [107] demonstration of microprocessor [9], and a crossbar switch scheduler [10].

### 5.3 Next generation of complex digital circuits under fabrication

The next generation of digital circuits under fabrication include components for the transmit side of the digital-RF transceiver, new ADRs, and Multi-Chip Module (MCM) chips. The most notable components of the All Digital Transmitter (ADT) are: the digital interpolation filter, the digital up converter and the Digital to Analog Converter (DAC) [102, 108, 109]. The next generation ADRs are being implemented with new multi-bit higher order modulators and multi-bit channelizers (multi-bit digital  $I/Q$  mixer and higher order multi-bit digital decimation filters). The third order digital decimation filter for example is about three times more complex than second order digital decimation filter with each slice containing 255 JJs being 50% larger and

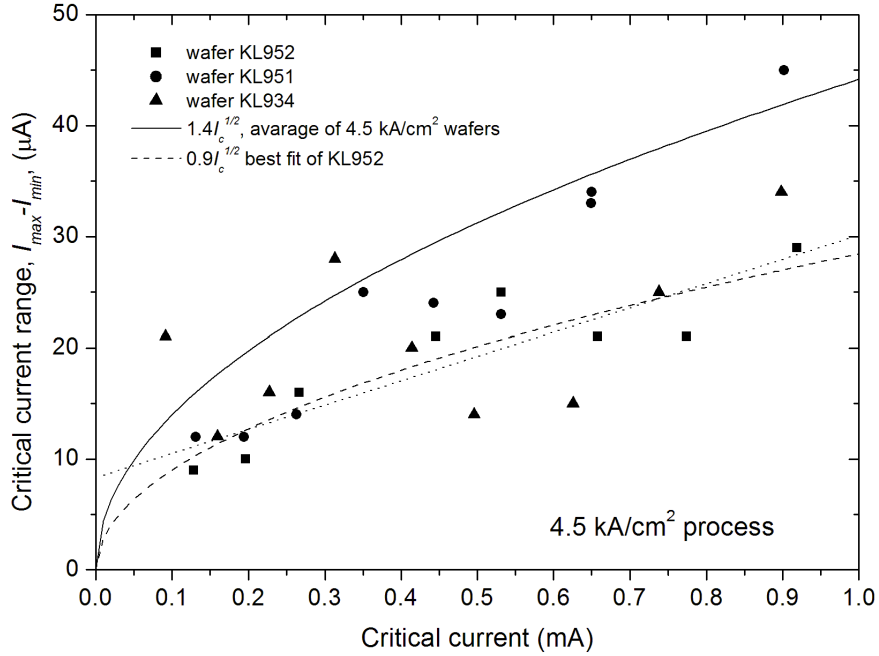


Figure 5.12: The typical range of the critical current spread  $I_{max} - I_{min}$  in 20-JJ arrays of unshunted junctions with  $4.5 \text{ kA/cm}^2$  critical current density. Linear fit (dotted line) and a fit to  $I_{max} - I_{min} = kI_c^{1/2}$  are shown. Some data scattering is most likely caused by flux trapping during the automated measurements.

requiring about 80% more slices[110].

## 5.4 Yield issues

On-chip uniformity of JJ critical currents and defect density are two of the most important parameters for VLSI superconducting circuit fabrication which restrict circuit complexity and yieldable circuits. For all JJ sizes used in the circuits, the  $I_c$  uniformity was measured on 20-junction arrays of unshunted junctions as shown in figure 5.12. Also, a thirty and hundred junction arrays were used to measure the  $I_c$  spreads for two representative values: the smallest  $I_c$  and the most frequent  $I_c$  used in the circuits. The results are summarized in Table 4. The full range of spread (the difference between the largest and the smallest current in the array) was used to estimate the standard deviation  $\delta I$  by assuming a normal distribution.

If we assume that the  $I_c$  spreads are mainly caused by variations of JJ

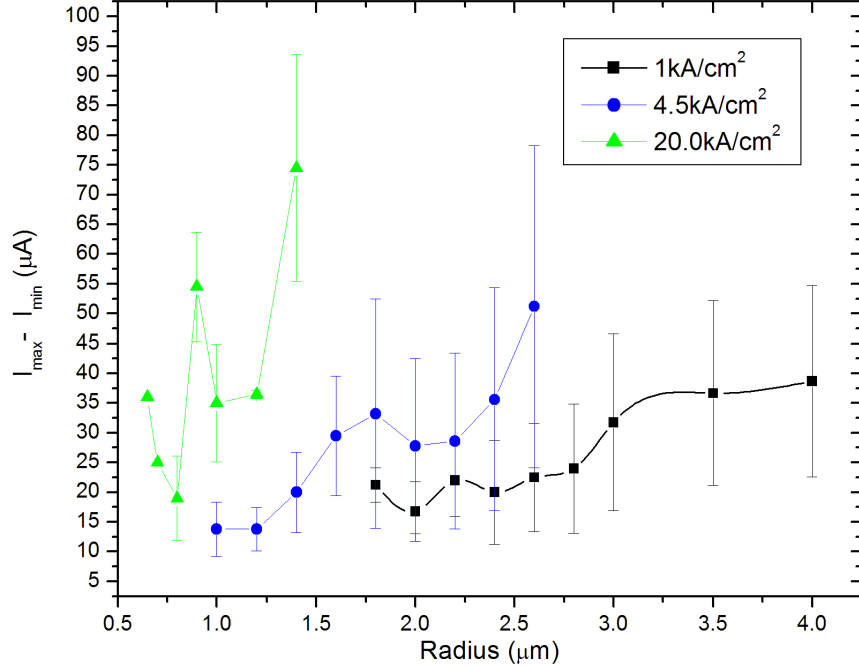


Figure 5.13: Critical current variation as a function of Josephson junction radius for 1.0, 4.5 and 20.0  $kA/cm^2$  processes. No expected scaling with the critical current density was observed.

dimensions induced by lithographic and etching processes, then the range of  $I_c$  variation can be estimated as  $\delta I_c = (2\pi r j_c) \delta r = (4\pi j_c I_c)^{1/2} \delta r$ , where  $\delta r$  is the range of variation of the junction radius. The fit to this  $k I_c^{1/2}$  dependence is shown in figure 5.12 for one of the wafers as well as for the averaged data on 5 wafers. A linear fit,  $a + b I_c$ , is included for a comparison. The smallest  $I_c$  spreads were found in the 4.5  $kA/cm^2$  process, though the  $k I_c^{1/2}$  dependence describes the critical current spreads for other current densities as well. The average coefficient  $k$  was found to be 1.54, 1.40, and 1.92 for 1.0, 4.5 and 20  $kA/cm^2$  processes, respectively. Estimating the range of JJ radius variation  $\delta r$  from the values of  $k$ , we find  $\delta r$  to be from about 0.02 to 0.08  $\mu m$ , that turns out to be close to the accuracy (the beam spot) of our e-beam-written, 1x projection photo-masks.

However, what we find surprising is that  $k$  is almost independent of the  $j_c$ , although, in the model of junction size fluctuation caused by lithography and etching,  $k$  is proportional to  $I_c^{1/2}$ . In order to investigate this issue further, we compared the critical current variations in junctions of the same nominal radius, printed using the same photo-mask but with different current density,

Table 5.2: Typical on chip  $I_C$  uniformity and largest yieldable circuits.

$Process(kA/cm^2)$	1.0	4.5	20
Minimum JJ $I_c$ ( $\mu A$ )	120	120	160
Standard deviation ( $\mu A$ )	4.2	3.8	6.1
Most frequent $I_c$ ( $\mu A$ )	250	250	250
Standard deviation ( $\mu A$ )	6.1	5.5	7.6
Largest yieldable circuit size, $N$	$1.2 \times 10^4$	$2.6 \times 10^4$	$5.7 \times 10^3$

as shown in figure 5.13. For the junctions of a given size, one would expect the current spreads to grow with  $j_c$ . However, for small JJ sizes, the spreads in  $4.5 kA/cm^2$  junctions are less than in  $1.0 kA/cm^2$  junctions. This strongly suggests that the observed variations of  $I_c$  are not related to random variations of the junction sizes but have a different origin. A likely candidate is variations of  $j_c$  rather than the junction size. In this model  $\delta I_c = r^2 \delta j_c$ , that would correspond to term  $bI_c$  in the linear fit in figure 5.12. The measurement equipment noise could be responsible for the constant term  $a$ . The  $j_c$  variations can be caused, e.g., by a charging damage to tunnel barriers induced during plasma processing steps of the wafer fabrication. This damage mechanism should diminish as  $j_c$  increases due to increase in junction normal conductance. So, it is possible that only a part of the observed  $I_c$  spreads is intrinsic. Currently we are undergoing a series of experiments to verify this fact [111]. The cells of HYPRES design library have  $I_c$  margin of  $\pm 20\%$  with respect to a uniform shift of  $I_c$ s of all junctions or a random deviation of any single junction. However, the influence of random variations of  $I_c$ s of many junctions on complex  $I_c$ s is not known. A common belief is that the critical current of any junction should not deviate from the target by more than  $\pm 10\%$ . That is  $USL - LSL = 0.2I_c^i$ , where  $USL$  and  $LSL$  are the upper and lower specification limits, respectively. Statistically, this condition is most difficult to satisfy for the smallest and the most frequently used JJ in the circuit.

Assuming the normal distribution of junction  $I_c$  variation, the average maximum number of junctions in the yieldable circuit,  $N$  can be estimated as  $\min\{(2f_i \times P(z_i, \infty))^{-1}\}$ . Here  $P(z_i, \infty)$  is the far right tail probability of the normal distribution,  $f_i$  is frequency of appearing of the  $i^{th}$  junction,  $z_i = 0.1I_c^i/\sigma_i$ , and  $\sigma_i$  is the standard deviation of critical current  $I_c^i$ . The  $f_i$  for the smallest JJ in the typical HYPRES circuit is 0.02 and for the most frequent JJ is 0.5. Then, using the data in Table 4,  $z_i = 2.86$  and  $3.16$  for  $1.0$  and  $4.5 kA/cm^2$  processes, respectively. The estimate for the maximum yieldable circuit becomes, respectively  $N$  about  $1.2 \times 10^4$  and  $2.6 \times 10^4$ . Considering

only the most frequently used JJ would give  $N$   $4.8 \times 10^4$  for  $1.0 \text{ kA/cm}^2$  and  $7.4 \times 10^4$  for the  $4.5 \text{ kA/cm}^2$  process, seemingly predicting a possibility of making 3 - 4 times more complex circuits. However, it is an overestimation because, for the considered designs, failures in the smallest-size junction have higher probability and hence they determine the size of the yieldable circuit (the circuit complexity). The currently observed good yield of  $1.1 \times 10^4$ -JJ circuits seems to support the validity of these estimates. So we see that the maximum yieldable circuit complexity is determined by deviations of the smallest junctions in the circuits from the target value. This statistical observation is in a good agreement with experimental results on low-speed testing of digital filters where failure of the circuit could be traced to a particular logic cell and ultimately to a particular junction or a small set of junctions [110]. Therefore, further improvements in the lithography are necessary in order to achieve VLSI level of fabrication, especially for the high- $j_c$  processes. If the cost of lithography upgrade is prohibitive, the same result can be achieved by increasing the minimum JJ size and by decreasing the frequency of its appearance. These design solutions may well be a less costly alternative to a hardware upgrade.

## 5.5 Conclusion

In this chapter the focus has been on the digital and mixed signal implementations of the new fabrication process. The first part of the chapter deals with the very simple circuits with less than 100 JJs that test the maximum operating frequency - the static Digital Frequency Divider (DFD) as well as digital functionality test using a 4-bit counter. The DFD has been accepted as the benchmark testing device for maximum operating frequency of a given fabrication process. The maximum operating frequencies for  $1.0 \text{ kA/cm}^2$ ,  $4.5 \text{ kA/cm}^2$  and  $20.0 \text{ kA/cm}^2$  have been  $120 \text{ GHz}$ ,  $230 \text{ GHz}$ ,  $400 \text{ GHz}$  respectively. The second part of the chapter starts with the most complex circuits having more than 10,000 JJs. A low pass phase modulation demodulation all digital receivers (LP PMD ADR) operating at  $24.35 \text{ GHz}$ , a Band Pass ADR operating at  $30 \text{ GHz}$ , serial analog to digital converter (ADC) operating at  $34.0 \text{ GHz}$  constitute some of the successful implementations described. Then two components of the digital RF receiver with more than 500 JJs, i.e., the digital  $I/Q$  mixer and 4-slices of digital decimation filter are discussed in some detail. The two components have been used as digital test vehicles for characterizing all the fabrication runs. Typical results have been the  $I/Q$  mixer operating  $44 \text{ GHz}$  and the low frequency functionality test for bias margins with more than 20%. The third part deals with next generation implementations that are under fab-

rication now. The last part discusses the issue of yield as dictated by the on chip  $I_c$  uniformity. Statistically it has been inferred that maximum yieldable circuit complexity is determined by deviations of  $I_c$  for the smallest junctions in the circuits from the target value and is backed by the latest observation. The issue can be alleviated through lithographic upgrades or by increasing the minimum JJ size and decreasing the frequency of its appearance which could be less costly alternative to an expensive hardware upgrade.



# Chapter 6

## RESULTS AND DISCUSSION

### 6.1 Main results on fabrication process

HYPRES fabrication process is multi-chip, multi-project allowing the implementation of up to 508, 5 x 5 mm chips of different designs with different complexities on a single 150 mm diameter wafer per mask release. Since the beginning of the thesis work there have been 24 mask releases. The complexity (measured by the density of Josephson junctions) of each chip in each mask release has been compiled and representative data from four (M303, M317, M321, M323) wafers is shown in figure 6.1. Comparing the latest wafer releases to those at the beginning of the thesis work we see that there have been at least a threefold increase in number of chips with complexities more than  $90 \text{ JJ}/\text{mm}^2$ , doubling every 16 months. This is driven in part by the success of respective implemented projects, upgrade to the fabrication facility and process upgrades.

In order to produce junctions of high electrical quality, it is important to optimize the argon sputtering gas pressure to produce near zero stress in all thin film depositions [112]. Small junctions of sub micrometer-size are particularly sensitive to film stress [113]; which tends to increase sub-gap leakage current and decrease critical current uniformity [114]. For that matter stress in the deposition systems is constantly monitored and corrected accordingly by adjusting the sputtering gas (argon) pressure in the chamber during sputtering. A typical stress versus pressure measurement for the first superconducting layer (M0) deposition is shown in the figure 6.2. An argon pressure of about 12 mT gives a stress free niobium thin film.

HYPRES uses a projection lithography tool having resolution of  $0.8 \mu\text{m}$  for isolated lines. The process control during the photolithography includes a critical dimension (CD) measurement on  $1 \mu\text{m} - 4 \mu\text{m}$  bars using a 150x

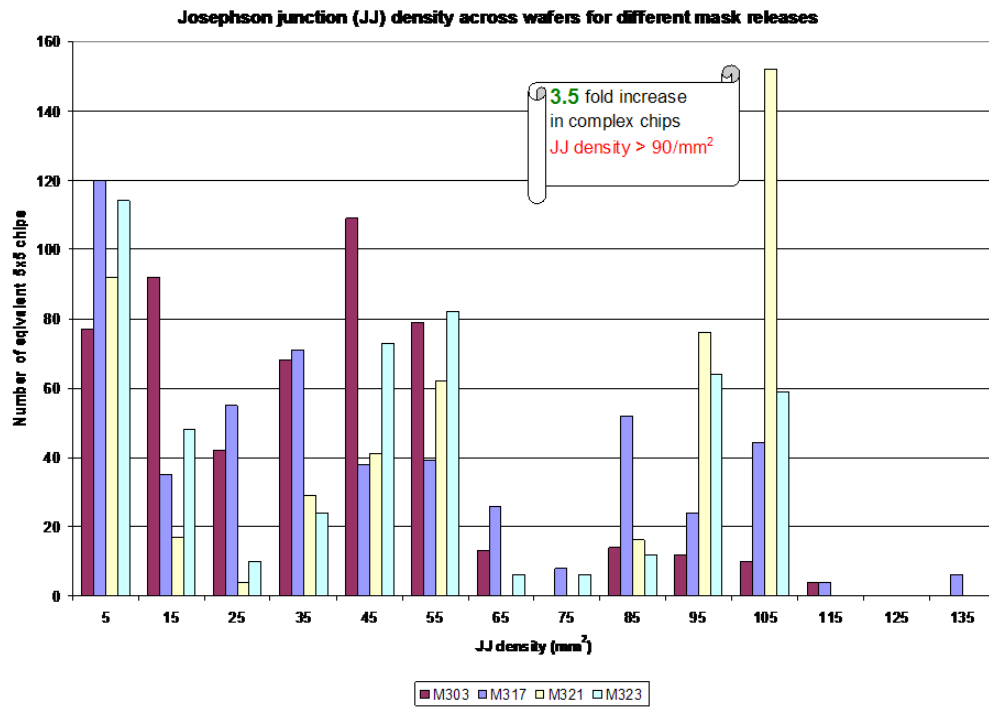


Figure 6.1: There has been a 3.5 fold increase in the number of complex chips with JJ density  $> 90/mm^2$  per mask release since the start of the thesis work, which is the direct result of the fabrication and process upgrades.

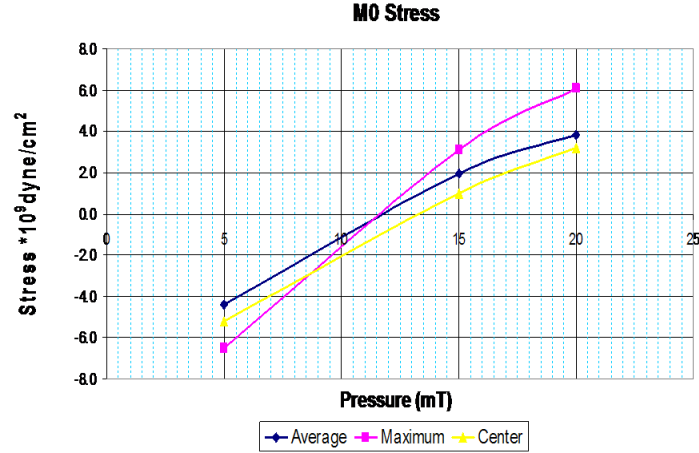


Figure 6.2: Stress due to deposition the first metal layer ( M0 ) measured as a function of chamber pressure, 12 mT pressure gives stress free deposition condition.

objective optical system. The exposure dose is controlled by monitoring lines and spaces of size from  $1 \mu m$  to  $2 \mu m$ . The tool is equipped with an Automatic Fine Alignment (AFA) providing alignment tolerance  $3\sigma \simeq 0.25 \mu m$ . Scanning electron microscopy was also used for controlling the photoresist profile and CD during the process development phase shown in figure 6.3.

The standard requirement for any lithography process is that final line widths should be controlled to within 10% of the nominal feature size and the accuracy of the placement of feature should be within 20 - 25 % of the minimum feature size. However a  $\pm 10\%$  variation in the junction size would translate into  $\pm 20\%$  variation in the junction area and hence, of its critical current. For instance, advanced SCE operating at  $80 GHz$  clock frequency would require a Josephson junction (JJs) with  $20 kA/cm^2$  critical current density and the smallest area of  $0.5 \mu m^2$  corresponding to a circular junction of  $800 nm$  in diameter [1]. This critical dimension (CD) must be controlled within  $\pm 40 nm$  in order to have JJ critical current uniformity with  $\pm 10\%$  that is believed to be sufficient for yielding superconductor integrated circuits (SCIs) with about  $10^4$  JJs. In order to improve the resolution and the junction area definition accuracy, a resolution enhancement technique (RET) on double (cross) exposure has been developed and implemented. During etching an emission optical spectrometer is used for etch end-point detection for all wiring layers (fig-

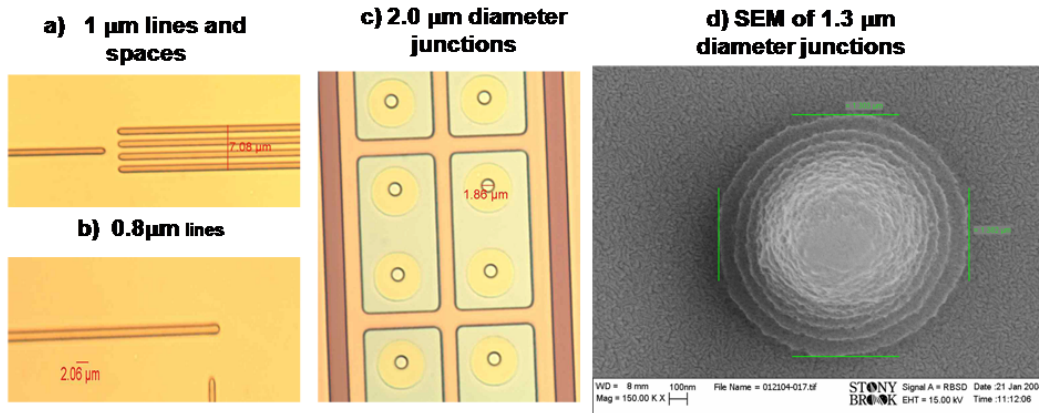


Figure 6.3: Optical and SEM micrographs of features used to characterize the projection lithography resolution limitations which were found to be  $1 \mu m$  for dense lines and spaces,  $0.8 \mu m$  for single lines  $1.3 \mu m$  for isolated circular features.

Table 6.1: Reactive ion etch rates for metal layers.

Metal layer	Etch time (min)	Thickness (Å)	Rate (Å/min)
M0	1.87	1035	554.5
M1	4.39	1186	270.3
M2	4.83	2964	614.1
M3	8.01	5964	744.9
I1A	4.02	515	227.3
R2	2.01	577	287.5

\*Data is an average RIE etch done on 275 runs since August 2004.

ure 6.4), resistors as well as contact hole etching. Since the anodization layer around the junction is only 560 nm thick, precise end-point detection is needed to minimize damage and formation of shorts. To ensure complete opening of contact holes, extra process control is done using profilometer for step height measurement on test structures spread throughout the wafer.

For niobium etch the most common used plasma is  $SF_6$  plasma. The etch rate for different metal layers is summarized in the table 6.1 for 20 sccm  $SF_6$  flow rate and 2 Pascal chamber pressure with an RF power of 40 watts. M0, M2 and M3 niobium metal layers are deposited by magnetron sputtering in the same machine. The etch rates (figure 6.5) for M0 and M2 is recalculated to be equal to  $652 \text{ \AA}/min$  after subtracting about 17 sec from the etch time (the time it takes for the plasma to set in and start etching at full rate) the

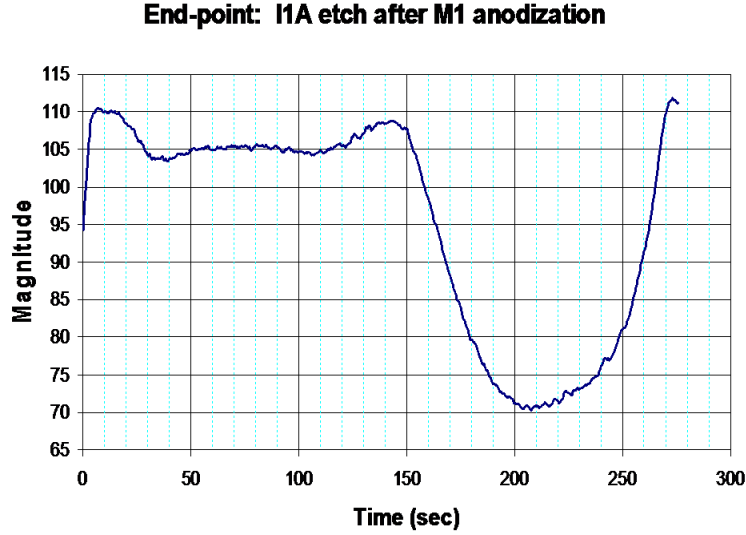


Figure 6.4: Typical End-point detection trace, the magnitude (Y-axis) is normalized fluorine line intensity.

assumption here is that the same grain size and roughness for M0 and M2 thin films.

The  $SiO_2$  dielectric is etched in  $CHF_3$  and  $O_2$  plasma, 8 sccm of  $O_2$  and 45 sccm of  $CHF_3$  is flown in to the chamber held at a pressure of 13.33 Pa. Etching is done at 150 W RF power and the temperature on the back of the wafer is kept constant by a chiller set to about  $11^\circ C$ . Etch rate for the etch chemistry described above is summarized figure 6.6.

Ion beam milling has been used to remove about  $500 \text{ \AA}$  of  $AlO_x/Nb_2O_5$  bilayer after anodization. At pressure of  $2 \times 10^{-4}$  T, Argon gas flow rate of 16 sccm and beam voltage of 500 V with 200 mA beam current the milling rate and uniformity for an M1 mill is  $72 \text{ \AA}/min$  with  $\pm 8 \%$  uniformity. Milling is stopped right after clearing of the  $AlO_x$  barrier (500- 650  $\text{ \AA}$  of M1 material is milled)[84].

## 6.2 Main results on process monitor control

Monitoring  $j_c$  in five locations on the wafer has allowed us to reveal the existence of a reproducible none-uniformity of  $j_c$  over the wafers. Most notably, the  $j_c$  in the middle of the third quadrant (-x,-y) is significantly (up to 50%) larger than in other locations on the wafer. The possible causes of this effect are currently under investigation. If this "hot spot" is excluded from the

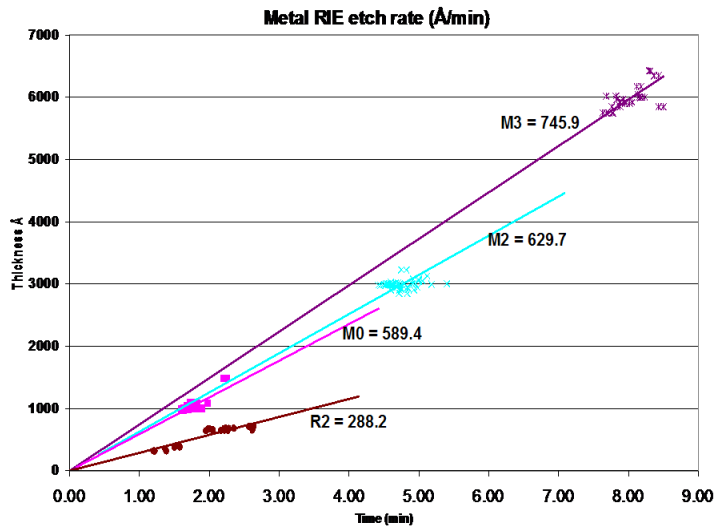


Figure 6.5: Measured thickness versus RIE etch duration for metal layers (Nb) as well as the resistor material (Mo).

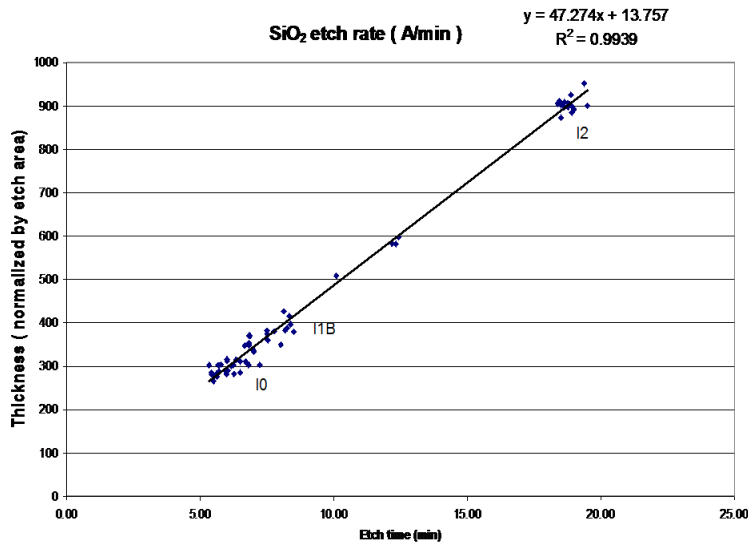


Figure 6.6: Interlayer dielectric etch rate: etched thickness normalized by etch area as a function of time. The linear fit shows the time it takes for the plasma to set in to be 17.5 sec and the etch rate per unit area of  $47.3 \text{ \AA}/\text{min}$ .

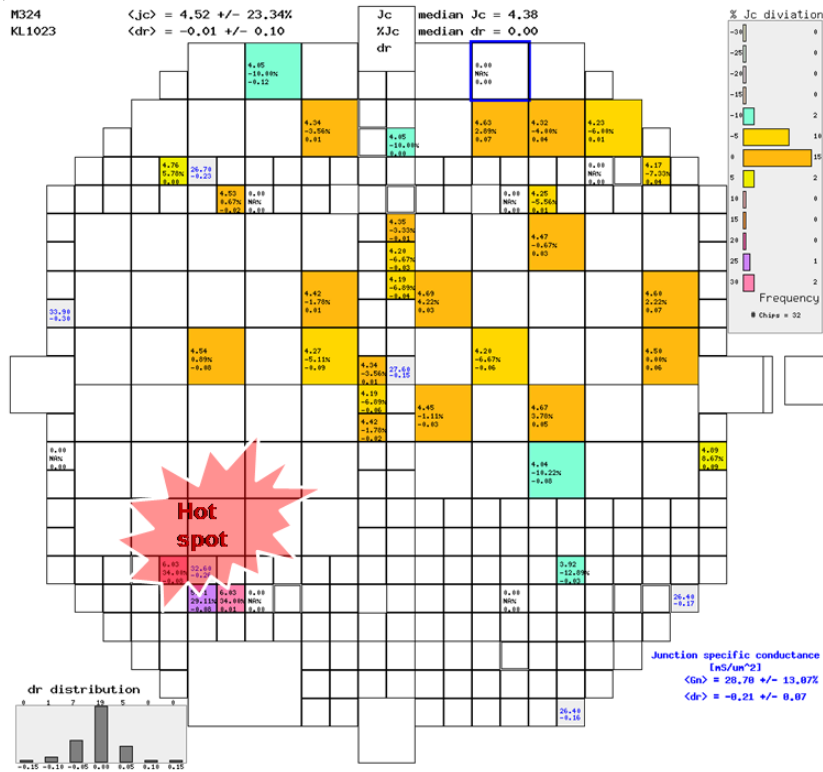


Figure 6.7: Across wafer  $j_c$  and  $dr$  distribution for KL1023. From the 32 chips that have been characterized 4 of them lie on the hot-spot of the wafer with  $j_c$  s on average  $> 25\%$  higher than the rest. The wafer layout template has been used to depict  $j_c$ , its % deviation from nominal value and  $dr$  in each box correspond to the respective chip.

analysis, the  $j_c$  variation over the rest of the wafer is within  $\pm 10\%$  (figure 6.7).

The trend chart in figure 6.8 shows the  $j_c$  in different locations on the wafers since the  $4.5 \text{ kA/cm}^2$  process monitoring has been started. Without the (-,-) region, the average  $j_c$  over all wafers produced in 2006 is  $\langle j_c \rangle = 4.85 \text{ kA/cm}^2$  with standard deviation  $\sigma = 0.736 \text{ kA/cm}^2$ . The design margin on  $j_c$  for HYPRES circuits is  $\pm 20\%$ . That is the  $USL - LSL = 0.4j_c$ . For the  $4.5 \text{ kA/cm}^2$  process, the capability index  $C_p = (USL - LSL)/6\sigma = 0.41$  is less than 1, indicating that the process is still very immature from the point of view of statistical process control (SPC). However, if only a central part of the wafer or (+,+) quadrant is considered, the capability index becomes acceptable,  $C_p = 1 - 1.2$ . It indicates that the main problem that needs to be addressed is non-uniformity of the critical current across 150-mm wafers rather than run-to-run reproducibility. One can see from above that the mean,  $\langle j_c \rangle$  is higher than

Table 6.2: Average etch rates for the three dielectric layers.

Layer	Etch time (min)	thickness(Å)	% Area	Adjusted rate(Å/min)
I0	6.9	1590.2	12.5	301
I1B	7.5	2176.3	16.9	302
I2	18.0	5317.8	17.1	300

\* calculated from about 250 etch runs since August 2004. The rate is adjusted by using the % of area covered.

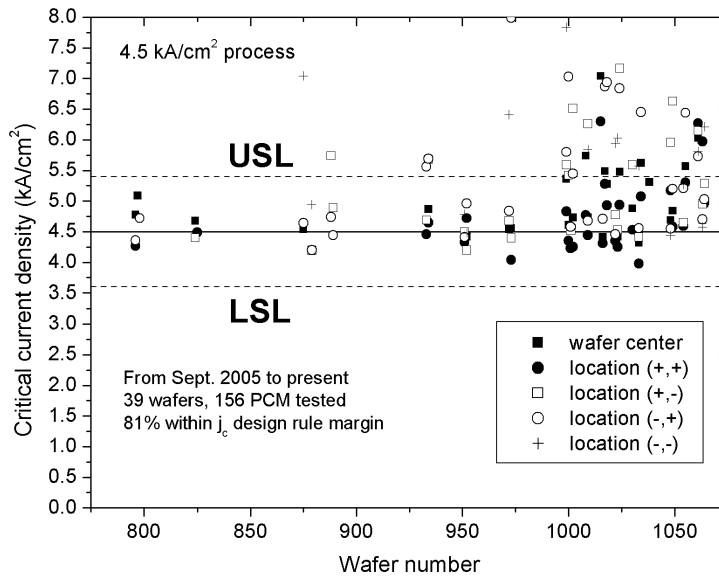


Figure 6.8: Average critical current density extracted from arrays of shunted and unshunted JJs in five locations across  $4.5 \text{ kA/cm}^2$  wafers. The data on shunted and unshunted arrays agree within  $\pm 5\%$ . The target  $j_c$  is shown by a solid line, and dashed lines show the upper and lower specification limits.



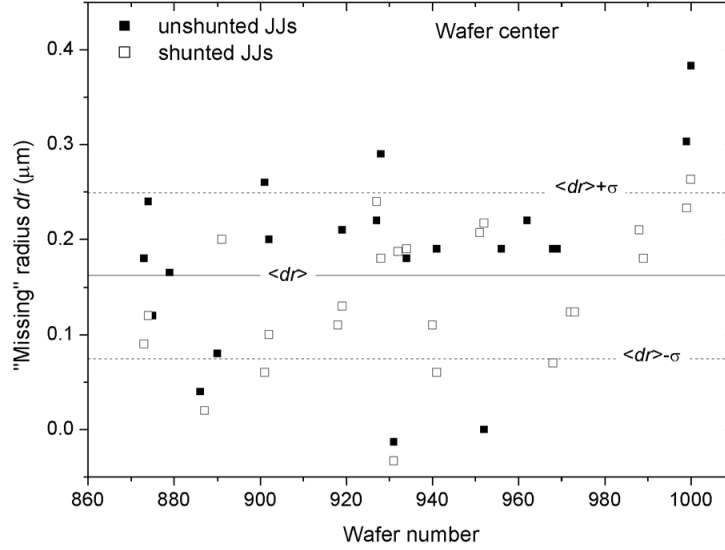


Figure 6.9: Run-to-run variation of the Josephson junction size bias ("missing" radius) in the center of wafers produced since Sept. 2005 (data on 1.0, 4.5 and 20  $kA/cm^2$  current density processes included). Mean  $\langle dr \rangle = 0.16 \mu\text{m}$ ,  $\sigma = 87 \text{ nm}$ .

the target value for the  $4.5 kA/cm^2$  process. From the point of view of SPC, this indicates an incorrectly centered process. However, a decision was made to introduce no corrective measures (e.g., do not change tri-layer oxidation parameters) and keep the  $\langle j_c \rangle$  a bit higher than the target. An annealing at  $215^\circ\text{C}$  in inert atmosphere was used to reduce the critical current density on chips of interest. This allowed us to study the operation of the very same SICs at different critical current densities in order to accumulate statistical data on margins of operation of different SICs. With this additional tool of  $j_c$  adjustment, practically any chip on the wafers could be brought to the proper  $j_c$  that made it operational.

Figure 6.9 shows the run-to-run variation of the "missing" radius  $dr$  in the center of the wafers. It is interesting to note that there is a small statistical difference between the  $dr$  values extracted from arrays of shunted JJs and unshunted JJs. This difference could have been expected because the critical current of small unshunted junctions could be more suppressed by noise that effectively would look like "missing" junction area. The mean "missing" radius  $\langle dr \rangle$  was found to be  $0.16 \mu\text{m}$  with standard deviation of  $\sigma = 87 \text{ nm}$ . The run-to-run  $dr$  distribution was found to be very close to the normal distribution, with skewness  $a_3 = -1.5 \times 10^{-3}$  and kurtosis  $a_4 = 3.03$  (for purely

normal distribution they are 0 and 3, respectively). In the past, compensation for  $dr$  was done in the individual designs. Since March of 2006, a uniform compensation has been applied to the photo-masks. Although the cells of HYPRES design library have  $I_c$  margin of  $\pm 20\%$ , the influence of a systematic shift of critical currents of all junctions in complex ICs is not exactly known. A deviation of  $dr$  from the target causes a systematic, nonlinear shift of all critical currents in the circuit  $dI_c^i = \sqrt{(4\pi j_c I_c^i)} \times dr$ . A common belief is that the critical current of any single junction should not deviate from the target by more than  $\pm 20\%$ . A  $\pm 20\%$  margin of  $I_c$  requires  $dr/r$  to be within  $\pm 10\%$ , that is  $dr$  variation of less than  $\pm 178$ ,  $\pm 84$ , and  $\pm 50$  nm for the smallest JJs in 1.0, 4.5 and 20  $kA/cm^2$  processes, respectively. With the junction size standard deviation of 87 nm determined for our process above, these  $dr$  margins correspond to  $\pm 2\sigma$ ,  $\pm 1\sigma$ , and  $\pm 0.57\sigma$ , respectively. Even well centered on the mean, the current lithography process may likely produce, respectively, 1 out of 22, 1 out of 3, and 2 out of 3 wafers out of specs on  $dr$  for 1.0, 4.5 and 20  $kA/cm^2$  runs, respectively.

### 6.3 Main results on digital and mixed signal applications

The maximum TFF divider frequency,  $f_{max}$  has become the benchmark characteristic of SICs fabrication processes. A summary of the obtained and published data for various Nb-based processes is shown in figure 6.10. All the available data fall onto the  $f_p$  vs  $j_c$  dependence Eq. 29. Interestingly, in order to achieve the ultimate performance, TFFs in [3] were optimized for  $\beta_c$  values higher than 1 (up to 2.5) whereas no such optimization was done in this work and [2]. It is clear from figure 6.10 that this optimization does not offer any real speed improvement.

It is also clear from figure 6.10 that increasing the process current density above 60 - 70  $kA/cm^2$  does not offer any advantages in the circuit speed even though the junctions eventually become self-shunted and no external shunts are required. Here, the  $I_c R_s$  product is limited by the Ambegaokar-Baratoff (AB) relationship  $I_c R_n = \pi\Delta/2e$  (2.1 - 2.2 mV for Nb) and, most often, for Nb/ $AlO_x$ /Nb junctions does not exceed 1.5 - 1.6 mV at 4.2 K due to strong coupling and proximity effect corrections. This translates into 725 - 775 GHz maximum frequency for Nb technology. Worth noting is that the  $f_{max}$  of TFFs in [4, 5] is higher than the gap frequency  $f_{2\Delta} = 2\Delta/h$  ( $\Delta$  is the energy gap) in Nb above which strong dissipation in the junction electrodes and Nb wiring is expected to set in due to pair breaking by Josephson oscillations. In this

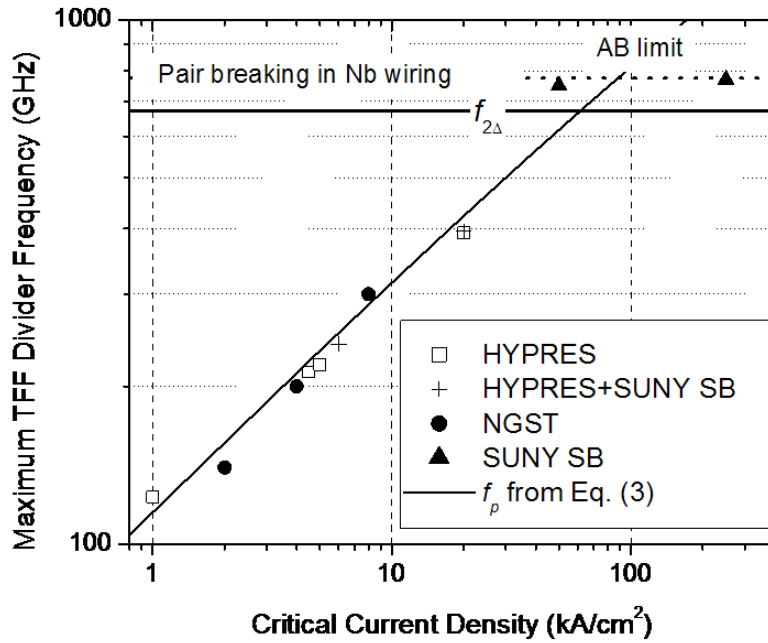


Figure 6.10: Maximum frequency of operation of TFF-based frequency dividers fabricated in various Nb-based processes. HYPRES data are from the [1, 2]; HYPRES+SUNY SB data are from [2]; NGST data are from [3]; SUNY SB data are from [4, 5]. Above the gap frequency of Nb ( 670 GHz) strong attenuation of SFQ pulses in Nb wiring and JJ electrodes should set in. The JJ plasma frequency  $f_p$  equation 2.29 is shown as a solid curve, AB limit as a dotted line.

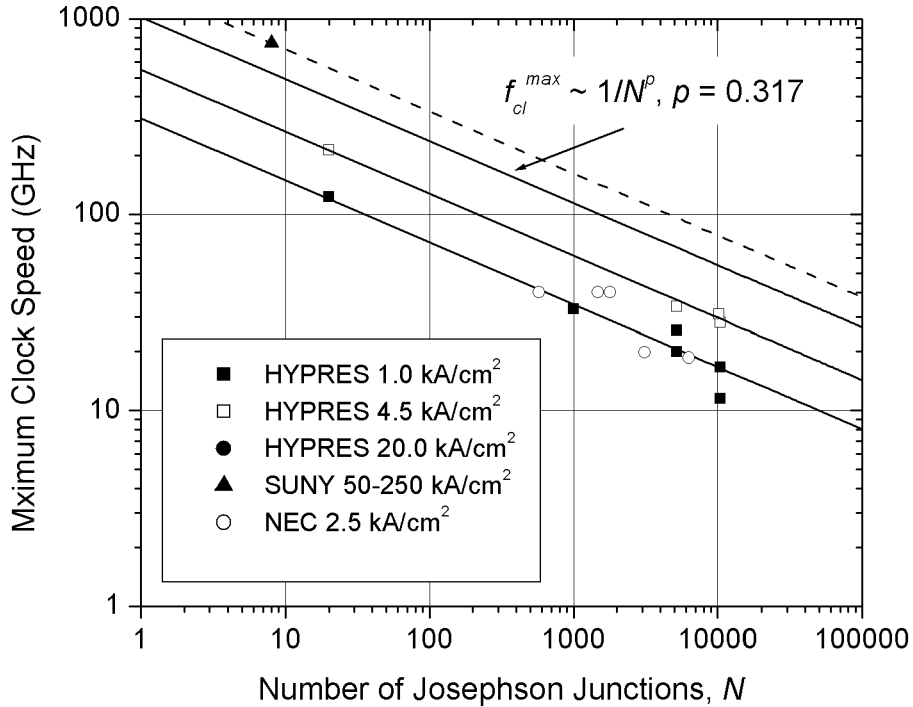


Figure 6.11: Dependencies of the maximum clock speed of RSFQ digital circuits on the number of Josephson junctions for the existing and projected Nb fabrication processes. The experimental data are from [4, 5] and [6–8]. The data for NEC process are from [9], [10–13]. Solid lines show the best fit to the data on 1 and 4.5 kA/cm<sup>2</sup> processes, and projections for the 20 and a hypothetical 250 kA/cm<sup>2</sup> (dash line) processes.

case the SFQ pulses should strongly attenuate if the distance between JJs in JTLs and logic cells is larger than the decay length. It is possible that double-SQUID TFFs in [4, 5] operated above  $f_{2\Delta}$  in some phase-locked mode that was achieved by using many bias sources, and also due to the Riedel’s peak in the intensity of Josephson oscillations at  $2\Delta$ . It is interesting to see how the maximum frequency of operation (maximum clock speed  $f_{cl}^{max}$ ) scales with circuit complexity (level of integration). It is shown in figure 6.11. Unfortunately, experimental data are very scarce, especially for circuits with  $> 10^4$  JJs. This limits the accuracy of the analysis.

Though circuit dependent, the general tendency is that the  $f_{cl}^{max}$  decreases strongly with the circuit complexity that we characterized by the number of

JJs,  $N$ . We find that, however limited, the data can be described by the power law decay  $f_{cl}^{max} \sim 1/N_p^p$  with  $p = 0.317$  for both the 1.0 and 4.5  $kA/cm^2$  processes. By assuming that this dependence holds for other  $j_{cs}$  as well, we draw the projected speed dependencies for the 20  $kA/cm^2$  and for future 50 - 250  $kA/cm^2$  processes. For a hypothetical circuit with  $10^5$  JJs that is, perhaps, the scale relevant most to Digital Signal Processing (DSP) and computing applications, the projected clock frequencies are 8  $GHz$ , 15  $GHz$ , and 27  $GHz$  for 1.0, 4.5, and 20  $kA/cm^2$  processes, respectively. For a hypothetical, yet to be developed, 250  $kA/cm^2$  processes, the same scaling gives 38  $GHz$  maximum clock frequency. It is a factor of 3 less than the best expectations in the field of superconducting electronics, but still a factor of 10 better than the existing Si chips. Note, that for a hypothetical  $5 \times 10^7$  JJs circuit comparable to the current Si-based processor chips, the maximum projected frequency is only 5  $GHz$ , that is about the same as for the most advanced Si technology existing already today. From the design point of view, it is not clear exactly why the circuit speed should significantly drop with the level of integration because, usually, only a small fraction of the circuit works at the highest frequency. From the data/clock timing consideration this highest frequency is  $f_c/7 \simeq f_p/7$ . Therefore, the data in figure 6.11 could be possibly explained by accumulation of timing errors due to jitter and random delays caused by variations of the circuit parameters as the circuit complexity grows. Computer simulations of some of these effects were presented in [115]. It may well be that more advanced chip architectures will be required in the future to address this performance vs. complexity issue. Also, for a complex circuit to operate, margins of operation of the individual logic cells comprising the circuit should overlap. Since the margins of operation of all individual cells shrink with frequency and because of random variation of the parameters, the probability of finding this common overlap diminishes as the circuit complexity grows. Therefore, the observed decrease of the maximum clock speed with the number of JJs could well be the issue of fabrication yield and random fluctuations of the circuit parameters. It remains to be seen to what extent these problems could be eliminated by further improving the fabrication processes.

# Chapter 7

## CONCLUSIONS

A new process for digital superconductor electronics has been successfully developed. The process has been implemented at a commercial fabrication facility in Hypres Inc. At the present time, the process has been implemented for a  $4.5 \text{ kA/cm}^2$  critical current density and is accepted as the standard fabrication process in HYPRES Inc. The complexity of chips thus far realized is about 12000 JJs operating at  $30 \text{ GHz}$ . The minimum JJ size and, hence, the maximum operating frequency of the digital circuits in the technology that was available at the beginning of the thesis work are limited by the diffraction effects in the optical lithography system and by the poor choice of the JJ shape (square). The maximum integration level of superconducting digital circuits in the HYPRES "old process" was limited by random structural defects, micro-shorts between the superconducting layers, and poor control over the line-width of superconducting strips forming circuit inductances. The last two were found to be a result of a particular choice of the layer process sequence and a reaction between Al layer, a part of  $\text{Nb/Al/AlO}_x/\text{Nb}$  tri-layer, and processing chemicals. An enhanced optical lithography process for JJ definition has been developed that uses a shorter wavelength for optical lithography and circular-shaped junctions in order to minimize diffraction-induced distortions of the junction shape and area. Electric and SEM characterization of JJ has been made. The minimum JJ size was reduced from about  $3.5 \mu\text{m}$  to  $1.2 \mu\text{m}$  for circular junctions and to  $0.8 \sigma\text{m}$  for the RET-defined junctions. A  $1\sigma$  spread of the critical currents of Josephson junctions of 1.2 % has been achieved in arrays of 100 Josephson junctions; and 2.4 % spread across  $5 \times 5 \text{ mm}$  chip. An advanced fabrication process with  $4.5 \text{ kA/cm}^2$  critical current density has been developed. The process is based on the advanced lithography process and incorporates an additional anodization step for JJ protection. A simple approach for scaling the existing circuit designs to newer higher  $j_c$  processes has been proposed and implemented. It allows for fast and low cost improve-

ments in the circuit speed. Fabrication process control and monitoring has been developed and implemented to control the Josephson junction quality and uniformity across 150-mm wafers as well as resistors, inductors, and other circuit parameters. A set of diagnostic chips has been developed for monitoring HYPRES superconducting IC fabrication process and extracting all the design parameters. It was found that the most reproducible and easiest to control parameters are inductances and resistors. The most difficult to control is the run-to-run variation of the Josephson junction size and variations across the 150-mm-wafer uniformity of the critical current limiting the complexity level of circuits. The observed on-chip  $I_c$  spreads cannot be explained by random variation of JJ sizes caused by lithography and etch processes. The  $I_c$  uniformity of the smallest junction in the circuits determines the size of the largest yieldable circuits. Deviations of  $I_c$  of the smallest junction from the target are the main source of circuits' failures. Although the existing 1.0 and 4.5  $kA/cm^2$  processes are capable of yielding circuits with 20k junctions, a significant upgrade of lithography is required for the 20  $kA/cm^2$  critical current density process currently under development. The 20  $kA/cm^2$  critical current density process has been demonstrated on circuits with less than hundred junctions, such as benchmark test circuit that operated to a maximum frequency of 400  $GHz$ . A resolution enhancement technique (RET) was developed for defining square and rectangular junctions. The RET is based on the double-exposure of mutually orthogonal lines. A number of complex digital circuits with greater than  $10^4$  JJ operating at clock frequencies in excess of 30  $GHz$  has been fabricated for the first time as well as less complex about 500 JJs circuits operating above 40  $GHz$  and simple circuits with about 20 JJs operating at around 400  $GHz$ . As the result of the thesis work, both the maximum operating frequency of superconducting integrated circuits and their complexity has been doubled with respect to the previous state-of-the-art. Realization of the full 80  $GHz$  speed potential in complex superconducting digital integrated circuits with more than  $10^4$  Josephson junctions may require more advanced design architectures and further process innovations.

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