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Instrumentation and Process Development for Resistive Memory Devices

A Thesis Presented
by

Esteban Monge

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Work was performed at the Stony Brook University's IC fabrication laboratory for superconducting and nano-scale devices, in the Physics and Astronomy Department. Since this fabrication laboratory is setup primarily for Nb/AlOx/Nb based devices for superconducting electronics, the MSI project focused on adapting the existing fabrication facilities to develop a commercial CMOS compatible fabrication process to produce a prototype hybrid semiconductor CMOS/nanoelectronic circuit. The research concentrated primarily on a new type of metal oxide based devices. Tasks involved refurbishing, upgrading and modifying existing thin-film processing equipment and developing fabrication processes compatible with the new materials required for the resistive memory devices.

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Acknowledgements

There are numerous people I need to thank, who played central roles in the achievement of this work. First I want to thank my wife and my kids who have been a marvelous source of support during my years at Stony Brook. To my advisor, Research Professor Vijay Patel, for his excellent advice and guidance through the project. The director of the Low Temperature Solid State group under which this project took place, Professor James Lukens, whose weekly group meetings were sources of great insight. There were fellow students in the group who provided assistance during the last couple years. Shih-Sheng Chang was a great lab partner. Pete Davis assisted with his technical advice. Mark Jablonski from the student machine shop provided much help with his mastery in the shop, as well as Walter Schmeling, manager of the Physics Department Machine Shop and all the guys who work there. Thanks are also in place to Zhongkui Tan for his collaboration with the experimental results from the fabricated devices.

Introduction

The work described in this volume arises from an Air Force Office of Scientific Research (AFOSR) funded project aimed to develop a prototype hybrid semiconductor-nano electronic device (CMOL) using metal oxide resistive memories. The interest in this technology comes from the rapid advance towards saturation in its dimensions of semiconductor digital integrated circuits following the exponential "Moore's Law" [1]. These devices are to be part a nano crossbar structure that is to be gown at the top of available commercial foundry CMOS chips as an add-on in its surface. Prof. Konstantin Likharev created the CMOL concept and the project has advanced under his supervision as well as that of Prof. James Lukens. My work was supervised by Research Prof. Vijay Patel who is in charge of the fabrication facilities. At this point there has been great improvement in the development of the devices and the project is moving into its second stage, which involves the removal of the passivation layer on top of the CMOS chips, a process never attempted before for single chips. One approach that is being considered is the Chemical-Mechanical Polishing (CMP) of the surface of the CMOS chip; were the nano crossbars containing the devices are meant to be grown. Another approach is to perform a reactive ion etch of the passivation layer consisting of quartz and a nitride. The CMOL idea is elegantly visualized in the following figure from a Prof. Likharev's publication [1].

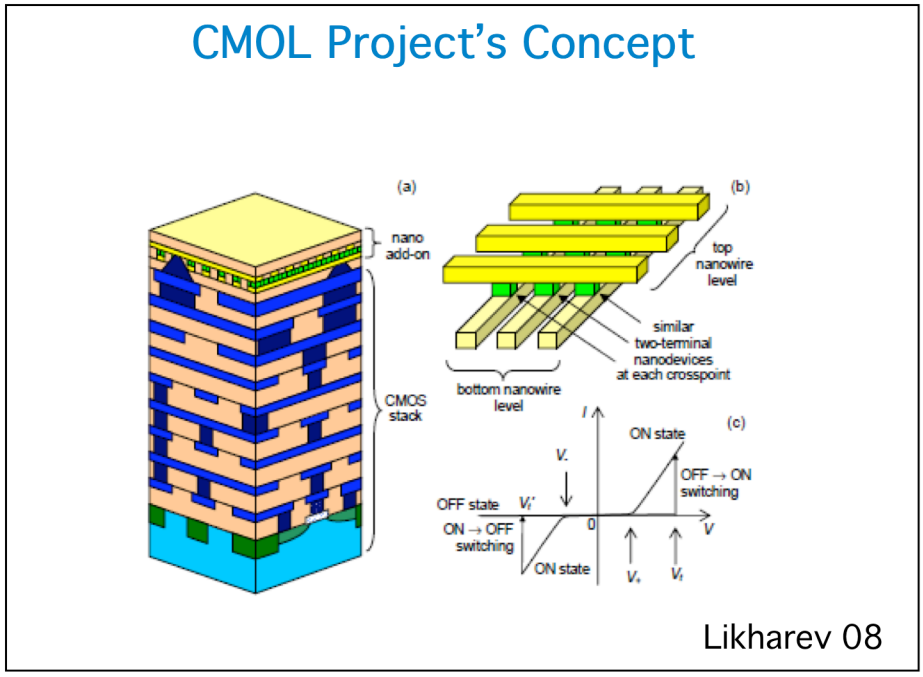


Figure1. (a) The general idea of a hybrid CMOS/nanoelectronic circuit, (b) the nanowire-crossbar add-on, and (c) the required I–V curves of the two terminal cross point devices (schematically).

The nano crossbar structure allows for very high integration density of devices and is easy to fabricate with the existing equipment in our fabrication facility. The devices used in this structure can be of different nature, including molecular devices, metal oxide based devices or amorphous silicon devices. The requirement for this add-on to be used as memory is that the devices present the very characteristic switching behavior presented in the schematic I-V curve in figure1. The next figure shows the commercial CMOS chip designed for this project.

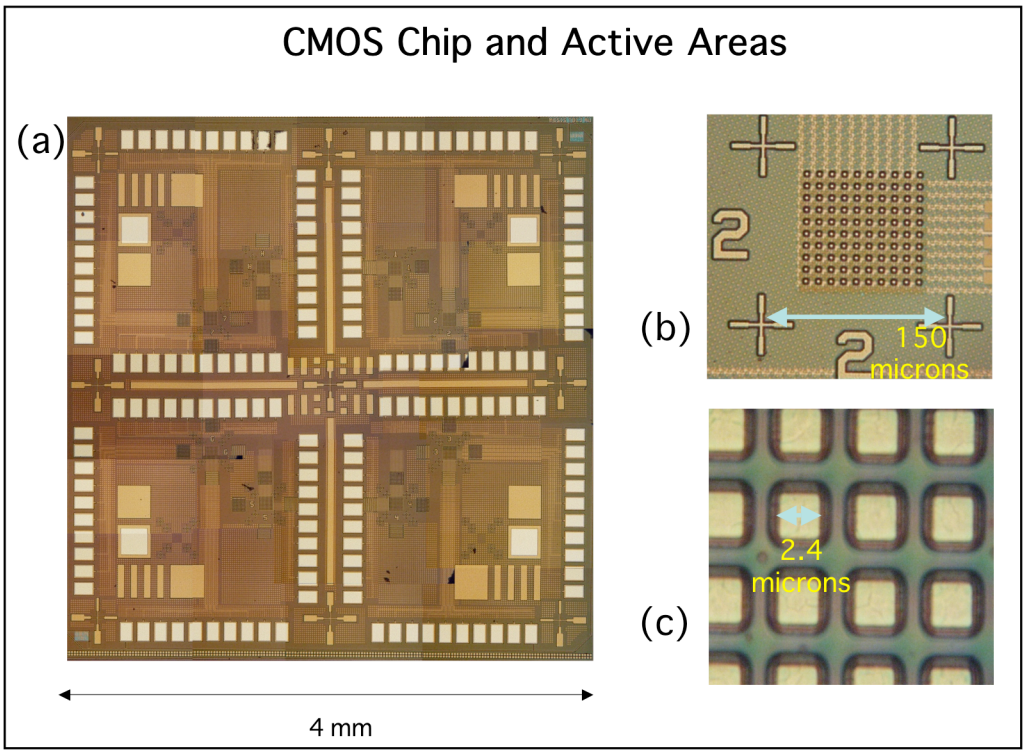


Figure 2. (a) Commercial CMOS chip designed for the CMOL project. The chip has four sections, with two active areas per section. (b) shows the active area contact pins, were the nano crossbar is to be grown. (c) close up of the contact pins.

The CMOS chip was fabricated by IBM through MOSIS, which is a commercial foundry. These chips were designed specifically for this project. The chip has four sections with two active contact areas per section. On the right we see detail of the active area where the nano cross bar would be grown. The active areas are a 10 x10 contact grid where each of the nano wires contacts one point, with 50 connections for the top bars and 50 connections for the bottom bars. At the bottom we see a close up of each connection. Each contact point is connected to the drain of a transistor in the CMOS chip, and the larger contact pads seen around the four larger sections are used to connect to the transistors collector and gate terminals. In this way, such a small array of only 100 transistors would control two thousand five hundred devices in the nano crossbar add-on.

These resistive memories are two terminal devices with a metal/insulator/metal structure. This configuration presents a high-resistance (off) state between the two terminals. In the presence of an applied potential the top metal migrates through the insulator in the form of filaments and makes contact with the bottom metal resulting in a low resistance (on) state of the device. This process can be reverted by applying an inverse potential at the terminals, causing the filament to recede back. The main device configurations studied during my work in this project were: Cr/Cu/CuOx/Nb, Cr/Pt/TiOx/Ti and a variation from the metal oxide barrier with p-Si/α:Si/Ag. Research on these devices was conducted in the micrometer range in a size scaling fashion, looking to downsize in the future into the nano scale region. The following figure shows the characteristic behavior of the resistive memories.

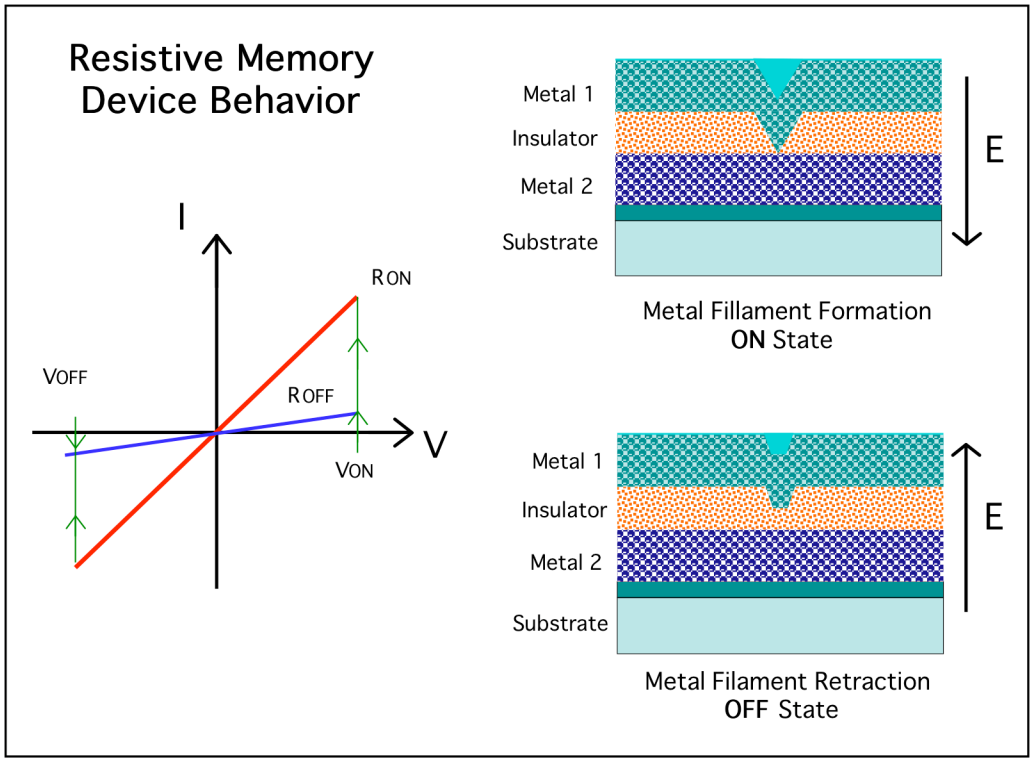


Figure 3. Characteristics and behavior of resistive memory devices. The I-V curve presents the switching behavior corresponding to the on-off resistive states of the device. The device illustrations show the process of filament growth and retraction in the presence of an applied potential.

The work was performed at the Stony Brook University's IC fabrication laboratory for superconducting and nano-scale devices, in the Physics and Astronomy Department. This fabrication laboratory is setup primarily for Nb/AlOx/Nb based devices for superconducting electronics. The MSI project focused on adapting the existing fabrication facilities to develop a commercial CMOS compatible fabrication process to produce the hybrid CMOS devices. This was achieved by refurbishing, upgrading and modifying existing thin-film processing equipment and developing fabrication processes compatible with the materials required for the resistive memory devices.

The presentation of this work is organized in the following way: Chapter II gives an overview of the instrumentation development part of the project. Chapter III discusses process characterizations of the new materials to be used in these devices. Chapter IV outlines the fabrication processes for the three kinds of devices studied. Chapter V discusses the results. Appendix A presents the fabrication process sheets for the three kinds of devices that were fabricated.

I. Instrumentation Development

The instrumentation development part of this project was a very labor intense process. The CMOL project required the use of many new materials not previously used in the fabrication laboratory. Every new material had to be carefully characterized to obtain the best processing approach during the fabrication stage of the project. It was for this reason, that some of the systems had to be modified and upgraded in order to introduce the new processes. Since two of the devices to be studied are metal oxide based, it was necessary to add plasma oxidation capabilities to two of the systems in the laboratory. One of these systems was the electron beam evaporator, and the other one was a sputter deposition system. Plasma oxidation was chosen for this research since it provides a much more energetic approach to produce thick oxides as opposed to thermal oxidation. It also provides more parameters that can be varied in other to modify and improve the quality of the oxides, like pressure and power.

Only the most important modifications and upgrades are presented in this chapter, since the task was very involved and time consuming. There were many more aspects to this part of my work but they are too numerous to be included in this writing. It took a better part of my first year, and continuous work during the rest in the project, to achieve and maintain the modifications and proper functioning of every system in the laboratory.

Electron Beam Evaporator

This system is known as the “Pb System” in the laboratory. At the time I started working in the fabrication lab the system was only being used for evaporation of thin films such as Pb, Al, Cu and Au to name a few. My work regarding this system was to maintain all components and modify it to handle two new process steps in the fabrication of devices for the CMOL project. Here I present the major components of the system before any modifications were done.

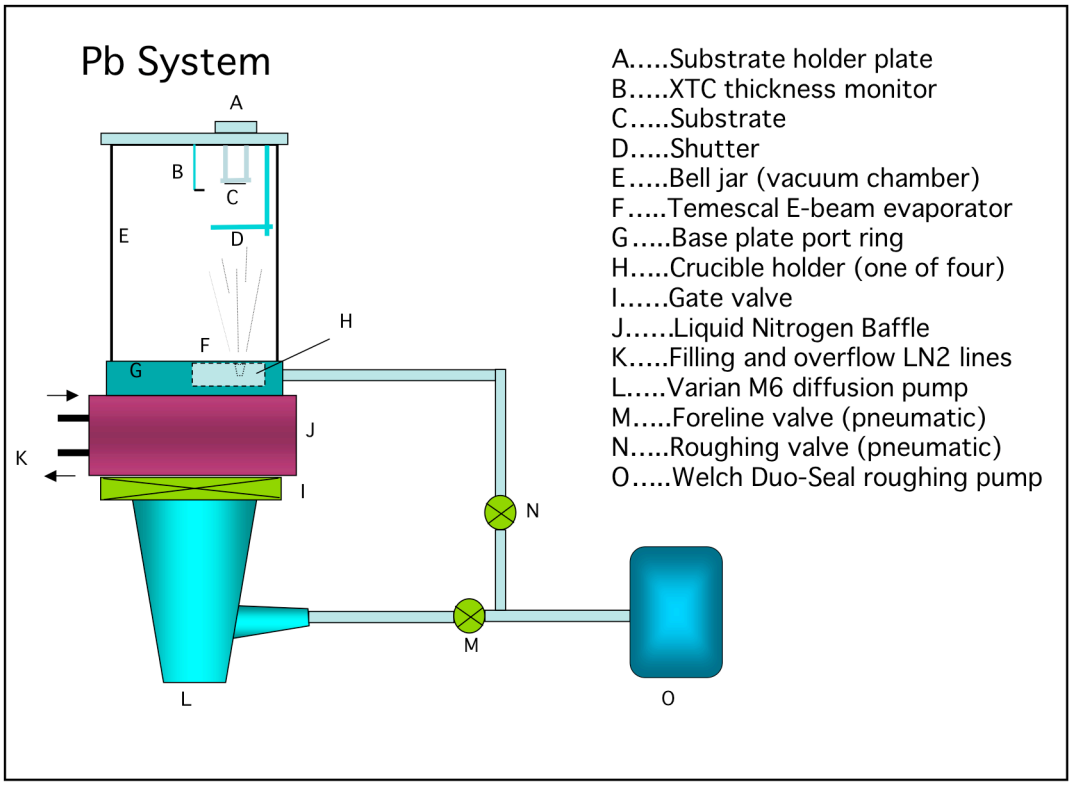


Figure 4. Pb system major component diagram.

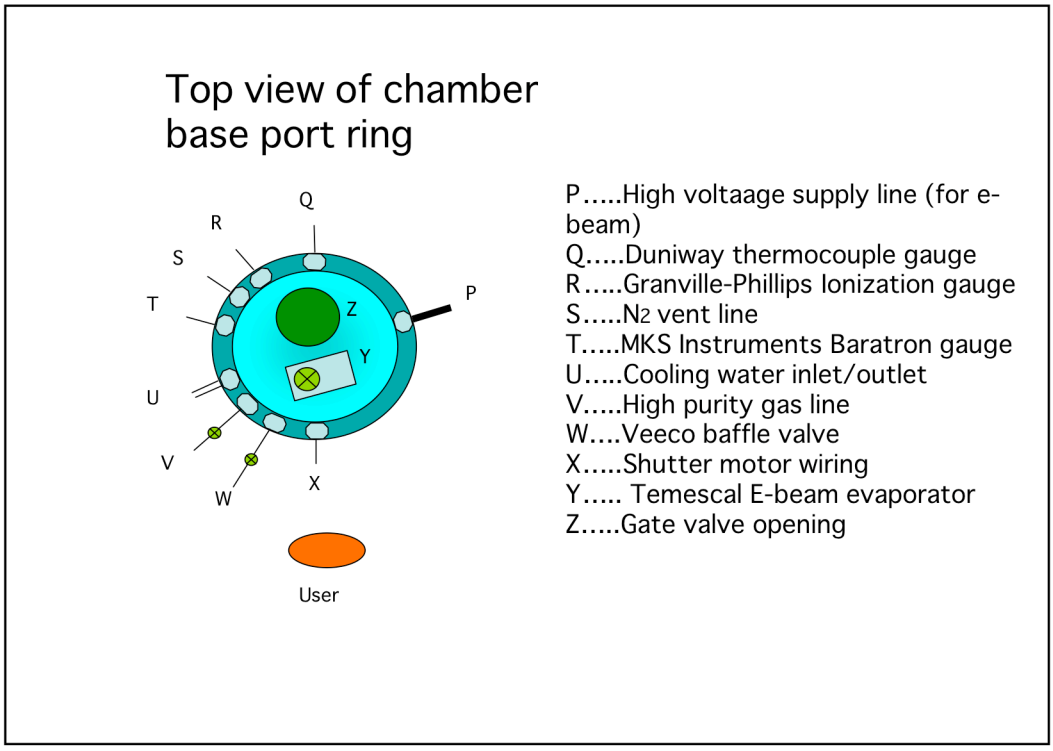


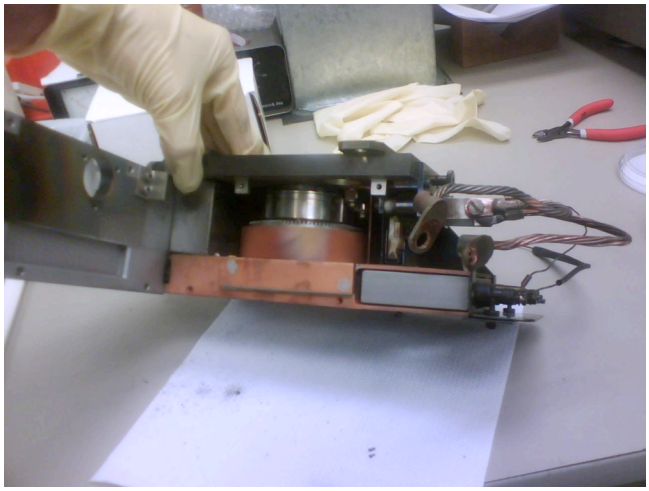
Figure 5. Top view of Pb system major component diagram.

There were a number of maintenance procedures and repairs that needed to be performed, mainly in the vacuum system. The UHV environment for this system is achieved with a Varian VHS series diffusion pump. A diffusion pump uses directional vapor jets to transport gas molecules by momentum transfer on collision with the vapor stream. The vapor is produced from heated oil, such as hydrocarbon oil or an organic liquid. These vapors go up a central chimney and out through a series of nozzles in a supersonic flow with a downward momentum and are ejected into a region of higher pressure [2].

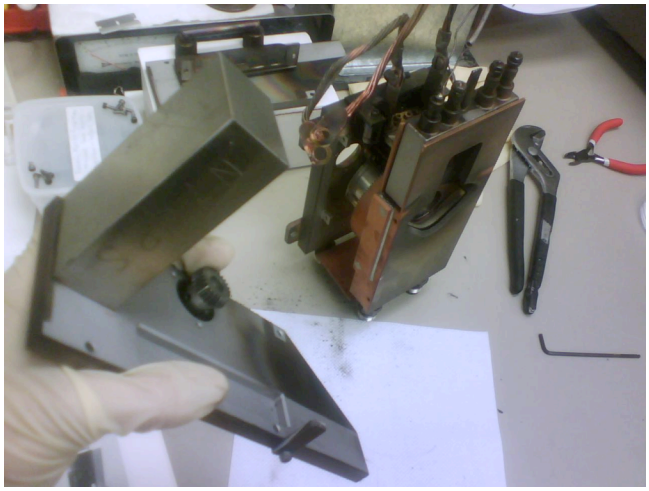
The heating element of the diffusion pump had shorted out and needed to be replaced. While replacing the pump the central bolt that holds the heater broke. The pump was removed and a new bolt was welded into place. At this time all its interior surfaces were thoroughly cleaned of burnt oil layers that had accumulated over time. The toggle valve's mechanism had become partially detached and only one side of the two shutter halves was working while the other remained closed at all times. The toggle valve was completely disassembled for cleaning and reassembled back with full operational capability. Fixing this problem already improved pumping speed and ultimate base pressure, which is in the low 10^{-7} torr. The interior surface of the bell jar was thoroughly cleaned of accumulated films that tends to peel and cause cross contamination of the samples used for evaporation. Another upgrade was done on the vacuum line connecting the mechanical "roughing" pump to the Pb system. The original line was made of many sections of PVC tubing and had presented several leaks in the past. I drilled a hole through the wall between the fabrication lab and the adjacent room where the mechanical pumps sit, and ran a direct line of 2.5" bore wire reinforced suction hose instead.

Further maintenance was done on the four-hearth electron beam gun. This Airco Temescal electron gun has four 7cc crucibles that are evenly spaced in a circle and are presented sequentially to the electron beam. The path of the electron beam in the vacuum environment is determined by a permanent magnet and can be fine tune by a coupled magnetic field. The electron beam gun works as an energy source capable of producing enough heat to melt any known material to the point of evaporation [4].

The system presented both static and dynamic vacuum leaks, which were associated with the four-hearth *e*-beam turret holder. The leak was determined to be related to the cooling water line for *e*-beam evaporation and the rotational mechanism used to manually choose the desired source. The *e*-beam gun was taken out for a full maintenance procedure. Several of the o-rings presented signs of wear, particularly the quad-ring, which is the direct seal for the cooling water line. All vacuum seals were replaced and accumulated metal deposits were removed.

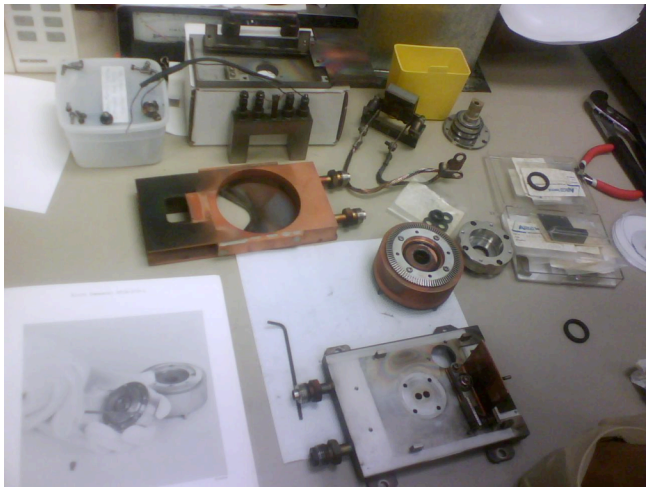


Picture 1. Lateral view of the four-hearth's interior components.

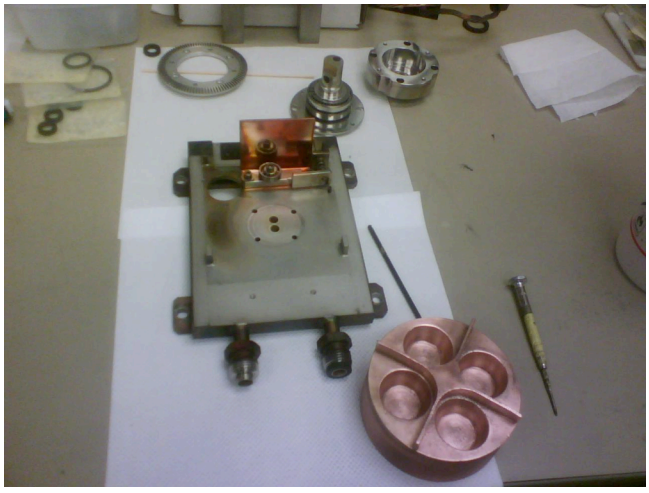


Picture 2. Permanent magnet for e-beam's rough path.

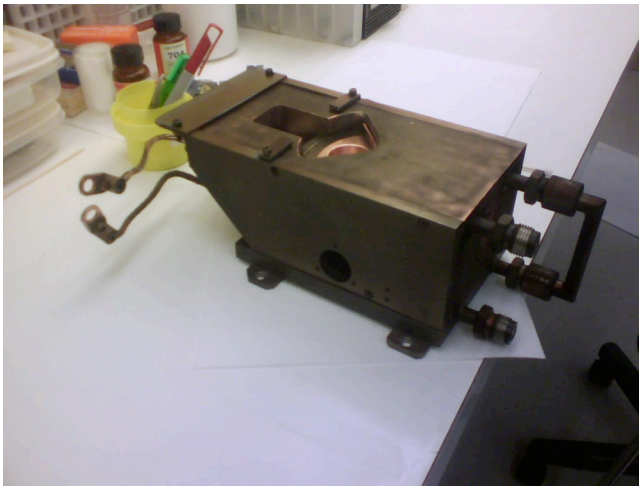
Picture 3. State of the four-hearth previous to cleaning process. Notice the heavy deposits on the turret holders.



Picture 4. Completely disassembled e-beam gun. Notice the o-ring replacement kits.



Picture 5. Clean four-hearth chuck with rotational and cooling components in the back.



Picture 6. Completely reassembled four-hearth e-beam gun, ready for reinstallation on Pb system.

There were a number of modifications done to the system that were necessary for the CMOL project. It was necessary to add backsputtering and oxidation capabilities; both processes were to be achieved with an r.f. plasma. Backsputtering was used for cleaning the surfaces prior to the deposition of thin films. In this case the sputtering gas is Ar, which can also be used for etching a material depending on the characteristics and intensity of the plasma; whereas oxidation provides an insulating layer for the devices being studied.

When sputtering an insulating material with a glow discharge plasma, AC power is usually employed so that power may pass through the insulator by capacitive coupling. In the presence of an applied potential, the surface of the insulator will charge up to floating potential causing recombination of the fluxes of electrons and ions, canceling them out. In order to get any sputtering action, it is necessary to use an alternating field with a frequency high enough as to be less than half the period it takes the insulator to charge up. From the electric field, a DC plasma will ignite an ion current towards the surface of the substrate across the cathode sheet. The time it takes for the surface to charge positively as a result of this ion current is determined by the capacitor operative equation [5],

$$I=j_{+}A=C(dV_w/dt)$$

where

I= current, A
j_{+}= ion current density, A/m^2
A= area of the insulation substrate and of the electrode, m^2
C= capacitance, F
V_w= voltage drop across the capacitor, V
T= time, s

A typical r.f. plasma generator is designed to deliver its power with a standard 50Ω output impedance. At the other end, the impedance of the plasma is very complex and can vary easily due to variations in gas pressure or system geometry. The wave propagating through the power transmission line will reflect some of its power if there is a mismatch in the impedance between the two ends. The effects of this power reflection result in heating of the line and possible damage to the generator. In order to avoid this effect, an impedance matching network is introduced between the power source and the load. Excellent treatment of the details of this process can be found in a variety of sources [5].

The evaporator system had existing gas lines for high purity Ar and O_2 that come together at a "T" connection. The gas is delivered to a base port of the chamber through a single gas line, which is regulated by a mass flow controller. The following figure shows the gas delivery configuration in the Pb system.

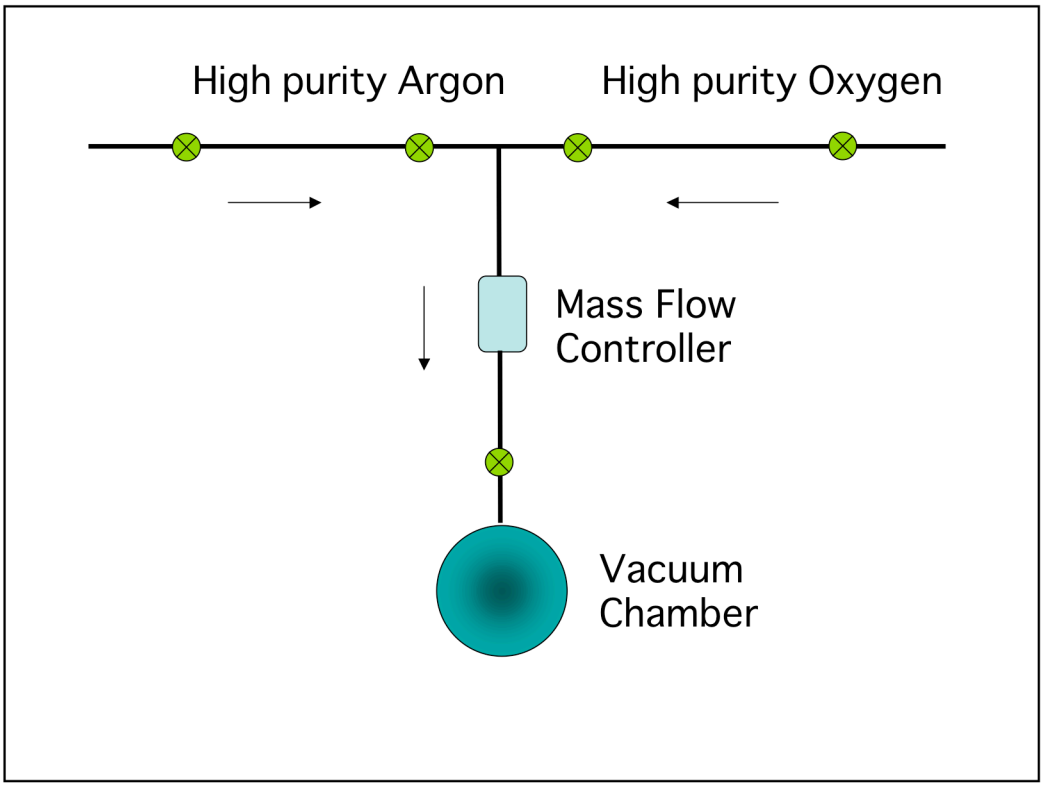


Figure 6. Diagram of high purity Ar and O_2 gas lines in Pb system.

It was also necessary to modify the substrate holder in order to achieve a plasma-generating configuration for the chamber. The original substrate stage was made out of a stainless steel structure in electrical contact with a substrate holder chuck. Though the substrate holder was insulated from the chamber's body by the o-ring that provides the vacuum seal, it was in electrical contact with the chamber by screws that hold the plate in place. Therefore, I had to redesign this piece in order to deliver the power directly to the substrate holder chuck. The substrate holder was fitted with two individual ceramic-insulated feedthrough electrodes on the top of the substrate stage plate. These were used to deliver the electrical power. The existing columns emerging from the top plate were used to support the substrate's holding chuck. high grade G10 PC Board was used as an insulator, screwed to the column ends. The original design was used for the chuck's mounting mechanism: a central hole that fits on a pin and is secured with a screw. The pin is the modified end of a screw that connects to the top plate's electrode through the insulating plate. Furthermore, the insulating plate was wrapped around with a thin copper foil matching the dimensions of the chuck. This facilitates the flow of current, since the wire is then secured to the copper and the power is delivered through a larger area rather than just through the holding pin at the center of the chuck. A 12 AWG copper wire was used and protected with vacuum grade ceramic beads to avoid backsputtering of the wire. A cover for the screws that hold the insulating plate in place was needed, since some of the films to be deposited are conductors and this would eventually create a path between the chuck and the rest of the holder that is in electrical contact with the chamber. The following figure shows a diagram of the modified stage and substrate holder.

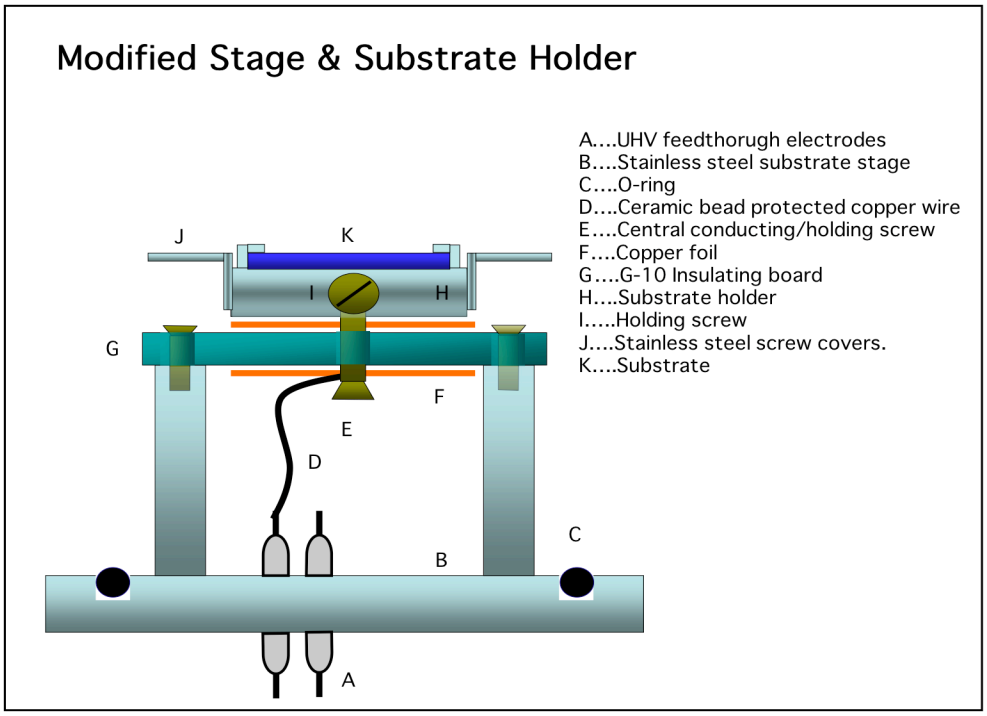
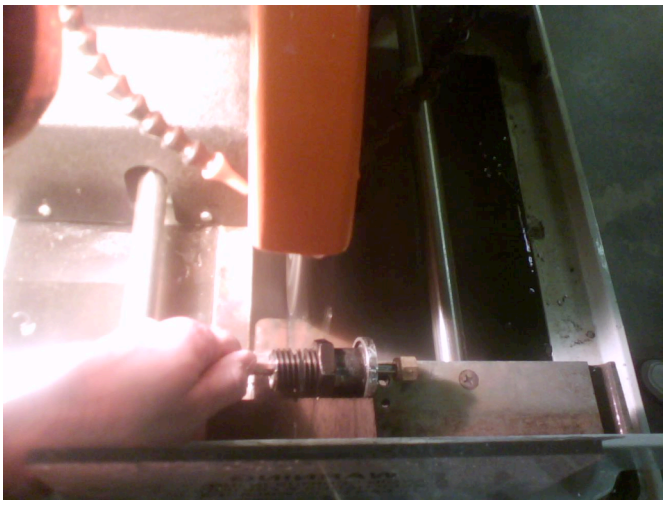
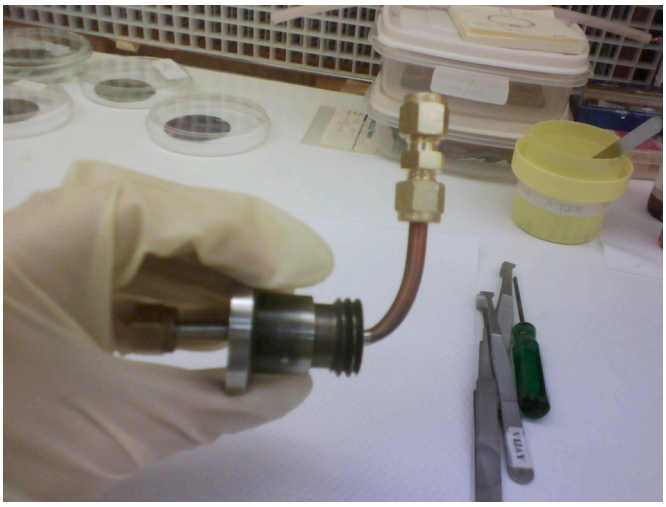


Figure 7. Modified stage and substrate holder.

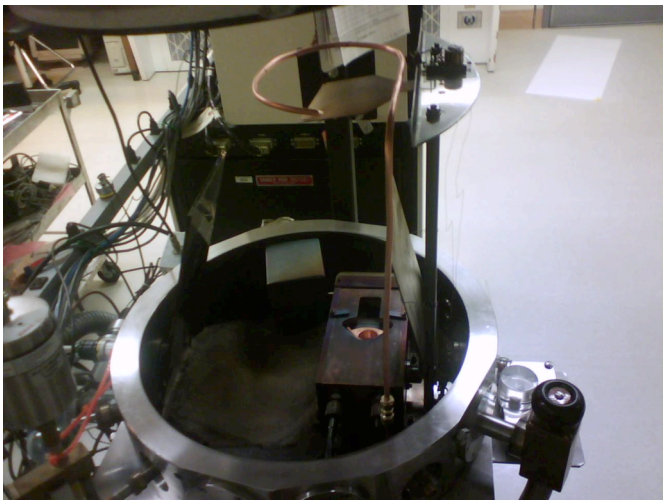
During the first plasma tests, it was noticed that the plasma characteristics were not optimal. The plasma was not localized near the substrate and the backsputtering rates were very low. It was determined that the gas distribution near the substrate was poor due to the fact that the gas delivery port for this chamber was too close to the gate valve and too far from the substrate itself. This caused the majority of the gas to be evacuated before reaching the substrate's side of the chamber. To correct this problem a gas delivery line was installed from the gas port and was coiled around the substrate holder with evenly spaced holes for the gas around the ring. The existing UHV high purity gas delivery feedthrough was used for this gas line, but it had to be modified to fit the new connections. After this modification, we noticed an improved plasma distribution and higher backsputtering rates. The calibration and characterization results from these tests will be presented in a later chapter. The following pictures show the fabrication and installation of the new gas distribution line.



Picture 7. Reducing the UHV stainless steel feedthorough.



Picture 8. UHV feedthorugh with copper pipe and swagelok connection.



Picture 9. Installed redistribution gas line.

Reactive Ion Etcher

This system was being used to etch Nb using high purity Sulfur Hexafluoride (SF6) gas; referred to as the RIE system in the lab. Maintenance procedures were performed to meet modifications and upgrades needed for the latter stages of the CMOL project. Here I present the major components of the system.

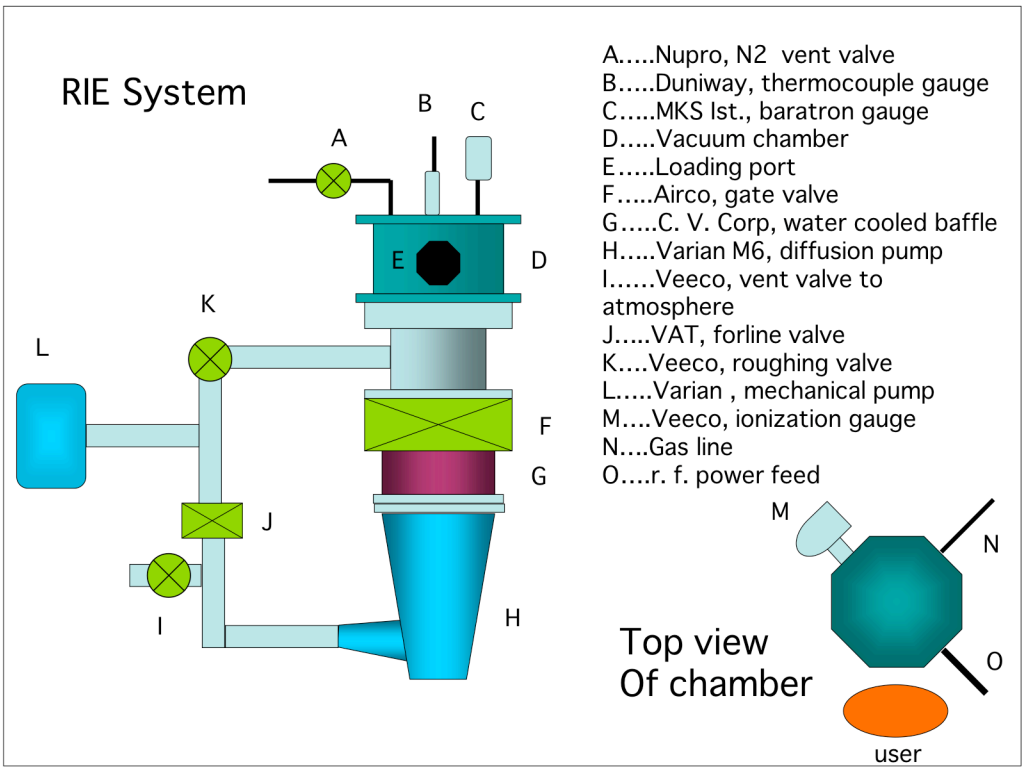


Figure 8. RIE System major component diagram.

The system was presenting anomalous behavior with respect to the chamber's base pressure. The concern was the performance of the Varian M6 series diffusion pump; base pressure remained one order of magnitude larger than the expected 10^{-5} Torr. Therefore, the system was shut down for maintenance.

Upon reassembling the system, it still would not pump below high 10^{-5} torr after five hrs (ample time to reach the desired pressure in the system). It was thought that there could be a problem with the o-ring that provides the seal between the pump and the baffle, since it had not been recently replaced. Replacing this o-ring did not improve the pressure, and both pump and baffle were dropped together to replace the baffle to gate valve o-ring. The 18 Ω - 208 VAC pump heater was also replaced at this time.

A persistence in the leak suggested that the pump's opening diameter was slightly smaller than it should be for the contact surface diameter of the baffle and the o-ring was not sealing properly since it sat right on the edge of the sealing surface. In order to remedy the situation it was decided to provide a custom made flange that would solve this problem. The flange was machined out of a solid piece of aluminum. The following figure presents a diagram showing the dimensions of the flange followed by pictures of the machining process.

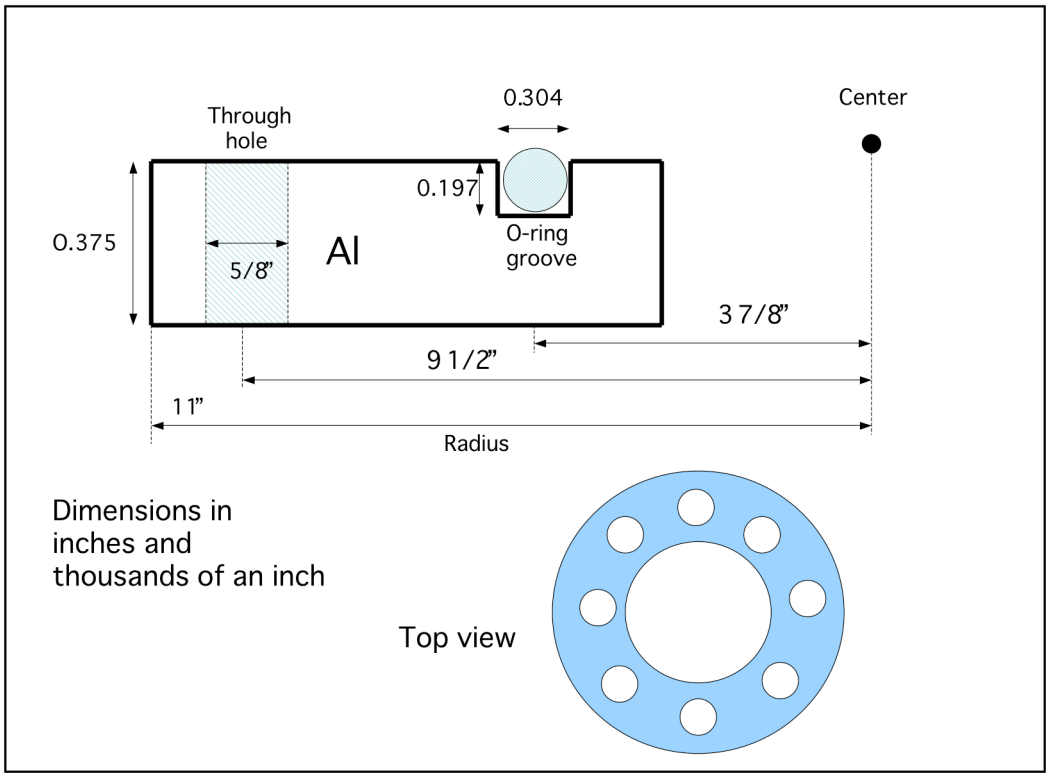
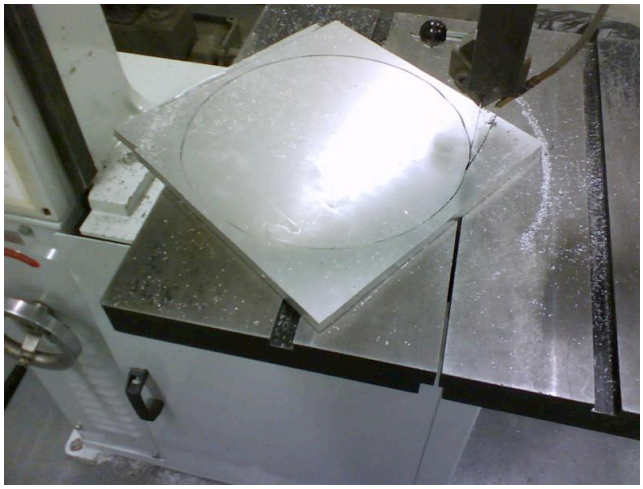
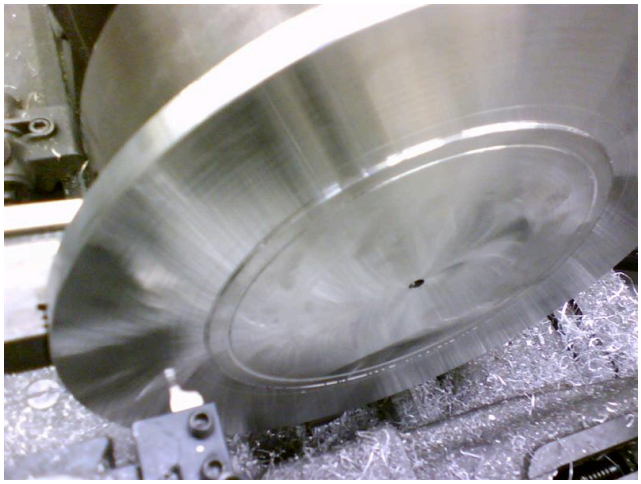


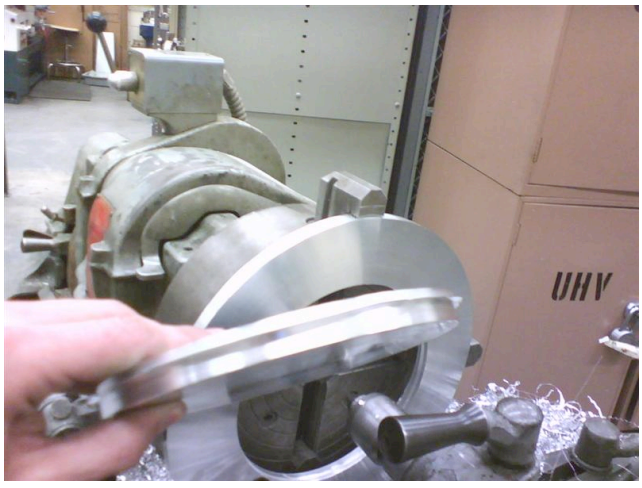
Figure 9. Dimensions of custom made flange for the diffusion pump.



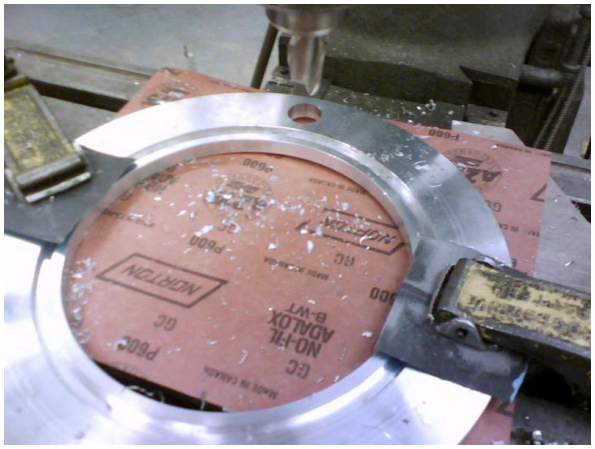
Picture 9. 14” X 14” X ¾” Aluminum plate being cut into a rough circle.



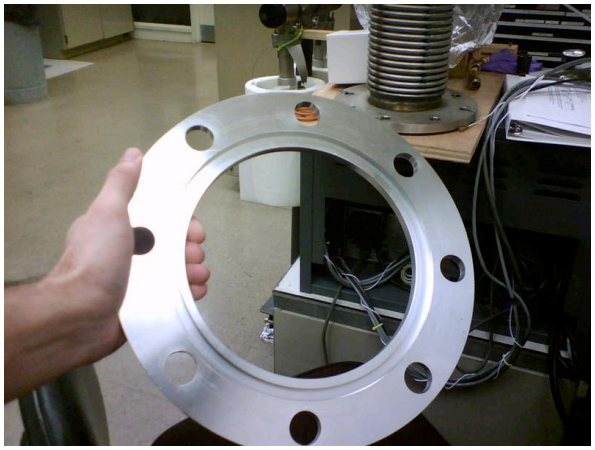
Picture 9. Plate has been rounded and “faced”. Now the center piece (inner diameter) is being cut out.



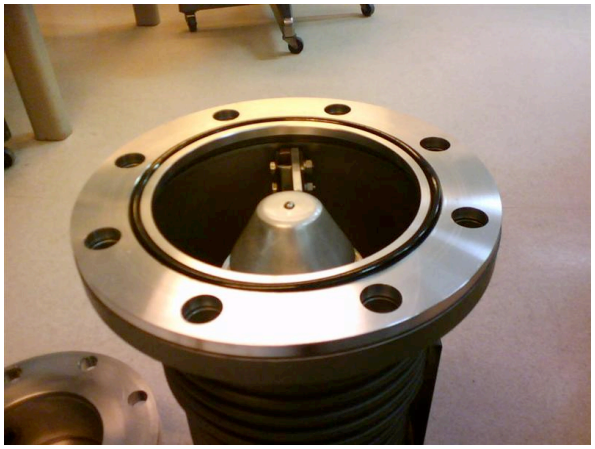
Picture 9. Center being removed. Next is the o-ring groove and final surface preparation. Since this is for a vacuum application, it is essential that the surface is free of defects.



Picture 9. Through holes being drilled with the milling machine. There are a total of eight holes in the flange.



Picture 9. Finished flange ready to install.



Picture 9. Flange in position with o-ring in place. Pump is ready to be remounted on RIE system.

After installing the flange and tightening connections in the SF6 gas line, a base pressure of low 10^{-5} Torr for etching with this system was achieved. Differing from the other systems in the lab, the tuning network for the r.f. system of this etcher is home made.

There are many gas mixtures that can be used for etching so the system also counts with a spectrum analyzer with a computer interface to monitor and record the gas species present in every process. Although there were multiple gas lines from high purity sources, the SF6 line was the only one that was connected to the system. The other gas lines and gas controlling devices were disconnected during the first stages of device fabrication for the CMOL project. SF6 was the only gas needed for etching of Nb and Ti. After completing the device fabrication processes, the rest of the high purity gases for future etchings of the of SiO_2 and Nitride were reconnected; these etchings are necessary for commercial CMOS chips in the second stage of the CMOL project. This etching process is part of the CMOS chip surface preparation for interfacing with the CMOL device layer to be deposited. The gases involved in the new processes are: CF4, CHF3, O_2, and Ar. The SF_6, CF_4, and CHF_3 gasses come from small high purity bottles designated to this system, while the Ar and O_2 come from larger bottles that supply the rest of the systems as well. The installation of the Ar line required the addition of a designated mass flow controller and pinch needle valve, elements that were already present for each one of the other gases. He following figure shows a diagram of the gas distribution lines for the RIE system.

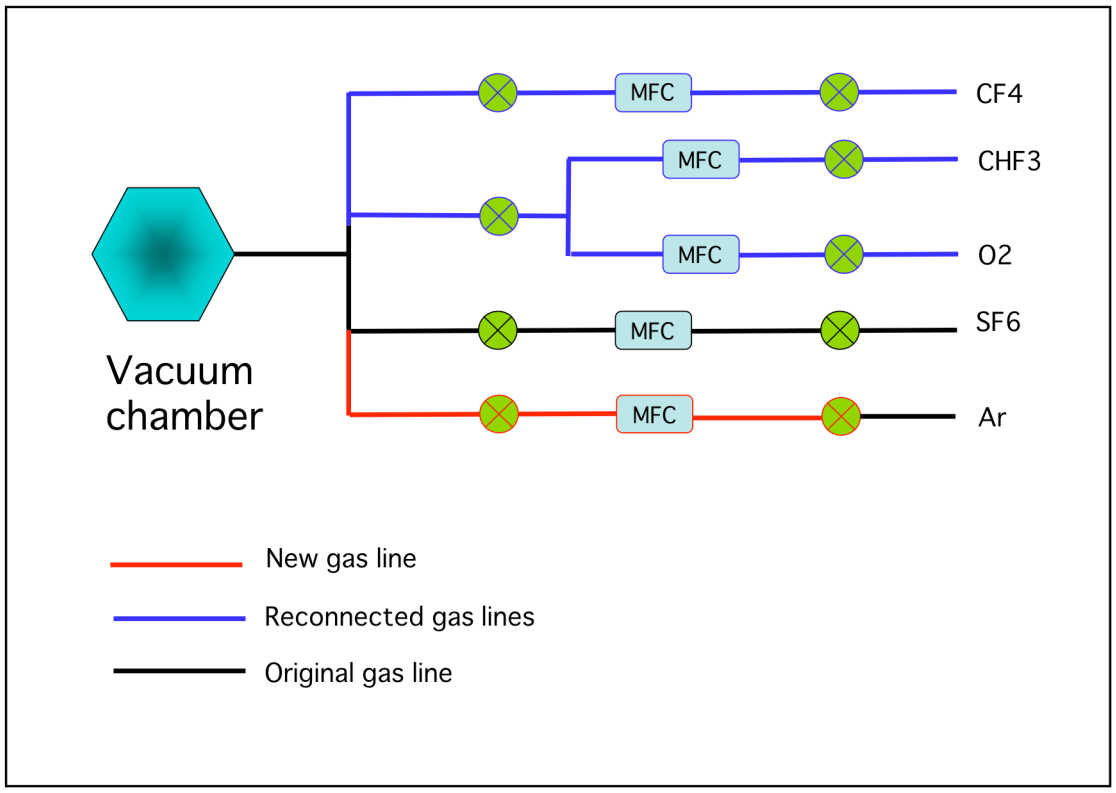


Figure 10. Gas distribution lines for RIE system.

Sputter Deposition Systems

This sputter system was donated from surplus by the IBM Thomas J. Watson Research Center and subsequently split into independent systems for developing high quality Nb/AlOx/Nb tri-layers and Quartz deposition. Of these only the Quartz system (SiO_2 system) was operational, while the other IBM system had been non operational for a period of about ten years.

The IBM system is composed of two chambers, one for DC sputter deposition and a sample loading chamber which counts with an extendible track and sample cart, as well as an r.f. system for various processes. The samples are manipulated within the chambers by the use of UHV remote manipulation arms. This sample loading and transfer system is necessary since the deposition chamber needs an ultra clean environment in order to avoid impurities that can alter the quality of the films. Both the IBM system and the Quartz system achieve UHV with the use of Balzers turbo-molecular pumps. The turbo-molecular pumps are molecular turbines that compress gas by momentum transfer from high speed rotating blades to the gas molecules. They usually operate at speeds between 25,000 to 60,000 rpm and are run by solid-state power supplies or motor-generator sets. They are particularly advantageous compared to a diffusion pump in the fact that they don't backstream any oil nor do they require a trap of any kind [7].

In this system, sputtering is achieved with D. C. Magnetron sputtering guns. In a typical D.C. plasma, energetic ions bombard the surface of a metal, resulting in ejection of surface atoms or molecules. The plasma is generated near the surface of a conducting target kept at a positive potential, and a substrate is placed some distance away facing the target. If the ejected atoms or molecules are energetic enough, they will deposit on the surface of the substrate. Here we can see why it is of great importance that the conditions inside the chamber be optimal for the resulting quality of the films. The following figure shows a schematic of a D.C. torus planar-magnetron gun describing its structure and behavior [5].

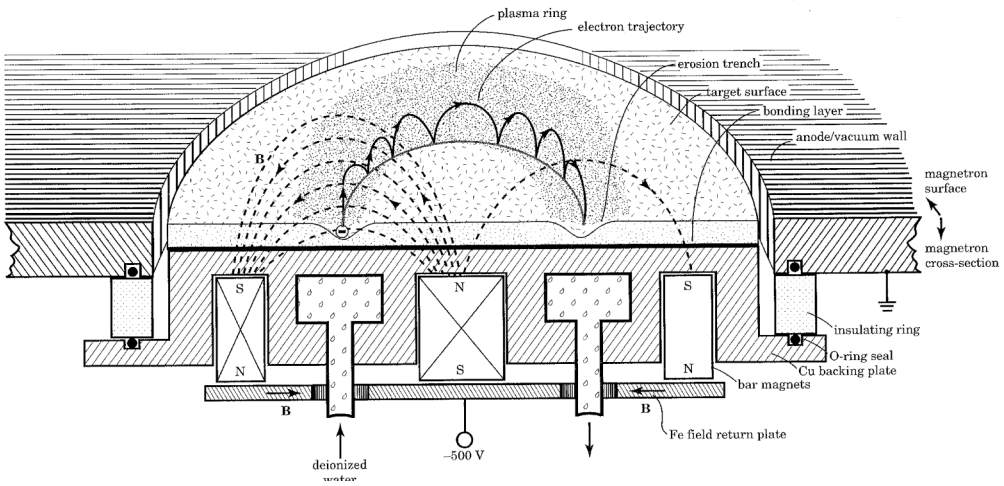


Figure 11. Planner-magnetron structure and behavior.

The IBM system was computer automated in order to improve the quality of the trilayer fabrication and was intact from the time it was last used, with the exception of the vacuum system which had been scavenged for parts over the years. The task for this system was, not only to reassemble the vacuum and correct various possible start up problems to bring it back to full functionality, but also to modify the system for the new research intended to be carried on it. The following figures show the main components of the IBM System.

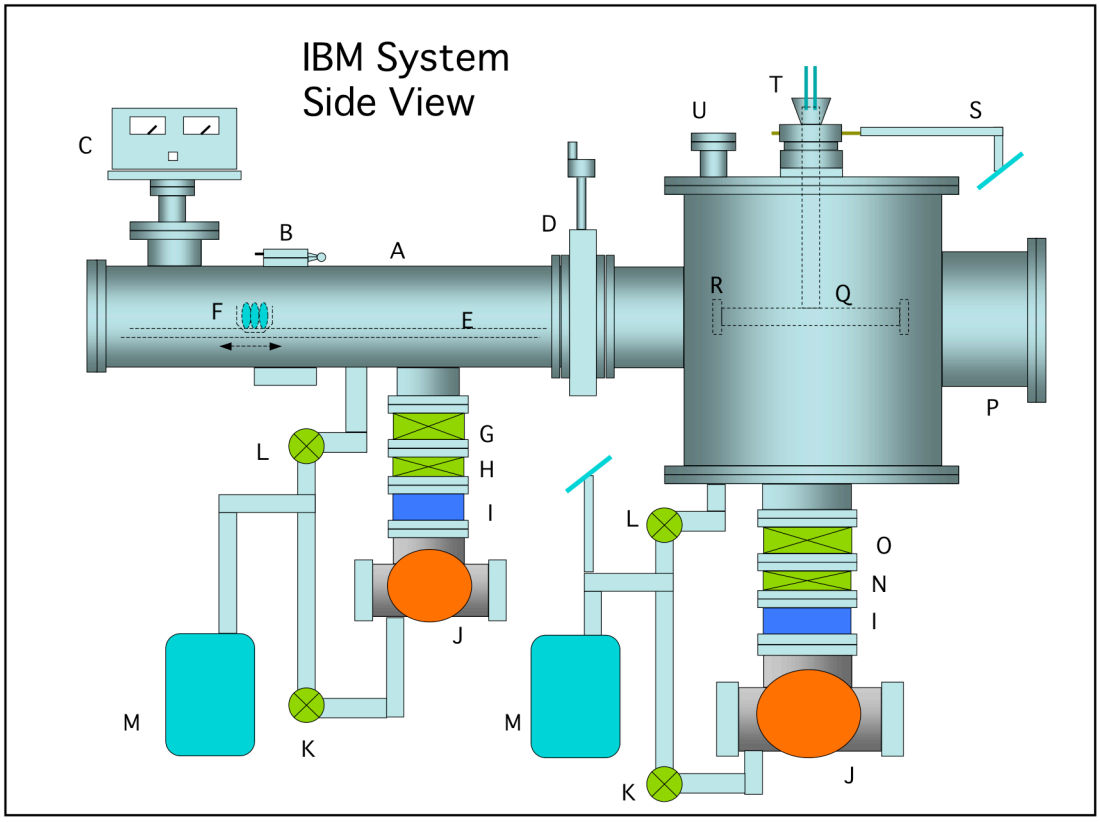


Figure 12. Side view of IBM System's major components.

s

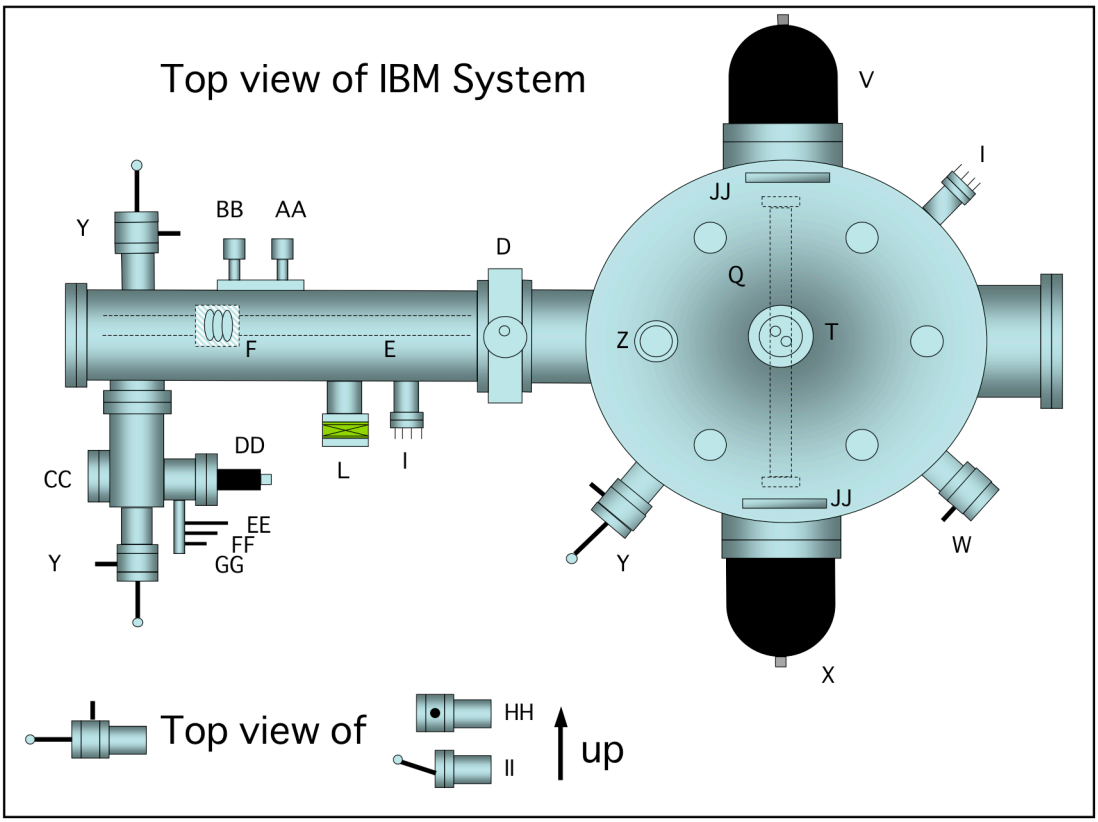
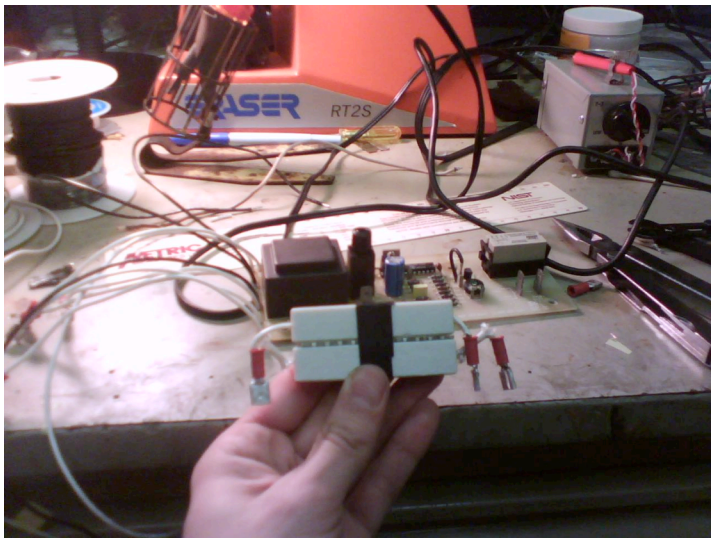


Figure 13.Top view of IBM System's major components.

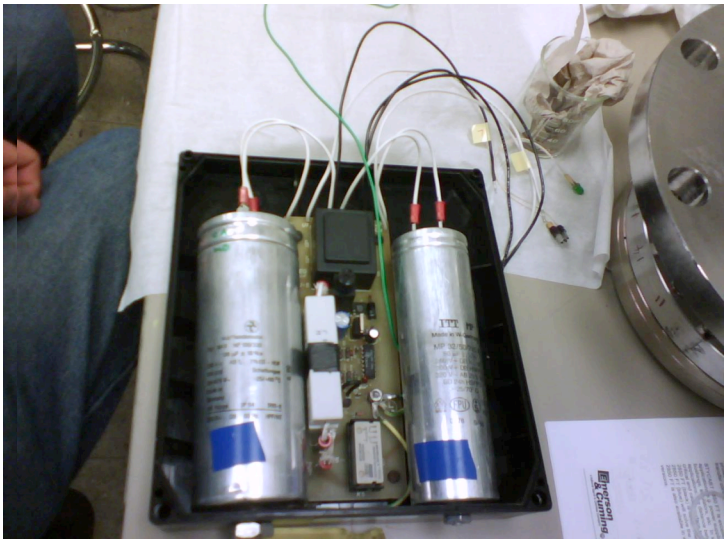
A.	Stainless Steel Loadlock Sample Transfer UHV Chamber.
B.	Hinged Access Hatch (Conflat).
C.	R. F. Tuner for Backsputtering Gun.
D.	Manual Gate Valve for Sample Loading.
E.	Sample Transfer Track (1-D Motion).
F.	Sample Transfer Cart (1-D Motion).
G.	Iris Throttle Valve.
H.	High Vacuum Pneumatic Gate Valve.
I.	Nude Ion Gauge.
J.	Blazer's Horizontal Shaft Turbomolecular Pump.
K.	Pneumatic Foreline Valve.
L.	Pneumatic Roughing Valve.
M.	Balzer's Rotary Vane Backing Pump.
N.	Pneumatic Throttle Valve.
O.	High Vacuum Pneumatic Gate Valve.
P.	Stainless Steel Trilayer Deposition UHV Chamber.
Q.	Two Station Water cooled Rotating Substrate Stage.
R.	Remote Loading Substrate Holder.
S.	Differentially Pumped Rotary Feedthrough.
T.	Water Feedthrough for Substrate Cooling.
U.	Lighted Viewport for Sample Transfer Point.
V.	Niobium D. C. magnetron Gun.
W.	Viewport with UHV Feedthrough Shutters.
X.	Copper D. C. Magnetron Gun.
Y.	Top View of II and JJ.
Z.	Lighted Viewport for Sample Transfer Point.
AA.	Rotary Feedthrough for Track Translation.
BB.	Rotary feedthrough for Sample Cart Translation.
CC.	Backsputtering Station Port for Direct Loading.
DD.	R. F. Backsputtering Gun.
EE.	Convectron Vacuum Gauge.
FF.	High Purity Argon Line.
GG.	High Purity Oxygen Line.
HH.	Viewport with UHV Feedthrough Shutters.
II.	3-D Non-rotatable Remote Manipulator Arms.
JJ.	Sputtering Gun Shutter.

Table 1. Index for components of IBM system's previous figures.

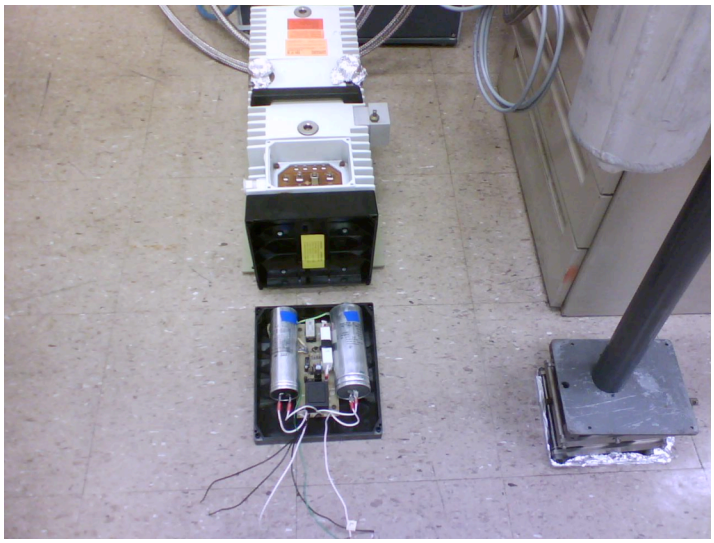
The first task was to reassemble the vacuum system. There were several Balzers DUO16 backing pumps around the lab, which had been swapped with the Quartz system at one point or another. This kind of pump is not water-cooled and it generates a lot of heat. Over time it degrades the wiring and other components of the pump, resulting in pump malfunction. One of the biggest problems with both the pumps being installed in the IBM system was the electronic components, these pumps presented burnt and brittle wiring from continuous hot environment, that had also resulted in burnt main power resistors. It was necessary to provide new wiring for both pumps, new power resistors and rewiring of some electronic circuits. The operating agent was drained and later reused since was still in good condition. The following pictures show the maintenance and repair work performed on the backing pumps for the IBM System.



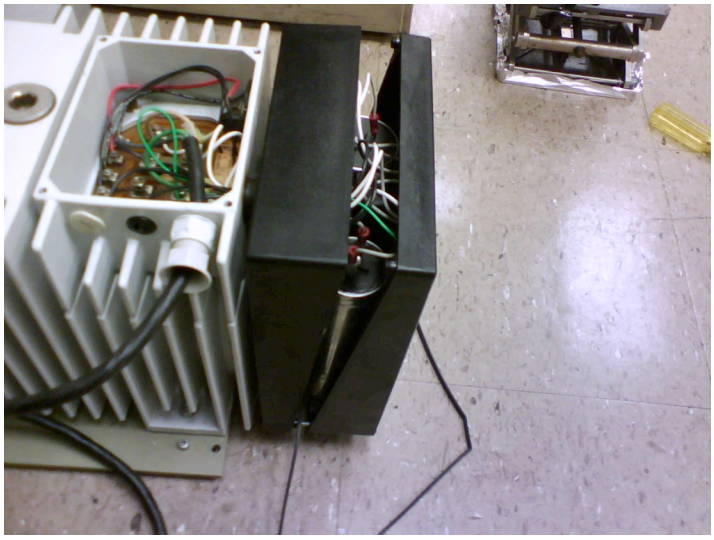
Picture 10. New 2Ω, 20W power resistors.



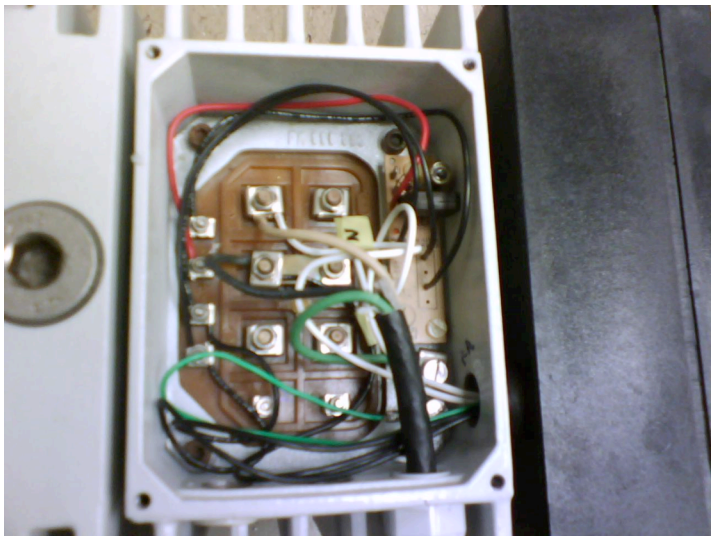
Picture 11. All new wiring, and electronic components reassembled. Starting and running capacitors on the sides.



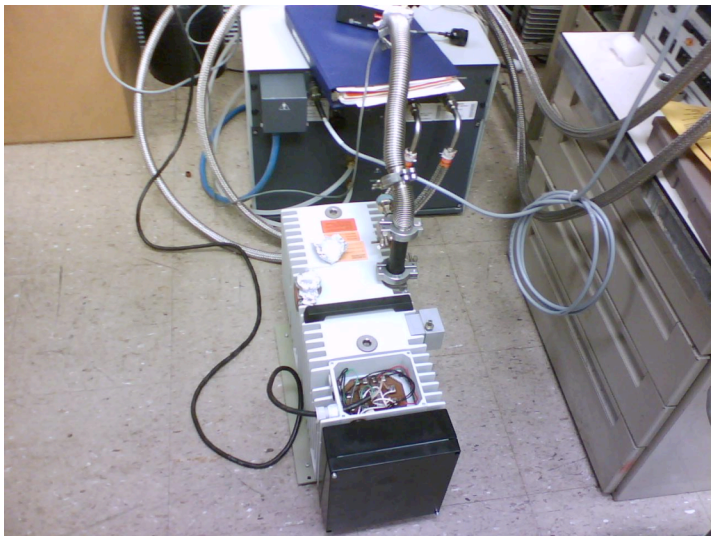
Picture 12. Capacitor box ready to be reinstalled on mechanical pump.



Picture 13. Wiring complete, showing capacitors placement in box.



Picture 14. Wiring close-up, with 120VAC line coming in from the bottom and DC rectifier (also with new wiring) at the top right.



Picture 15. Pump being tested for ultimate pressure and overall functioning.

Both pumps use Krytox oil as their operating agent. They were individually tested for base pumping pressure as well as for proper functioning of the safety vent valve which vents the inner chambers of the pump without losing vacuum to the system [7]. This safety mechanism is important in the event of power loss, as it avoids back streaming of oil to the system.

The "turbo" pumps operating agent had not been drained and it presented some light coloration with a total volume of 90 cc that was replaced by new operating agent. The lab counts with several controllers for these pumps: TCP 300, TCP 310, TCP 380, of which the TCP 380 is the newest, most reliable model. The TCP 300 and 310 are rather old and continuously break down or simply malfunction sporadically. To this date, they have been repaired several times by the electronics shop.

The task of connecting the turbo pumps is not a trivial one given the amount of interlocks and possible operating configurations, there was a great deal of time dedicated to setting up and fine tuning the three turbo pumps in the lab, including the Quartz system one. The basic interlocking mechanisms are for the water cooling, overheating of the backing pump and venting valve, any of this interlocks will shut down the pumps in the event of anomalies [7].

Another vital component to the system is the pressurized N_2 lines that feed dozens of valves, a couple of blowers and vent lines for the chambers. The pressurized N_2 is taken from a LN_2 bottle in an adjacent room and delivered to the system by ¼" copper pipe. The line is pressurized to ~120 psi but is regulated to the valve's operation rating of ~70 psi. The minimum pressure required to operate any of the pneumatic gate valves is of 60 psi, in order to ensure that the gate closes and locks for the venting of the chamber.

The distribution of pressurized N_2 is done with 1/8" plastic tubing connected by pressure nipple fittings. There was an extensive leak test of this gas distributing network and several leaks and defects were found in the process. The main method used to check for leaks was the spraying of the connections with a "liquid leak detector" which bubbles easily in the presence of a gas leak. After correcting all the tubing leaks, there still was a significant leak in the network. It was noticed when performing pressure leak tests by pressurizing the network and then closing the gas supply and observing the pressure drop at the pressure regulator gauge. The leak's rate was of 70 to 0 psi in 2 min, and after much inspection it was found at the foreline valve for the transfer chamber, which had to be replaced.

There is only two species of high purity gases for the IBM and Quartz systems, Ar and O_2. They are provided by pressurized ultra high purity bottles (99.999%) and delivered to the systems via ¼" copper pipe. As part of the new processes to be carried by these systems it was necessary to give oxidation capabilities to the transfer chamber of the IBM system using its already existing r.f. gun, previously used only for Ar backsputtering. An O_2 line was added to that chamber accompanied by a reconfiguration of the O_2 lines to the different systems from the high purity O_2 bottle. The following figures show the gas distribution lines for Ar and O_2, as well as N_2 in the sputter deposition systems.

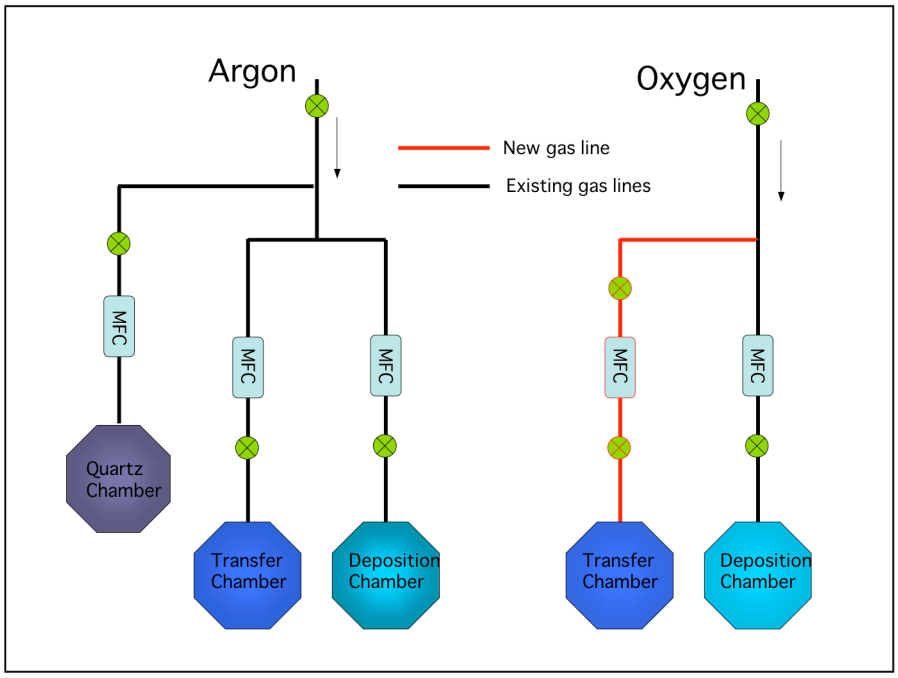


Figure 14. Ar and O_2 supply flow diagram.

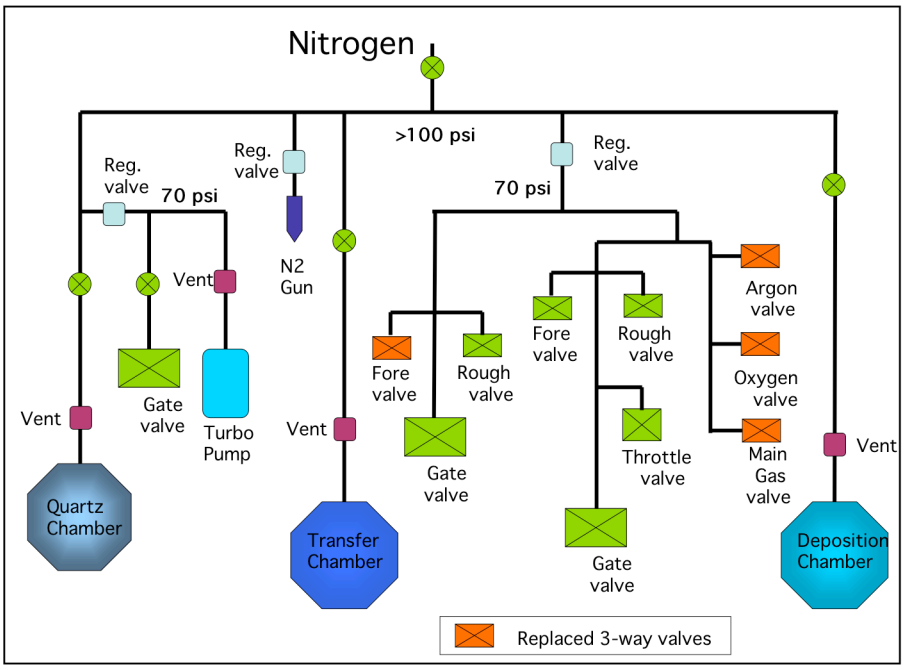


Figure 15. Pressurized N_2 flow supply diagram.

As previously mentioned, the system had been upgraded with a computer added automation program that allowed for remote control of the different process stages in the fabrication of Nb/AlO_x/Nb trilayer. Both software and hardware modifications had been achieved but the hardware components were not connected to a computer and all the interfaces were idle. This didn't matter for the new fabrication processes being undertaken as the system was intended to be used manually. The transfer and deposition chambers share a switchboard that controls the different roughing, foreline, gate and throttle valves of the system. It was found that the throttle and gate valves were not operable manually, meaning that they had been left wired to operate only by remote control. To solve this problem a 2-way switch for each valve was installed, enabling manual or remote control of the valves. The diagram of the wiring modification is shown below.

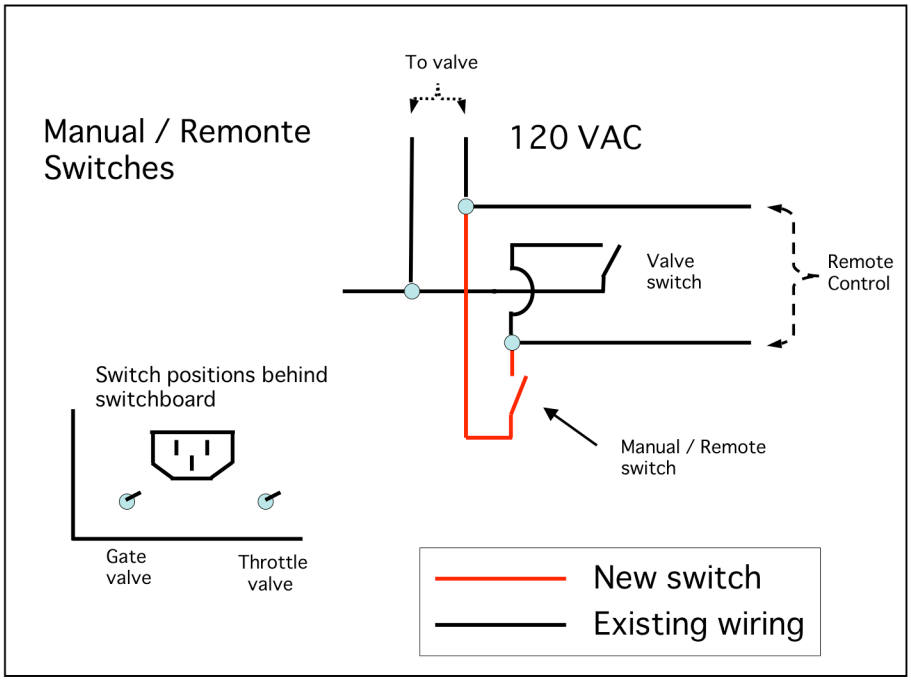


Figure 16. Switchboard Manual / Remote switch circuit diagram.

As part of the modifications to this system, an existing D.C. magnetron sputtering gun loaded with an aluminum target was used, and the target was replaced with a copper one. This was supposed to be a simple operation and yet following Murphy's law, we encountered that the new target was 3" by 1/8" and the gun accepted 2.95" targets. In order to use the target we had, it was necessary to very carefully machine the target to the right dimension without contaminating it (target was 99.999% pure copper). In addition to the diameter reduction the new target required a 1 mm spacer to fit correctly in the gun. We also used Ag paste on all contact surfaces to ensure proper thermal contact for the water-cooling of the target during operation.

II. Process Characterizations

This section will describe the basic principles and procedures involved in the characterization of thin films. All characterization of thin films and subsequent fabrication of devices was performed on 2" Si wafers with, bare Si, oxidized Si and/or doped Si. The wafers were 280 micron thick on average and from different suppliers. The growth of a thin film is straight forward, starting with securing the wafer to a substrate holder and loading it to a specific system. The system is then tuned to specific parameters such as vacuum base pressure, specific power, evaporation rates and gas pressure, in the case of glow discharge processes. These parameters will determine the specific characteristics of a film, so it is necessary to perform individual tests of each process and material being used. Characterization was not only performed on thin film growth but on various etching processes, oxidation of material surfaces and lithographic processes as well as backsputtering rates.

The CMOL project required extensive characterization of new processes and new materials, and was performed as an ongoing endeavor in conjunction with the process development of the new devices. Some characterization had to be done to correct or improve a particular step of a fabrication stage of the project. The importance of this characterization cannot be stressed enough as it is essential to ensure the quality, reproducibility and yield of devices being fabricated. Upon gathering the resulting parameters from the characterization process it is possible to establish specific guidelines or “recipes” for the fabrication of a particular device. These guidelines are produced in the form of “fabrication sheets”, which outline each fabrication step in order of execution

and provides the specific parameters and relevant information for each process. The studied parameters are expected to be very stable and yield "equal" results provided no changes are done to the instrumentation, geometry of the systems, etc. The instrumentation used to achieve these parameters is very reliable and is easily calibrated to international standards with the instructions provided in their respective operation manuals.

Dynamic Flow Characterization of AR and O_2

The first characterizations were carried out in the IBM system and dealt with the Ar and O_2 gases to be used for fabrication of devices in that system. These tests were aimed at establishing an accurate measure of the gas flow and pressure in the chamber as read by the different instruments. Both the deposition and transfer chambers count with convectron gauges to monitor pressures in the mtorr range at which the turbomolecular pumps would be able to start pumping on the chamber. To monitor the gas or gas mixture's pressure in a chamber it is desirable to use a Baratron gauge, a capacitance diaphragm pressure gauge, which is extremely accurate by measuring absolute pressure regardless of gas mix in the chamber [9]. The following figures show the results of these calibrations for the deposition chamber in the IBM system.

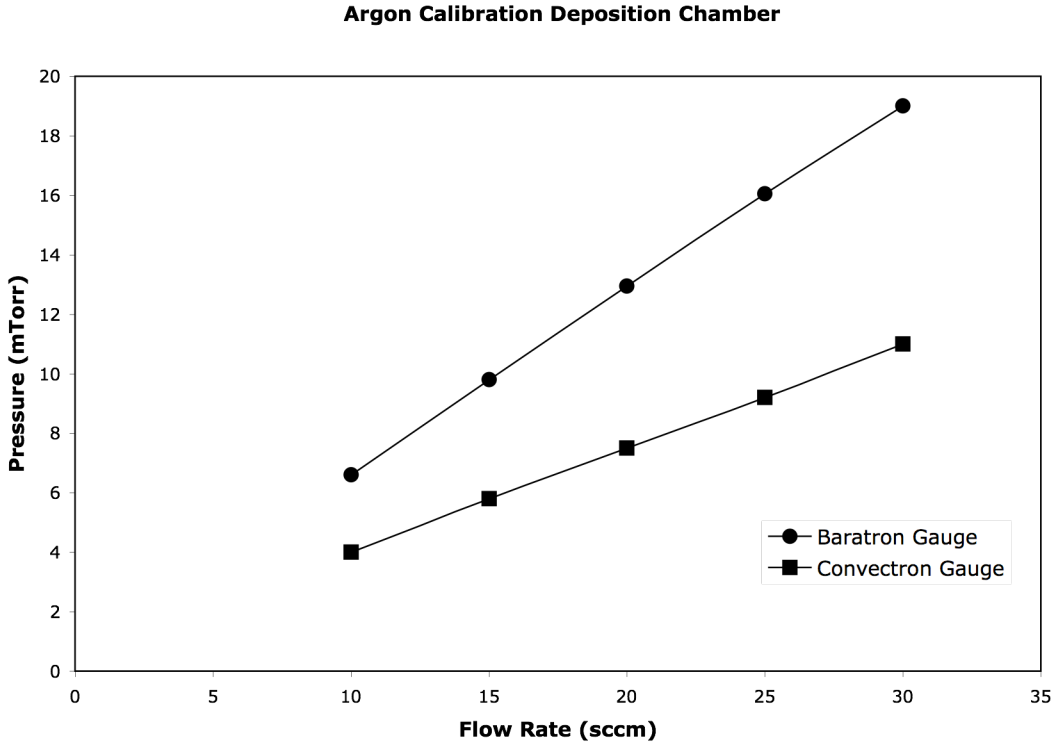


Figure 17. Ar calibration in IBM deposition chamber.

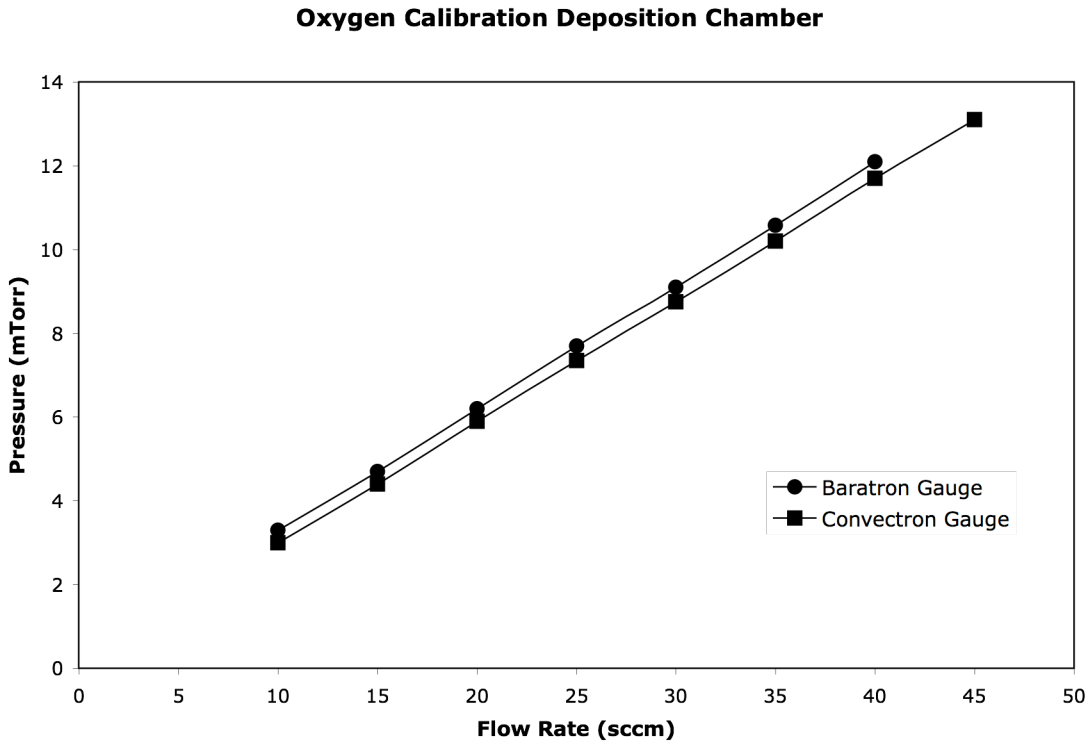
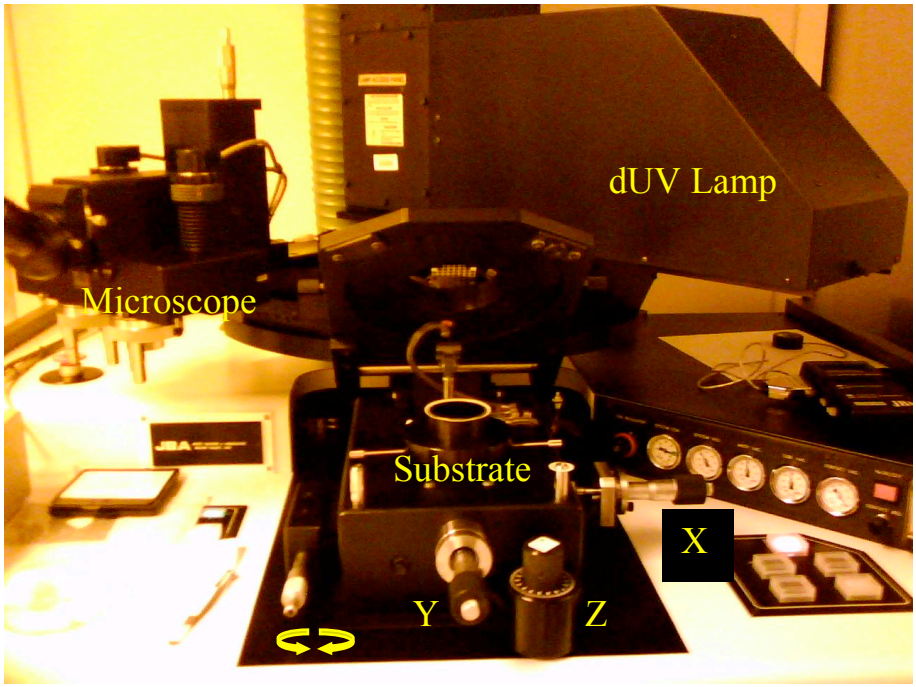


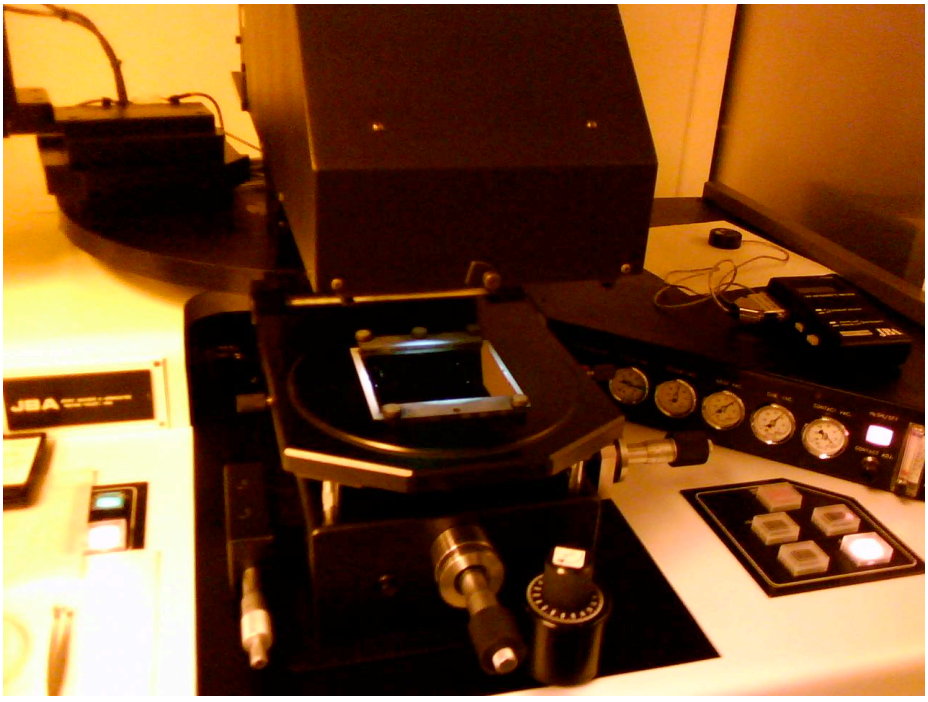
Figure18. O_2 calibration in IBM deposition chamber.

Optical Lithography with dUV Resists

A characterization process involving growth or removal rates will aim to determine how much material is being deposited or removed by a particular step of fabrication. The most common way to get this information is through the use photolithography and a surface profiler that performs very sensitive scans of a surface topography. Photolithography uses positive and negative photo resists to transfer geometric shapes to the surface of a wafer, hence protecting or exposing a particular area. Depending on the chemical composition of the photo resist, it will become hardened or more soluble to a developer after exposure to dUV light. The basics of photolithography involve photo resist application, pos coating soft baking of wafer, mask alignment, exposure and development, and hard baking [8]. A JBA mask aligner was used for the photolithographic processes, the following pictures show the main components of the instrument.



Picture 16. JBA mask aligner's main components and mask aligning tools.



Picture 17. dUV light exposure.

While preparing a photo resist application, whether it is for characterization or a fabrication step, it is necessary to provide a coating of sufficient thickness and take into account how much deposited material is to be “lifted off” the wafer and/or what the etching rate is for a particular photo resist if a material is to be etched or backsputtered. The following figure shows the basics of dUV photolithography.

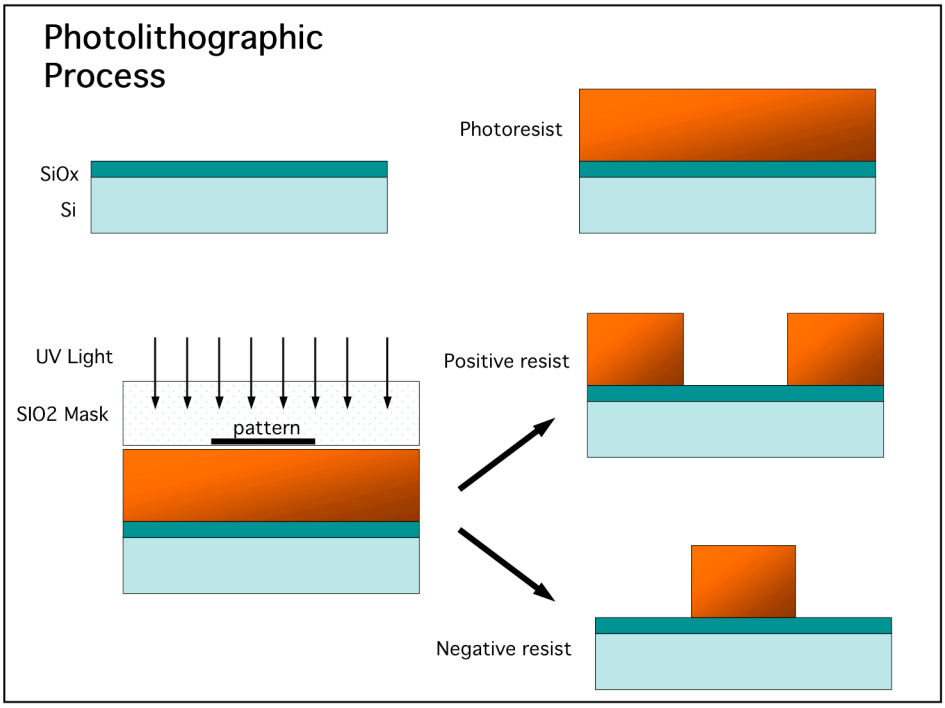


Figure 19. Photolithographic process for positive and negative photo resists.

In the case of a thin film's deposition rate, the wafer would be patterned using a clear quartz mask with the desired pattern and a material deposited on its surface with a particular set of predetermined parameters. After lift off, the patterned regions remain standing with well-defined areas. At this point, the wafer is loaded on the surface profiler and scanned with a "step height" function. The profiler used for these characterizations was a Tencor Inst., Alpha-Step 200. This instrument uses a stylus arm calibrated to 8 mg of force applied to a surface with a 12.5 μm radius needle tip, and has a vertical resolution down to 5 Å in the kÅ range and 5 nm in the μm range [11]. The surface profiler does not provide a sensitive enough measurement of surface roughness at the atomic level like an Atomic Force Microscope would, but it provides a glance of surface uniformity at the scale of its lowest resolution. The following figure shows a simple thickness measurement.

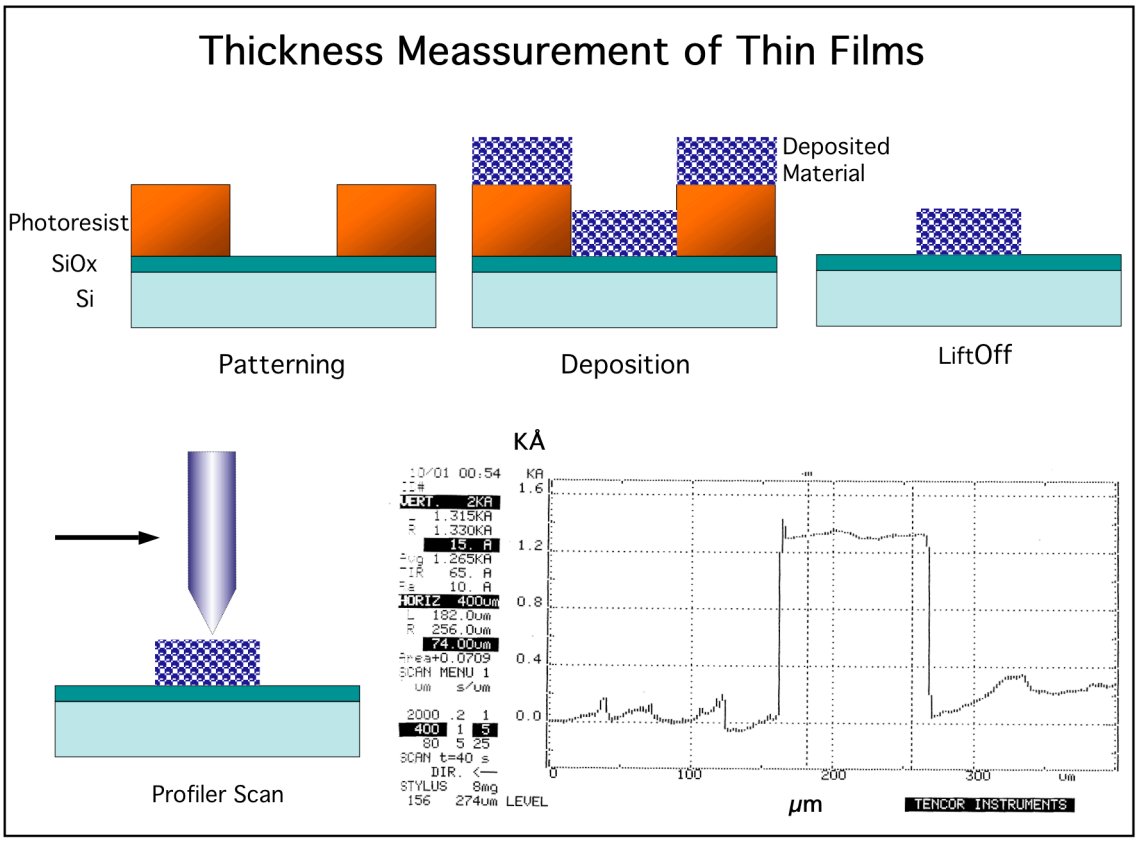


Figure 20. Characterization of thin film deposition parameters.

Etch Rate Characterization

Photo resists will have lower etching rates than most materials used for device fabrication, such as Ag, Cu or Nb. When choosing the photo resist thickness the etch rate and dimension change is taken into account, in order for a measurement to be taken between processes without removing the resist. The following figure shows an example of this consideration.

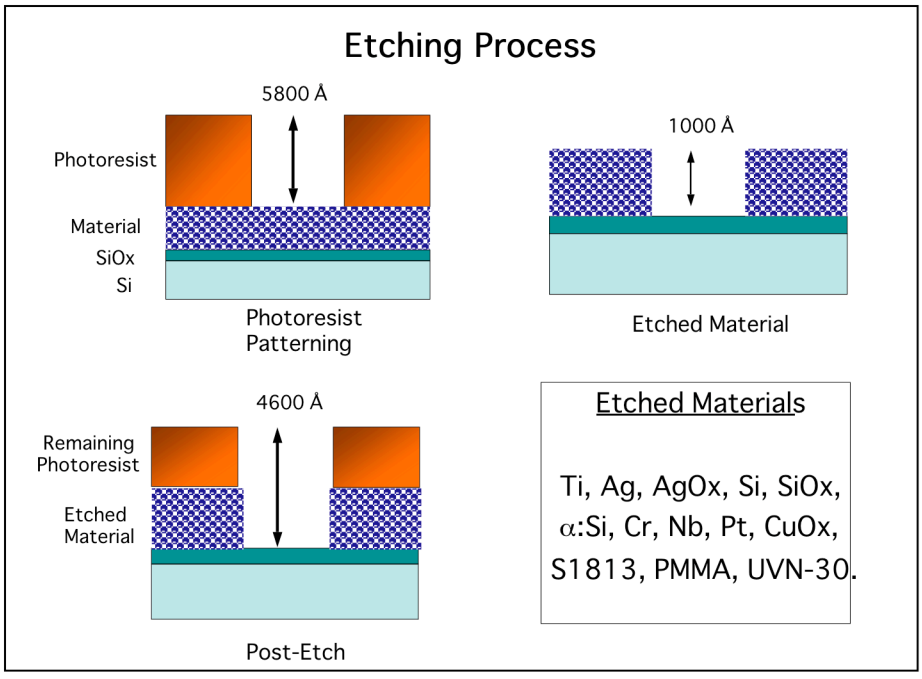


Figure 21. Etch rate characterization.

From figure 21 we see how one etching step would allow for the characterization of the photo resist etching rate, as well as the material one. This same procedure can be carried out for the different etching techniques that are used in the fabrication process, like Ar backsputtering, wet etch and RIE using SF_6 gas. In cases where a chemical effect is involved, like in RIE or wet chemical etch, there can be significant etch rate variations between different materials. For example, an oxide layer deposited under a Nb layer would act as a "stopper" in an RIE etch with SF_6 gas, where the etching action would slow significantly once all the Nb is removed.

In the case of further processing required, the photo resist is not removed and the thickness change measurement needs to take into account the thickness change from the etched photo resist. This is a step related to process development, yet is worth mentioning at this time for illustration purposes. In a simple material etch rate characterization, the photo resist is removed and a straightforward measurement is performed. The following figures show an etch/ash/backsputter rate sheet used for single processes and a table of etch rate results.

RESIST ETCH/ASH/SPUTTER RATE TEST

SAMPLE # _____ **Substrate :** _____ **Date** _____

1. Protective Metal Deposition **Date** __/__/__ **Run #**_____

Process	**B.P.** (Torr)	**Current** (A)	**Outgas** (A)	**Thickness** (Å)	**Time** (min)	**Rate** (Å /sec)

2. Resist Patterning **Mask** _____ **Temp.**_____ **R.H.**_____**%**

----Resist _____

----Spin @ _____ rpm, _____ sec

----Bake (Temp _____^{o}C, Time ____ min)

----Expose (JBA) Intensity A= _____ mW/cm^2 , B = _____ mW/cm^2

Time _____ sec. C.Vac. _____

----Post Exposure Bake (Temp ____^{o}C, Time ____ min)

----Developer _____ Concentration: _____

Develop @ _____^{o}C [21] , Time _____ min, Buzz _____ min

----Inspect, Comments _____

----Plasma Ash @ 50W, 1Torr, _____ min

----Plasma Etch **Date** __/__/__ **Run #**_____

Gas	**BP** (10^{-5} Torr)	**Flow rate** (ccm)	**Gas Pres.** (mT)	**Power** (W)	**V_{bias}** (V)	**Time** (min)	**End-point** @ (min)
SF_6		11.2					

----Sputter Clean **System:**_____ **Date** __/__/__ **Run #**_____

Process	**B.P.***10^{-7} (Torr)	**Position**	**Shutter**	**Ar Pr** (mT)	**Power** (W)	**Voltage** (V)	**Tuning** C_L/C_T	**Time** (min)
Sputter								

Thickness Measurements:

	(0,0)	**Left**	**Right**	**Top**	**Bot**
Resist					
Post Etch					
Thickness Change					
Rate					

Figure 22. Generic Etch Process Sheet

Material	Etchant	Recipe	Wafer #	Rate A/min)
Ti	SF6	30 W, 25 mTorr	TiPb3	338
Ti	SF6	50W, 25 mTorr	TiPb2	437
Ti	Ar	Nb sys, 150 W, 9.5 mTorr		15
Ag	Ar	Xfer, 100 W, 10 mTorr	VJAg01	250
Ag	Ar	Xfer, 100 W, 20 mTorr	VJAg01	300
Ag	Ar	Pb sys, 100 W, 15 mTorr	VJAg01	62
Ag	Ar	Pb sys, 150 W, 10 mTorr	VJAg02	62
Ag	Ar	Nb sys, 150 W, 10 mTorr	VJAg02	222
Ag	HNO3 (20%)	1:5 (DI)	VJAg01	No etch
Oxid. Ag	Ar	Xfer, 100 W, 10 mTorr	VJAg01	100
Si wafer	Ar	Xfer, 100 W, 10 mTorr	VJAg01	60
α:Si	Ar	Nb sys, 150 W, 10 mTorr	VjaSi01	86
α:Si	Ar	Xfer, 100 W, 20 mTorr	VjaSi01	98
Cr	Ar	Nb sys, 150 W, 10 mTorr	CrPb3	33
Pt	Ar	Nb sys, 100 W, 10 mTorr	VJPt01	78
Pt	Ar	Nb sys, 150 W, 10 mTorr	VJPt01	87
Pt	SF6	30 W, 25 mTorr	VJPt01	10
Pt	SF6	50W, 25 mTorr	VJPt01	35
CuOx	Ar	Xfer, 100 W, 10 mTorr	CuOx01	117
S1813	SF6	30W, 25 mTorr	CrPb1	910
S1813	SF6	50W, 25 mTorr	TiPb2	910
UVN-30	O2	50 W, 1torr	CuOx01	274
PMMA (6%, 2500 rpm)	SF6	30W, 25 mTorr	CrPb1	2304
PMMA (6%, 2500 rpm)	SF6	50W, 25 mTorr	CrPb1	1478
PMMA (6%, 2500 rpm)	O2	50 W, 1torr	TiPb3	148
PMMA (6%, 8000 rpm)	O2	50 W, 1torr	TiPb3	383
PMMA (6%, 10000 rpm)	O2	50 W, 1torr	TiPb3	300
PMMA (6%, 3000 rpm)	Ar	Xfer, 100 W, 10 mTorr	CuOx01	170

Table 2. Etch rate test results.

Copper, Niobium and Quartz Deposition Rates

Characterization of thin films is a long multi-step process, so it is achieved by acquiring a minimum of points, sufficient to provide a qualitative relation of parameters. The idea is to establish a process that will yield reproducible film characteristics even in the presence of small, inevitable fluctuations in the growth process. Cu films for this project were exclusively grown on the IBM system with a D.C. magnetron sputter gun using a fresh copper target. The chosen sputtering gas pressure for these depositions was selected from previous known parameters used by other systems in which thin films of Cu were previously studied. We sputtered these copper films at a base pressure in the low 10^{-7} torr range, with a dynamic Ar pressure of 10 mtorr. The tests were performed at such pressure despite the fact that the deposition chamber is been observed to reach pressures in the mid 10^{-8} torr, yet those pressures require optimal conditions that are not always attainable during normal processing. In a single characterization run, a wafer would be patterned with photo resist of sufficient thickness (for example 5000 Å), loaded in the transfer chamber and upon reaching the necessary pressure, the wafer would be transferred to the deposition chamber. There, a particular power setting is selected using the DC power supply and a short time measured in minutes is selected for the test. Upon retrieval of the wafer, the photo resist is removed from the wafer and a profiler step-height scan is performed on the deposited Cu. The test is repeated several times with increasing power and fixed Ar gas pressure until we get a good idea of a linear relation between pressure and power for this process. The following figure shows the collected points during this characterization.

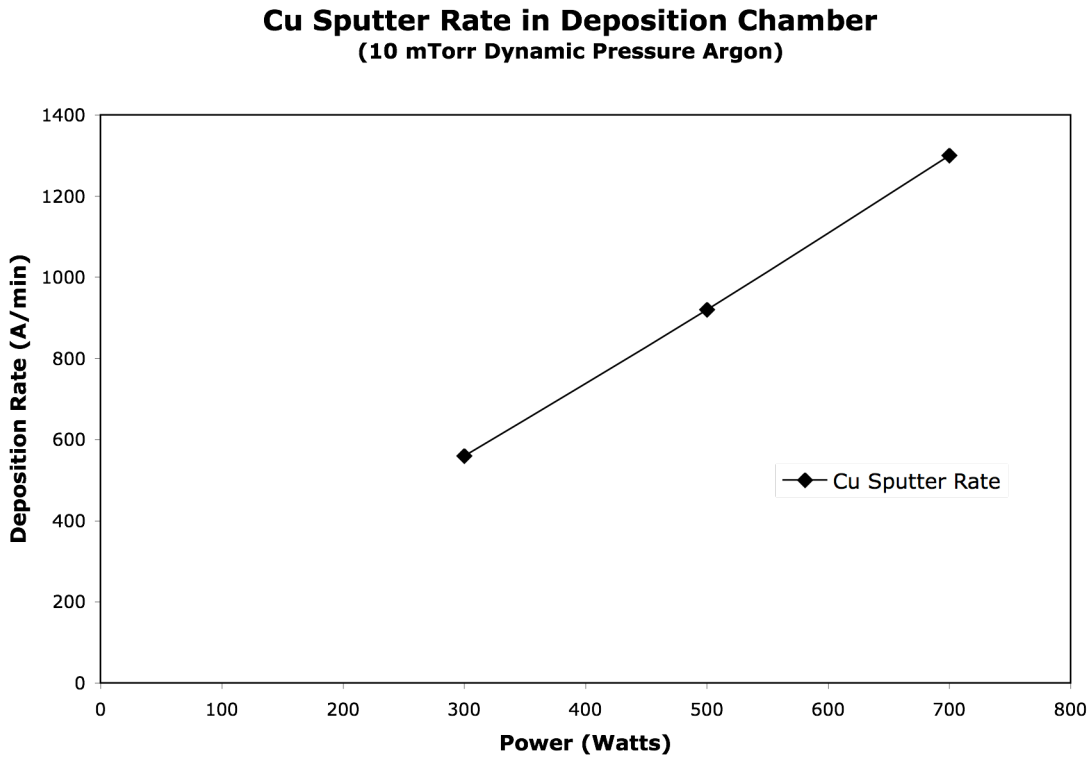


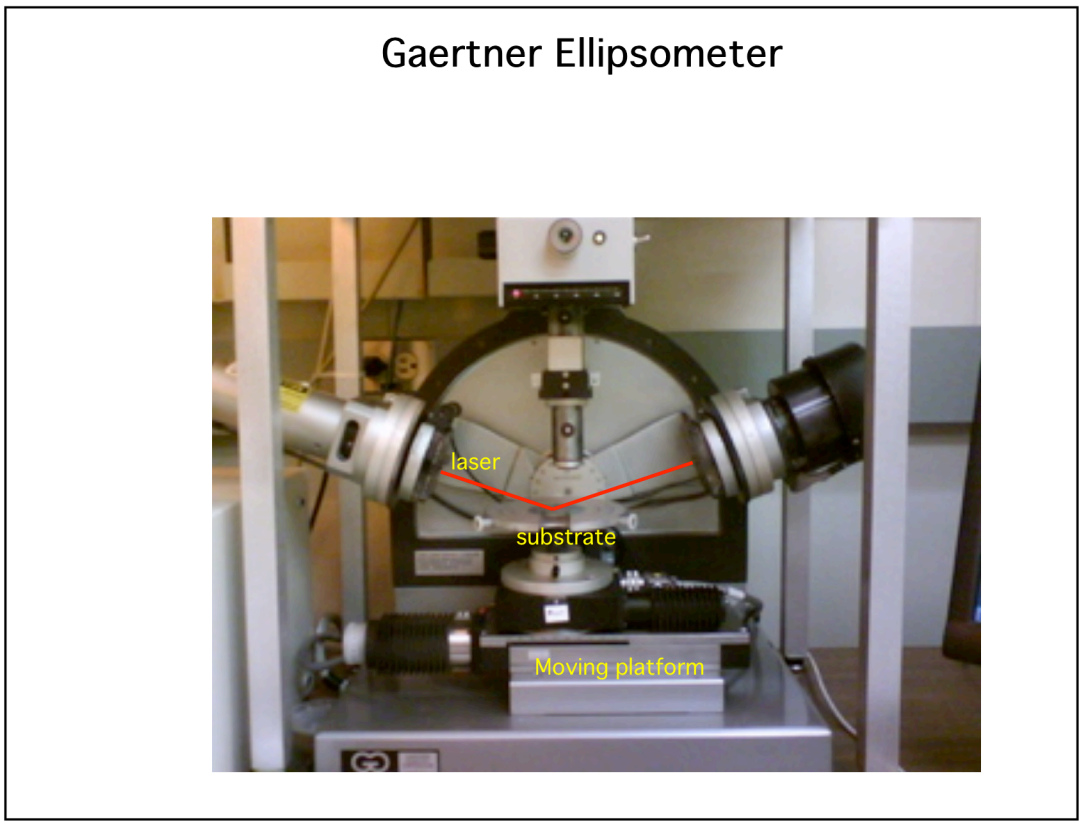
Figure 23. Cu sputter deposition rate in IBM system.

From these results it was decided to continue using the following parameters for device fabrication, 500 W, 10 mtorr for a deposition rate of approximately 1000 Å/min. Usual thickness for Cu films were between 1000 Å and 1500 Å. The Nb film characterization was carried in the same way as in Cu. Following the sputter deposition parameters used in another active system, the Nb system, for 700W and 10 mtorr dynamic pressure for a resulting 500 Å/min rate was achieved. These parameters were reproduced for the rest of the fabrication of devices. The usual thickness of Nb films ranged between 1000 Å and 1500 Å.

In the case of quartz films, a characterization run after the target was removed from cleaning in the SiO_2 system was performed. The sputtering gun had a lot of quartz deposits that were removed, and silver paste was applied between the target and the gun to ensure proper cooling of the target during sputtering. The variation in thermal conductivity for the cooling process also varies the sputtering rate for quartz, resulting in a lower deposition rate for the quartz films, as more energy is required in the process.

The characterization of quartz deposition rate was carried using ellipsometry which is a method used to characterize the optical constants and thickness of thin films. Ellipsometers are sensitive to several material characteristics such as layer thickness, optical constants (refractive index and extinction coefficient), surface roughness, composition and optical anisotropy (directional dependence), etc. The three types of data typically acquired with the ellipsometer are transmission, reflection and ellipsometry [12]. The ellipsometer used for these measurements was a Gaertner Scientific Corp. Model L115C, and the results yielded the expected target thicknesses. Parameters for these films settled at 400 W and 2.5 mtorr for a deposition rate of approximately 180

Å/min. Usual films thickness grown with this system were between 1000 Å and 2000 Å. The following picture shows the ellipsometry instrument.



Picture 18. Gaertner ellipsometer.

Stress Calibration of Nb Films in IBM System

This calibration was performed as a result of anomalies in the fabrication of Cr/Cu:CuOx/Nb devices. As one of the early steps of this fabrication process, a 1000 Å layer of Nb is sputtered over a layer of oxidized Cu, and further processed into individual devices. The deposited films presented pealing during later stages of processing, which suggested that the films could be under stress. There are two kinds of stress for a deposited film, tensile and compressive, and its presence reveals information about the deposition process. The level of stress in a film can be determined by the resulting concave or convex curvature in the substrate. The basic physical behavior in question can be described by the stress-strain curve, where the force applied per unit cross-sectional area is the stress, σ (N/m^2 or Pa), tensile being positive and compressive negative. The fractional amount by which stress causes a material to stretch along a particular direction is called strain, and is defined by $\varepsilon_x = \Delta x / x$. This stress-strain relation behaves linearly up to the "yield point" where the deviation from linearity reaches 0.2% and the material is no longer considered elastic. The slope resulting from the elastic region is given by $\sigma_x = Y\varepsilon_x$. The following figure shows this relationship [5].

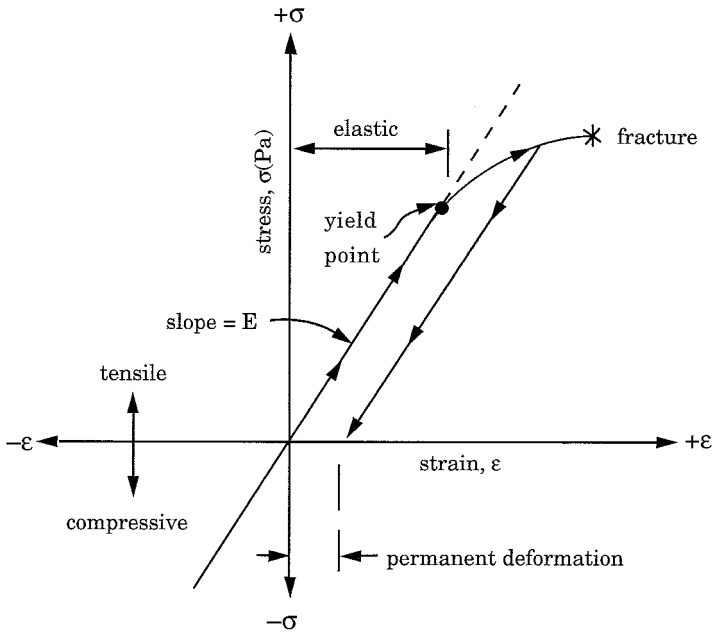
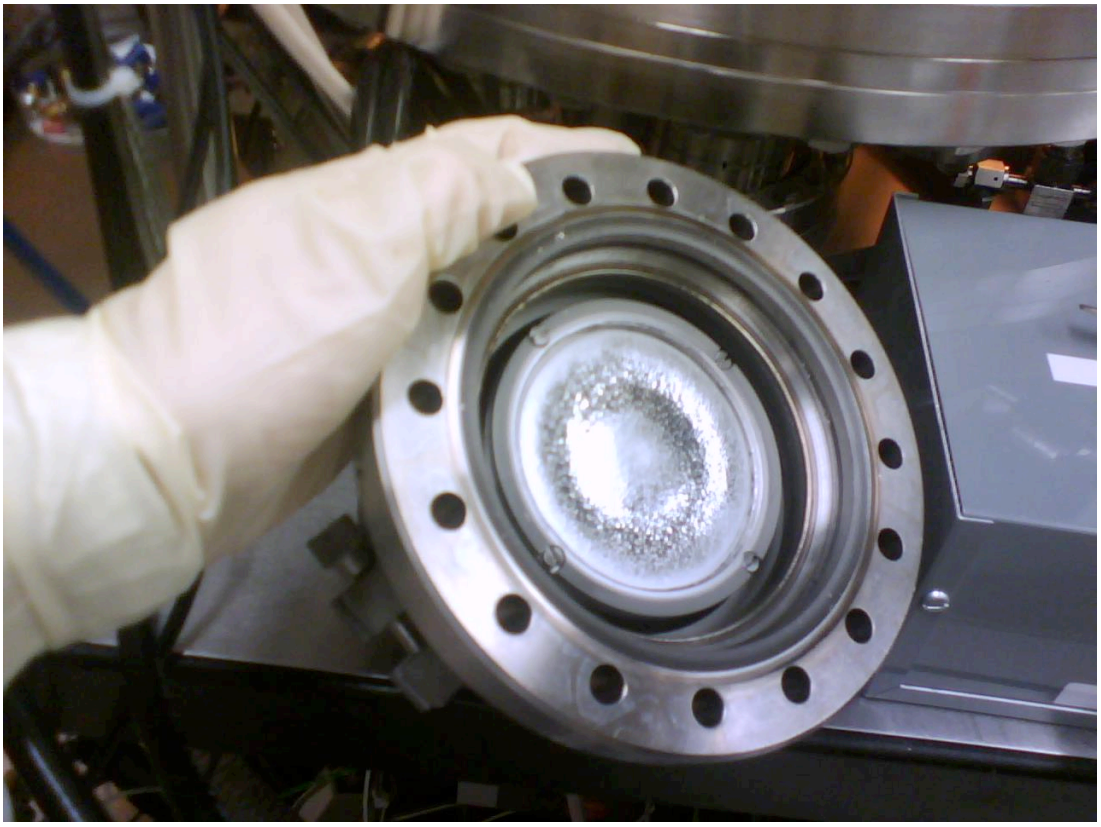


Figure 24. Characteristics of the stress-strain relationship [5].

The stress calibration was performed as a function of the pressure during the sputter deposition. Along the point of no stress the slope behaves in a linear fashion and this allows one to find a minimum stress pressure for a particular target, in this case Nb. As a target erodes due to repeated ion bombardment, the point of no stress on a film deposition is shifted from its original calibration parameters, and this occurs with an increasing rate as the target becomes more eroded over time. The following picture shows the actual Nb target we used and its erosion tracks.

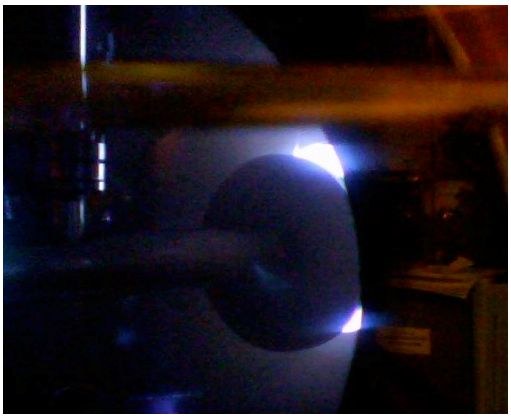


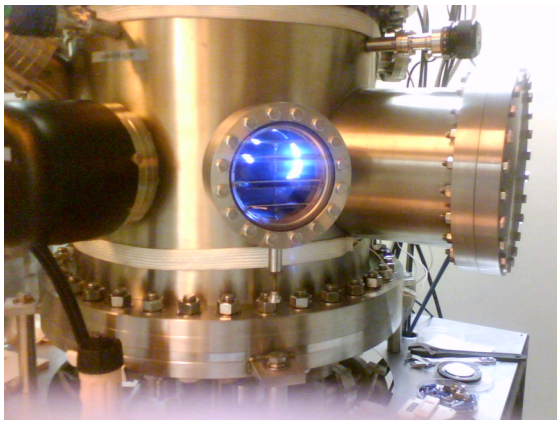
Picture 19. Eroded Nb target in D.C. Magnetron Gun. Notice the concentric erosion ring resulting from the magnetic field configuration of the gun.

The instrument used to perform these calibrations was a KLA-Tencor P-10 Surface Profiler, on the stress calibration mode [11]. For this process a bare silicon wafer is pre-scanned carefully for surface conditions in a two-dimensional grid in order to acquire a good characterization of its original surface characteristics. Then a few hundred nanometers of niobium are deposited on the wafer and a post-scan is performed to observe the surface changes due to the film's stress. There were a total of three scans spread along the x direction of the wafer's surface and three along the y direction. Each one of the six surface scans is saved as an individual file and is matched with individual post-deposition scans, performed on the exact same positions along the wafer. The test

deposition is repeated by varying the pressure while keeping the rest of the parameters fixed, and this is done enough times to get a slope along the no-stress region.

For the first few device fabrication runs we were using an Ar dynamic pressure of 10 mtorr. The results of the stress calibration showed that the Nb films were under considerable tensile stress and the pressure was hence corrected to a lower pressure of just 7.5 mtorr. The problems observed on these Nb films were corrected by the calibration. The following images show an Ar sputter deposition of Nb in the IBM system and the plot shows the calibration results for this process.





Picture 20 & Picture 21. Left: Close-up of substrate holder and Ar plasma in IBM system. Right: Ar sputter deposition of Nb in IBM system, notice the Cu D.C. magnetron gun directly opposite to the Nb gun's position.

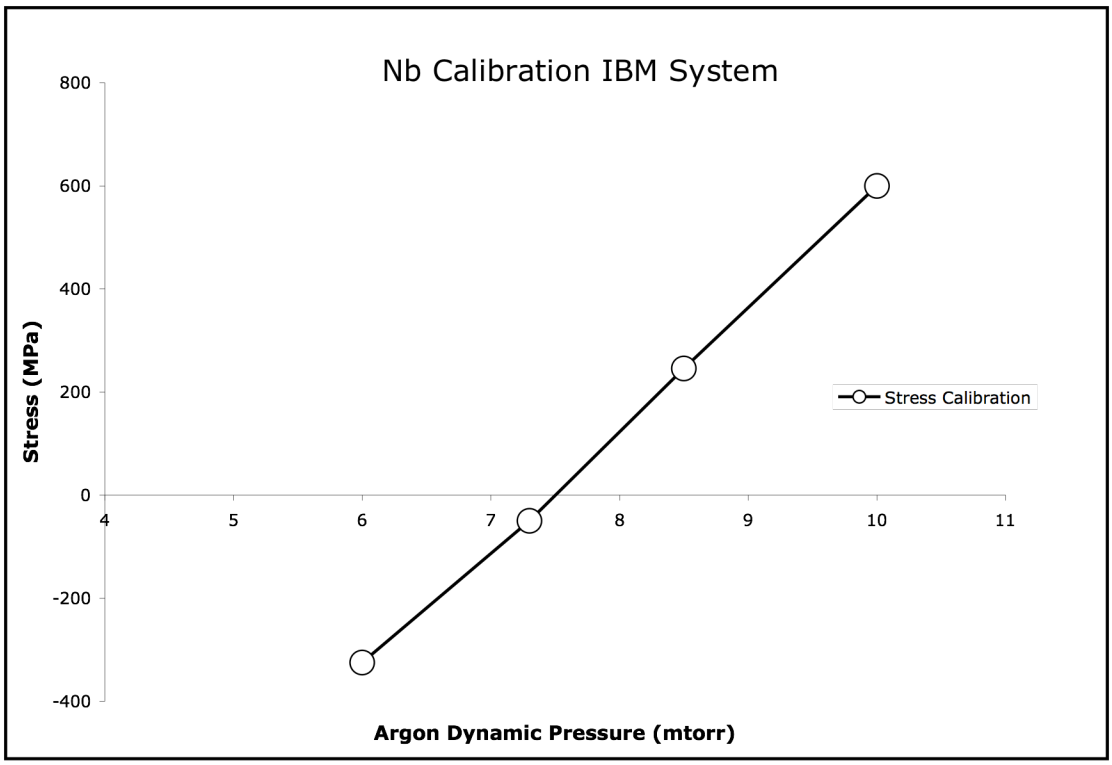


Figure 25. Nb Stress Calibration in IBM System.

Plasma Oxidation of Copper and Titanium Films.

The characterization of these plasma oxidations was performed in two different systems. The Cu tests were done in the IBM system, while the Ti ones were done in the Pb system. In both cases we used an r.f. plasma for the oxidation, and a base chamber pressure in the mid 10^{-7} torr was use. It was for this process step that we installed the O_2 line in the transfer chamber of the IBM system, which previously only had Ar backsputtering capabilities. The Pb system had existing Ar and O_2 lines, but the gas delivery configuration had to be modified, and substrate holder modifications were necessary for the glow discharge processes to be carried in that system. In the case of normal thermal oxidation, the thickness change of the films is negligible and would require an atomic force microscope to characterize it. It is for that reason that we used intense oxidation conditions to generate films thick enough to be measurable with a profilometer.

This characterization process entails the patterning of the freshly deposited material and subsequent oxidation using specific relations between power and pressure for the oxygen plasma. A dynamic Ar pressure of 10 mtorr was used for both system's tests, while the power and time duration of the oxidation process varied. After oxidation the wafer is striped of the resist and the thickness variation on the material is measured with a surface profiler. The target thickness needed for the memory is of a few nanometers. Some examples of the different designs are explained in the process development chapter of this work. The following figure shows a typical oxidation characterization process.

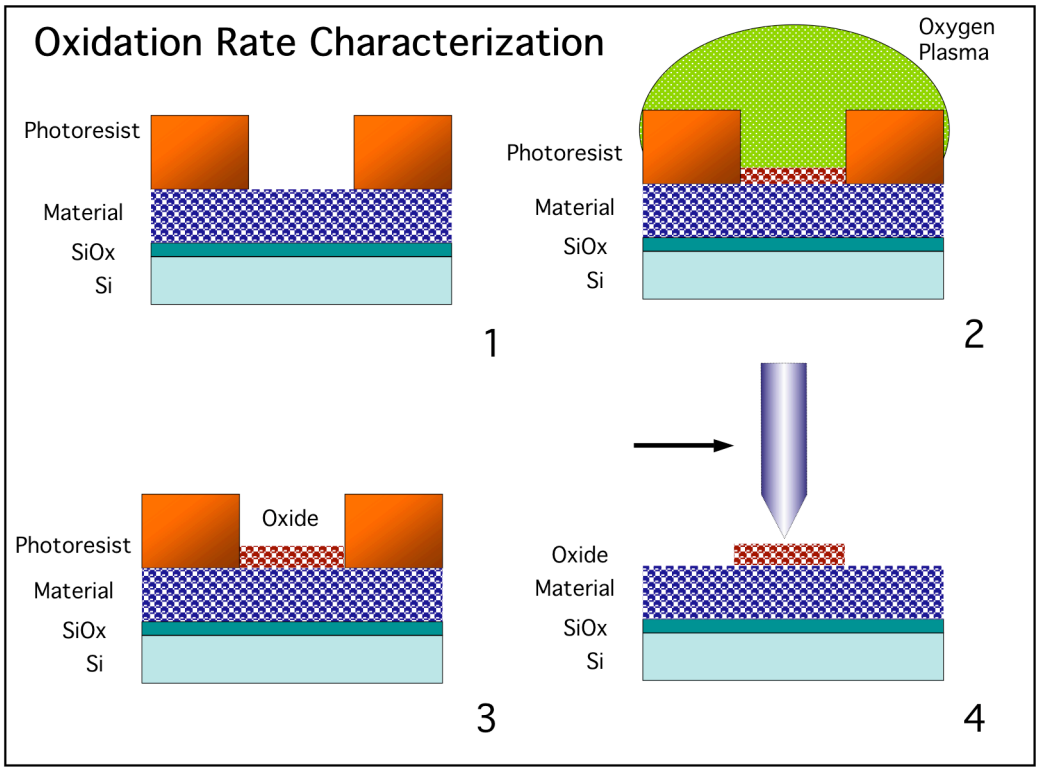


Figure 26. Process steps 1-4 in characterization of plasma oxidation of thin films. For example, a 3 minute, 300 W, 10 mtorr Cu oxidation in the IBM system would yield ~ 50 Å thick oxides.

Electron Beam Evaporation of Cr, Ti, Pt, α:Si, Ag

The characterization of thin films by *e*-beam evaporation is a straightforward process, consisting of ratifying the growth rates as acquired by an XTC Film Thickness and Rate Monitor. The XTC uses a quartz crystal as a sensor to monitor the amount of material deposited on its surface. Quartz is a piezoelectric material and is widely used for its accuracy in maintaining very stable frequencies. The instrument sets a particular frequency on the crystal and monitors the frequency change as the mass deposited on the surface of the crystal leads to a change in the frequency read by the instrument, with a thickness display resolution of one Å. There are three main parameters that need to be identified to ensure the proper reading for the deposition rate of a particular material; the bulk density of the material, the Z-ratio and the tooling factor. All three parameters can be determined experimentally with this instrument, yet the first two are easily acquired from various sources as well as the operation manual of the XTC. The tooling factor had to be calibrated in order to ensure an accurate reading from the crystal monitor.

For films exceeding a few hundred Å, an uncertainty of ± a few decades is well within the accepted error of 5% to 10% depending on the process. Yet some of the processes required very thin films, as thin as just a few monolayers as in the case of Cr, where 20 Å was deposited and the case of Ti, where as little as 15 Å were evaporated onto a substrate.

In order to perform a tooling calibration, a substrate is placed in the substrate holder of the system and a short deposition is made. From this deposition we can

determine the actual thickness using a surface profiler and then use the following relation to obtain the tooling factor [13],

$$Tooling(\%) = TF_I \times \frac{T_M}{T_X}$$

where

T_M = Actual thickness at substrate holder

T_X = Thickness reading in the XTC

TF_I = Initial tooling factor

The resulting percentage is rounded off to the nearest %, and the new value is entered in the XTC. If the calibration is done correctly, T_M and T_X will be equal, which was the obtained result from our calibration.

Typical evaporation rates in Pb system using *e*-beam evaporation are of 0.5 Å /s for most processes, and can range between 0.5-1 Å/s for thicker films like the Ti counter-electrode which is 750 Å. In the case of the Ti:TiOx interface, it would start at a low Ti deposition rate on top of the freshly grown TiOx and after reaching 100-200 Å, the rate can be slightly increased. The relevance of that particular thickness is explained in the fabrication process chapter. Such low deposition rates are important for the quality of the evaporated films as they help ensure single atom deposition for smooth monolayer growth. Larger evaporation rates cause clusters of atoms to be deposited on the surface of the substrate, resulting in very uneven films. Such film defects would result in poor yield and decreased, or non-present functionality of devices.

III. Fabrication Processes

There were three particular device configurations that were developed and studied for the CMOL project during the time of my participation in this research: Cr/Cu/CuOx/Nb, P-Si/α:Si/Ag and Cr/Pt/TiOx/Ti. These were two terminal devices with the following characteristics: metal/ insulator/ metal. As explained before, these are CMOS compatible non-volatile resistance switching memory devices, intended for ultra-high density memory. The switching occurs between an off (high resistance) and an on (low resistance) state, and as a result of a metal filament formation (or retraction) between the two metal layers sandwiching the insulator. The insulator acts as a diffusive matrix for the metal filament, and the switching is accomplished by applying a positive or negative threshold voltage to obtain the on/off states of the device. Previous research has shown excellent scalability from large micron-sized devices down to sub-100 nm scale, high on/off ratio (10^3) and low power consumption to name a few [14].

In order to gather statistics, it is desirable to fabricate as many devices as possible in every processed wafer. We fabricated devices of three different sizes: 300μm×300 μm, 30μm × 30 μm and 3μm × 3 μm, with the intention of studying the scalability of their characteristics. There are six devices of each size in every chip and a total of 57 chips in every processed wafer. The processing of a wafer refers to a multilayer fabrication process involving the methods described so far in previous sections, i.e. thin film deposition, photolithography, etching and backsputtering. Details of the fabrication for the different types of devices will be presented later in this section.

Since the purpose of these devices is exclusively to extract parameters and statistics, the architecture of the chips is aimed to provide easy connections to individual devices. Every device is fabricated on two large, individual electrode bonding pads, and every chip has four larger common base electrodes. The chips have a square surface area, and the devices are layered along the four sides of the chip. The only other features in the chip are its position number on the wafer, and the mask aligning marks of which there are three. These marks are used for fine mask alignment between photolithographic steps. Each of the three quartz masks, has a printed pattern on its surface corresponding to a different step of the fabrication. The masks are named: Base Electrode (M2), Junction Patterning (M3) and Wiring Layer (M4).

The next sections will present sequentially the step by step processes involved in the fabrication of a single wafer, followed by graphical descriptions of the fabrication steps. The "process sheets" used to document the specific parameters and characteristics of the processes are included in appendix A, with data corresponding to one particular fabrication run. The following figures show the device characteristics, the chip's design and the wafer layout.

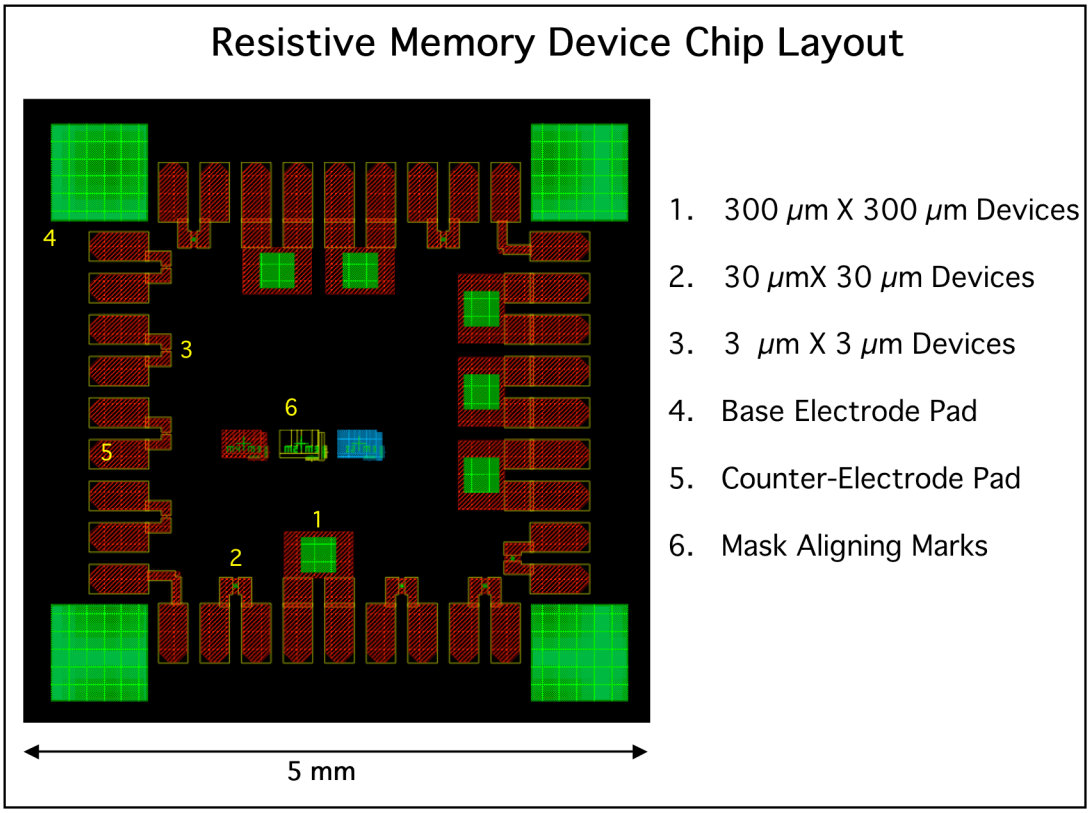


Figure 27. Resistive Memory Device Chip Layout. There is a total of eighteen devices per chip.

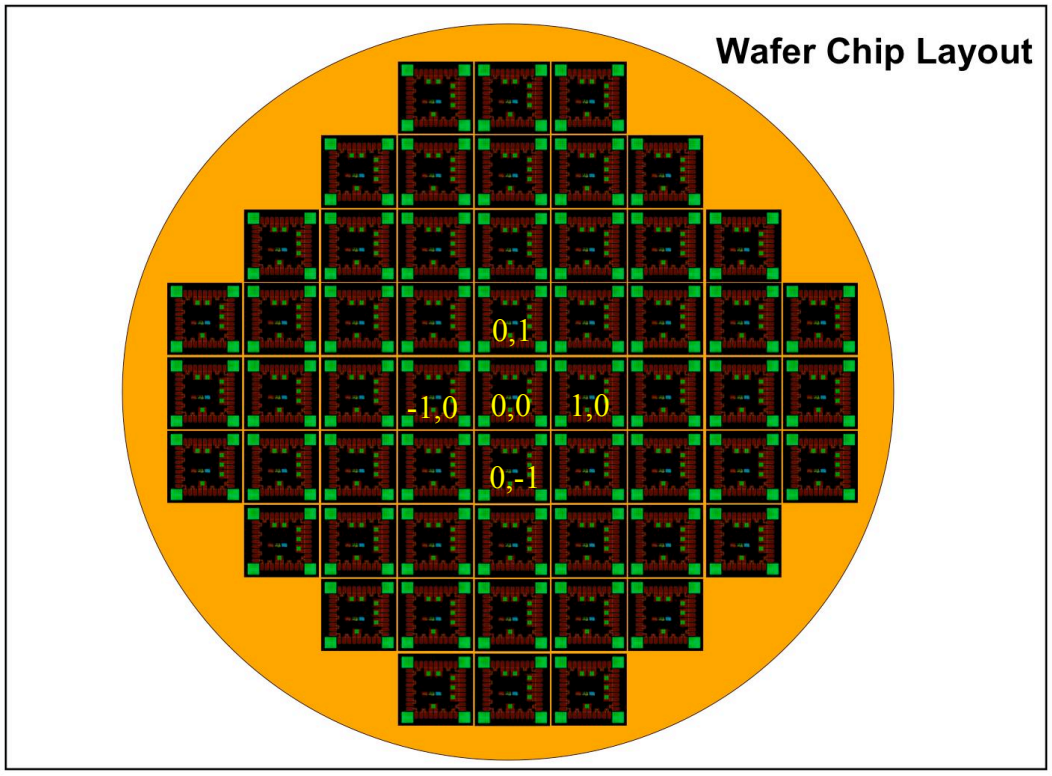


Figure 28. Wafer's Chip Layout and numbering system for 2" wafers. There is a total of fifty seven chips per wafer.

Cr/Cu/CuOx/Nb Device Fabrication Process

In this and subsequent sections is detailed the fabrication steps followed in the processing of a single wafer. There were numerous changes to the fabrication process determined from experimental results and aimed to accomplish or improve fabrication steps.

The first fabrication process will be explained in detail, paying close attention to every step of the fabrication, including the system and method utilized. That will be omitted from subsequent device fabrication processes, such as the manipulation of wafers in the IBM system, etc.

Most devices we fabricated were single oxide layer devices, yet we also studied multilayer oxidation were we would deposit 15 Å of Cu or Ti and oxidize all the way through. We fabricated five and ten oxide layer devices for both Cu and Ti wafers, besides the single oxide layer devices. Another variation we tried was evaporating TiO_x instead of evaporating Ti and then oxidizing it in situ, but this approach yielded poor results and was discontinued.

The process begins by selecting an oxidized silicon wafer, as mentioned before we use 2", 280μm thick wafers. The wafer is mounted on a substrate holder, cleaned with pressurized N_2 gas and loaded in the Pb system for a surface backsputter cleaning with Ar gas and *e*-beam evaporation of a 50 Å thick layer of Cr. The Cr layer is required to improve the level of adhesion of the Cu layer to the substrate. Typical pumping time for this system is about four hours and the LN_2 trap for the diffusion pump needs to be refilled every two hours, base pressures for these processes are in the mid 10^{-7} torr. The Ar backsputtering will clean the surface of the wafer by removing about 200 Å in 2

minutes. The Ar plasma is run with a dynamic pressure of 10 mtorr, so after the backsputter it is necessary to wait a period of time for the system to pump down to the right pressure for the deposition step, where the Cr layer is then deposited on a freshly cleaned surface. The wafer is then loaded on the transfer (Xfer) chamber of the IBM system for a trilayer sputter deposition of $Cu/CuO_x/Nb$. The substrate is ready to be transferred to the deposition chamber at a pressure starting in the low 10^{-6} torr. The wafer in taken from the translating sample cart by means of remote manipulation arms and placed on one of the two stations of the rotary substrate stage in the deposition chamber. In order to ensure the purity of the Cu to be sputtered, there is a pre-sputtering run of 40 seconds to clean the target's surface and then 1500 Å of Cu is deposited on the substrate. At this point the substrate is taken back to the Xfer chamber for a 3-minute plasma oxidation of the freshly deposited Cu, without breaking the vacuum during this process. This oxidation should produce approximately 50 Å of CuO_x on the surface, constituting the insulating layer for the device. Finally, the substrate is taken back to the deposition chamber for sputter deposition of 1000 Å of Nb, thus concluding the trilayer deposition in the IBM system. At this point there is a uniform multilayer on the wafer with the following dimensions: Cr (50 Å)/ Cu (1500 Å)/ CuO_x (50 Å)/ Nb (1000 Å).

For the base electrode patterning, we perform the first photolithographic process on this wafer by spin coating 10000 Å of photo resist (PMMA 6%) on the surface, followed by a 5-minute bake at 140 C and subsequent exposure to dUV light in the JBA mask aligner. The mask used for this step contains only the counter electrode pads seen in figure 26, indexed by the number 5. PMMA requires a long exposure time (≥ 15min) and is a positive photo resist so the areas exposed to the dUV light are fixed to the surface of

the wafer and the areas corresponding to the base electrode pads are eliminated, leaving a patterned bare Nb surface. Developing for PMMA is about a minute and is done with 1:1 solution of MIBK developer and isopropyl alcohol (IPA), adding to the developing time some ultrasonic buzz to ensure maximum elimination of photo resist from the surface. The wafer is then examined under the microscope to look for possible defects in the pattern, since it could have been under or over developed depending on factors like time and/or strength of the developer. A post developing "plasma ash" (O_2 plasma clean), is performed to remove any remaining photo resist from the surface of the wafer, and a thickness measurement is taken. The thickness measurements are performed with a profilometer at symmetrically opposite points across the wafer including the center. This process is illustrated in figure 19. The surface is prepared for RIE with a phosphoric acid bath right before being loaded in the RIE system. The photo resist used in this process needs to be sufficiently thick since two different plasma etch processes will get rid of ~2500 Å of material (the trilayer) in the following steps.

Nb is etched in the RIE system using SF6 gas. The matching network for the r.f. system has been tuned to the desired parameters previous to loading the wafer in the chamber; it is a necessary step in this system since this matching network can only be set manually. The process is monitored with a gas analyzer allowing us to track the gas species present in the chamber during the etch, thus ensuring the right conditions for the process. After this etch there is CuO_x exposed in the surface of the clear pattern, which will be removed together with the remaining Cu and Cr, by Ar backsputtering in the IBM system. The next step is to strip the photo resist from the surface; this is accomplished by soaking the wafer in an acetone bath for several minutes followed by an ultrasonic buzz.

A plasma ash is performed to ensure all photo resist is cleared from the surface and a thickness measurement is taken.

The wafer is now ready for junction patterning. The spin coating of photo resist is done following the same steps as the previous photolithographic process, yet this time it is necessary to perform the first mask alignment. The junction patterning mask has the marks for aligning with the patterned marks left in the wafer, as well as new marks that will aid in aligning the next mask to be used. This can be a lengthy and trying process since there are many adjustments to get a proper alignment. The pattern in this mask (M3) contains the different size junctions as well as the base electrode pads. After development of the photo resist, the surface is cleaned with a plasma ash as before, thickness measurements are taken and the phosphoric acid clean is performed. Another RIE is performed at this time in order to remove the Nb layer all the way to the CuO_x layer, which is as mentioned before, an excellent stopper for the Nb etch with SF6.

With the Nb layer gone the wafer is ready for SiO_2 deposition in the SiO_2 system. This is an insulating layer between the final wiring layer and the bottom electrode of the devices. The pumping time for this system is about twenty four hours to reach the deposition base pressure of low 10^{-7} torr. SiO_2 is sputtered with an Ar gas r.f. plasma and it is performed in steps of up to 5 minutes each in order to allow for cooling of the target as well as the substrate. The deposition thickness for this insulator is 1700 Å, and requires a long lift off time, usually overnight soaking in acetone, ultrasonic buzz and mild scrubbing with a q-tip to remove all remains from the surface.

Patterning for the wiring layer is now performed, aligning this third mask (M4) with the marks left on the wafer by the previous one and following the same PMMA spin coating procedure as before. The material used for the wiring layer is 1500 Å of Nb and we sputter it on the IBM system following the loading and sputter procedure described for the trilayer deposition of Cu and Nb. As a final step the photo resist is striped from the wafer and spin coated with an S1813 photo resist layer to protect the surface of the chips. The wafer is then diced with a precision dicing machine and taken for experimental measurements. The following figures show the fabrication steps described above.

Cr/Cu/CuO_x/Nb Device Fabrication Process

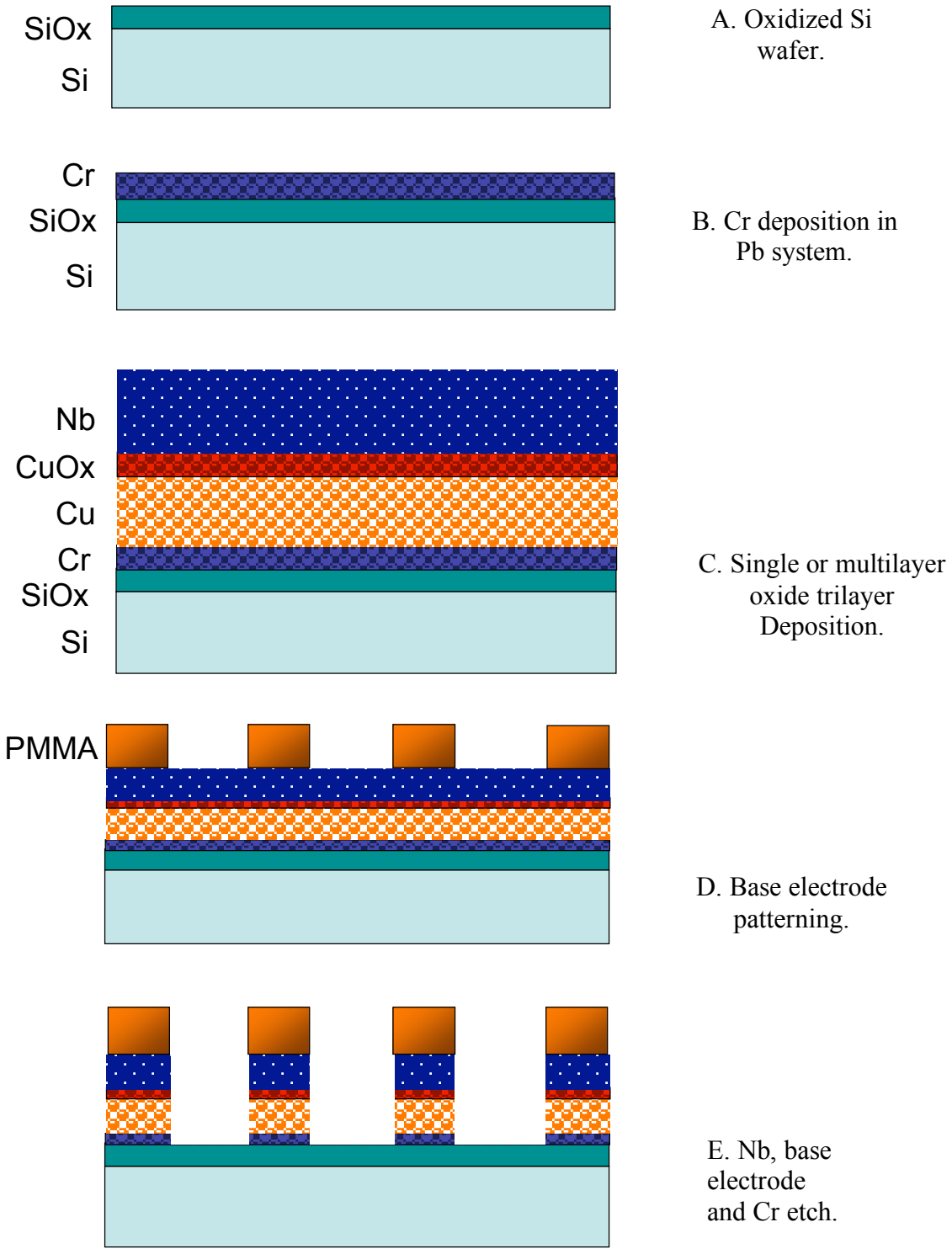
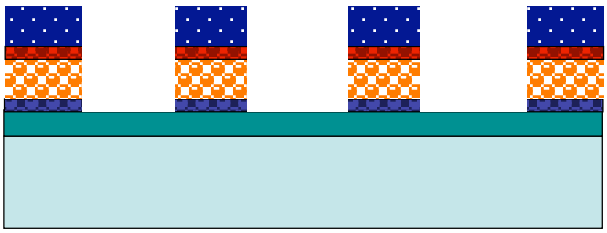
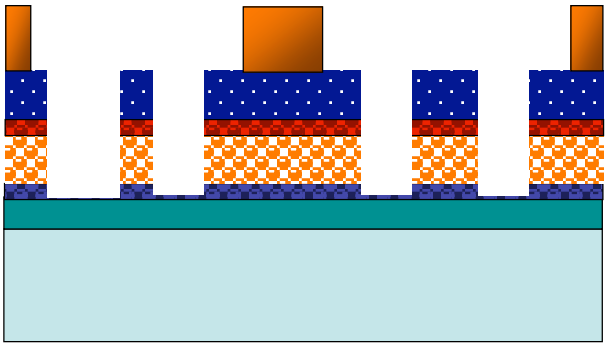


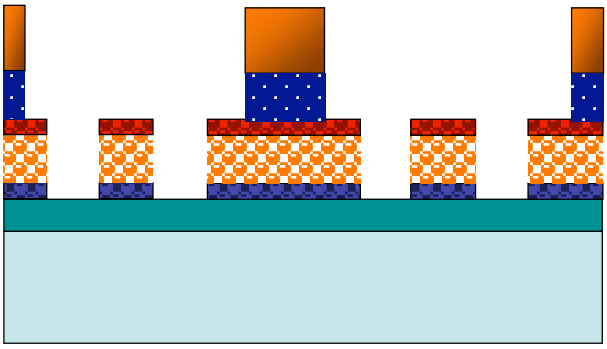
Figure 29. Cr/Cu/CuOx/Nb Device Fabrication Process, steps A-E.



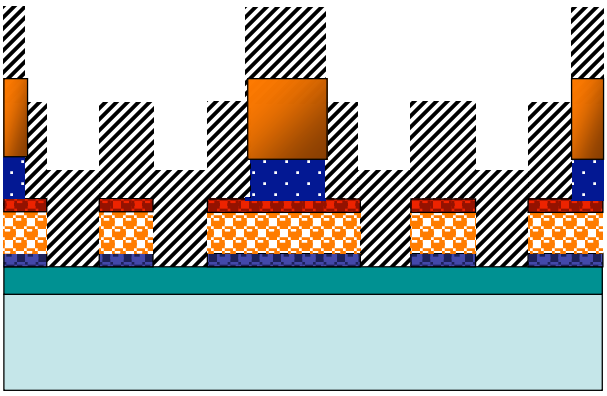
F. Photoresist lift off.



G. Junction Patterning.

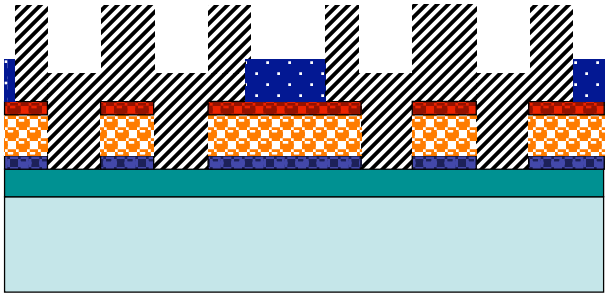


H. Counter electrode RIE etch.

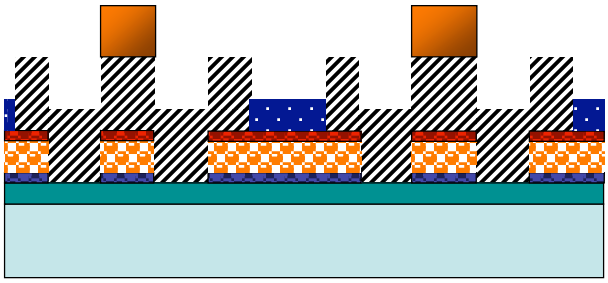


I. Quartz sputter deposition.

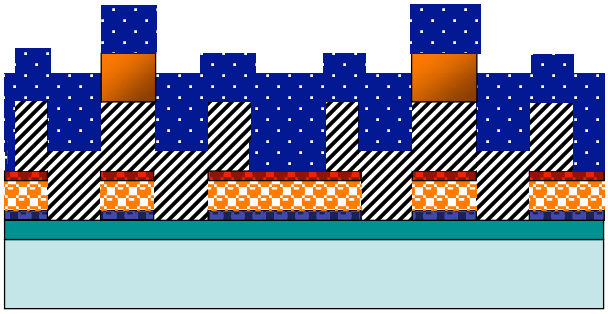
Figure 29 (cont.). Cr/Cu/CuOx/Nb Device Fabrication Process, steps F-I.



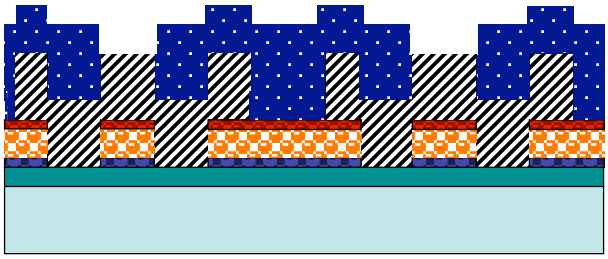
J. Quartz lift off.



K. Wiring layer Patterning.



L. Nb wiring layer deposition.



M. Metal lift off.

Figure 29 (cont.). Cr/Cu/CuOx/Nb Device Fabrication Process, steps J-M.

Cr/Pt/TiOx/Ti Device Fabrication Process.

In this fabrication process we have settled for a different approach from that of the CuOx device wafers. There, we deposited the Cr adhesion layer followed by the trilayer of Cr/Cu/CuO_x/Nb and then we etched away the patterned base electrode pads. In the case of the TiO_x we found experimentally that the Pt base electrode was rather difficult to etch away by the processes we have set up in the lab. Instead, in order to avoid the Pt etch we set up a process with negative resist to cover the regions were Pt would have to be otherwise etched away. We start by depositing 20 Å of evaporated Cr as a protective layer, this layer will work as an etch stop for the RIE Nb etch and is done in the Pb system. Next is the base electrode patterning, yet this time we use a negative resist so that the base electrode area is covered by the photo resist and the rest of the surface exposed. The negative photo resist we use in this step is UVN-30 and we spin coat about 6000 Å. Earlier fabrication runs presented problems at the time of base electrode lift off, so before the UVN-30 coat we apply a few hundred angstroms of PMMA to facilitate the lift off process. Unlike PMMA's long exposure time, UVN-30 takes only 4.5 seconds under the dUV light. Development is carried with full strength Microposit CD-26, followed by several 2-minute long plasma ashes to completely remove the photo resist from the wafer. The repeated O_2 plasma cleaning is necessary due to the very low etch rate presented by UVN-30 during characterization runs. Once all the photo resist has been removed, thickness measurements are performed and the wafer is loaded back on the Pb system for the base metal deposition.

Once the base pressure is reached in the chamber, we do an Ar backsputter for thirty seconds to clean the surface and continue to deposit 50 Å of Cr and 1000 Å of Pt. The wafer is the taken for lift off, plasma ashing and thickness measurements. At this point we have a continuous base electrode film of Pt, and a clear counter electrode pattern, is time for the oxide barrier and counter electrode metal deposition.

The wafer is loaded on the Pb system where a backsputter is performed to clean the surface, followed by the multilayer process resulting in the TiO_x barrier. A multilayer oxidation in the Pb system is a long process since both the evaporation of Ti and the oxygen plasma are performed in the same chamber, so the system needs to be allowed to pump the chamber back to the right base pressure before being able to evaporate another layer of Ti. The thickness of evaporated Ti per layer is only 15 Å, with a ten-minute oxidation per layer. In the process sheet for this fabrication run data was recorded for ten layers of TiO_x. Finally a 750 Å layer of Ti is evaporated, constituting the counter electrode. The wafer is then ready for junction patterning with PMMA, where after developing the photo resist we perform the typical plasma ash and thickness measurements.

The next step is to etch the exposed Ti in the RIE system. This etch will eliminate the Ti as well as the TiO_x all the way to the protective layer of Cr in the base electrode area and Pt in the rest of the wafer. After the etch, the wafer is translated to the Pb system to remove the protective Cr layer by a thirty-second Ar backsputter. Then a 1700 Å layer of SiO_2 is deposited to insulate the junctions and the wafer is left overnight for lift off in an acetone bath, followed by ultrasonic buzz, plasma ash and thickness measurements. The final steps are the wiring layer patterning with PMMA photo resist in the same

fashion as before and deposition of 1500 Å of Nb in the IBM system. After lift off from the Nb deposition the chips are inspected under the microscope on last time and a spin coat of S1813 photo resist is applied on the surface to protect the wafer. The following figures show the fabrication steps described above.

Cr/Pt/TiOx/Ti Device Fabrication Process

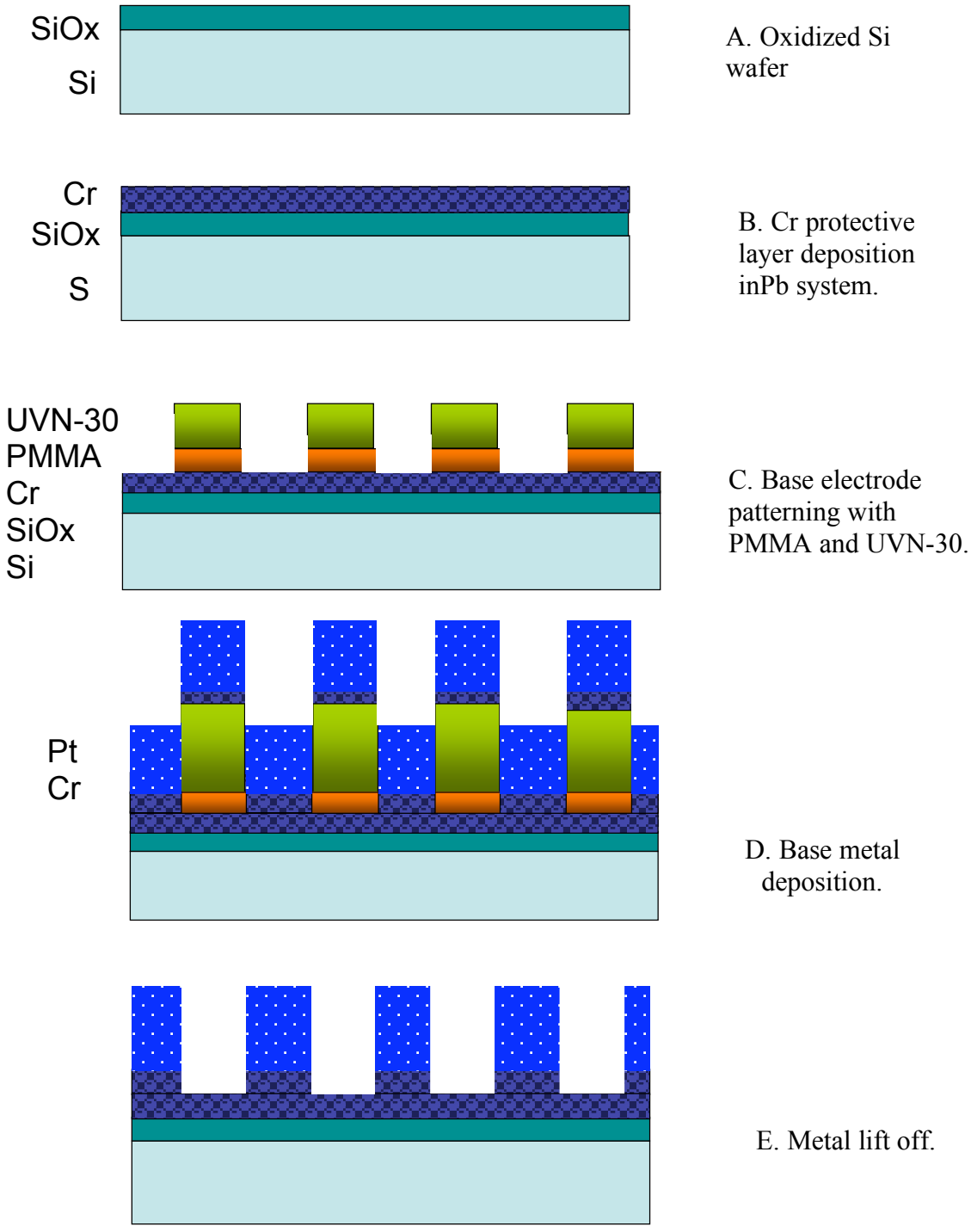
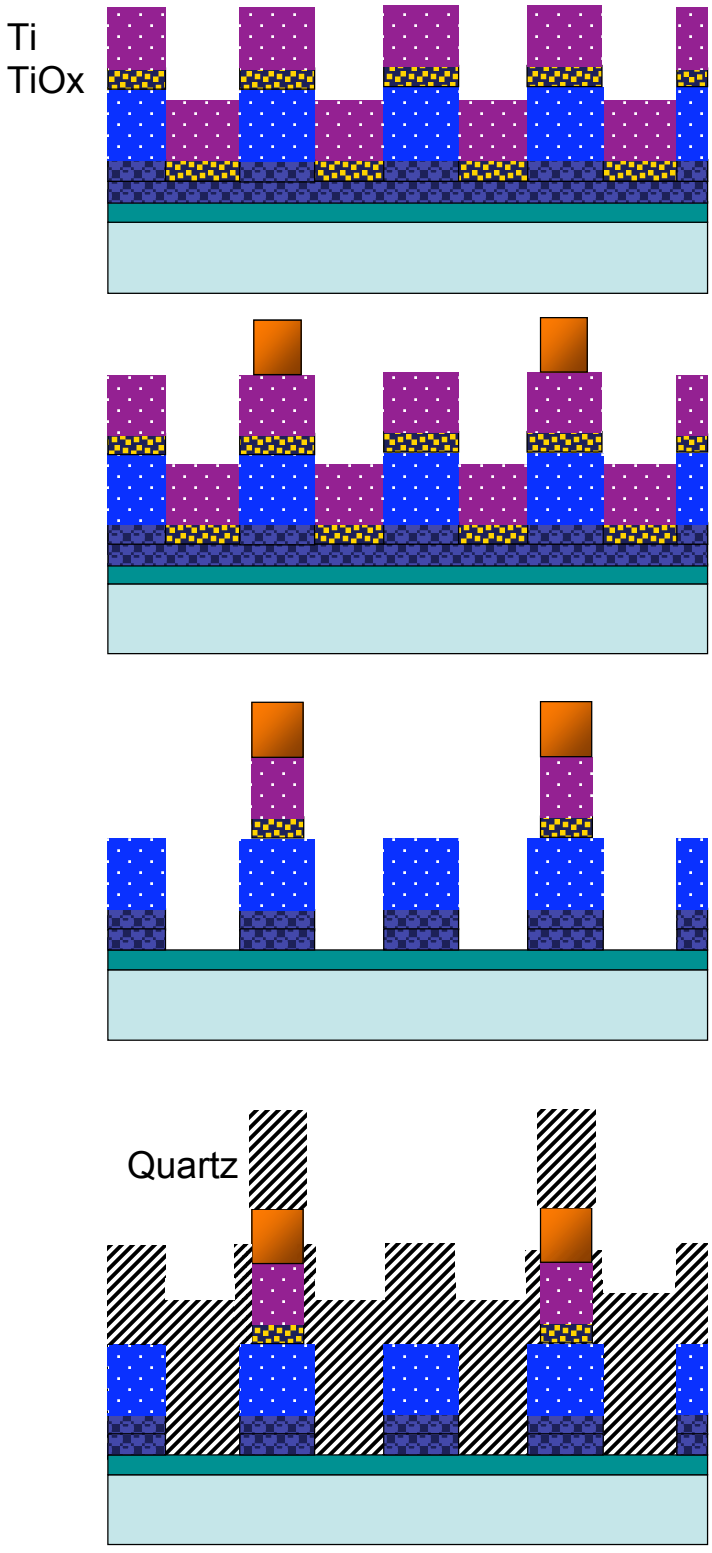


Figure 30. Cr/Pt/TiO_x/Ti/ Device Fabrication Process, steps A-E.



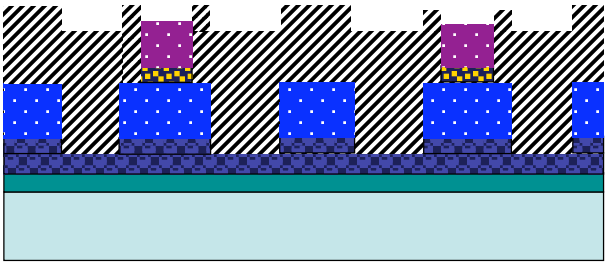
F. Barrier and metal deposition.

G. Junction Patterning.

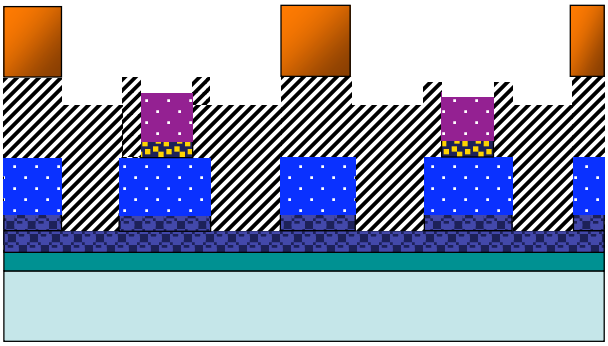
H. Counter electrode RIE etch.

I. Quartz sputter deposition.

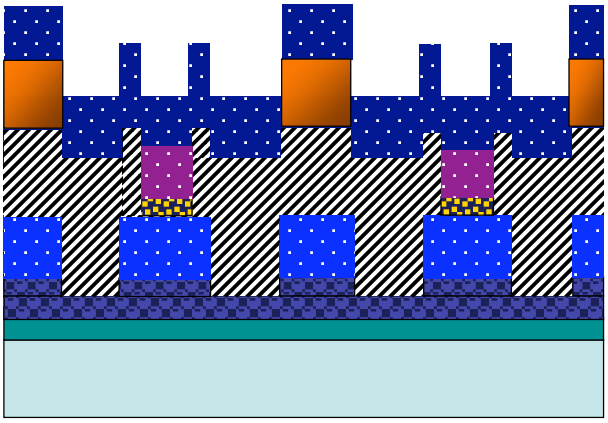
Figure 30(cont.). Cr/Pt/TiO_x/Ti Device Fabrication Process, steps F-I.



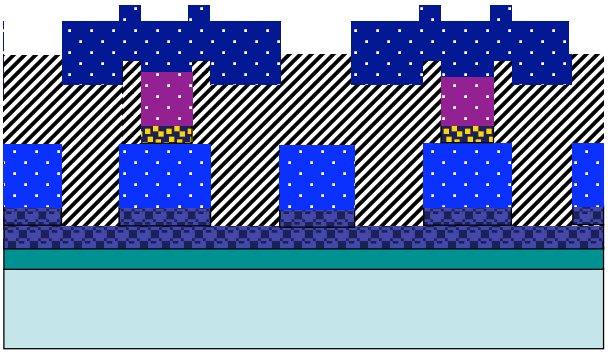
J. Quartz lift off.



K. Wiring layer patterning.



L. Nb wiring layer deposition.



M. Metal lift off.

Figure 30(cont.). Cr/Pt/TiO_x/Ti Device Fabrication Process, steps J-M.

P-Si/α:Si/Ag Device Fabrication Process

The fabrication process for these devices is slightly different from the previous ones in that it uses the a bare p-type Si substrate as the base electrode and amorphous Si (α:Si) as the insulator. Since the surface of the bare Si wafer is to be used as part of the device, it needs to be decontaminated properly before depositing the insulator layer directly on top of it. This is accomplished through a standard industry procedure known as RCA clean. The process consists of three chemical steps: an organic clean where you remove insoluble organic contaminants, an oxide strip for removal of a thin silicon dioxide layer where metallic contaminants may have accumulated, and an ionic clean for removal of ionic and heavy metal atomic contaminants (see process sheet in appendix A). Upon finishing the chemical clean, the wafer is rinsed with de-ionized water (DI water) and loaded on the Pb system. Once the chamber's the pressure is right, the wafer is sputtered cleaned with an Ar plasma followed by a 500 Å deposition of evaporated α:Si. In latter runs we have allowed a cooling time of up to four hours between the α:Si deposition and the Ag one. This was decided based on experimental results obtained from previous runs. After the proper cooling time, a 1000 Å layer of Ag is deposited on top of the α:Si completing the Si/α:Si/metal structure. The wafer is then pattern with the junction mask (M2) and PMMA photo resist, and loaded on the IBM system for Ag backsputter etching with an Ar plasma. That constitutes the counter electrode removal and the wafer is then loaded on the SiO_2 system for the quartz insulation sputter deposition. Finishing with the wiring layer patterning, deposition and lift off as performed for the previous two wafers and spin coating of protective photo resist. The following figures show the fabrication steps described above.

P-Si/α:Si/Ag Device Fabrication Process

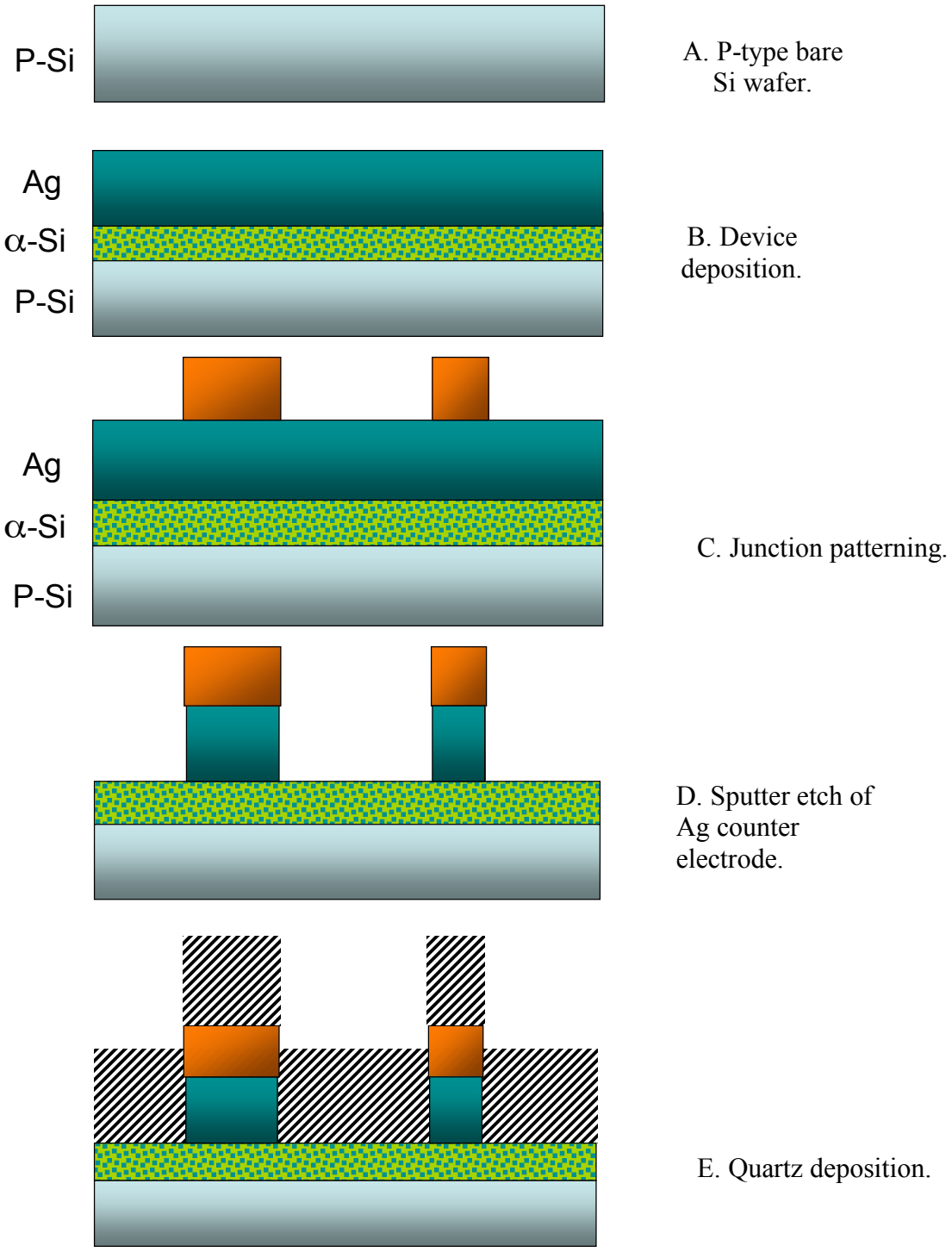
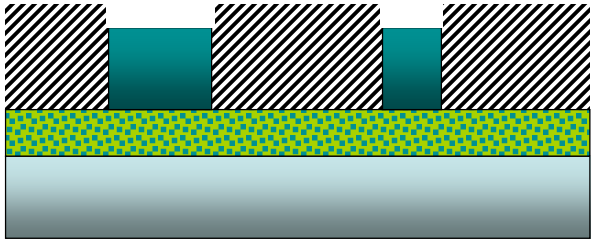
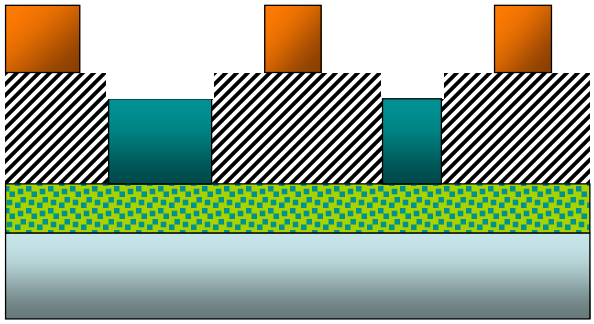


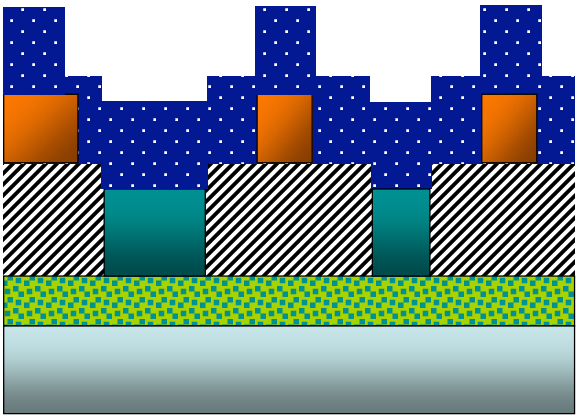
Figure 31. Cr/P-Si/α:SI/Ag Device Fabrication Process, steps A-E.



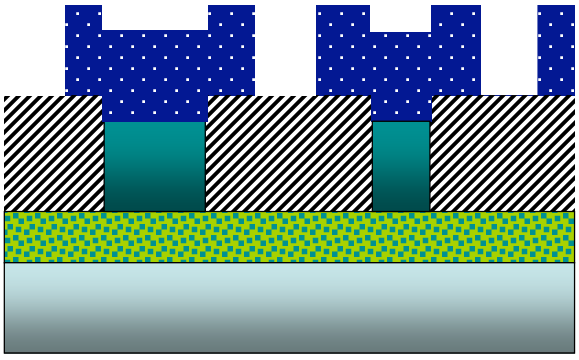
F. Quartz lift off.



G. Wiring layer patterning.



H. Nb wiring layer deposition.



I. Metal lift off.

Figure 31 (cont.). Cr/P-Si/α:SI/Ag Device Fabrication Process, steps F-I.

IV. Results

Finished wafers were diced into individual chips and given to Zhongkui Tan for experimental measurements, performed as part of his doctoral research. These results were presented at the 2009 APS March meeting, as a power point presentation and will be summarized here. Single layer TiO_x devices from early runs already presented switching behavior with about an order of magnitude resistance ratio, this is shown in figure 31. It was also observed that the devices presented short switching cycle life as seen in figure 32. By far the fabrication run that produced more information until now has been VJTiOx8, a five oxide-layer device wafer. The parameters for this devices were studied pre and post rapid thermal annealing (RTA), a process were the Si substrate is rapidly heated to temperatures of up to 1200 C and slowly cooled back again. This process allows for the reflowing of metals as well as many effects aimed to improve layer interfaces and oxygen rearrangement in the oxide layer, amongst other things. Multilayer metal oxide devices show better results than single-layer ones and, pre-RTA for multilayer device results showed much lower on/off ratios regarding the switching resistance, where post RTA showed much-improved ratios (10^3). Results for the multilayer devices are shown in figure 33 and figure 34. One aspect that still needs to improve in future fabrication is the reproducibility shown in figure 35.

So far the p-Si/α:Si/Ag devices, where the α:Si replaces the metal oxide, have presented poor results are. It is uncertain if further research will be done in this kind of device. An IV for these devices is shown in figure 36. The TiO_x devices remain as the focus of work in the near future by the group along with device size reduction into the nanometer realm.

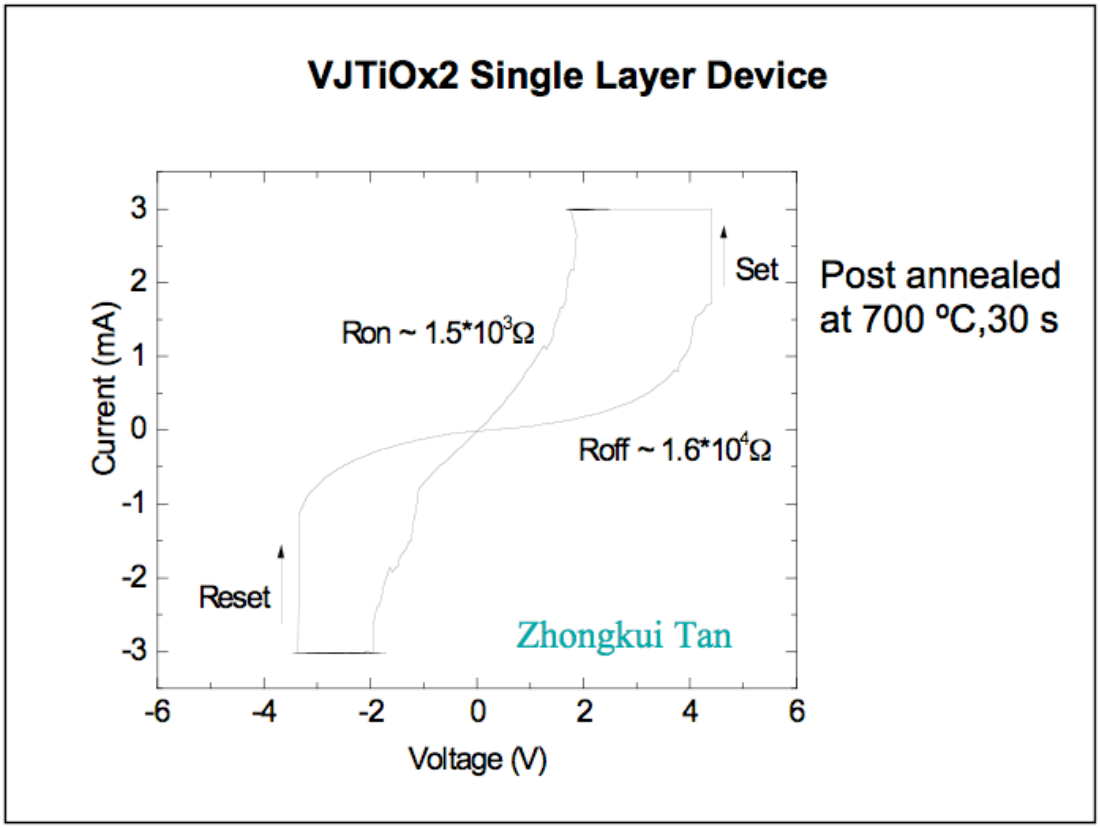


Figure 32. Single layer TiOx device showing switching behavior with a marked current cut-off from the measuring instrument at the switching point.

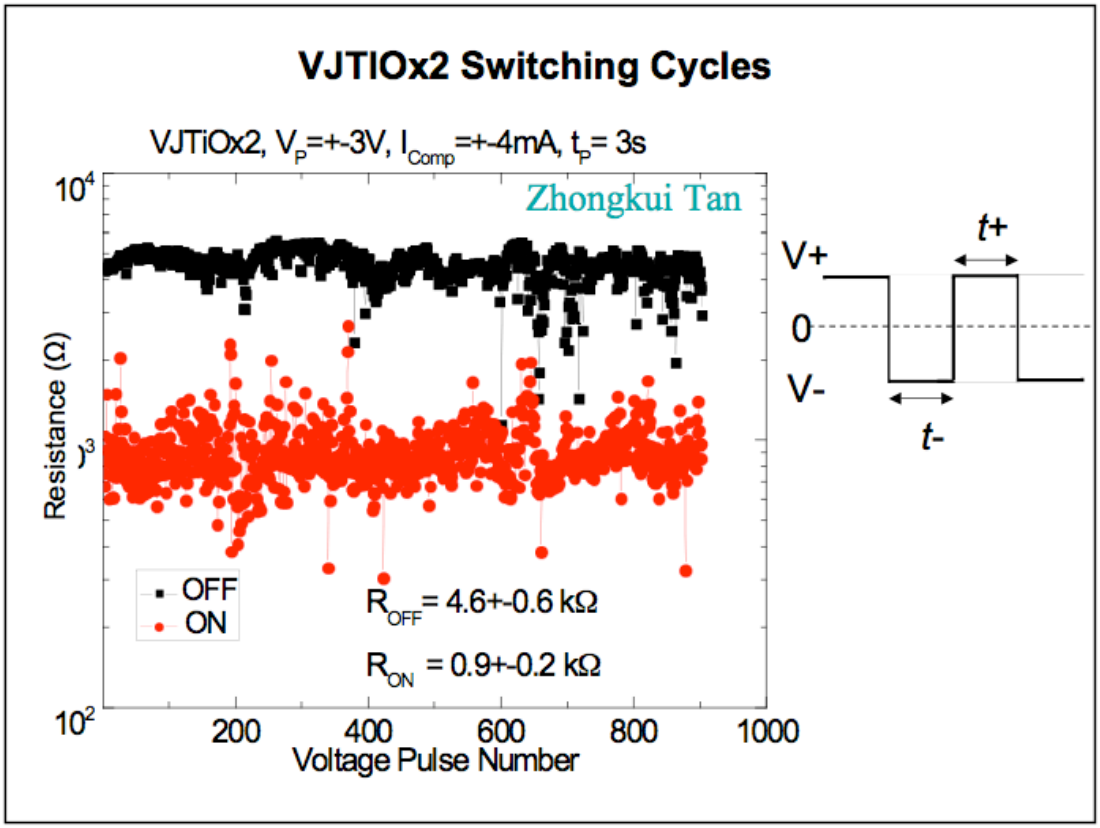


Figure 33. Same TiOx device showing poor cycle life (10^3). After this point devices present lose the ability two switch and remain shorted.

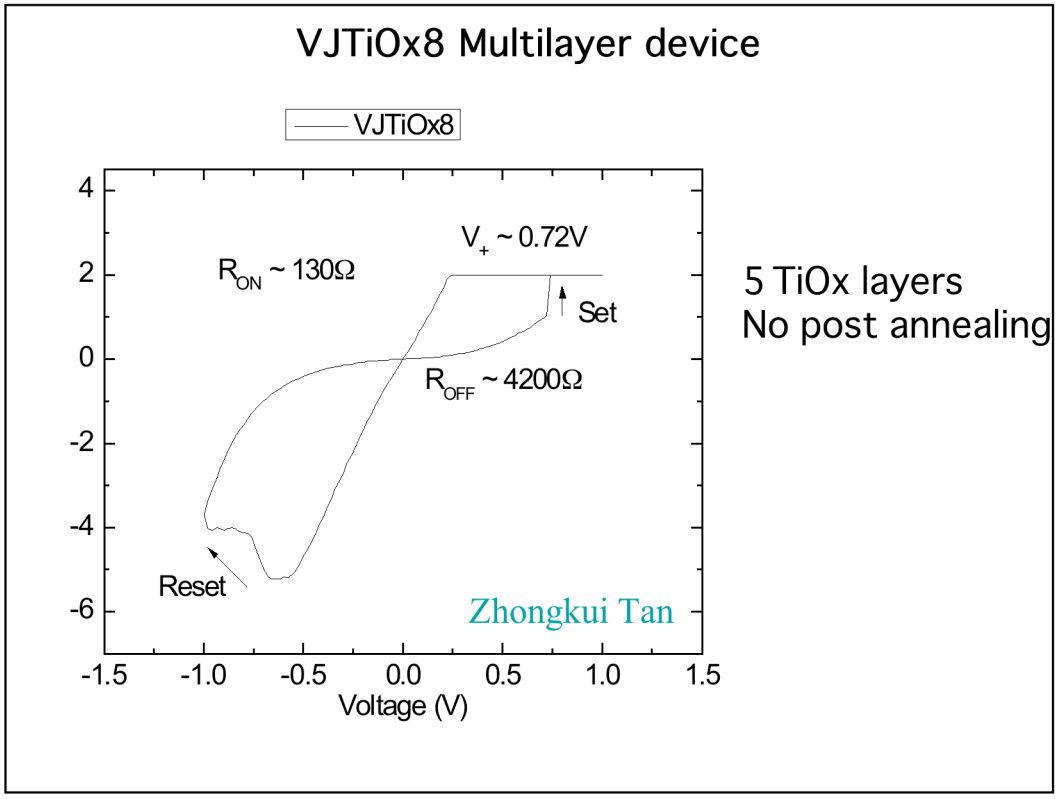


Figure 34. Multilayer TiO_x showing switching behavior, no post annealing.

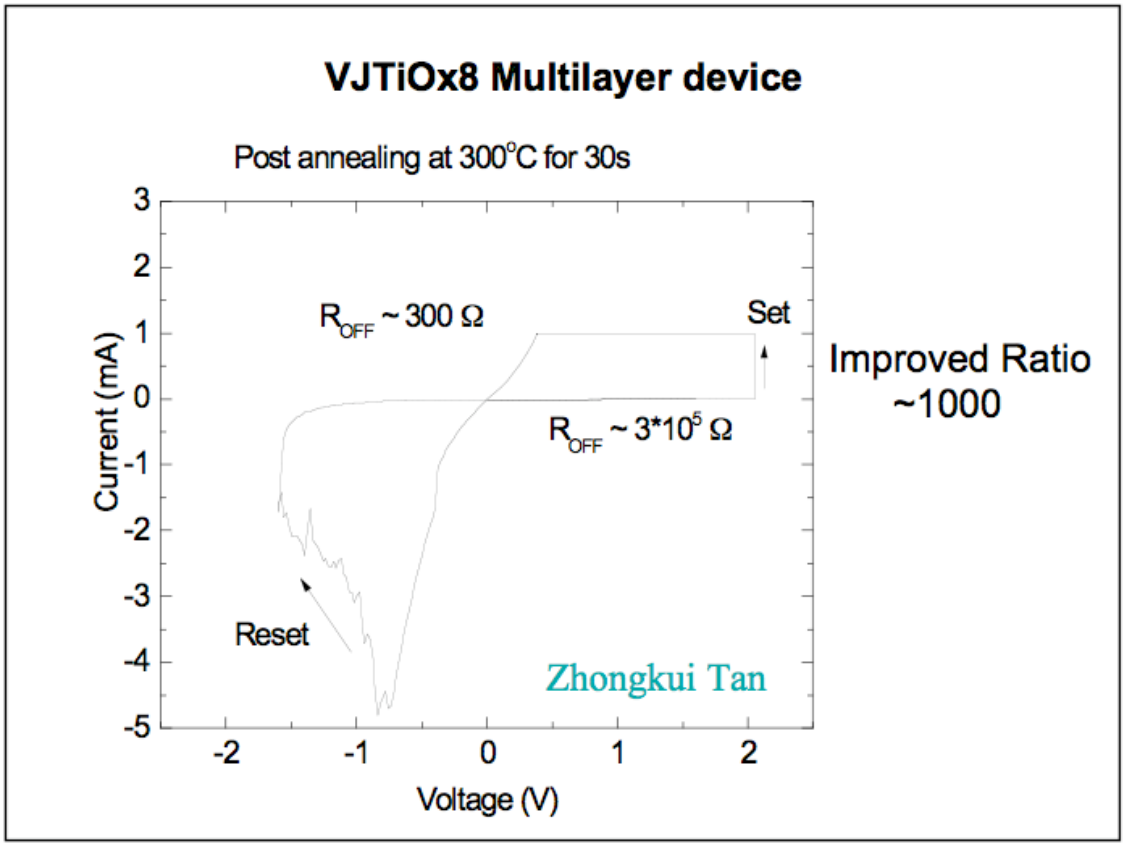


Figure 35. Same multilayer device showing post annealing improved resistance ratio.

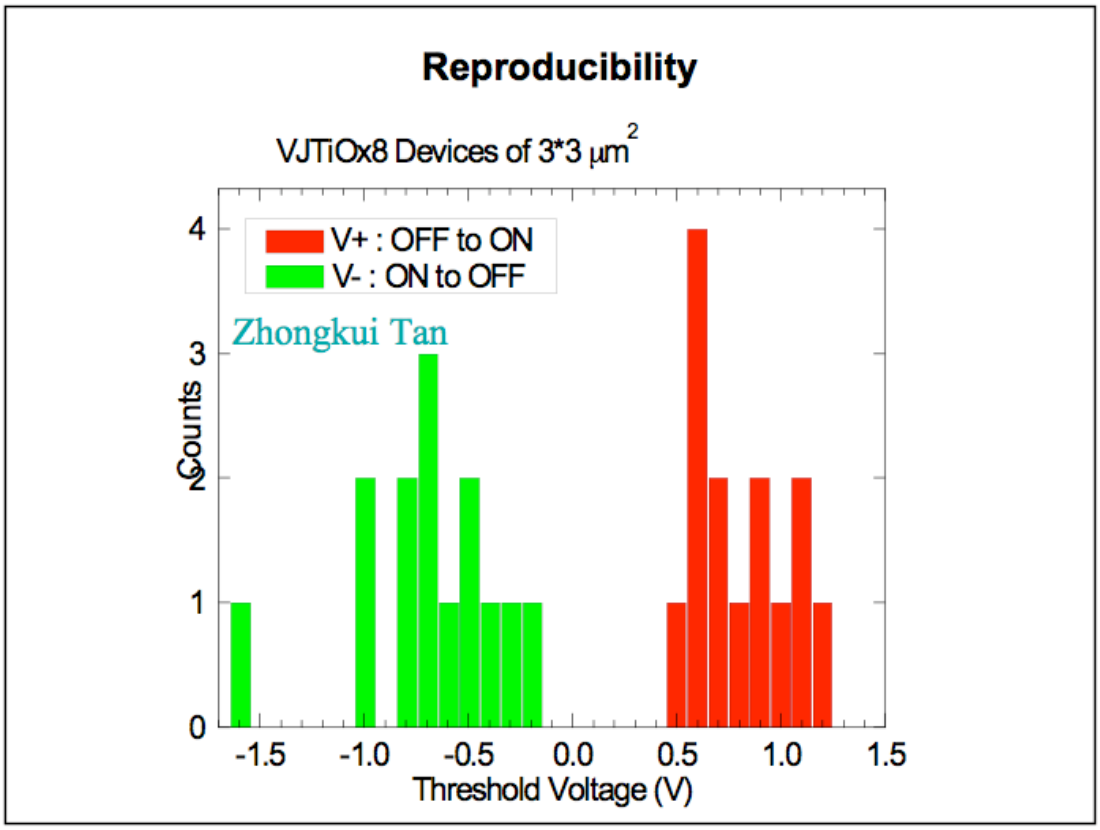


Figure 36. Reproducibility of same multilayer device. This refers to the level for the set-reset voltage as the device is repeatedly switched.

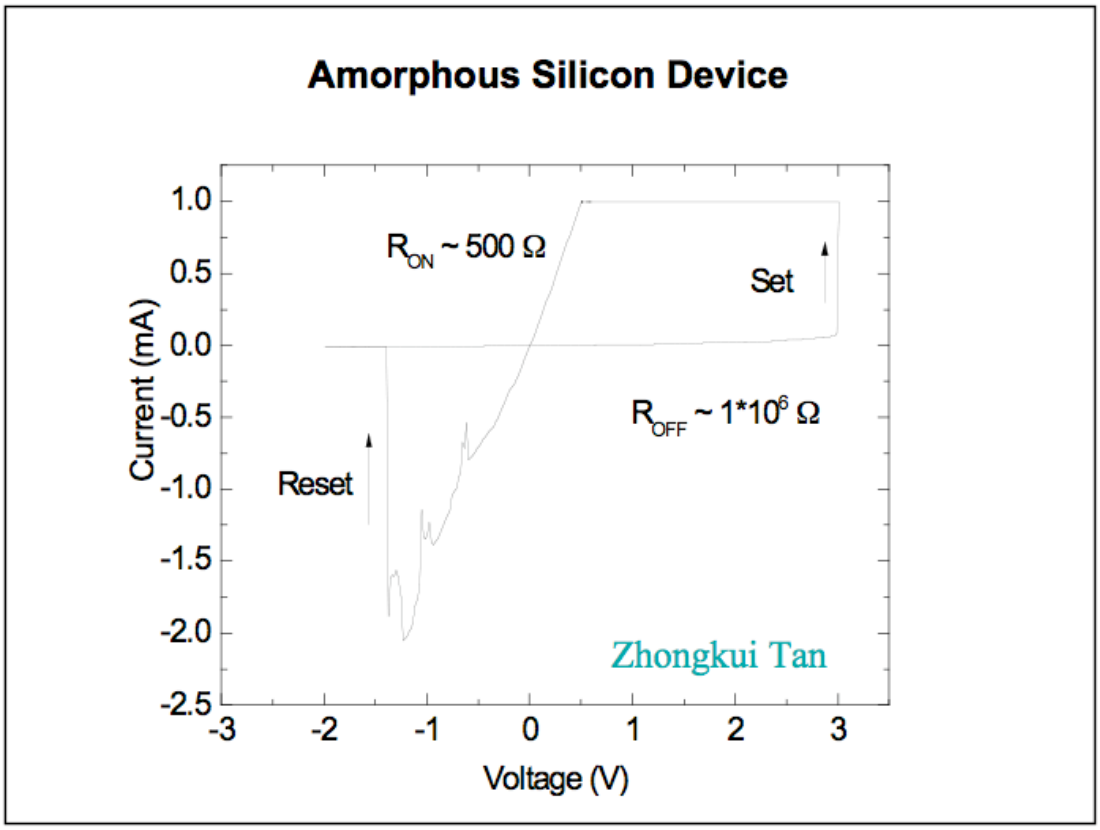


Figure 37. Amorphous Silicon device showing switching behavior.

V. Conclusion

Refurbished, upgraded and modified existing thin-film processing equipment and assisted in developing fabrication processes compatible with the materials required for the resistive memory devices, at the Stony Brook University's IC fabrication laboratory for superconducting and nano-scale devices, in the Physics and Astronomy Department. The MSI project focused on adapting the existing fabrication facilities to develop a commercial CMOS compatible fabrication process to produce the hybrid CMOS devices. Fabricated devices presented the expected switching behavior and the project moved into its second stage of CMP removal of the surface protective layer in CMOS commercial chips. At the time of this writing there is still much improvement to be done regarding yield and performance of devices, yet numerous modifications to the fabrication process have been identified that should produce significant advance. Fabrication of devices for this project is now moving into the nano realm with the use of e-beam lithography.

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Appendix A

Process fabrication sheets are presented in this section. Information of one particular fabrication run has been filled, corresponding to the process described for every one of the devices in the fabrication process section.

FABRICATION PROCESS SHEET
PROCESS VJCuOx1 (CMOL – IBM/Etch)

SAMPLE # _VJCuOx17 **Substrate :** P/Boron Therm Ox: 1000 Å **Date** _____
Resistivity: 1-10 Ωcm

Comments:_____

1. Adhesion Layer Deposition (Pb) **Date** __/__/__ **Run #**_____

Process	B.P. (10^{-7} Torr)	Ar/O2 (mTorr)	Power (W)	Volt (V)	Curr (A)	Thick (Å)	Time (min)	Rate (Å /sec)
Sp Clean	7.4	10	150	647			2:00	
Cr or Ti	7.4-4.5				0.51	50	1:17	0.5-1

2. Trilayer Deposition (IBM) **Date** __/__/__ **Run #**_____

Process	B.P.*10^{-7} (Torr)	Chamber / Wafer Position	Ar/O_2 Pr. (mT)	Power (W)	Current (A)	Voltage (V)	Time (min)
Sp. Clean (optional)							
Cu Presp.	0.85	60	10	500	1.05	470	0:40
Cu (BE)			10	500	1.05	471	1:38
Tune			20	300/68			0:30
Oxidation			20	300/68			3
Cu - Interlayer							
Oxidation							
Cu - Interlayer							
Oxidation							
Cu - Interlayer							
Oxidation							
Nb Presp.	2.5		7.5	700			
Nb CE			7.5	700	2.21	316	2:00

Comments:___Cr(50 Å)/ Cu(1500 Å)/ CuOx/ Nb(1000 Å)

3. BE Patterning (M2)

Mask __CR-142____ Temp.___72____ R.H.__33_%

----Spin PMMA 950K 6% (@ 3000 rpm, 60 sec)
----Bake (Temp 140^{o}C, Time 5 min)
----Expose (JBA): Intensity A= __1.51____ mW/cm^2 , B = __0.48___ mW/cm^2
Time ___999___ sec. C.Vac. _____
----Develop (MIBK : IPA 1:1) Temp _RT__ ^{o}C [21] , Time __1__ min [1] + Buzz_0:45_ sec [45]
----Inspect, Comments _____OK_____
----Plasma Ash (@50W, 1Torr) _40__ sec [40] Resist Thickness (see sheet) _____
----Surface Clean: (15% Phosphoric Acid @ 50^{0}C) __25_ sec [20]

----Plasma Etch Nb Date __/__/___ Run #_____

Gas	**BP** (10^{-5} Torr)	**Flow rate** (ccm)	**Gas Pres.** (mT)	**Power** (W)	**V_{bias}** (V)	**Time** (min)	**End-point** @ (min)
SF_6	3.0	**11.2**	25	20		3+2	Not clear

----Inspect/Comments_____

----Thickness measurement (Resist + Nb counter electrode):

----Sputter Etch BE & Adhesion Metal (Cr) Date __/__/___ Run #_____

Process	**B.P.*** 10^{-7} (Torr)	**Stage Position**	**Shutter**	**Ar Pr.** (mT)	**Power** (W)	**Tune** C_L/C_T	**Voltage** (V)	**Time** (min)
Sp. Clean	**6**	Up (Out)		**10**	**100**		**648**	**5+5+5+5+5**

----Inspect/Comments_5 extra min to clear Cu from central area
----Thickness Measurement (see sheet)

----Resist Strip
----Soak Acetone __5___ hrs [4-5] Q-tip Scrub? _no__
----Ultrasonic in Acetone __20__ min [60]
----Inspect/Comments____OK, no pealing_____
----Thickness Measurement (see sheet):

----Plasma Ash @ 50W, 1Torr, ___2__ min [2]

4. Junction Patterning

Mask: CREST-M3 **Date:_____** **Temp: 72 °F Humidity: 34 %**

----Spin PMMA 950K 6% (@ 3000 rpm, 60 s)
----Bake (Temp 140 °C, Time 5 min)
----Expose (JBA) Intensity A= 1.51 mW/cm^2 , B = 0.48 mW/cm^2
Time 999 sec. C.Vac. -2
----Develop (1:1 MIBK:IPA) , Temp. RT °C , Time 1:30 min [1] + Buzz 15 sec [45]
----Inspect/Comments OK

----Plasma Ash @ 50W, 1Torr, 40 sec [40]
----Thickness Measurement (see sheet):

----Plasma Etch Nb CE **Date / /** **Run #_____**

Gas	**BP** (10^{-5} Torr)	**Flow rate** (ccm)	**Gas Pres.** (mT)	**Power** (W)	**V_{bias}** (V)	**Time** (min)	**End-point** @ (min)
SF_6	3.0	11.2	25	20	-1.0	2:20	100 sec

----Inspect/Comments_____

----Thickness measurement (Resist + Nb counter electrode):

5. SiO_2 (Quartz) Deposition **Date / /** **Run #_____**

B.P. (10^{-7} Torr)	**Ar Press.** (mT)	**Power** (W)	**V_{bias}** (V)	**V_{p-p}** (V)	**Time** (min)/Wait Total :	
3.3	2.5	400	-860 -859 -856	1500 1490 1490	5 5 3:30	5 5

----Inspect/Comments total~2400 A

Quartz Liftoff
----Stripper (Acetone) – Soak 23 hrs
----Ultrasonic in Acetone 1 min Q-tip scrub ? mild
----Inspect, Comments OK
----Thickness Measurement (see sheet):
----Plasma Ash @50W, 1Torr, 2 min [2]

6. Wiring Patterning

Mask: CREST-M4 Date:_____ Temp: 72 °F Humidity: 34 %

----Spin PMMA 950K 6% (@ 3000 rpm, 60 s)
----Bake (Temp 140 °C, Time 5 min)
----Expose (JBA) Intensity A= 1.51 mW/cm^2 , B = 0.48 mW/cm^2
Time 999 sec. C.Vac. _____
----Develop (1:1 MIBK:IPA) , Temp. RT °C , Time 1:00 min [1] + Buzz 45 sec [45]
----Inspect/Comments_____

----Plasma Ash @ 50W, 1Torr, 40 sec [40]
----Thickness Measurement (see sheet):

7. Nb Wiring Layer Deposition Date / / Run #_____

Process	**B.P.*** 10^{-7} (Torr)	**Shutter**	**Ar Pr** (mT)	**Power** (W)	**Current** (A)	**Voltage** (V)	**Time** (min)
Sp. Clean	2.2		10	100/29		651	2:00
Nb Presp.							0:30
Nb CE			7.5	700	2.21	314	3:00

Nb Liftoff
----Soak in Stripper (Acetone) 90 min
----Ultrasonic in Acetone 2 min
----Inspect, Comments OK, ~ 1500 Å _____

Thickness Measurements

Process \ Location	Center (0,0) (Å)	Top (0,4) (Å)	Bottom (0,-4) (Å)	Left (-4,0) (Å)	Right (4,0) (Å)
M2	**10100**	**9775**	**9755**	**9645**	**9545**
Nb RIE (3:00 min)	**8325**	**7795**	**7855**	**7815**	**7575**
Nb RIE (2:00 min)	**6860**	**6255**	**6330**	**6270**	**6145**
Cu Backsputter (20 min)	**5590**	**4885**	**4915**	**4540**	**3685**
M2 Strip	**3510**	**3400**	**3220**	**2885**	**2300**
M3	**10150**	**9505**	**9525**	**9535**	**9805**
Nb RIE (140 sec)	**9210**	**8560**	**8875**	**8555**	**9020**
Quartz Lift Off	**1335**	**1730**	**1495**	**1420**	**1770**
M4	**10650**	**10580**		**8350**	
M4 Lift Off	**1485**			**1380**	

FABRICATION PROCESS SHEET
PROCESS VJTiOx15 (CMOL - Liftoff)

SAMPLE # _VJTiOx9 **Substrate :** P/Boron Therm Ox: 1000 Å **Date** _____
Resistivity: 1-10 Ωcm

1. Cr Undercoat (protective layer)

Process	**B.P.** (10^{-7} Torr)	**Ar/O_2** (mTorr)	**Power** (W)	**Tune** C_L/C_T	**Volt** (V)	**Curr** (A)	**Thick** (A)	**Time** (min)	**Rate** (A/sec)
Sp Clean	**7.8**	**10**	**150**	**51/22**	**633**			**2:00**	
Cr	**7.8**						**20**	**0:49**	**0.5**

2. BE Patterning (M2)

Mask CREST –M2 **Temp.** 73 **R.H.** 36 **%**

----Spin PMMA 950K 2% (@ 10000 rpm, 60 sec)
----Bake (Temp 140°C, Time 5 min)
----Plasma Ash (@50W, 1Torr) 1:15 min [1]
----Spin Negative Resist UVN-30 (@2000 rpm, 60 s) [5800 Å]
----Soft Bake (Temp 90°C, Time 1 min)
----Expose (JBA): Intensity A= 1.55 mW/cm^2 , B = 0.49 mW/cm^2
Time 4.5 sec. C.Vac. -2
----Post Exposure Bake (Temp 90°C, Time 1 min)
----Develop (Microposit CD-26 : DI water 2:1) Temp RT °C [21] , Time 0:42 min [1]
----Inspect, Comments _____
----Thickness Measurement (see sheet):
----Plasma Ash (@50W, 1Torr) 2+2 min [2+2]
----Thickness Measurement (see sheet):

3. Base Metal Deposition **Date** / / **Run #**_____

Process	**B.P.** (10^{-7} Torr)	**Ar/O_2** (mTorr)	**Power** (W)	**Tune** C_L/C_T	**Volt** (V)	**Curr** (A)	**Thick** (Å)	**Time** (min)	**Rate** (Å /sec)
Sp Clean	**8**	**10**	**150**	**48/22**	**640**			**0:30**	
Cr	**4**					**0.53**	**50**	**1:35**	**0.5**
Pt	**4**					**0.78**	**1000**	**24:52**	**0.5**

----Metal Lift-off
---- Soak Acetone overnight hrs [4-5]
---- Ultrasonic in Acetone 2 min [10]
---- Inspect/Comments_____
----Plasma Ash (@50W, 1Torr) 2 min [2]
Metal Thickness (see sheet) _____

4. Barrier & CE Metal Deposition **Date __/__/__** **Run #_____**

Process	B.P. (10^{-7} Torr)	Ar/O_2 (mTorr)	Power (W)	Tune C_L/C_T	Volt (V)	Curr (A)	Thick (Å)	Time (min)	Rate (Å /sec)
Sp Clean	**6.2**	**10**	**150**	**48/22**	**656**	**0.62**		**0:30**	
Ti	**5.6**					**0.65**	**15**		**0.5**
Oxidation	**5.2**	**10**	**150**	**49/22**	**649**			**10:00**	
Ti	**8->4.8**					**0.65**	**15**		**0.5**
Oxidation		**10**	**150**	**49/22**	**649**			**10:00**	
Ti	**8.1->3.8**					**0.64**	**15**		**0.5**
Oxidation		**10**	**150**	**52/22**	**652**			**10:00**	
Ti	**6.8->4**					**0.64**	**15**		**0.5**
Oxidation		**10**	**150**	**49/22**	**652**			**10:00**	
Ti	**7.8->4.4**					**0.65**	**15**		**0.5**
Oxidation		**10**	**150**	**49/22**	**650**			**10:00**	
Ti	**6.4->3.7**					**0.64**	**15**		**0.5**
Oxidation		**10**	**150**	**49/22**	**647**			**10:00**	
Ti	**8->4.2**					**0.65**	**15**		**0.5**
Oxidation		**10**	**150**	**49/22**	**649**			**10:00**	
Ti	**7.5->4**					**0.65**	**15**		**0.5**
Oxidation		**10**	**150**	**52/22**	**652**			**10:00**	
Ti	**7.2->4.2**					**0.66**	**15**		**0.5**
Oxidation		**10**	**150**	**52/22**	**656**			**10:00**	
Ti	**7.5->3.9**					**0.66**	**15**		**0.5**
Oxidation		**10**	**150**	**52/22**	**645**			**10:00**	
Ti	**7.8->4**						**750**		**0.5**

5. Junction Patterning

Mask: CREST-M3 Date:_____ **Temp: 72 °F** **Humidity: 39 %**

---- Spin PMMA 950K 6% (@ 2000 rpm, 60 s)

---- Bake (Temp 140 °C, Time 5 min)

---- Expose (JBA) Intensity A= 1.55 mW/cm^2 , B = 0.49 mW/cm^2

Time _____ sec. C.Vac. -2

---- Develop (1:1 MIBK:IPA) , Temp. RT °C , Time 1:45 min [1] + Buzz _____ sec [45]

---- Inspect/Comments _____

----Plasma Ash (@50W, 1Torr) 0:40 min [2]

----Thickness Measurement (see sheet):

--- Plasma Etch Ti CE **Date __/__/__** **Run #_____**

Gas	**BP** (10^{-5} Torr)	**Flow rate** (ccm)	**Gas Pres.** (mT)	**Power** (W)	**V_{bias}** (V)	**Time** (min)	**End-point** @ (min)
SF_6	2.5	11.2	25	30	-2	3:23	

----Inspect/Comments _____
----Thickness Measurement (see sheet):

----Sputter Etch Cr Underlayer **Date __/__/__** **Run #_____**

Process	**B.P.***10^{-7} (Torr)	**Stage Position**	**Ar Pr** (mT)	**Power** (W)	**Tune** C_L/C_T	**Voltage** (V)	**Time** (min)
Sp. Clean	**12**	UP (Out)	**10**	**150**	**48/22**	**621**	**0:30**

----Inspect/Comments _____
----Thickness Measurement (see sheet):

6. SiO_2 (Quartz) Deposition **Date __/__/__** **Run #_____**

B.P. (10^{-7} Torr)	**Ar Press.** (mT)	**Power** (W)	**V_{bias}** (V)	**V_{p-p}** (V)	**Time** (min)/Wait Total :	
2.6	**2.5**	**400**	**-842**	**-1510**	**3:00**	**6:00**
			-866	**-1500**	**3:00**	**5:00**
			-860	**-1500**	**3:30**	

Quartz Liftoff
----Stripper (Acetone) – Soak ___40__hrs [overnight]
----Ultrasonic in Acetone ____5___min Q-tip scrub ? __yes__
----Inspect, Comments _____
----Thickness Measurement (see sheet):
----Plasma Ash (@50W, 1Torr) __2_ min [2]

7. Wiring Layer Patterning

Mask: CREST-M4 Date:_____ Temp: 68 °F Humidity: 43 %

----Spin PMMA 950K 6% (@ 3000 rpm, 60 s)
----Bake (Temp 140 °C, Time 5 min)
----Expose (JBA) Intensity A= 1.55 mW/cm^2 , B = 0.49 mW/cm^2
Time 999 sec. C.Vac. -2
----Develop (1:1 MIBK:IPA) , Temp. RT °C , Time 1 min [1] + Buzz 45 sec [45]
----Inspect/Comments_____
----Plasma Ash (@50W, 1Torr) 0:40 min [2]
----Thickness Measurement (see sheet):

8. Nb Wiring Layer Deposition Date / / Run #_____

Process	**B.P.***10^{-7} (Torr)	**Stage Position**	**Ar Pr** (mT)	**Power** (W)	**Current** (A)	**Voltage** (V)	**Time** (min)
Sp. Clean	**5.2**	UP (Out)	**9.5**	**150**		**592**	**30+ 1:30**
Nb Presp.		UP (Al-S)	**10.95**	**600**	**2.13**	**592**	**2:00**
Nb CE		Down (Nb)	**10.95**	**600**	**2.13**	**592**	**2:00**

Nb Liftoff
----Soak in Stripper (Acetone) 120 min
----Ultrasonic in Acetone 2 min
----Inspect, Comments _____

Thickness Measurements.

Location / Process	Center (0,0) (Å)	Top (0,4) (Å)	Bottom (0,-4) (Å)	Left (-4,0) (Å)	Right (4,0) (Å)
UVN-30, M2 before ash	**6180**	**6120**	**6090**	**6110**	**6130**
After 2 min ash	**6200**	**6230**	**6190**	**6285**	**6350**
After 2+2 min	**6325**	**6310**	**6290**	**6130**	**6135**
After 2+2+2 min ash	**6505**	**6140**	**6090**	**5950**	**5935**
M2 lift off	**1040**	**1125**	**1095**	**1135**	**1215**
M2 Lift off+ after ash	**1145**	**1125**	**1145**	**1125**	**1130**
After M3	**9950**	**9430**	**9595**	**1135**	**1215**
After RIE	**4950**	**4170**	**4360**	**4675**	**4200**
After Cr spt. cl.	**4325**	**3805**	**3756**	**3970**	**3945**
Quartz lift off	**890**	**1060**	**1040**	**880**	**875**
M4	**8205**	**8075**	**8056**	**8265**	**7845**

FABRICATION PROCESS SHEET
PROCESS VJaSi-Ag2 (CMOL)

SAMPLE # _____VjsSi-Ag2____ **Substrate:** ___**Si (bare) P-type**___ **Date** _____
Resistivity:_____ Ωcm, Dopant: __P/Boron__
Comments:_____

1. Wafer Clean (RCA)

----Organics [5:1:1 H_2O (150 ml) : H_2O_2 (30 ml) : NH_4OH (30 ml)] @ _71 ^{0}C [70] _15_ min [15]
----Oxide (10:1 H_20 : HF or BOE) @ _RT_ ^{0}C [RT] __30_ sec [20]
----Organics [6:1:1 H_2O (150 ml) : H_2O_2 (25 ml) : HCl (25 ml)] @ 72 ^{0}C [70] __15_ min [15]
----DI rinse

2. Device Deposition **Date** ___/___/___ **Run #**_____

Process	**B.P.** (10^{-7} Torr)	**Ar/O_2** (mTorr)	**Power** (W)	**Tune** C_L/C_T	**Volt** (V)	**Curr** (A)	**Thick** (Å)	**Time** (min)	**Rate** (Å /sec)
Sp Clean	**7**	**10**	**150**	**53/21**	**683**			**2:00**	
α:Si	**5.5**						**500**	**0.5-1**	**4 hr**
Ag	**3**					**0.57**	**1000**	**0.5-1**	

Comments:_____

3. Junction Patterning

Mask: CREST-M3 Date:_____ **Temp:** _72_ **°F** **Humidity:** __34__**%**

----Spin PMMA 950K 6% (@ 2000 rpm, 60 s)
----Bake (Temp 140 °C, Time 5 min)
----Expose (JBA) Intensity A= ____1.51___ mW/cm^2 , B = ___0.47___ mW/cm^2
Time __999_ sec. C.Vac. ___-2__
----Develop (1:1 MIBK:IPA) , Temp. _RT_ ^{o}C , Time __1:00_ min [1] + Buzz _0:45__ sec [45]
----Inspect/Comments_____
----Thickness Measurement (see sheet):

----Sputter ETCH Ag CE **Date** ___/___/___ **Run #**_____

Process	**B.P.***10^{-7} (Torr)	**Stage Position**	**Shutter**	**Ar Pr.** (mT)	**Power** (W)	**Tune** C_L/C_T	**Voltage** (V)	**Time** (min)
Sp. Clean		Up (Out)		**10**	**100**			**2+1:45**

----Thickness measurement (Resist + Ag counter electrode):

4. SiO_2 (Quartz) Deposition **Date __/__/__** **Run #_____**

B.P. (10^{-7} Torr)	**Ar Press.** (mT)	**Power** (W)	**V_{bias}** (V)	**V_{p-p}** (V)	**Time** (min)/Wait Total :	
1.9	**2.5**	**400**	**-869**	**1500**	**3:00**	**5**
			-863	**1490**	**3:00**	**5**
			-858	**1490**	**3:30**	

Quartz Liftoff

----Stripper (Acetone) – Soak __4:07_hrs
----Ultrasonic in Acetone __3___min Q-tip scrub ? __mild__
----Inspect, Comments _____extra scrub_____
----Thickness Measurement (see sheet):

5. Contact Hole Patterning

Mask: CREST-I2 Date:_____ Temp:____ °F Humidity:_____%

----Spin PMMA 950K 6% (@ 3000 rpm, 60 s)
----Bake (Temp 140 °C, Time 5 min)
----Expose (JBA) Intensity A= _____ mW/cm^2 , B = _____ mW/cm^2
Time _____ sec. C.Vac. _____
----Develop (1:1 MIBK:IPA) , Temp. ____^oC , Time _____ min [1] + Buzz _____ sec [45]
----Inspect/Comments_____
----Thickness Measurement (see sheet):

----Sputter ETCH CE + α:Si Date __/__/__ Run #_____

Process	**B.P.**$*10^{-7}$ (Torr)	**Stage Position**	**Ar Pr.** (mT)	**Power (W)**	**Tune** C_L/C_T	**Voltage** (V)	**Time** (min)
Sp. Clean		Up (Out)					

----Thickness Measurement (see sheet):

6. Wiring Layer Patterning

Mask: CREST-M3 Date:_____ Temp: 72 °F Humidity: 34 %

----Spin PMMA 950K 6% (@ 3000 rpm, 60 s)
----Bake (Temp 140 °C, Time 5 min)
----Expose (JBA) Intensity A= 1.51 mW/cm^2 , B = 0.48 mW/cm^2
Time 999 sec. C.Vac. _____
----Develop (1:1 MIBK:IPA) , Temp. RT °C , Time 1:30 min [1] + Buzz 15 sec [45]
----Inspect/Comments_____

----Thickness Measurement (see sheet):

Nb Wiring Layer Deposition Date / / Run #_____

Process	**B.P.***10^{-7} (Torr)	**Stage Position**	**Ar Pr**. (mT)	**Power** (W)	**Current** (A)	**Voltage** (V)	**Time** (min)
Sp. Clean	**7.3**	UP (Out)	**10**	**100**		**650**	**0:30**
Nb Presp.		UP (Al-S)			**2.25**	**309**	**0:30**
Nb CE	**1.4**	Down (Nb)	**7.5**	**700**	**2.20**	**316**	**3:00**

Nb Liftoff
----Soak in Stripper (Acetone) 120 min
----Ultrasonic in Acetone 2 min
----Inspect, Comments _____

Thickness Measurements:

Location / Process	Center (0,0) (Å)	Top (0,4) (Å)	Bottom (0,-4) (Å)	Left (-4,0) (Å)	Right (4,0) (Å)
M3	**10070**	**9675**	**9995**	**9780**	**9965**
After Ag backsputter	**10210**	**9770**	**10090**	**9775**	**10120**
After SiO2 lift off	**815**	**790**	**860**	**850**	**845**
M4	**8645**	**8505**	**8465**		