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Experimental Study of Electron Transport through Nanometer-Scale Metal-Oxide Junctions

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Abstract of the Dissertation

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This work presents results of an experimental study of electron transport through few nanometer-scale metal oxide junctions of two types:

First, we have measured transport properties of Nb/Al/Nb junctions fabricated using thermal oxidation or rf-plasma oxidation at various conditions, with rapid thermal post-annealing (RTA) to improve junction endurance in electric fields in excess of 10 MV/cm. The results indicate that such junctions may combine high field endurance (corresponding to at least 10^{10} write/erase cycles in floating-gate memories) and high current density (corresponding to 30-ns-scale write/erase time) at high voltages, with very low conductance (corresponding to retention time scale ~0.1 s) at low voltages. We discuss the improvements necessary for the use of such junctions in advanced floating-gate memories.

Second, we have studied resistive bistability (memory) effects in junctions based on

several metal oxides, with a focus on sample-to-sample reproducibility which is necessary for the practical use of such junctions, in particular as crosspoint devices of hybrid CMOS/nanoelectronic circuits. Few-nm-thick layers of NbO_x, CuO_x and TiO_x have been formed by thermal and plasma oxidation, at various deposition and oxidation conditions, both with or without rapid thermal post-annealing. The resistive bistability effect has been observed for all these materials, with particularly high switching endurance (over 10^3 switching cycles) obtained for single-layer TiO_2 junctions, and the best reproducibility reached for multi-layer junctions of the same material. Fabrication optimization has allowed us to improve the OFF/ON resistance ratio to about 10^3, though the sample-to-sample reproducibility is so far still lower than that required for large scale integration.

Key Words: electron transport, metal oxide, crested barrier, rapid thermal annealing, endurance, resistive bistability, reproducibility.

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Chapter 1
Introduction

Semiconductor integrated circuit technology (whose most wide-spread version is usually dubbed CMOS) has been perhaps the most significant technological advance of our civilization during the past half century. It was driven by the demand for higher computing power and larger data storage capacity. Fundamentally, the integrated circuit (IC) industry has employed the "top-down" approach, in which electron devices are fabricated by such processes as silicon doping and thin-film deposition, and patterned using optical lithography. The key advantage of this approach is that the components are built in place, so that no part assembly is needed. In the last few decades, the number of individual transistors that can be placed on a single integrated circuit chip has been doubled every 18 months or so (the "Moore's Law", first noted by Gordon E. Moore of Intel). This exponential progress has enabled all the information technology revolution including the Internet, and wide proliferation of inexpensive, high-performance silicon chips into every pore of our everyday life.

However, it is generally accepted now that this progress will turn into a crawl at some time during the next decade. [1] Among several reasons of this anticipated crisis, (i.e. device performance degradation and power dissipation growth [2]), probably the most fundamental one is that the workhorse active device of the integrated circuits, the silicon field-effect transistor (MOSFET), requires an accurate definition of several dimensions including the length and width of its conducting channel. As these devices are scaled down, arising quantum mechanical effects require the definition to be more and more precise [3-7], which in turn requires more and more complex and expensive patterning tools. At some point, the scaling will start bringing diminishing returns, and the IC industry will stall ("mature"). This would have innumerable negative consequences for the industry, technology, and everyday life.

It is frequently argued [8] that the "Moore's Law" demise may be avoided by switching to the "bottom-up" approach, in which active device components of the integrated circuits are chemically synthesized and thus have the nature-given, fundamentally similar size and shape. This approach has indeed resulted in the successful experimental demonstration of several molecular versions of active electronic devices, for example, single electron transistors [9-16]. However, to our best knowledge, there have been virtually no practicable ideas how much nanometer-scale multi-terminal devices could be effectively integrated into a very large scale integrated (VLSI) circuit, because this requires nanometer-accurate placement of the components. This is why, while the silicon-based technology may still serve as a mainstream platform for most IC

technologies in the next few decades, alternative technologies, including new materials, devices, circuits and system-level architectures are clearly needed [17]. This Ph. D. thesis describes my work in the following two directions of this general field, where such advances look especially promising.

A. Advanced Memories.

Memory is one of the most important parts of any contemporary electronics systems, including all modern computers, mobile phones, digital cameras, portable digital audio/video players, etc. [18, 19]. It can store digital data for a certain period of time, either requiring external power supply or not. Most types of random access memory (RAM), including dynamic random access memory (DRAM) and static random access memory (SRAM), are "volatile", i.e. require power supply for data storage. On the contrary, "nonvolatile" memories, e.g., read-only memory (ROM), flash memory, etc., can retain the stored information without power supply for years.

Among all kinds of nonvolatile memories, NAND flash memory is the fastest growing segment of the memory market because of its high density. However, such memory has much lower program and erase speed (in the μs and ms ranges, respectively), compared to that of CMOS logic (whose clock cycles are in sub-ns range). It would be a great achievement to develop a nonvolatile memory with high operation speed (comparable to volatile RAMs), while still keeping the standard 10-year data retention ability.

The operation of current flash memory cells is based on Fowler-Nordheim tunneling

through an 8-nm-scale-thick SiO_2 layer (Figure 1.1a) separating a virtually isolated electrode called floating gate, located between the control gate and the MOSFET channel, from the latter electrode. Any electrons placed on the floating gate are trapped there and, at low voltages applied to the control gate, would not discharge for many years. High (~15 V) voltage applied to the control gate induces a very high (~10mV/cm) electric field in the SiO_2 layer. This field tilts the potential barrier as shown in Figure 1.1, and thus suppresses the potential barrier for electron tunneling to/from the floating gate. As a result, the quantum-mechanical transparency of the tunnel barrier increases by more than 10 orders of magnitude, and the floating gate recharges. However, as already mentioned above, this huge difference is still insufficient to provide the difference between the retention and write/erase time necessary to combine memory's nonvolatility and randon-access operation.

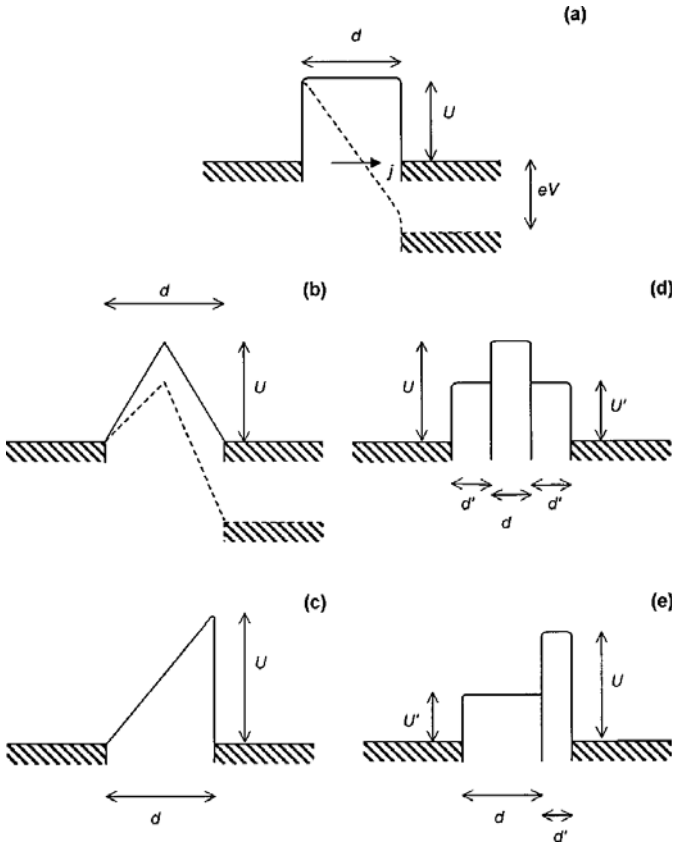


Figure 1.1 Conduction band edge diagrams of various tunnel barriers: (a) a typical uniform barrier; (b) idealized crested symmetric barrier; (c) idealized asymmetric barrier, (d) crested, symmetric layered barrier, and (e) asymmetric layered barrier. Dashed lines in panels a) and b) show the barrier tilting caused by applied voltage *V*.

Other panels of Figure 1.1 show the conduction band edge diagrams of various non-uniform ("engineered") tunnel barriers [20]. According to calculations [20-25], the rate of quantum-mechanical tunneling of electrons through such barriers, in particular those with "crested" potential profile peaking in the middle, may be much more sensitive to the voltage applied to the barrier [26]. This sensitivity may enable fast and scalable nonvolatile random-access memories ("NOVORAM") [20, 22] with a simple cell structure (Figure 1.2), and a matrix architecture similar to that of NOR flash – see, e.g.,

Reference 27. The main difference of the NOVORAM cell from the flash is that the tunneling layer, responsible for write/erase operations, is moved to the back of the floating gate. In this geometry, the floating gate may be metallic, and its thickness reduced to a few nanometers, thus dramatically reducing the electrostatic crosstalk of the adjacent cells, and making the cells scalable to at least 10 nm.

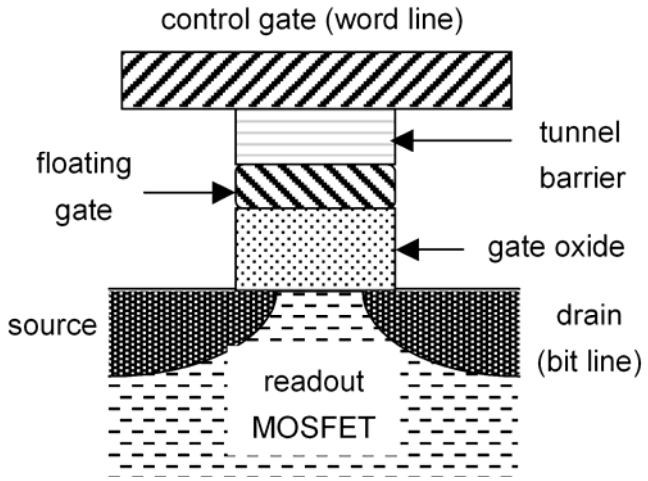


Figure 1.2 Possible cell structure of NOVORAM/FGRAM.

There are several factors that need to be taken into account when selecting the appropriate materials to demonstrate a crested barrier. The key parameters to characterize a tunnel barrier include the barrier height, dielectric constant, thickness and effective mass of charge carriers in each dielectric layer. The barrier height U relates to work function W of the metal electrode and the electron affinity χ of the dielectric by $U = W - \chi$. (W is defined as the difference between the vacuum level and the Fermi

energy of the metal electrode and χ is the difference between the vacuum level and the conduction band edge of the dielectric.) U is the most important parameter that determines the barrier performance. Ideally, the barrier height in the middle of the "crested" barrier should be 1 to 2 eV higher than that of its sides (Figure 1.1b). Simple quantum-mechanical (say, WKB) calculations show that the fast suppression of such barrier by the applied voltage may provide the fast change of the tunnel current.

The dielectric constant k will also affect the performance of the barrier. Under applied voltage bias, the electric field in the barrier automatically redistributes so that it is inversely proportional to the dielectric constant, changing the potential barrier profile. In addition, the effective mass m_e and physical thickness d of each layer will affect the performance of crested barriers as a whole $(m_e/m_0)^{1/2}d$. Table 1.1 lists the reported (relative) dielectric constants k, band gaps and conduction band offset of interesting dielectric materials.

Table 1.1 List of values of dielectric constants, band gaps and conduction band offset for several dielectric materials [28-35].

Material	k	V_G (eV)	U – Si (eV)	U – Au (eV)	U – Nb (eV)	m_e
SiO_2	3.9	9	3.5	4.0	3.2	0.5
Al_2O_3	9	9	2.8	3.4	2.6	0.2-0.5
Si_3N_4	7.8	5.3	2.4	2.9	2.1	0.4
HfO_2	18	6	1.5	2.1	1.3	0.2
$ZrSiO_x$	12.6	6	1.5	2.1	1.3	0.3
ZrO_2	25	5	1.4	2.0	1.2	0.3

In summary, to build a crested barrier with steep $I-V$ curves, we need to consider the electron affinity and dielectric constant of the dielectrics, the work function of the metal electrode and the effective thickness of each layer. Just a few known CMOS compatible materials [36] may combine the barrier height sufficient for thermionic current suppression at room temperature (above 1.5 eV), with the necessary high breakdown field (above 10 MV/cm) and negligible trap-assisted tunneling. The list of such candidate materials is essentially limited to:

(1) silicon dioxide;

(2) low-trap density silicon nitride [37, 38]; and

(3) aluminum oxide grown by a variety of methods including thermal [39] and plasma [40] oxidation.

Published experimental work has shown that layered barriers made of several material combinations, including SiO_2/ZrO_2 [41], Si_3N_4/SiO_2 [42-45], Si_3N_4/Al_2O_3 [46], HfO_2/Al_2O_3 [46], $HfON/Si_3N_4$ [47], SiO_2/HfO_2 [48, 49], and $Al_2O_3/HfO_2/SiO_2$ [50], can indeed improve the sensitivity of tunneling transparency to voltage in comparison with the traditional uniform (e.g., SiO_2) barriers. Unfortunately, the transparency change scales demonstrated so far are still insufficient for the implementation of the NOVORAM concept. In particular, attempts by our group to combine two different (thermally-grown and plasma-grown) species of aluminum oxide [51] to form high-performance layered barriers have not been working so far, apparently due to the uncontrollable interfacial chemistry and/or charge trapping. However, in the process of this work we have found that uniform plasma-grown AlO_x, a material with high dielectric constant, large band gap and large barrier height, may approach the requirements of the so-called Floating-Gate Random-Access Memories (FGRAM) [52, 53]. The cell and matrix structure of FGRAM is similar to those of NOVORAM (Figure 1.2), and essentially the only difference is the necessity to refresh the FGRAM periodically, due to the relatively short retention time, just like this is being done in the usual dynamic random-access memories (DRAM). The goal of this work was to study the high-field endurance of AlO_x-based tunnel junctions, which is necessary for NOVORAM and FGRAM applications, within a much broader range of the aluminum oxidation and rapid thermal post-annealing (RTA) conditions than it had been done in our group's initial study [51].

In Chapter 2, I describe the results of our study of electron tunneling through junctions based on thin aluminum oxide layers, especially post-processed using rapid thermal annealing (RTA), with a focus on the bias voltage effects, including high field endurance.

B. Hybid CMOS/Nanoelectronic Circuits.

During the past few decades, numerous research groups have run into the experimental fact that thin layers of quite a few materials, including several organic compounds (sometimes with embedded metallic clusters), chalcogenides, metal oxides, amorphous silicon, and self-assembled molecular monolayers exhibit the "resistive memory effect" (resistive bistability).

The device with resistive bistability has an *I-V* curve with two branches corresponding to its two possible internal states, i.e. low-resistive (OFF) state and high-resistive (ON) state (Figure 1.3a). It may be switched between its ON and OFF states by applying voltages exceeding the corresponding threshold values V_t and V'_t. These studies have led to a virtual consensus that the resistive bistability, at least in metal-oxide and amorphous-silicon junctions, is due to the reversible formation and dissolution of one or few highly conducting spots (sometimes called "filaments"), due to field-induced drift of ions (depending on the particular material, either anions or cations) through the amorphous matrix of the layer – see Figure 1.3b-d [55, 56, 64].

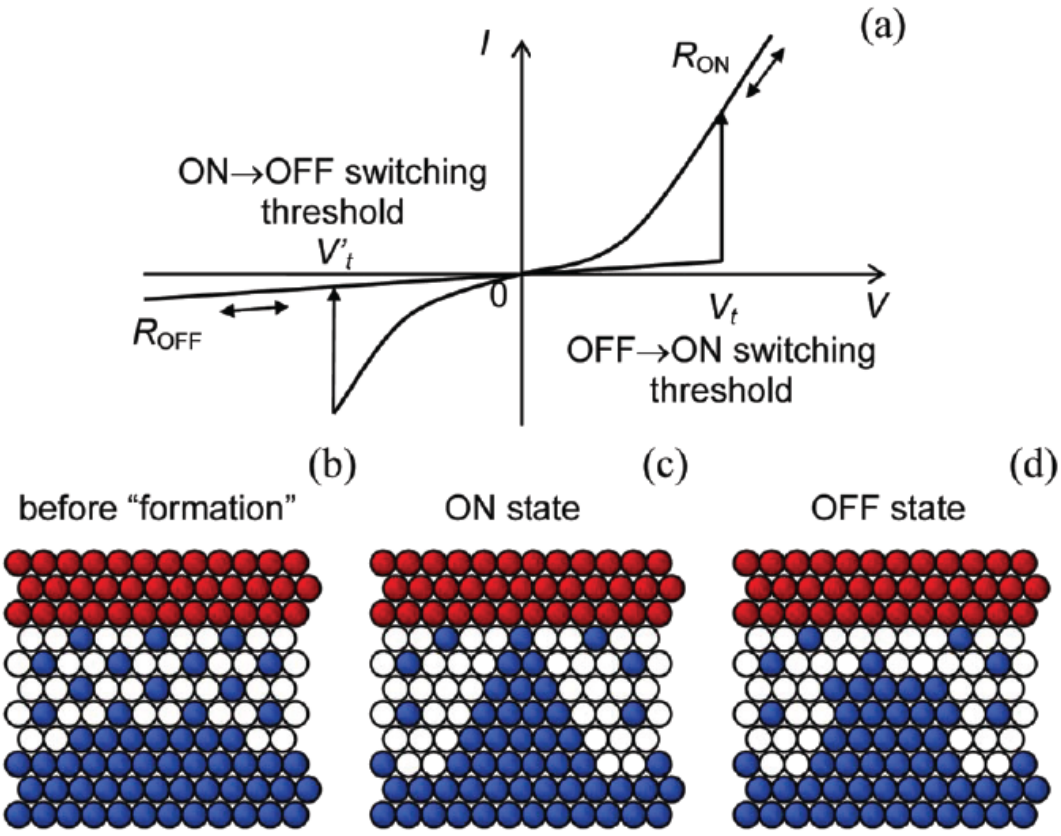


Figure 1.3 Resistive bistability in metal oxides: (a) the dc *I-V* curve (schematically), and the parameter nomenclature; (b), (c), (d) a cartoon of the apparent bistability mechanism.

Such simple two-terminal devices can serve as a memory cell storing one bit of information in its internal state, but cannot amplify signals as a transistor, and hence cannot be the sole basis for useful integrated circuits. However, a layer of very small devices of this kind, being added to a semiconductor-transistor circuit with much cruder features (Figures 1.4 and 1.5), can strongly enhance its functionality, without an unacceptable increase of the fabrication costs. This idea of hybrid CMOS/nanoelectronic circuits (in particular their variety called CMOL, initially standing for CMOs/MOLecular

circuits) [4], [54] has a fast progress during the past couple years.

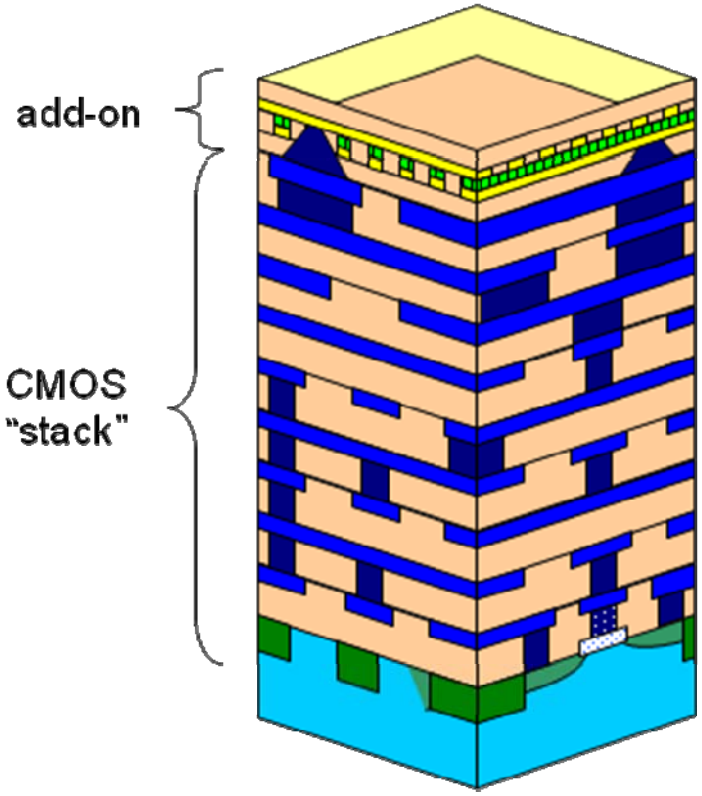


Figure 1.4 The general idea of a hybrid CMOS/nanoelectronic circuit.

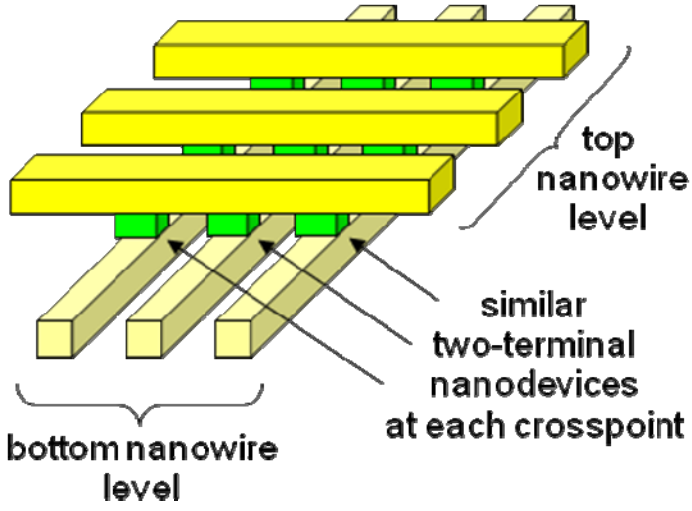


Figure 1.5 The nanowire-crossbar add-on (schematically).

A nanowire crossbar (Figure 1.5) contains simple, similar nanodevices (with resistive bistability, in our case) at each crosspoint. The crosspoint device would include a single-bit memory cell whose contents could control the connection of two nearby nanowires. In this way, the distributed crossbar memory may control the configuration of the system. Due to the sharp switching thresholds of these devices with resistive bistability (Figure 1.3a), each of them may be uniquely addressed, e.g., turned ON or OFF, applying appropriate voltages (close to $\pm 2/3\ V_t$) to the two corresponding nanowires. This produces the net voltage higher than V_t across the selected device, and switches it, without changing the states of other, "semi-selected" devices contacting just one of the nanowires.

In several recent studies, prospects of CMOL circuit applications in which the following systems have been explored [1].

1. CMOL memories, which are just a hybrid-circuit extension of resistive memories, with each bit stored in the internal state of a certain crosspoint device, but peripheral functions embodied in the CMOS subsystem, may enable eventually terabit-scale integration.
2. CMOL reconfigurable (FPGA-like) logic circuits may provide a density advantage of about 2 orders of magnitude over purely CMOS circuits of the same functionality and power density, at comparable speed.
3. Though custom CMOL VLSI circuits have not been explored to any detail yet, there are preliminary indications that these circuits will have a lower advantage in density, but substantially increased speed (again, at the same power).
4. Mixed-signal neuromorphic CMOL networks ("CrossNet") may provide extremely high performance for certain advanced information processing tasks such as pattern classification (including ultrafast feature recognition), and more intelligent tasks, in particular those requiring in-situ training and global reinforcement learning.

Based on these studies, one can summarize the requirements for resistive memory cells as follows [57]:

1. WRITE voltages V_{wr} should be in the range of a few hundred mV to few V. The desired duration of the WRITE voltage pulses τ_{wr} is below 100 ns.
2. READ voltages V_{rd} need to be significantly smaller than V_{wr}, but because of constraints by circuit design, V_{rd} cannot be less than approximately one tenth of

V_{wr}. In the ON state, the minimum READ current I_{rd} should not be less than approximately 1 μA to allow for a fast detection of the state by reasonably small sense amplifiers. The READ time t_{rd} must be in the order of τ_{wr} or preferably shorter.

3. A resistance ratio R_{OFF}/R_{ON} >10 is required to allow for small and highly efficient sense amplifiers.
4. The resistive memory should provide at least the same number of WRITE cycles as those of contemporary flash memories, which is 10^3 to 10^7, depending on the particular application.
5. A data retention time τ_{ret} in excess of 10 years is required for universal nonvolatile memories. This retention time must be kept at thermal stress up to 85ºC and small electrical stress such as a constant stream of V_{rd} pulses.

Chapter 3 describes our work on the fabrication and electrical characterization of junctions with resistive bistability, based on metal oxide thin layers of NbO_x, CuO_x, and TiO_x. In contrast to earlier work, we have emphasized the sample-to-sample reproducibility, as well as key parameters of resistance bistability, such as threshold voltages, ON/OFF conductance ratio and cycling endurance. High-resolution TEM studies have been carried out to reveal the microscopic structures of our junctions.

Chapter 2
Aluminum oxide tunnel barriers with high field endurance

2.1 Fabrication and experiment procedures

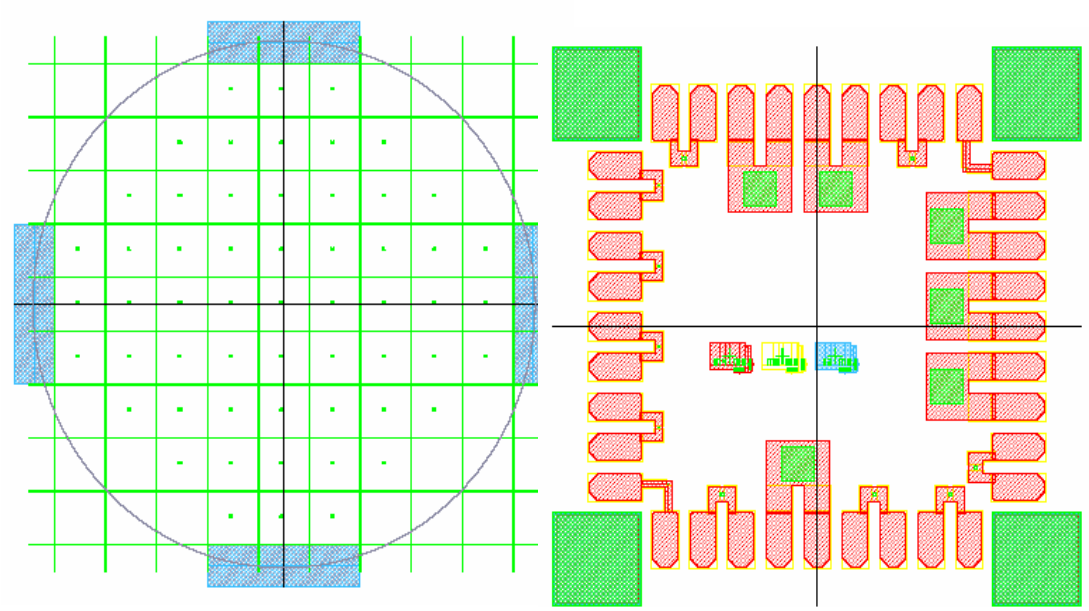
Tri-layer structures, which were the basis of our samples, have been grown on 2-inch silicon wafers (*p*-doped to resistivity ρ = 1-10 Ω·cm), covered by 500 nm of thermally grown SiO_2. Such a wafer has been loaded into a vacuum system, with a base pressure at $2\text{-}3\times10^{-7}$ Torr, which had been developed earlier for fabrication of standard Nb-trylayer junctions. The first layer of a 150-nm-thick niobium base film has been deposited by dc-magnetron sputtering at a rate of 1.6 nm/s. Without a vacuum break, a few-nm (usually 3 to 10 nm) aluminum thin film has been deposited by the same method at a lower rate of 0.5 nm/s. Under these conditions, aluminum thin films wet the niobium surface [58], forming a smooth uniform coating.

Following the aluminum deposition, it has been oxidized by either thermal oxidation or plasma oxidation. For thermal oxidation, a fixed amount of ultra-high-purity oxygen has been let into the vacuum chamber for a certain time (at room temperature). On the other hand, during plasma oxidation, we have used the same gas (static) as well as an oxygen flow (dynamic) at a fixed flow rate controlled by a mass flow meter, at oxygen pressure ranging from 5 to 75 mTorr. In this case, a 13.56 MHz rf power source has been

connected, via a tuned resonant circuit, to a dc-insulated copper plate on which the substrate had been mounted. This has resulted in a 10 to 250 W rf plasma discharge and wafer dc self-biasing to approximately -80 V relative to the ground (See Tables 2.1 and 2.2 for detailed fabrication parameters). This wafer has always been kept at room temperature by its thermal anchoring to the water-cooled copper plate.

After the oxidation, the chamber has been pumped down to the base pressure shown above, and a niobium counter-electrode (100 nm) has been deposited by the same method as the base electrode.

After the tri-layer deposition, the sample has been patterned (with areas A ranging from 3×3 to 300×300 μm^2, see Figure 2.1b for top view of a chip configuration) using deep ultra-violet (DUV) lithography with photo resist (PMMA) and reactive ion etching (RIE) in SF_6 plasma. Here, the same photomask was first used for the counter electrode definition using RIE, and later for a self-aligned lift-off of a dc sputtered 150-nm SiO_2 as insulation layer. This lift-off has opened contacts of junction counter-electrodes with another thicker niobium layer as wiring layer.



(a) Top view of 2-inch wafer (b) Top view of 5 × 5 mm^2 chip

Figure 2.1 (a) Top view of a 2-inch oxidized silicon wafer. This wafer has been diced into 57 5×5 mm^2 chips for further electrical characterization. (b) Top view of one 5×5 mm^2 chip containing 18 junctions whose areas has been defined to be 3×3 μm^2, 30×30 μm^2 and 300×300 μm^2.

After initial characterization, several samples from each wafer have been subjected to rapid thermal post-annealing (RTA) in an argon flow for 10 to 180 seconds at a temperature between 300 and 550°C.

Two-terminal DC current-voltage (*I-V*) measurements of both "as grown" and annealed junctions have been carried out at both room (~300 K) and liquid helium (LH, 4.2 K) temperatures, by a special low-noise, high-sensitive source meter (Keithley 6430). Voltage sweeps with different amplitudes and steps have been used to characterize transport properties until the oxide hard breakdown. In order to present low-voltage data

in more obvious form, we have frequently plotted the dynamic (differential) junction conductance $G \equiv dI/dV$ (in the log scale) as a function of V (in the linear scale).

2.2 Thermally oxidized (TO) wafer

Table 2.1 Fabrication parameters of thermally oxidized wafer.

Wafers	Base Electrode	Al	O_2 Pressure	Time	RTA
VJCB4	Nb, 50 nm	3 nm	100 Torr	50 min	400 to 500°C, 30 s

Table 2.1 has lists parameters of our only thermally oxidized wafer, VJCB4. Specifically, a 3-nm aluminum layer was deposited on top of the Nb base electrode for a thorough oxidation in pure oxygen. Some chips have been subject to RTA at 400 to 500°C for 30 s to improve transport properties.

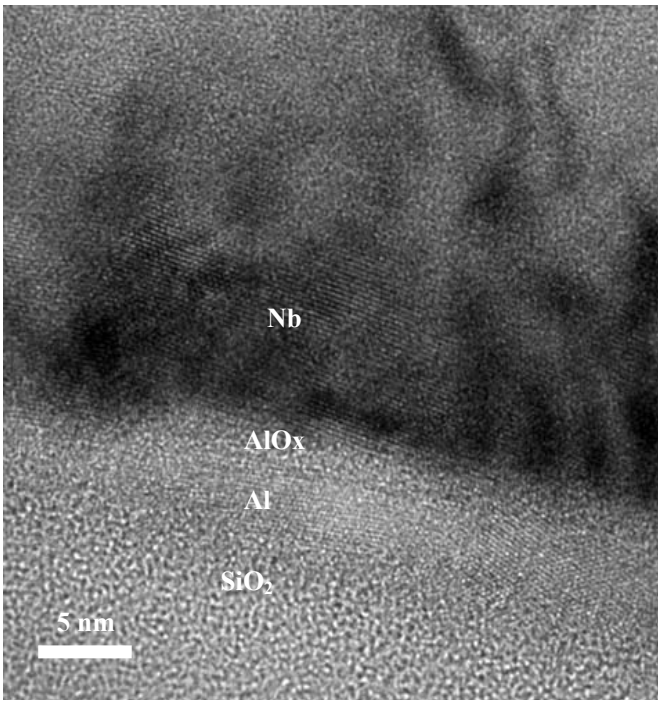


Figure 2.2 An HR TEM image of a sample from wafer VJCB4. The layer of aluminum oxide is amorphous and about 1 to 2 nm thick.

High resolution transmission electron microscopy (HR TEM, see Figure 2.2) study has shown that the aluminum oxide layer was amorphous, with a thickness of 1 to 2 nm.

Electrical characterization at room and LH temperatures has shown that the deep refrigeration shifts *I-V* curves by a small fraction (<5%), a good indication of direct quantum-mechanical tunneling – see Figure 2.3. However, the breakdown voltages were low (~1 V), which are not suitable for FGRAM applications. Further variation of RTA parameters did not improve the breakdown voltages.

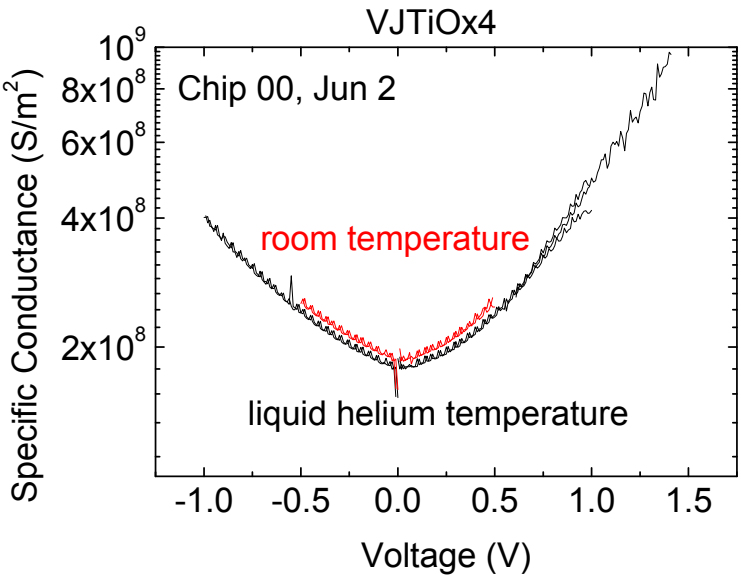


Figure 2.3: *G-V* curves for a junction from wafer VJCB4.

2.3 Plasma oxidized (PO) wafers

Table 2.2 Fabrication parameters of rf plasma oxidized wafers.

Wafers	Base Electrode	Al Layer	Rf Power	O_2 Pressure	Time
VJCB1	Nb, 125 nm	6 nm	50 W	15 mTorr	10 min
VJCB2	Nb, 125 nm	6 nm	50 W	15 mTorr	10 min
VJCB3	Nb, 100 nm	6 nm	50 W	75 mTorr	10 min
VJCB6	Nb, 50 nm	6 nm	50 W	15 mTorr	3 min
VJCB7	Nb, 50 nm	5 nm	50 W	15 mTorr	30 min
VJCB14	Nb, 50 nm	6 nm	50 W	15 mTorr	10 min
VJCB13b	Al, 50 nm	-	50 W	15 mTorr	10 min
VJCB17a	Al, 50 nm	-	10 W	15 mTorr	10 min
VJCB17b	Al, 50 nm	-	10 W	15 mTorr	10 min
VJCB17c	Al, 50 nm	-	10 W	15 mTorr	10 min
VJCB18	Al, 50 nm	-	100 W	15 mTorr	10 min
VJCB20	Al, 50 nm	-	100 W	15 mTorr	10 min
VJCB21	Al, 50 nm	-	250 W	5 mTorr	10 min
VJCB22	Al, 50 nm	-	10 W	5 mTorr	10 min
VJCB23	Al, 50 nm	-	10 W	30 mTorr	10 min
VJCB24	Al, 50 nm	-	10 W	60 mTorr	10 min
VJCB25	Al, 50 nm	-	25 W	60 mTorr	10 min

Table 2.2 shows fabrication parameters of all our wafers which were grown in an rf oxygen plasma. The rf power ranged from 10 to 250 W, oxygen pressure, from 5 to 75 mTorr and oxidation time from 3 to 30 minutes.

This rf plasma oxidation results in a uniform amorphous AlO_x layer with a thickness from 2 to 4 nm - see Figure 2.4 for an HR TEM image of a junction from wafer VJCB3.

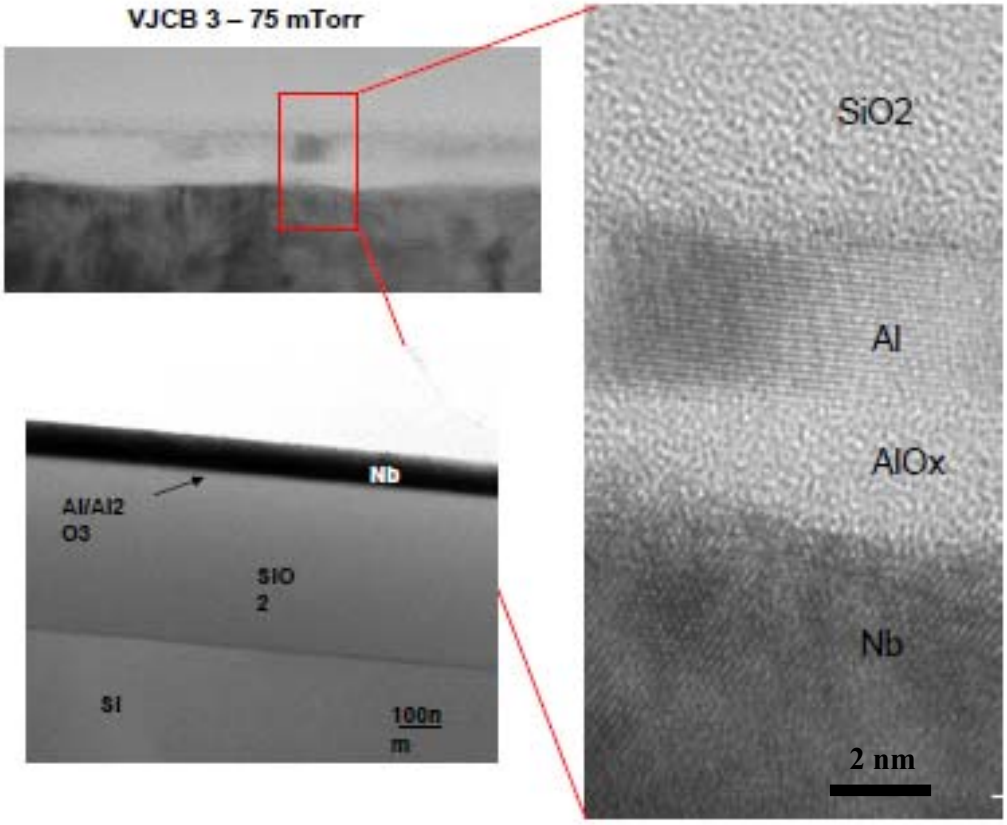


Figure 2.4 HR TEM images of a sample from wafer VJCB3.

For most wafers, several chips have been subjected to RTA for 10 to 180 seconds, at a temperature from 300 to 550°C. The reason not to anneal at higher temperatures is the existence of an aluminum layer whose melting point is close to 630°C. The electrical characterization has been performed as described above, and a few key features are summarized in Table 2.3 for as grown samples as well as samples after RTA, in most of wafers.

In the electrical measurements, we have first measured the zero-bias conductance $G(V=0)$ as dI/dV at zero bias voltage. During the voltage sweeps, their amplitudes have been carefully increased until the junction experienced an irreversible hard breakdown (to a very low resistive state, with $R \sim 10\ \Omega$). Then the breakdown voltage (V_{BD}) has been defined as the maximum amplitude of voltage sweeps (it is then always positive). For selected junctions, we have also done some extended study of the breakdown behavior in liquid helium temperature. This difference (if any) has also been shown in Table 2.3. The errors shown in the table is the r.m.s scattering of data from different junctions. (The actual accuracy of measurement of each sample was much better.)

Table 2.3 Breakdown voltage and zero conductance of plasma oxidized samples.

Wafer	V_{BD} at RT (V)	V_{BD} in LH (V)	$G(0)$ at RT(S/cm^2)	$G(0)$ in LH(S/cm^2)
VJCB1	3.1 ± 0.1	4.1 ± 0.1	0.71 ± 0.1	0.34 ± 0.1
VJCB2	3.0 ± 0.1	3.9 ± 0.1	0.19 ± 0.1	0.13 ± 0.1
VJCB3	3.1 ± 0.1	-	0.001 ± 0.1	-
VJCB6	2.5 ± 0.1	4.1± 0.3	0.63 ± 0.1	0.26 ± 0.1
VJCB7	2.7 ± 0.1	4.2± 0.1	0.25 ± 0.1	0.013 ± 0.1
VJCB13b	3.4 ± 0.1	4.1 ± 0.3	0.004 ± 0.1	0.003 ± 0.1
VJCB17a	2.5 ± 0.1	3.3 ± 0.1	8 ± 0.1	6 ± 0.1
VJCB17b	2.5 ± 0.1	-	95 ± 5	-
VJCB17c	2.5 ± 0.1	-	26 ± 3	-
VJCB18	3.2 ± 0.1	4.5 ± 0.2	0.0022 ± 0.0003	0.0010 ± 0.0003
VJCB20	3.1 ± 0.2	-	0.7 ± 0.1	-
VJCB21	3.4 ± 0.2	4.6 ± 0.2	0.0011 ± 0.0002	0.0006 ± 0.0001
VJCB23	2.5 ± 0.1	-	14 ± 2	-
VJCB24	2.8 ± 0.2	-	12 ± 2	-
VJCB25	2.5 ± 0.2	-	2.1 ± 0.3	-

Here in the table, V_{BD} and $G(0)$ have been measured for all wafers at room temperature (RT, i.e. ~300 K). Selected (not all) junctions have been dipped into a liquid helium (LH)

dewar with appropriate temperature meters and controllers, for measurement at cryogenic temperatures. These junctions are highly reproducible, with a nearly perfect scaling of the current with the junction area (Figure 2.5). Indeed, two junctions with the same area have shown virtually identical *I-V* curves, while the other junction with area of two orders of magnitude less, producing current at a lower level with the same current density. We also noticed a slight increase (usually ~ 0.1 to 0.2 V) of V_{BD} for smaller areas, indicating the potential of scaling down for performance improvements. Also, within all the range of fabrication conditions, the junctions show exponentially nonlinear *I-V* curves (Figures 2.5 and 2.6) with a very weak temperature dependence (<15% for most junctions, see, Figure 2.6).

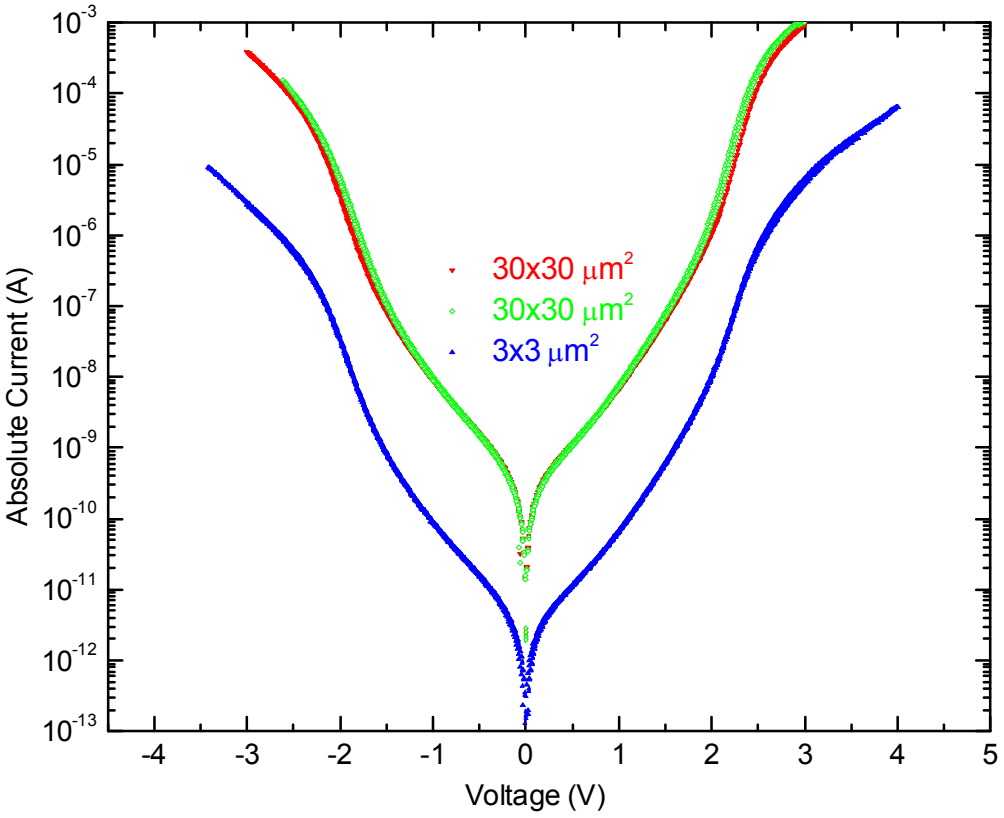


Figure 2.5 Typical *I-V*s from three junctions of wafer VJCB17a. These junctions show great reproducibility and scaling with areas.

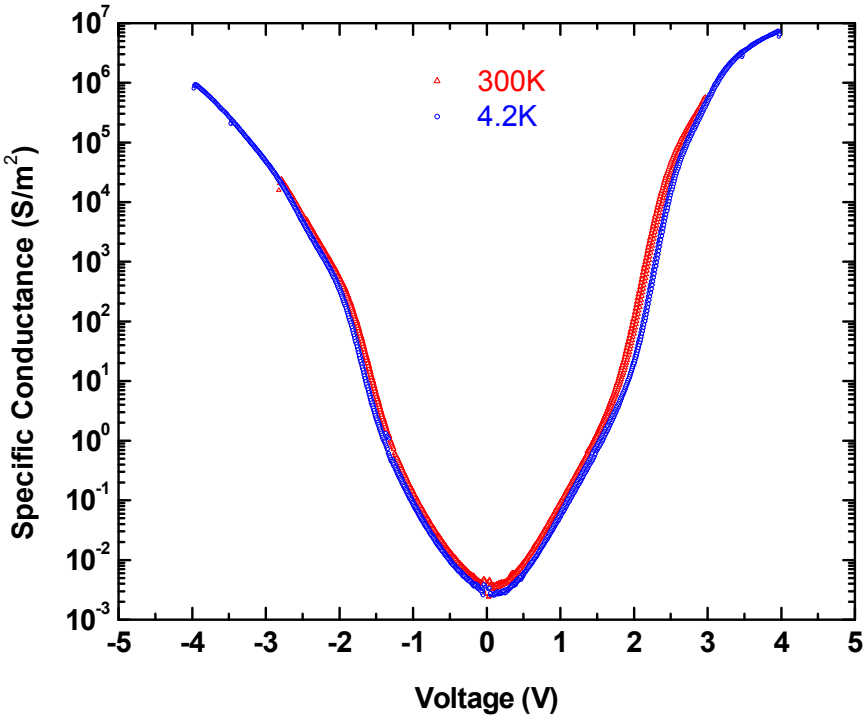


Figure 2.6 Temperature dependence of *G-V* curves from one junction of wafer VJCB17a.

These results may be explained by single-shot tunneling of electrons through the whole AlO_x layer [51].

We have also done some extended research on the RTA effect, and the results of an RTA at 400°C for 180 s have been summarized in Table 2.4.

Table 2.4 RTA (at 400°C for 180 s) effect on some plasma oxidized wafers.

Wafers	V_{BD} at RT (V)	V_{BD} in LH (V)	$G(0)$ at RT(S/cm^2)	$G(0)$ in LH(S/cm^2)
VJCB13b	3.0 ± 0.1	4.5 ± 0.1	0.008 ± 0.002	0.003 ± 0.001
VJCB17a	3.3 ± 0.2	4.5 ± 0.3	2.2 ± 0.2	1.6 ± 0.2
VJCB17b	3.1 ± 0.2	-	0.20 ± 0.05	-
VJCB17c	3.0 ± 0.2	-	1.0 ± 0.2	-
VJCB18	3.8 ± 0.2	4.0 ± 0.2	0.0020 ± 0.0005	0.0010 ± 0.0003
VJCB21	4.4 ± 0.4	5.1 ± 0.2	0.0010 ± 0.0002	0.0005 ± 0.0001
VJCB22	3.0 ± 0.2	-	4.4 ± 0.5	-
VJCB23	3.4 ± 0.2	-	1.1 ± 0.2	-
VJCB24	3.8 ± 0.2	-	0.58 ± 0.05	-

We have observed the increase of V_{BD} for virtually all junctions as well as the decrease of $G(0)$ after RTA at temperatures from 300°C to 500°C. Typical *I-V* curves of annealed samples were shown in Figures 2.7 and 2.8 for different annealing temperatures and duration, from junctions of wafer VJCB17b.

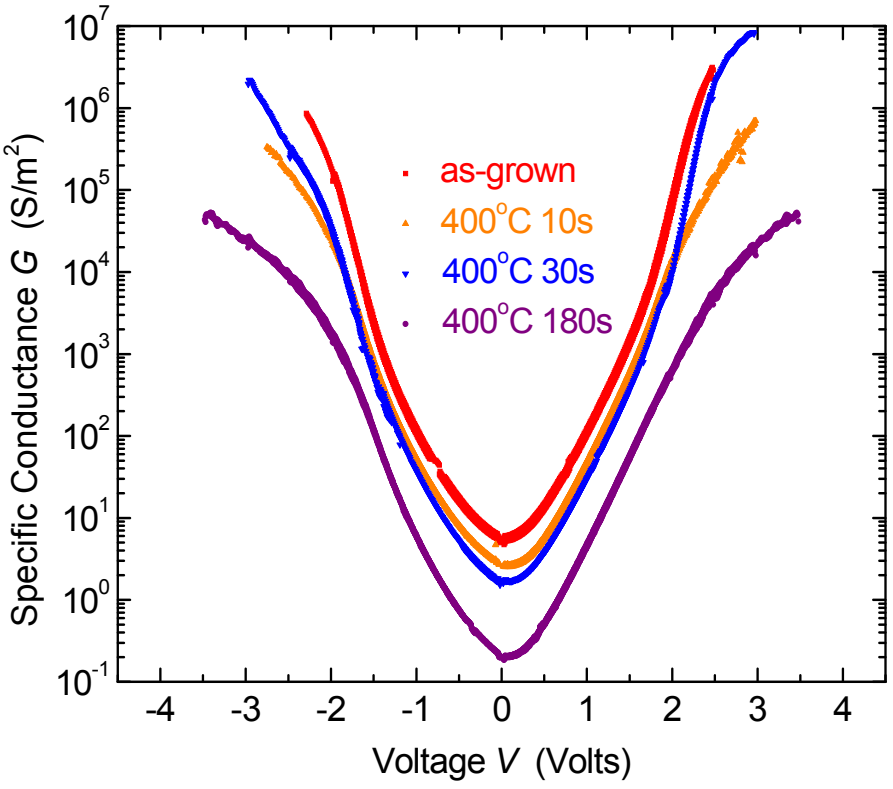


Figure 2.7 *G-V* curves of junctions of wafer VJCB17b for different durations of annealing at 400°C.

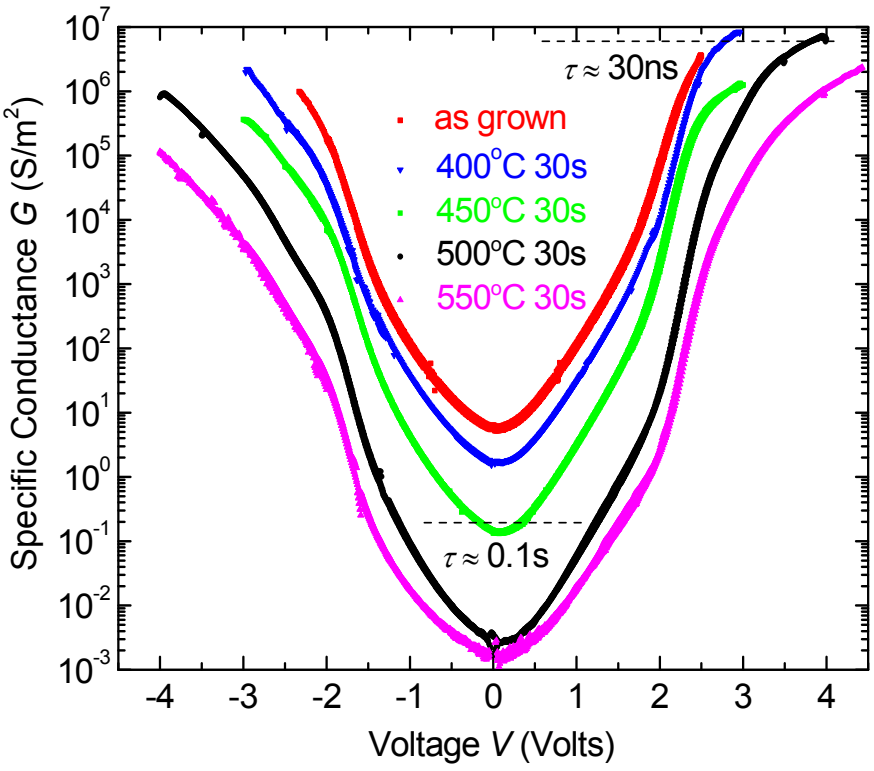


Figure 2.8 *G-V* curves of junctions from wafer VJCB17b, with different RTA temperatures, for 30 seconds.

As Figures 2.7 and 2.8 show, the junctions tend to have higher V_{BD} and lower $G(0)$ at higher annealing temperature and longer annealing time. We have also observed the post-annealing results in a substantial improvement of the junction endurance in high electric fields. In particular it increases the static breakdown field well above 10 MV/cm at room temperature (and above 15 MV/cm at 4.2K), i.e. substantially beyond that of the best SiO_2 layers we are aware of. The floating gate recharging time scale is defined as $\tau \equiv CV/I(V)$, where C is the junction capacitance, V and $I(V)$ are applied voltage and

tunneling current of the junction, respectively. Because of this high field endurance of our AlO_x junctions, the applied voltage may change the time scale τ by more than 9 orders of magnitude. i.e. the junction with RTA at 500°C for 30 seconds shown in Figure 2.8, has the write (program) time of $\tau \approx 10$ ns at $V \approx 3.5$V, and the retention time $\tau \approx 10$ s at $V = 0$ V.

2.4 Simulation and fitting results

Based on the free electron approximation [59], direct coherent tunneling current through typical metal-insulator-metal devices may be calculated by jointly solving the Schrodinger equation and Poisson equations. Assuming that the energy of the tunnel electron and the transverse component of the momentum are both conserved, the tunneling current density is given by:

$$J = \frac{em_e}{2\pi^2\hbar^3}\int_0^\infty dE_x \int_0^\infty dE_\perp \mathcal{T}(E_x, E_\perp)[f_L(E_x, E_\perp) - f_R(E_x, E_\perp)] \qquad (2.1)$$

where $\mathcal{T}$ is the transmission coefficient; E_x, $E_\perp$ are the local energy and the transverse energy of a tunneling electron; m_e is the effective mass of the transverse electron and f_L, f_R are the equilibrium Fermi-Dirac distribution functions in the left and right electrodes.

We can use a 1D model to describe the barrier profile. The tunneling current density includes the carrier transport in both directions between two metal contacts. In the case of $T = 0$, the Fermi energy function of the metal is written as:

$$f_i(E_x, E_\perp) = \begin{cases} E_{fi}, if\ E_x \le E_{fi} \\ 0, if\ E_x \ge E_{fi} \end{cases},\ i = L, R \qquad (2.2)$$

where E_{fL} and E_{fR} are Fermi energies of left and right metal layers, respectively. Using this function, the current density J may be simplified as:

$$J = J_{L\to R} - J_{R\to L} = \frac{em_e}{2\pi^2\hbar^3}\left[eV\int_0^{E_{fL}-eV}\mathcal{T}(E_x)dE_x + \int_{E_{fL}-eV}^{E_{fL}}\mathcal{T}(E_x)(E_{fL}-E_x)dE_x\right] \quad (2.3)$$

For the case of $T > 0$, we assume that the electrons are distributed according to equilibrium Fermi-Dirac distribution in both electrodes, determined by the bulk Fermi levels on the respective sides of the barrier:

$$f_L(E_x, E_\perp) = 1/(1+\exp\left(\frac{E_x+E_\perp-E_{fL}}{k_BT}\right); \quad (2.4)$$

$$f_R(E_x, E_\perp) = 1/(1+\exp\left(\frac{E_x+E_\perp-E_{fL}+eV}{k_BT}\right) \quad (2.5)$$

After integration over the transverse energy $dE_\perp$ for the second integral in equation (2.1), we obtain:

$$j = \frac{em_e}{2\pi^2\hbar^3}k_BT\int_0^\infty \mathcal{T}(E_x)\ln\left(\frac{1+e^{(E_{fL}-E_x)/k_BT}}{1+e^{(E_{fL}-E_x-eV)/k_BT}}\right)dE_x \quad (2.6)$$

This result is called the Tsu-Esaki formula, and the logarithmic term is named the "supply function".

The key parameter in the tunneling current is the transmission coefficient $\mathcal{T}$. To calculate $\mathcal{T}$, we have used the transfer matrix formalism method to numerically solve the Schrodinger equation and Poisson equation. [60] By breaking the potential barrier into N sequential pieces (Figure 2.9), the transmission coefficient can be calculated to arbitrary precision (in the independent-electron picture). For each slice i, the Schrodinger equation can be solved analytically, its transmission matrix found as:

$$\frac{1}{2}\begin{pmatrix} e^{jk_i a} & 0 \\ 0 & e^{-jk_i a} \end{pmatrix}\begin{pmatrix} 1+k_i m_{i+1}/k_{i+1}m_i & 1-k_i m_{i+1}/k_{i+1}m_i \\ 1-k_i m_{i+1}/k_{i+1}m_i & 1+k_i m_{i+1}/k_{i+1}m_i \end{pmatrix} \quad (2.7)$$

where $k = \sqrt{2m(E-U)}$ for slice i. Then the total transfer matrix may be found as a product of such matrices calculated for each slice, and the transmission coefficient $\mathcal{T}$ calculated as:

$$\mathcal{T} = \frac{m_L k_R}{m_R k_L}\left|\frac{A_{N+1}}{A_N}\right|^2 = \frac{m_L k_R}{m_R k_L}|\tau_N(1,1)|^2 \quad (2.8)$$

where m_L and m_R are the effective electron masses in the junction electrodes, $\hbar k_{L,R}$ is x component of the momentum of electron in left or right electrodes, $|A_0|^2$ is the amplitude of incoming wave function in the left electrode, $|A_{N+1}|^2$ is the amplitude of outgoing wave function in the right electrode. After the transmission coefficient $\mathcal{T}$ has been obtained for each value of E_x, current density may be calculated from Equation (2.6) by numerical integration over all substantial energies (typically, within a few hundred meV below the highest Fermi surface).

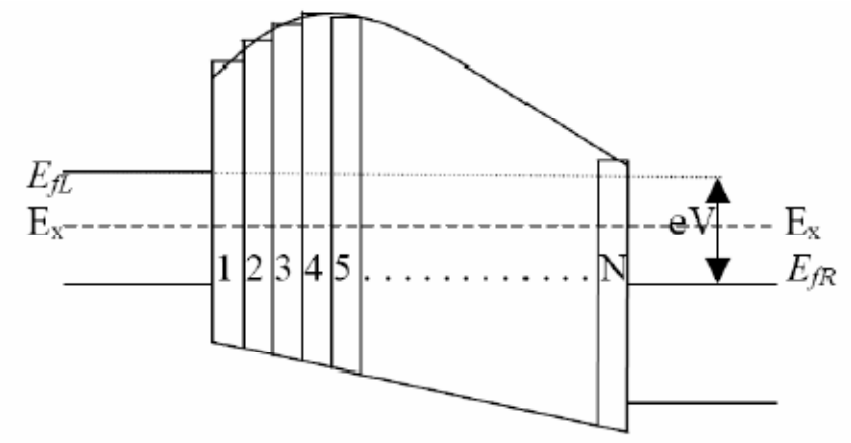


Figure 2.9 Illustration of the potential barrier diagram divided by *N* piece

Figure 2.10 and Figure 2.11 show quantitative simulation results by Matlab, using hot electron model to obtain the barrier height and thickness. The simplest junction geometry is a tilted tunnel barrier between two niobium electrodes.

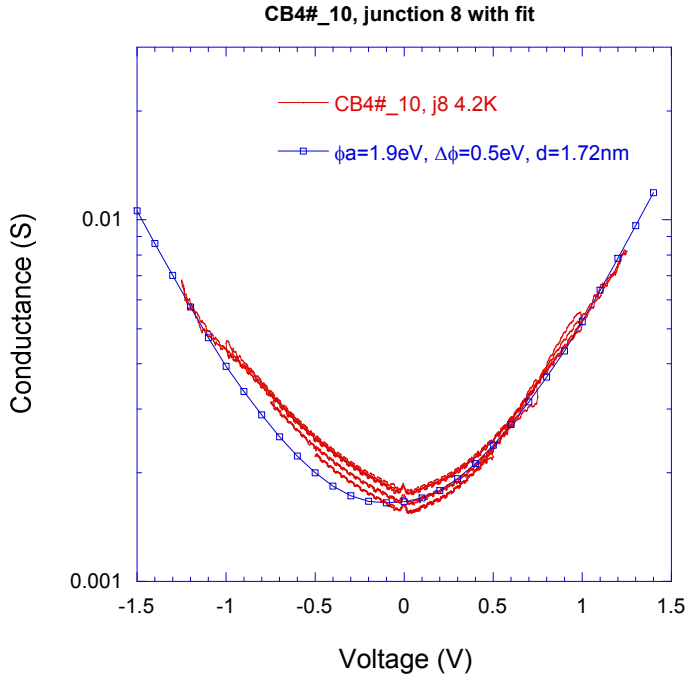


Figure 2.10 *G-V* fitting of a junction from thermally oxidized wafer VJCB4.

Figure 2.10 shows the results of such fitting for one of the thermally oxidized junctions from wafer VJCB4. Here the average barrier height of thermally oxidized aluminum oxide is φ=1.9 eV, with $\Delta\varphi$=0.5 eV, with the effective electron mass m_e=0.32m_0 and the barrier thickness is d=1.72 nm. This thickness is close to that obtained by the direct observation of the oxide layer in the HR TEM image of a similar junction (see Figure 2.2).

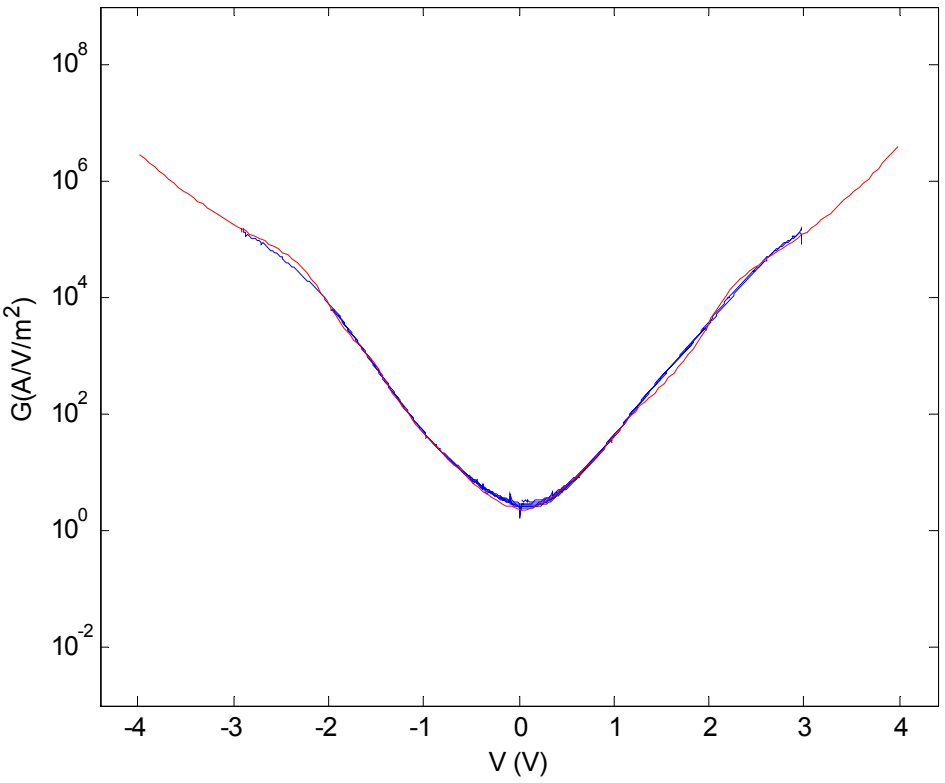


Figure 2.11 *G-V* fitting of a junction from plasma oxidized wafer VJCB3.

In Figure 2.11, the average barrier height is φ=2.5 eV, with $\Delta\varphi$=1.25 eV, with electron effective mass m_e=0.5m_0 and the barrier thickness is d=2.8 nm, with the last number close to the direct observation of the oxide layer in the HR TEM image of a similar junction in Figure 2.4.

This simulation method has also been applied to the post annealed junctions, in order to get an idea of the physical change of aluminum oxide tunnel barriers as a result of the RTA. Figure 2.12 shows simulation results of junctions from wafer VJCB17a at various

RTA temperatures for 30 seconds. Figures 2.13 and 2.14 summarize the fitting parameters.

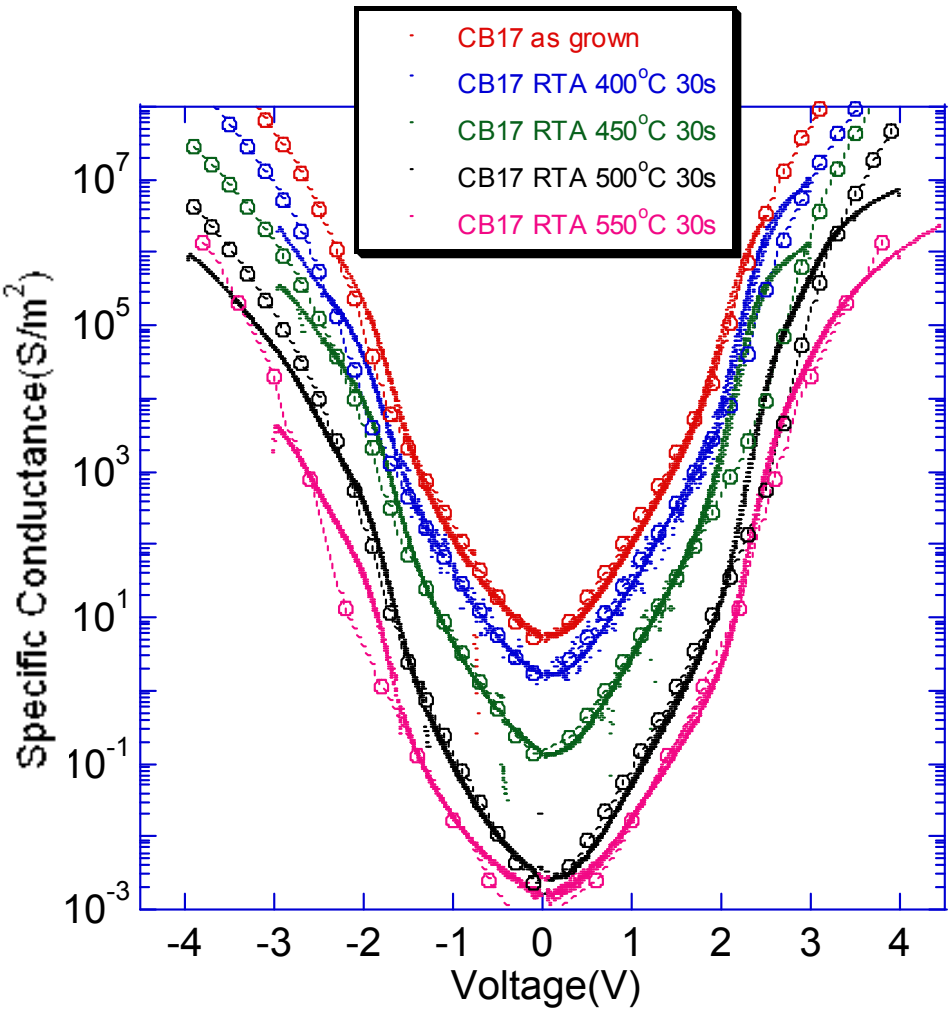


Figure 2.12 *G-V* fitting of a junction from plasma oxidized wafer VJCB17a with various RTA temperatures from 400 to 550°C for 30 seconds.

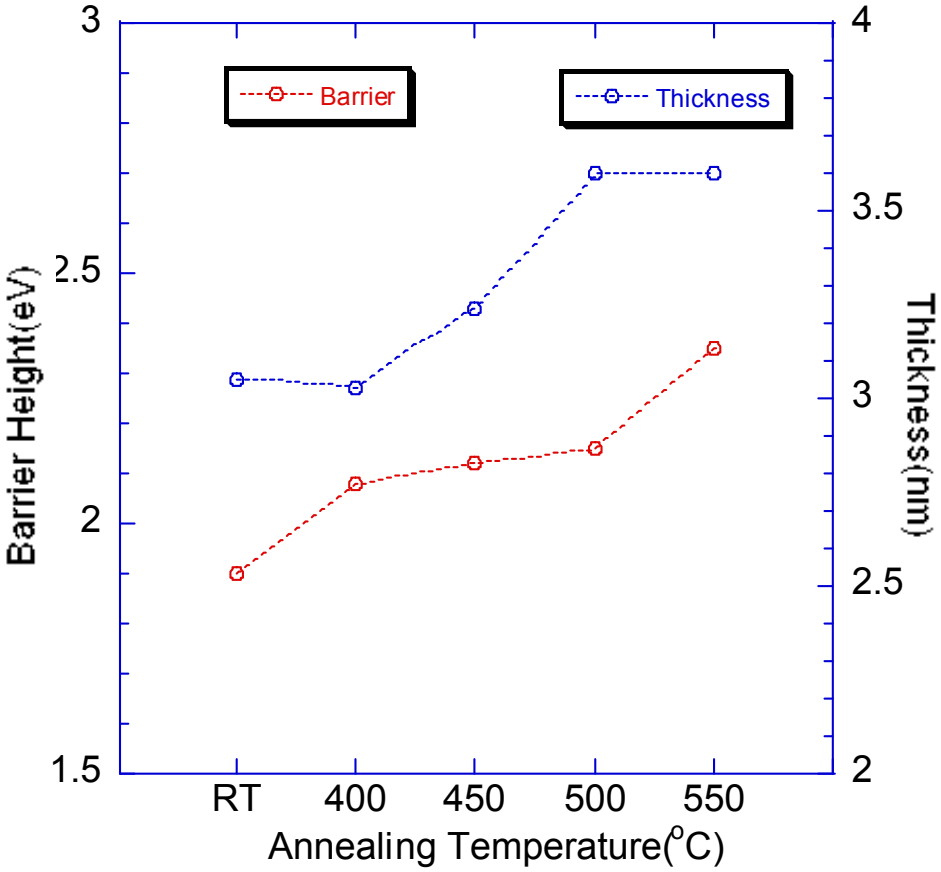
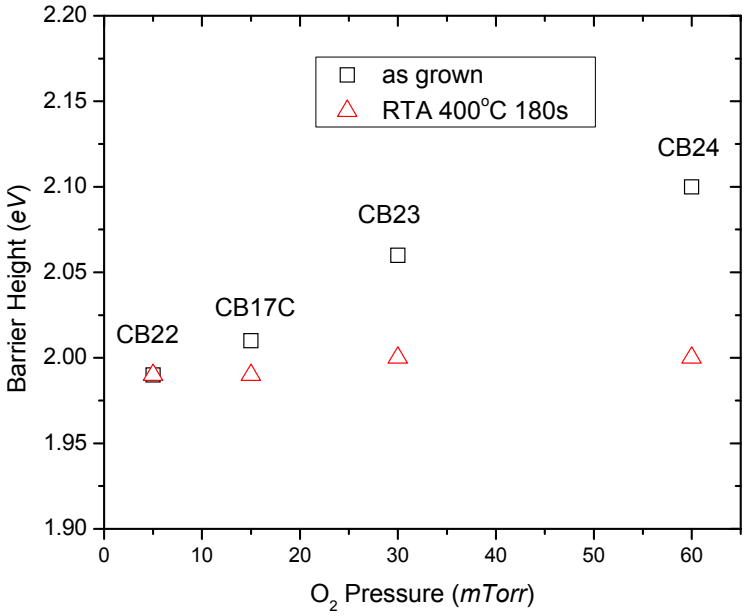


Figure 2.13 Aluminum oxide tunnel barrier height and thickness obtained from Matlab simulation for junctions of wafer VJCB17a within RTA temperatures ranging from 400 to 550°C for 30 seconds.



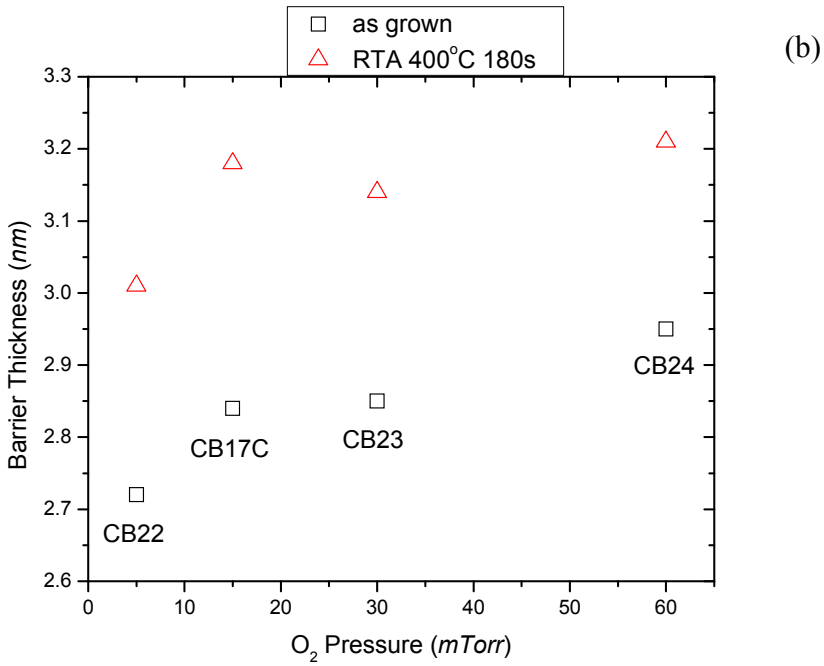


Figure 2.14 (a) Aluminum tunnel barrier height and (b) barrier thickness, obtained from Matlab simulation for junctions of wafer VJCB17c, 22, 23 and 24 with O_2 pressure ranging from 5 to 60 mTorr during plasma oxidation.

It shows a clear trend of increasing barrier height and thickness with higher RTA temperature, probably due to the diffusion-induced redistribution of oxygen anions, with an effective height from 1.9 to 2.5 eV and an effective thickness $d_{ef} \equiv (m_{ef}/m_0)^{1/2} d$ from 1.75 to 2.5 nm (depending on the particular oxidation and annealing parameters). The latter numbers may be reconciled with the HR TEM results (Figure 2.4), assuming that the effective carrier mass m_{ef} in the conduction band of the aluminum oxide is between 0.3 and 0.5 m_0 [29, 30].

2.5 Attempts at double layer fabrication

Since we were able to fabricate two types of aluminum oxide (PO and TO), with different barrier height, the realization of "crested barriers" seemed possible. Our initial attempts were just to combine these two kinds of aluminum oxide to form a double layer.

We have fabricated 3 wafers (Table 2.5) with TO/PO double layers. After the first wafer (VJCB11) with TO AlO_x followed by PO AlO_x, other two wafers (VJCB16 and 19) have been fabricated using PO AlO_x as the first layer. That was done because the strong power of rf-plasma discharge might influence on the thin layer of thermally grown aluminum oxide during the fabrication.

Figure 2.15 shows the $G-V$ characteristics of both versions of combined layers, measured at 4.2 K. Although we did see a lowering of the zero-bias conductance compared to PO AlO_x alone, the conduction change range is too small and the overall $G-V$ curves are very similar to those of PO AlO_x. This means that the effect of thermally

grown aluminum oxide is not prominent here, even after the rapid thermal annealing. The theoretical $G-V$ curve, calculated by using the best fitting parameters of the individual layers, predicts a zero-bias conductance which is smaller than the experimental value by at least two orders of magnitude.

We believe that the reason of this discrepancy is the crucial role of the interfacial geometry and chemistry in the double layer structure. If the first layer is too thin (~1 nm), the interface may not be continuous. Instead of the continuous layer, there are probably aluminum grains on the surface instead of the continuous layer, which could become traps that trap electric charges, strongly affecting the barrier profile and hence the current. Also, if the second aluminum layer is too thick, there will be part of it not oxidized thoroughly. As a result, the double layer structure would become sequential tunnel barrier, and does not form the crested barrier we expected. One more factor might be some uncontrollable interfacial chemistry.

Thus, our first few attempts at construction of "crested barriers" have failed probably due to the formation of an uncontrollable interface during our fabrication process.

Table 2.5 Fabrication parameters of PO/TO double layer aluminum oxide tunnel barriers.

Wafer	Oxidation	Base Electrode	Al layer	Power	O_2 Pressure	Time
VJCB11	Thermal	Al, 50 nm			100 Torr	40 min
	Plasma		3.8 nm	50 W	15 mTorr	10 min
VJCB16	Plasma	Al, 50 nm		50 W	15 mTorr	10 min
	Thermal		1.5 nm		100 Torr	40 min
VCJB19	Plasma	Al, 50 nm		50 W	15 mTorr	10 min
	Thermal		3.0 nm		100 Torr	40 min

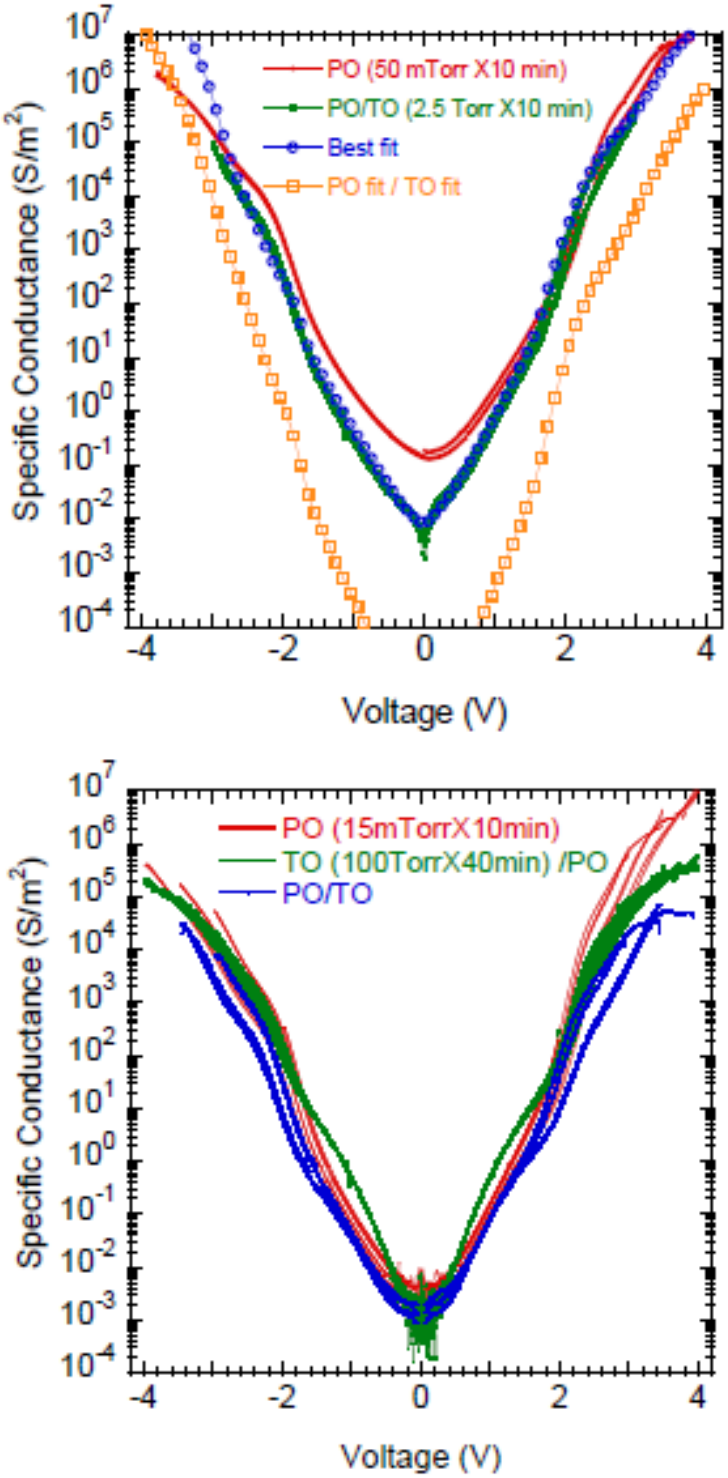


Figure 2.15 Typical *G-V* curves from junctions of double layer wafers.

2.6 Oxide breakdown and endurance test

Silicon oxide breakdown has been extensively studied for a few decades [61-63]. The generally accepted models of the breakdown include defect accumulation and/or local heating effects.

We have explored the field endurance characterized by the applied voltage resulting in oxide breakdown. We define V_{BD} as the threshold voltage of oxide breakdown, t_{BD} as the total time of a set of square-wave voltage pulses the junction can endure before its irreversible hard breakdown, $Q_{BD}= I(V)t_{BD}(V)$ as total charge transport before breakdown ("charge-to-breakdown", shortened as CBD). For example, Figure 2.16 shows values of V_{BD} at room temperature and liquid helium temperature, for junctions fabricated at various rf plasma power from 10 to 250 W).

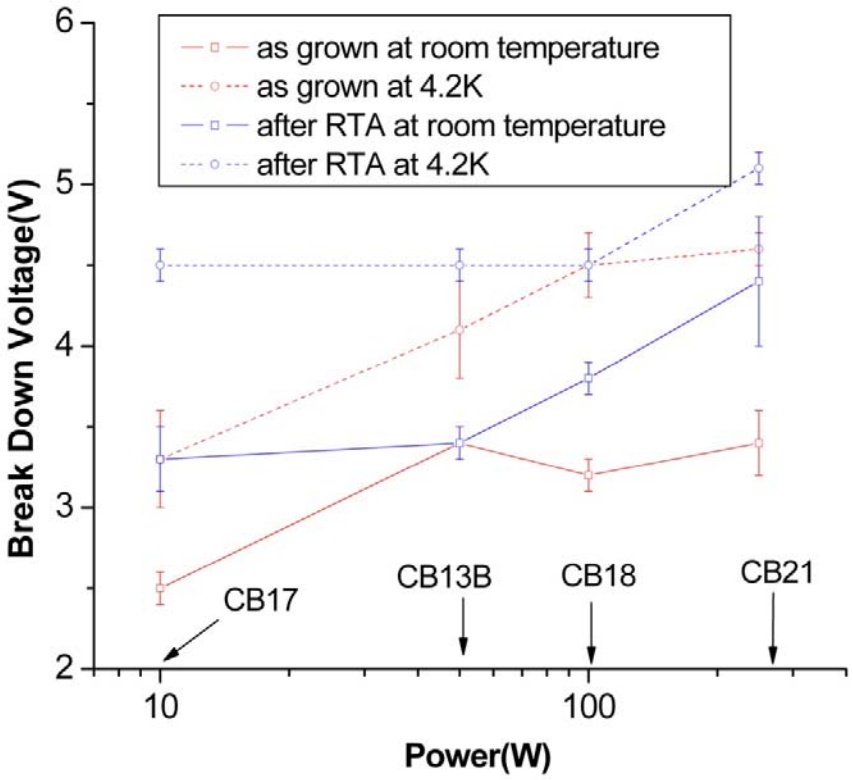


Figure 2.16 Breakdown Voltage V_{BD} at room temperature and liquid helium temperature, for junctions fabricated at various rf plasma power from 10 to 250 W, as grown or after RTA at 400°C for 30 seconds.

Figure 2.17 gives an example of voltage pulse sequences, with V_p (2 to 4 V) and t_p (100 ns to 10 ms) being the amplitude and duration of applied voltage pulses. After an individual voltage pulse, a small READ voltage (V_{rd} ~0.05 V) for a relatively longer period (t_{rd} ~a few hundred milliseconds) is applied to determine the state of the junction (i.e. "working" or "breakdown"). We have counted the total number of voltage pulses to calculate breakdown time $t_{BD}(V)$.

As Figure 2.18 shows, Q_{BD} depends on the applied waveform frequency f, increasing as the pulse duration drops to below a few microseconds. (This dependence may be explained by the defect accumulation mechanism [63].) However, even the lower values of Q_{BD}, observed for static applied voltage, may exceed 10^5 C/cm^2, the number to be compared with ~10^1 C/cm^2 for SiO_2 barriers used in the traditional floating-gate memories [27]. There are at least two reasons responsible for this huge difference. First, due to the lower energy barrier (~2 eV), AlO_x layers may operate at lower voltages (3 to 4 V), and Q_{BD} typically drops fast with voltage – see, e.g., Figure 2.19 [62]. Second, these layers may work with metal electrodes. Such electrodes have much smaller (0.1-nm-scale) field screening length and hence may reduce the back flow of holes from the anode, which is believed to be one of the main mechanisms for defect generation [61].

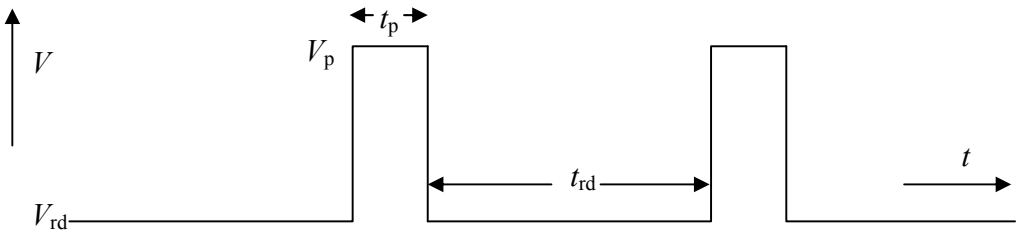


Figure 2.17 Schematic illustration of voltage pulses used in endurance test. V_p and t_p are the amplitude and duration of applied voltage pulses, and V_r and t_r are a small (~50 mV) reading voltage and its duration.

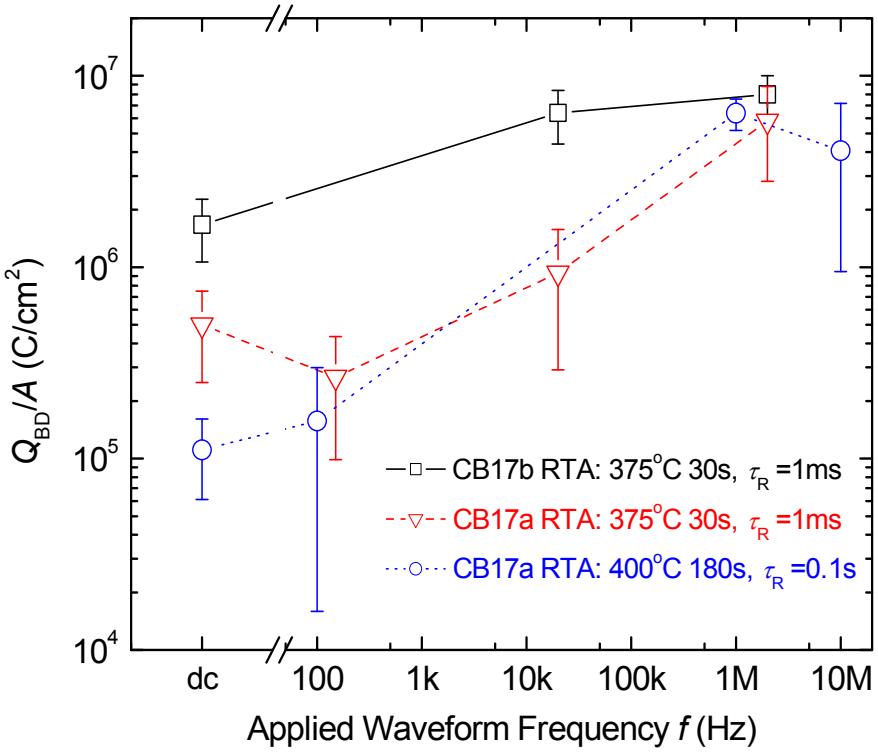


Figure 2.18 Frequency dependence of Q_{BD} for same amplitude of voltage pulses, in the range of 100 Hz to 10 MHz, as well as dc applied voltages.

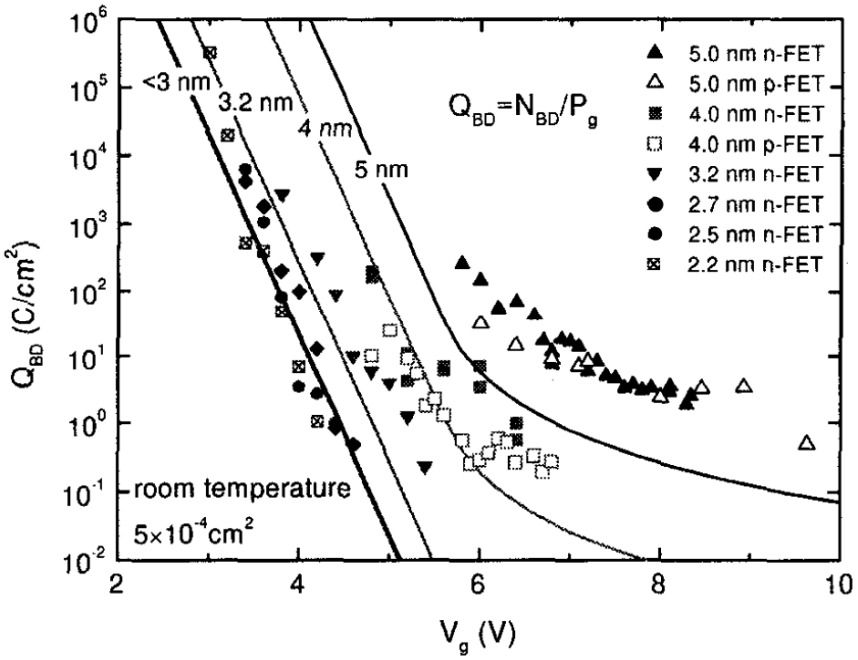


Figure 2.19 Q_{BD} dependence of applied voltages. [62]

Figure 2.20 shows Q_{BD} at various applied voltages for junctions from several wafers. It confirms that Q_{BD} has strong dependence on V_{BD} in the range of 2 to 4 V. Since the specific capacitance C/A of our junctions is between 1.5 and 2.2 μF/cm^2, which is somewhat higher than SiO_2, a more fair figure-of-merit of the endurance is $N(V) \equiv Q_{BD}(V)/CV$, which may be interpreted as the upper bound to the number of write/erase pulses the junctions may allow in memory cells. In particular, the higher values of Q_{BD}/A shown in Figure 2.18 correspond to N is excess of 10^{12}. Such endurance is already sufficient for those embedded RAM applications (in particular in mobile phones and consumer electronics microcontrollers) which currently serve as the main drivers for the integrated circuit technology progress. (The only required architecture modification is the

addition of simple wear-leveling circuitry.)

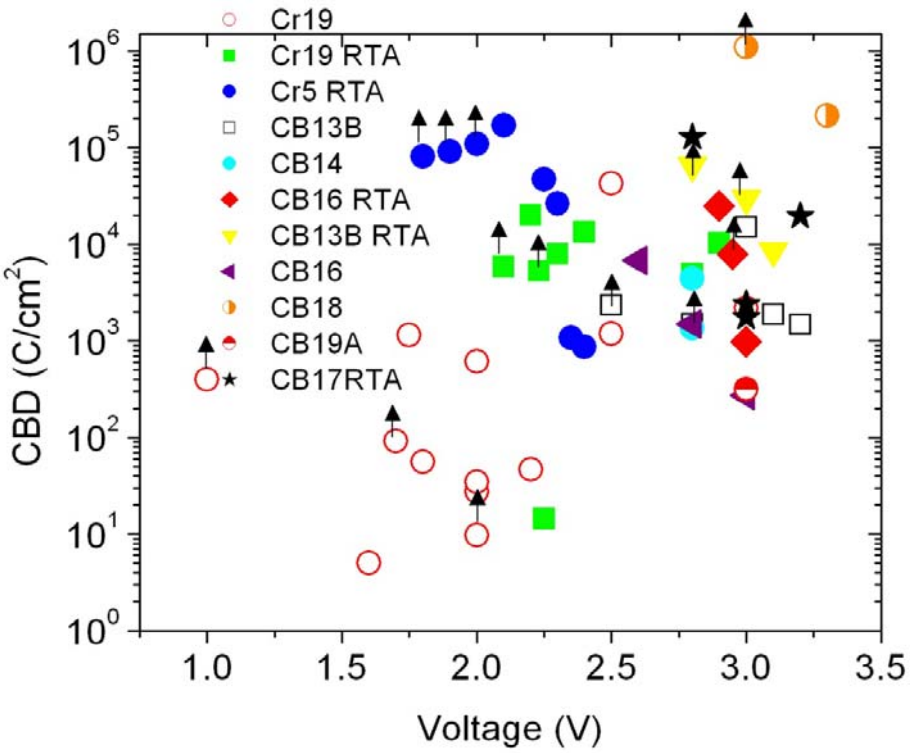


Figure 2.20 Voltage dependence of Q_{BD} for junctions of several wafers.

Both $Q_{BD}(V)$ and $I(V)$ are exponentially dependent on the applied voltage V [62], according to our results shown in Figures 2.5 and 2.20. In Figure 2.21, we have plotted N vs τ in Log scale to find quantitative characterization of breakdown behavior of our junctions from wafers VJCB17a, b and c (these three wafers are fabricated at same conditions to verify reproducibility). From what we have seen in the plot, most of data followed a linear relationship and we could expect that a combination N/τ^{α}, with some α, would be weakly dependent on V. Empirically we have found that $\alpha = 2$ is virtually the best choice, within the most interesting range of τ - between 10 and 200ns. Figure 2.22

shows a fitting curve of ln(N) vs ln(τ) with a linear slope of 2. Then the ratio N/τ^2 and the retention time scale $\tau_R \equiv C/G(0)$ as functions of post-annealing parameters and oxygen pressure at tunnel layer growth, have been shown in Figures 2.23 and 2.24, respectively. Notice that the plotted N corresponds to the static voltage endurance. Incorporating the improvement by the dynamics factor ~10 visible in Figures 2.7 and 2.8, we may estimate that after optimized fabrication and post-processing (see Figures 2.23 and 2.24) our junctions may combine sub-30-ns write/erase times with ~10^{12} cycle endurance, and retention time of the order of 0.1 s (sufficient for refresh). The scaling results (Figure 2.5) allow us to expect even higher endurance in smaller (i.e. sub-100-nm) junctions.

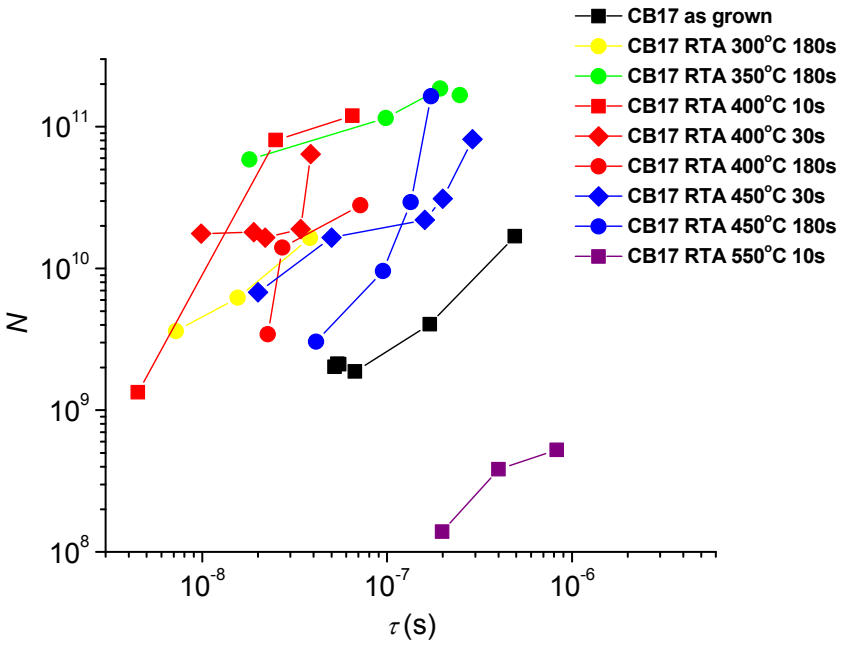


Figure 2.21 N vs τ for junctions of wafer VJCB17a, with different RTA conditions.

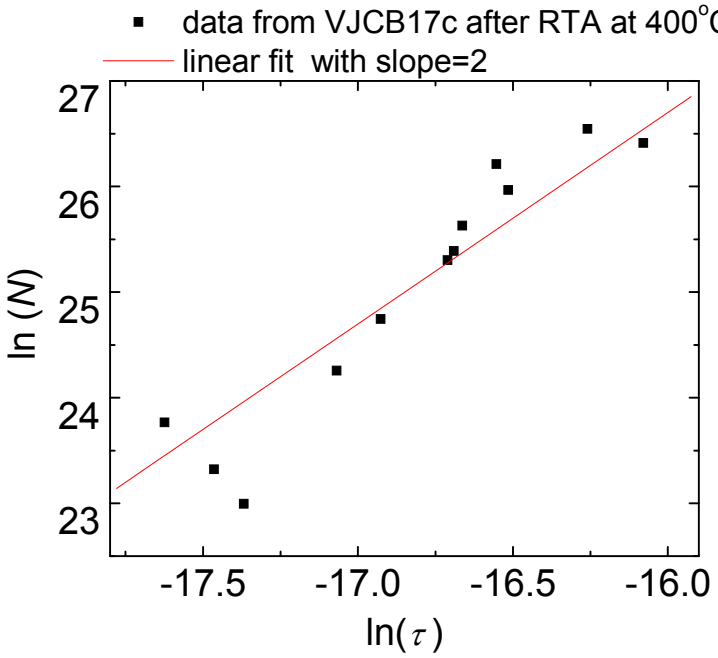


Figure 2.22 Linear fit of ln(N) vs ln(τ) for junctions of wafer VJCB17c, after RTA at 400ºC for 30 seconds.

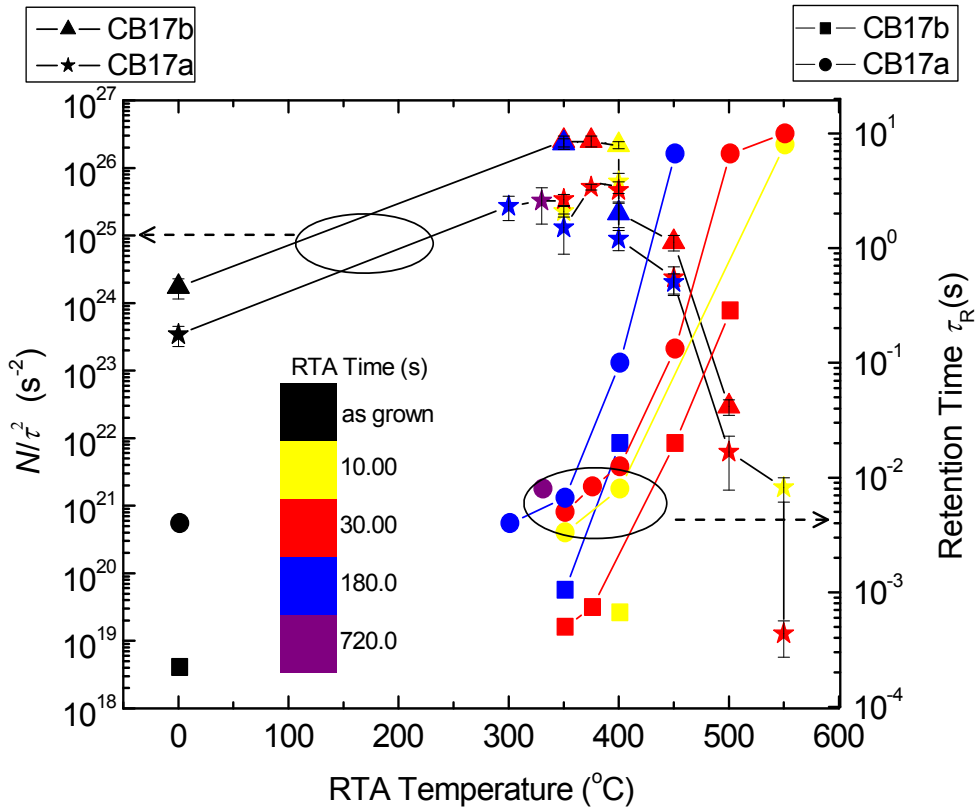


Figure 2.23 Field endurance parameter N/τ^2 and retention time scale τ_R as functions of RTA conditions. Error bars for τ_R are too small to be shown.

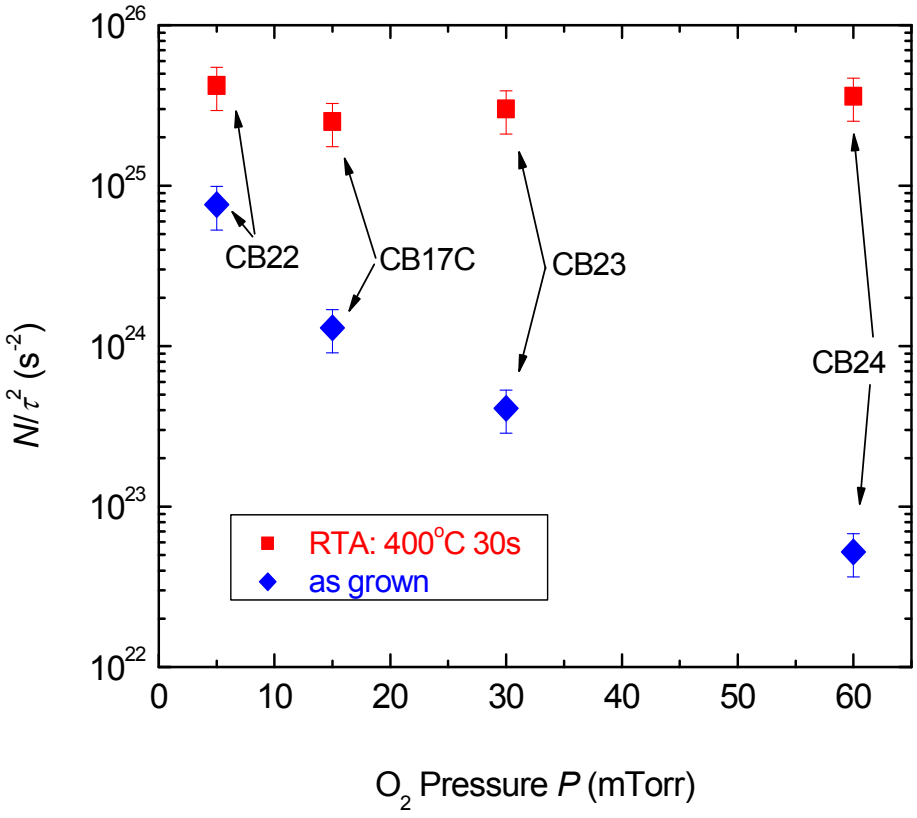


Figure 2.24 Field endurance parameter N/τ^2 as a function of aluminum oxidation conditions. Wafers CB22, CB17C, CB23 and CB24 were fabricated just as CB17a, but at different O_2 pressures.

2.7 Conclusions

We have measured transport properties of all-metallic tunnel junctions with $Nb/Al/AlO_x/Nb$ stack, fabricated using thermal oxidation or rf-plasma oxidation at various conditions. Rapid thermal post-annealing has been done to improve transport and endurance performance, in particular their endurance in electric fields in excess of 10 MV/cm. The results indicate that such junctions may combine high field endurance (corresponding to at least 10^{10} write/erase cycles in floating-gate memories) and high current density (corresponding to 30-ns-scale write/erase time) at high voltages, with very low conductance (corresponding to 0.1-s-scale retention time) at low voltages. We discuss the improvements necessary for the use of such junctions in advanced floating-gate memories.

The largest remaining problem with the application of these junctions in FGRAM is the "perturb effect" [27] , i.e. a substantial (by ~2 orders of magnitude) rise of their conductance at semi-selected conditions, i.e. at applied voltages close to 50% of the write/erase value, clearly visible in Figures 2.5 and 2.6. This issue should be addressed by the further improvement of the junctions, or altering the memory architecture, or both.

Chapter 3
Resistive bistability in metal oxide junctions

3.1 Recent experiments of resistive bistability

"Memory effects" in metal oxides and other amorphous inorganic dielectrics and semiconductors have been known for many decades. A typical *I-V* curve is shown in Figure 1.3a, followed by some brief discussions of key parameters and possible mechanisms. In this chapter, we are focusing on the experimental results of these devices. Table 3.1 lists some recent works and the sample parameters [56, 64].

Because of this atomic-scale mechanism, the most critical feature of the bistable junctions, especially in the view of their possible applications in VLSI circuits, is the device-to-device reproducibility. However, most publications do not give any quantitative information about the achieved reproducibility.

Table 3.1 Some recently reported results for latching switches based on metal oxides, sulphides, silicon oxide, and amorphous silicon [65-81].

Interlayer (nm)	Base-top electrode	R_{OFF}/R_{ON}	Switching time (s)	Retention time τ_{ret} (s)	Endurance (cycles)
CuO_x (12)	Cu-TiN	$\sim 10^3$	$<5\times10^{-8}$	$>10^6$	>600
Ag_2S (-)	Ag-Ag/Pt	~30	$<10^{-6}$	-	$>10^5$
$Cu_{2-x}S_x$ (-)	Cu-Pt	$\sim 10^3$	-	-	-
NiO_x (~40)	Ni-Pt	$\sim 10^2$	-	-	-
CuI_xS_y (700)	Pt-Cu	$>3\times10^3$	<0.1	-	$>10^3$
CuS_x (-)	Pt-Cu/Pt	$\sim 10^3$	-	-	~30
ZrO_2 (50)	Si-Au	$\sim 10^3$	-	$>10^3$	$>10^2$
SiO_2 (<50)	W-Cu	$\sim 10^3$	$\sim 10^{-6}$	$>5\times10^4$	$>10^7$
CuO_x (~7)	Cu-Ni, Co	10^3-10^4	$<10^{-7}$	-	-
TiO_2 (27)	Pt-Pt	~5	-	-	>30
a-Si (~5)	Si-Ag	$>10^4$	$<10^{-7}$	$>10^6$	$>10^4$
ZrO_2 (43)	Ti/Pt-Cu	$\sim 10^6$	$\sim 10^{-7}$	$>10^4$	$>10^4$
a-Si (80)	*p* Si-Ag	10^4	$\sim 5\times10^{-9}$	$\sim 10^7$	$\sim 10^6$
TiO_2 (15)	Ti/Pt-Ti/Pt	$\sim 10^4$	-	-	-
ZrO_2 (70)	n^+ Si-Cr/Au	$>10^6$	-	$>2\times10^3$	-
TiO_2 (50)	Ti/Pt-Ti/Pt	$\sim 10^3$	$<5\times10^{-8}$	-	>50
MO_x (-)	M_1-M_2	$>10^2$	$<10^{-8}/10^{-5}$	-	-

We are aware of just a few exceptions:

(i) A Samsung group has published [67] histograms of ON and OFF resistances of junctions of an unspecified metal oxide, with two substantially different areas, 0.2 and 0.0025 μm^2. In both cases, the statistical distributions of ON and OFF resistances form relatively narrow peaks (below one order of magnitude wide) which are well separated, by approximately factors 300 and 30, respectively. Unfortunately, no statistics has been given for switching threshold voltages V_t and V'_t (Figure 1.3a), the bistability parameters most critical for applications [64].

(ii) A Spansion team has presented [66] somewhat less impressive current histograms for their 0.18×0.18 μm^2 CuO_x junctions with a 12-nm oxide layer; still, the ON and OFF current values are separated by a gap of at least one order of magnitude wide. Again, no switching threshold statistics have been reported.

(iii) A University of Michigan at Ann Arbor group did present [79] a histogram of one of switching thresholds (V_t in Figure 1.3a) of their 50×50 nm^2 junctions with an 80-nm-thick amorphous-silicon layer. The histogram features a very narrow (~10%) peak, at apparently much larger split between average values of V'_t and V_t.

(iv) A collaboration of the Chinese Institute for Microelectronics and University at Albany have reported [78] a narrow but still clean separation of ~30%-wide histogram peaks for V'_t and V_t, in 0.5×0.5 μm^2 junctions consisting of three sequentially deposited ZrO_2/Cu bilayers, with a thickness of 20+3 nm each.

(v) Finally, very recently, a group from Gwangju, Korea reported [82] a huge (~4 orders-of-magnitude) gap between the threshold histogram peaks (each less than an order-of-magnitude wide) in 0.5×0.5 μm^2 junctions based on ~70 nm thick layers of a polyfluorene-derivative polymer [83].

However, even these publications report only the apparently best results, and do not describe how sensitive they have been to variations of the fabrication conditions. The goal of this work has been to explore bistability effects in junctions based on oxides of Cu and Ti, which looked most promising from literature data (plus Nb which was a

legacy metal for our laboratory), within a broad range of fabrication and post-processing conditions and procedures of the electric "formation" of the devices. In contrast to virtually all other publications in this field, we present experimental data on device reproducibility (and also other important properties such as OFF/ON conductance ratio and switching endurance), regardless of whether they look favorable or unfavorable.

3.2 Fabrication and experiment procedures

Most metal-oxide layers of our junctions have been fabricated by either rf plasma oxidation (PO) or thermal oxidation (TO) of a thin metallic layer (or layers) on 2" thermally-oxidized silicon wafers, at ambient temperature. The fabrication procedures of two types were used.

(i) Vacuum-break process (wafers VJCuOx3, 4, 5, 6, 7 and VJTiOx1, 2, 3):

A layer of metal base electrode (50-100nm) was first deposited in an electron beam evaporation system (the so-called "Pb system", see Figure 3.1), at a 0.05 to 0.08 nm/s rate, in a ~5×10^{-7} Torr vacuum. After a vacuum break, the sample was rapidly transferred to a sputtering chamber (see, e.g., Figure 3.2) with base vacuum of 2 to 3×10^{-7} Torr. After pre-cleaning in an rf Ar plasma for a time sufficient to remove ~5 nm of the base electrode, either the thermal oxidation (at 100 Torr pressure of dry oxygen, for 10 to 40 minutes), or rf plasma oxidation (at 10 to 300 W rf power, at 15 to 30 mTorr O_2 pressure, for 10 minutes) was performed. The few-nm-thick oxide layer was then sealed by a 100-nm-thick Nb counter-electrode film, dc-sputtered at the rate close to 2 nm/s.

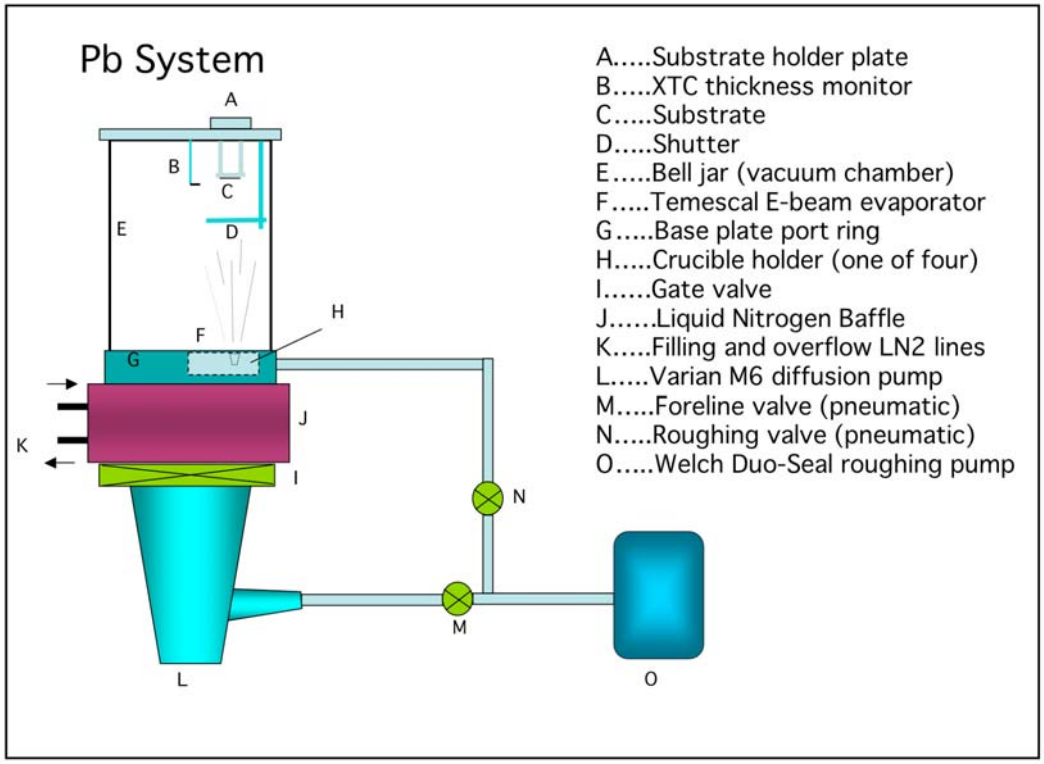
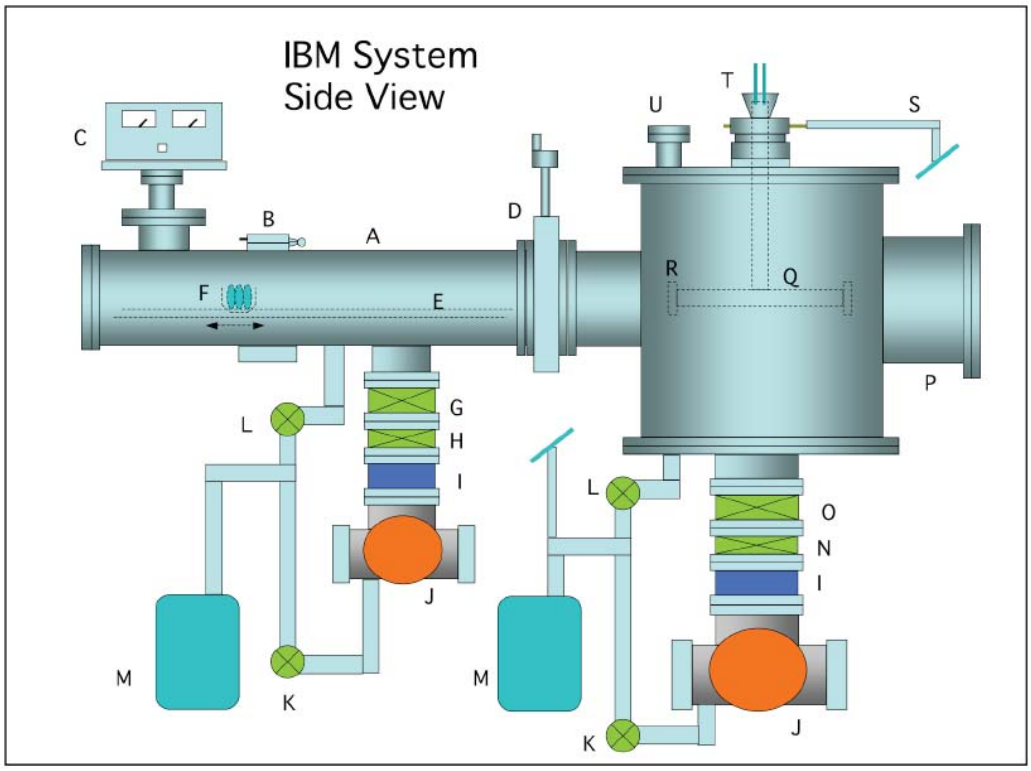


Figure 3.1 Diagram of our evaporation system (called "Pb system") with major components listed.



A. Stainless Steel Loadlock Sample Transfer UHV Chamber.
B. Hinged Access Hatch (Conflat).
C. R. F. Tuner for Backsputtering Gun.
D. Manual Gate Valve for Sample Loading.
E. Sample Transfer Track (1-D Motion).
F. Sample Transfer Cart (1-D Motion).
G. Iris Throttle Valve.
H. High Vacuum Pneumatic Gate Valve.
I. Nude Ion Gauge.
J. Blazer's Horizontal Shaft Turbomolecular Pump.
K. Pneumatic Foreline Valve.
L. Pneumatic Roughing Valve.
M. Balzer's Rotary Vane Backing Pump.
N. Pneumatic Throttle Valve.
O. High Vacuum Pneumatic Gate Valve.
P. Stainless Steel Trilayer Deposition UHV Chamber.
Q. Two Station Water cooled Rotating Substrate Stage.
R. Remote Loading Substrate Holder.
S. Differentially Pumped Rotary Feedthrough.
T. Water Feedthrough for Substrate Cooling.
U. Lighted Viewport for Sample Transfer Point.

Figure 3.2 Diagram of one of our sputtering systems (called "IBM system") with major components listed.

(ii) In-situ processes (all other wafers listed in Tables 3.3-3.6):

The whole junction structure was fabricated in a single vacuum system equipped either for sputtering (for NbO_x and CuO_x, see, e.g., Figure 3.2) or e-beam evaporation (for TiO_x, see figure 3.1). The in-situ process has enabled us to provide larger variety of metal electrodes (see Tables 3.3 to 3.6 below for details) and cleaner interface between the metal and metal-oxide layers. For NbO_x devices, a 50-nm-thick Al wiring level was first dc-sputtered at 0.5 nm/s, followed by a 10-nm-thick Nb base layer. For CuO_x samples, the substrate was pre-coated with a 5-nm Cr adhesion layer, followed by dc-sputtering, at a rate of ~2 nm/s, of a 150-nm-thick Cu base electrode. Following the surface oxidation, stacks of both types were completed by dc-sputtering of ~100-nm-thick Nb counter-electrodes at a rate ~ 2 nm/s.

For TiO_x-based junctions, the deposition of a similar Cr adhesion layer was followed by e-beam evaporation of 50 to 100 nm Pt wiring layer and its lift-off patterning. Then the wafer was cleaned from any resist and chemical residue in an oxygen rf plasma asher and moved into the e-beam chamber, where it was cleaned again in rf Ar plasma as described above, before the deposition of the titanium layers. For $Ti/TiO_x/Ti$ devices, a 50-100 nm thick Ti electrode was e-beam evaporated at ~0.05 nm/s, followed by e-beam evaporation of TiO_2 from a stoichiometric target. For $Pt/TiO_x/Ti$ type devices, a very thin (1.5 nm) layer of Ti was evaporated on the Pt base, and then exposed to oxygen-enriched rf plasma to completely oxidize the layer. For multi-layer TiO_x junctions, this process was repeated several times. In both cases, the oxide layer was sealed by e-beam evaporation

of a 100 nm thick Ti counter-electrode, as described above.

Figure 3.3 shows an annular dark-field scanning transmission electron microscopy (ADF STEM) image of one of our multi-layer samples (wafer VJTiOx8). It shows sharp, clean, and relatively smooth interfaces between the layers.

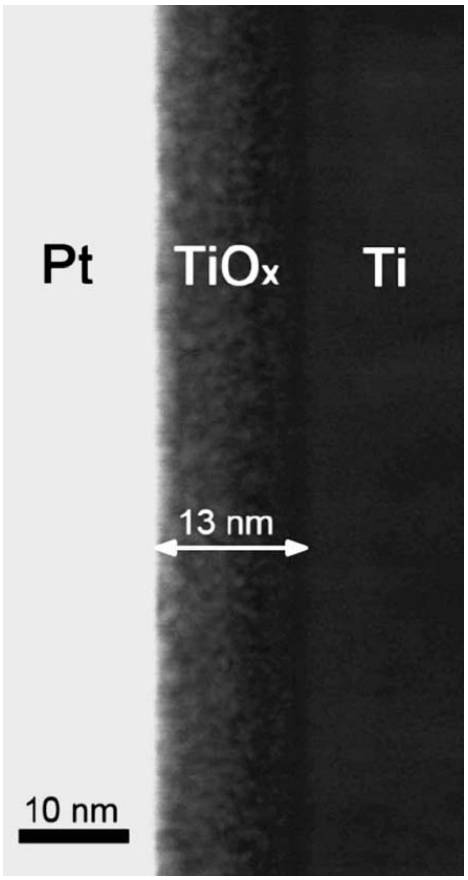


Figure 3.3 An ADF-STEM image of a sample from wafer VJTiOx8.

After the stack had been fabricated, it was patterned to define 18 junctions of areas 3×3, 30×30, and 300×300 μm^2, with appropriate wiring and contact pads, on each 5×5 mm^2 chip. (We also have a set of chips with variety of 4×4, 5×5 and 6×6 μm^2 junctions) For that, Nb and Ti electrode patterns were defined by the reactive ion etching (RIE, see figure 3.4) in SF_6 gas using a PMMA etch mask patterned with UV lithography.

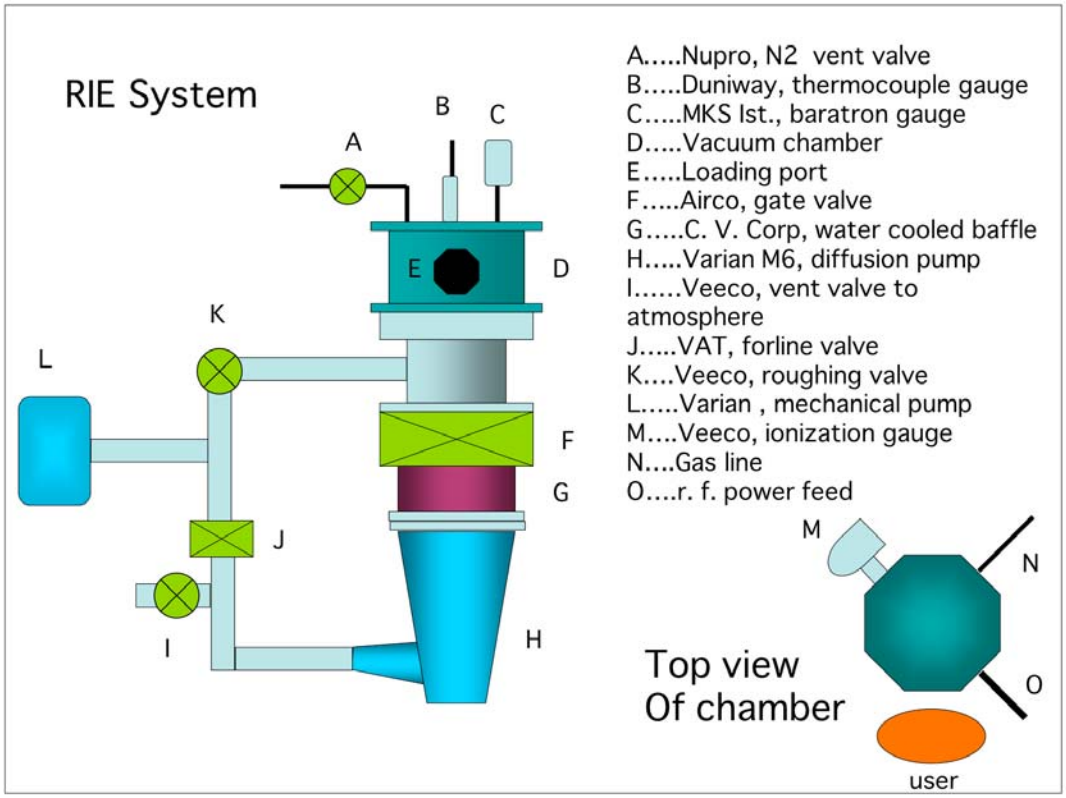


Figure 3.4 Diagram of the reactive ion etch (RIE) system with major components listed.

Other metals (viz. Al and Cu) were patterned by back-sputtering in Ar rf-plasma again using PMMA etch masks. A 150 nm thick rf-sputtered quartz layer was used as for insulation and patterned with a self-aligned-liftoff process using the junction layer etch mask. A final wiring layer of 200-nm-thick, dc-sputtered Nb was patterned via lift-off. Figure 3.5 shows schematic fabrication flow steps of a TiO_x wafer with $Pt/TiO_x/Ti$ stack.

(a) Starting: an oxidized Si wafer.

(b) Cr protection layer deposition.

(c) Base electrode patterning with PMMA (positive resist) and UVN-30 (negative resist).

(d) Base metal (Pt) deposition.

(e) Base metal liftoff.

(f) Metal oxidation (TiO_x) and top metal (Ti) deposition.

(g) Junction patterning with PMMA.

(h) Top metal RIE to define junction.

(i) Quartz deposition as insulating layer.

(j) Quartz liftoff.

(k) Wiring layer (Nb) patterning with PMMA.

(l) Wiring layer (Nb) deposition.

(m) Wiring layer (Nb) liftoff.

A detailed process sheet has been presented in Appendix.

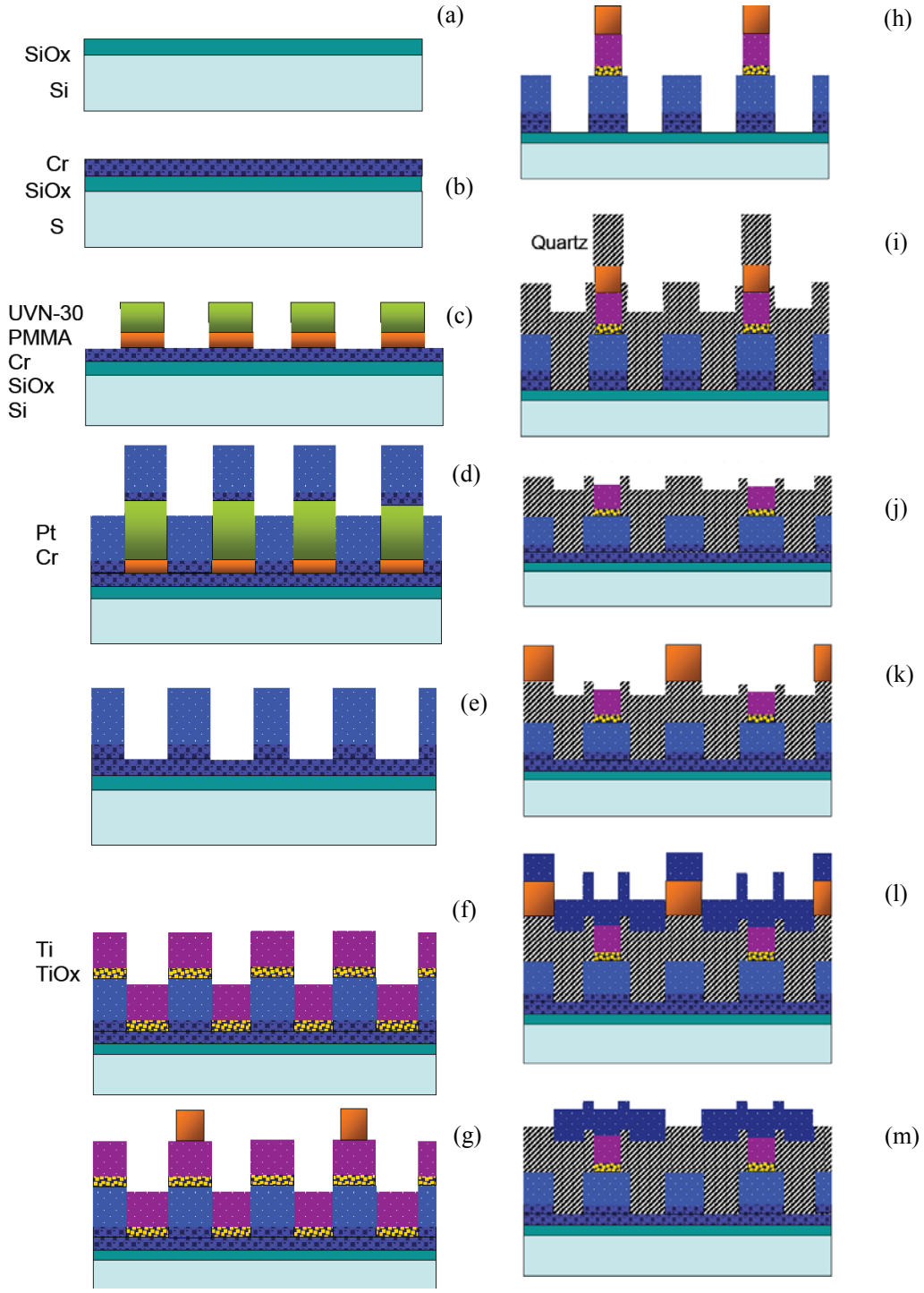


Figure 3.5 Schematic illustration of fabrication flow of one TiO_x wafer. Processes (a) to (m) have been listed above. Please refer to Appendix for details.

After an initial junction testing, several chips from most fabricated wafers were subjected to rapid thermal post-annealing (RTA) in argon flow, at temperatures from 200 to 800ºC, for 30 to 180 seconds. (For particular values, see Tables 3.3 to 3.6) The melting points and thermal expansion coefficients of all materials of the chips have been listed in Table 3.2.

Table 3.2 Melting point and coefficient of thermal expansion.

materials	Cu	Ti	Nb	Cr	Al	Si	SiO_2	CuO_x	TiO_x
melting point (ºC)	1084	1668	2477	1907	660	1414	1600	~1200	~1900
coefficient of thermal expansion ($\mu m \cdot m^{-1} \cdot K^{-1}$)	16.5	8.6	7.3	4.9	23.1	2.6	-	-	-

Since typical junction resistances were in excess of 10^2 Ω, i.e. larger than that of thin-film on-chip wiring, their electrical characterization was performed by simple two-terminal *I-V* measurements using Keithley 6430 soucemeter. For the initial formation of the ON-state (i.e. Figure 1.3b-d), applied voltage was increased, with current externally limited to a certain value, typically of a few mA. (The so-called "current compliance".)

Voltage sweeps were performed at a speed of 1 to 100 mV/s. In the junctions exhibiting resistive bistability, the typical OFF→ON switching time was less than 10 μs (our measurement technique limit), while the typical ON→OFF switching took much more time, in the range of milliseconds. For quantitative characterization of ON and OFF

states, the corresponding resistances R_{ON} and R_{OFF} were measured at low bias voltage (~50 mV). The resistive bistability cycle could be typically repeated several (N) times, usually followed by a hard breakdown to an irreversible state with a very low resistance.

ON/OFF switching statistics was recorded for all devices which exhibited the bistability. The "yield" listed in Tables 3.3 to 3.6, was defined as ratio of number of samples with resistive bistability behavior to the overall number of all samples without evident microshorts.

3.3 NbO_x-based junctions

Our laboratory has long experience of fabrication of high-quality thin-film structures based on niobium, so that in light of several prior publications [84-86] reporting the resistive bistability in junctions based on oxides of that material, it was natural for us to start our experiments with such devices. Table 3.3 summarizes the major parameters and properties of our $Nb/NbO_x/Nb$ junctions. Based on our experience of previous aluminum oxide tunnel barriers, we have also tried different oxidation methods (thermal oxidation, TO or rf plasma oxidation, PO) with a variety of oxidation conditions.

Table 3.3 Parameters and properties of NbOx samples.

Wafers	**Interlayer formation**	**Stack**	**RTA**	**Bistability/ Properties**	
VJNbOx1	thermal oxidation: 100 Torr O_2, 40 min	$Nb/NbO_x/Nb$	400˚C, 30 s	Y	yield <10% R_{OFF}/R_{ON} <10
VJNbOx2	plasma oxidation: 10 W, 15 mTorr O_2, 10 min	$Nb/NbO_x/Nb$	400 to 600˚C, 30 to 180 s	Y	yield <40% R_{OFF}/R_{ON} <10
VJNbOx3	plasma oxidation: 100 W, 15 mTorr O_2, 10 min			Y	
VJNbOx4	plasma oxidation: 300 W, 5 Torr O_2, 10 min			N	Schottky barriers

Our initial attempt was to form the oxide layer by simple thermal oxidation in dry oxygen (wafer VJNbOx1). The initial resistance didn't scale with areas, and was in range of a few tens of Ohms (microshorts) to a few thousand Ohms (lower than that of Nb_2O_5 thin film with the same area and thickness [84, 85], indicating that conducting channels exist in as grown samples). This wafer appears to produce a very low yield. The post-annealing did not help much.

The transfer to plasma oxidation, at modest rf power (wafers VJNbOx2 and 3), has not increased the yield of as-grown junctions. The IV curves of as grown samples and those after RTA have been shown in Figures 3.6 and 3.7, and there is still no evident area dependence. The current is usually below 1 mA for small applied voltage (V<1 V), with R_{ON} and R_{OFF} in $k\Omega$ range. However, such devices have benefited more from the RTA (Figure 3.8), with the yield clearly growing with RTA temperature until it reaches ~500°C. The highest yield it can reach is still no sufficient for any possible applications yet. And unfortunately, at approximately the same temperature, the OFF/ON resistance ratio starts to drop rapidly to below 10 (Figure 3.8). The error bars in Figure 3.8 correspond the r.m.s. scattering of the data among different samples from the same wafer, and the measurement accuracy was much better. Moreover, the switching endurance of such junctions, characterized by the number N of ON/OFF switching cycles (like those shown in Figures 3.6 and 3.7) was low, with the typical N of the order of 10 or so.

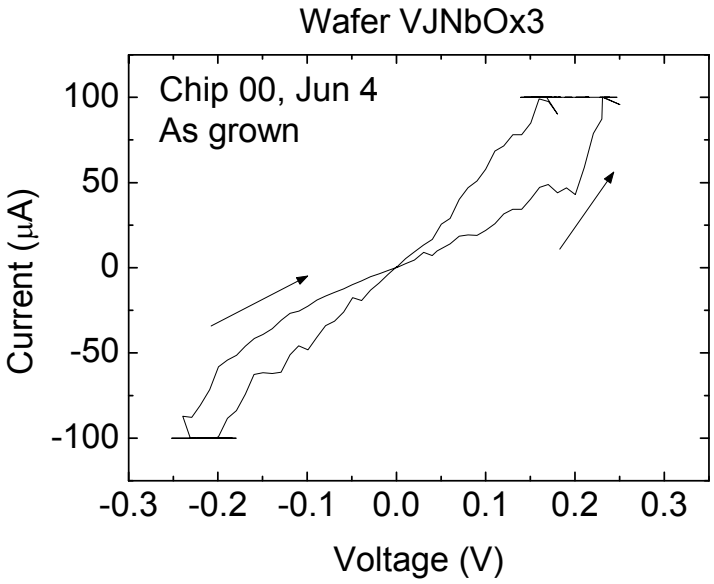


Figure 3.6 Typical dc *I-V* curve of a junction from wafer VJNbOx3.

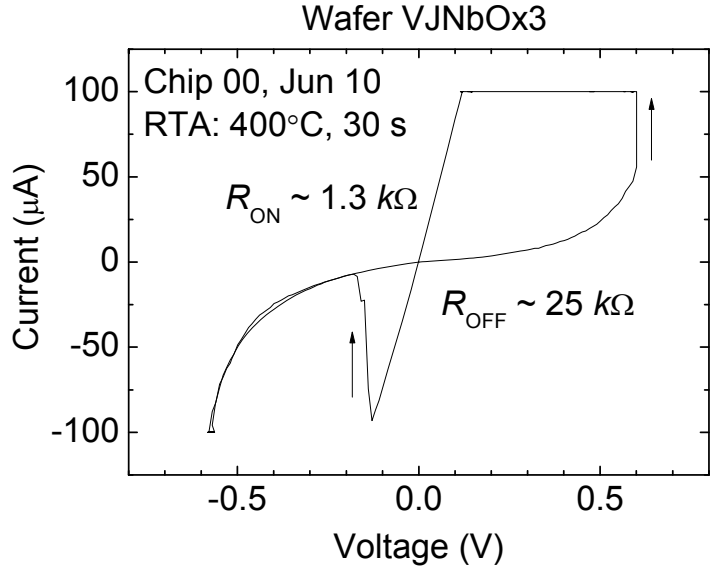


Figure 3.7 Typical dc *I-V* curve of a junction from wafer VJNbOx3 after RTA.

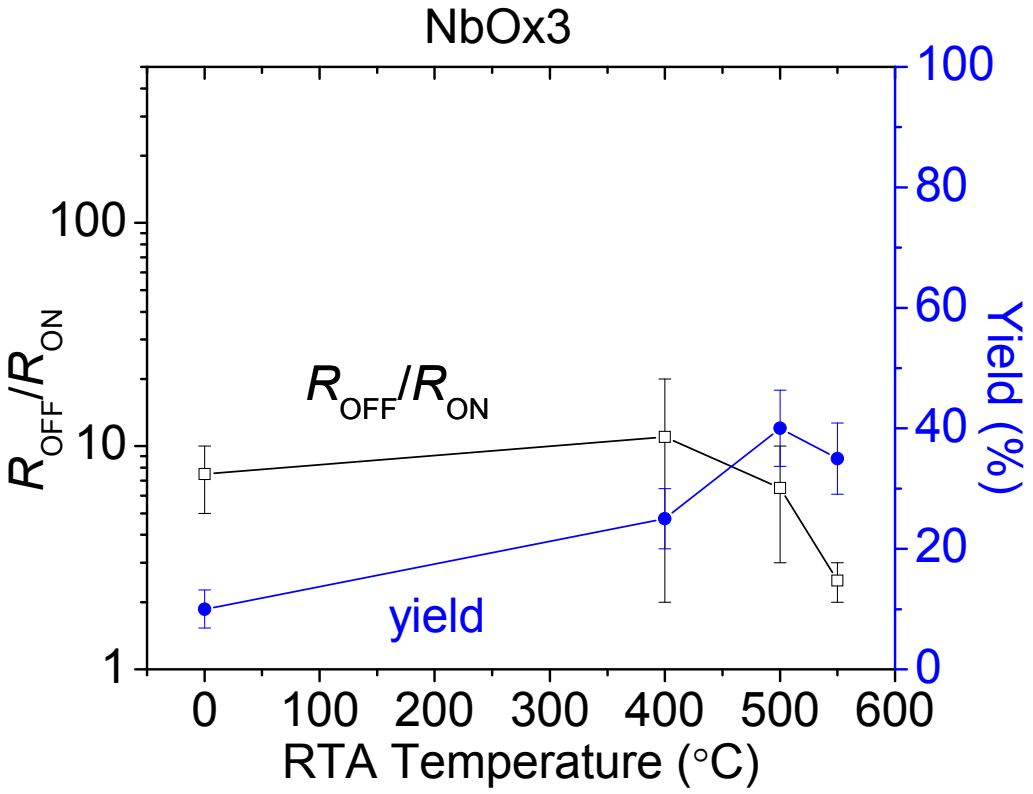


Figure 3.8 Effect of temperature of a 30-second RTA on the OFF/ON resistance ratio and the yield of good devices from wafer VJNbOx3.

Furthermore, we have observed the possible "multi-level" switching (Figure 3.9) for one sample from wafer VJNbOx2. This phenomenon has also been noticed by several research groups [56, 87].

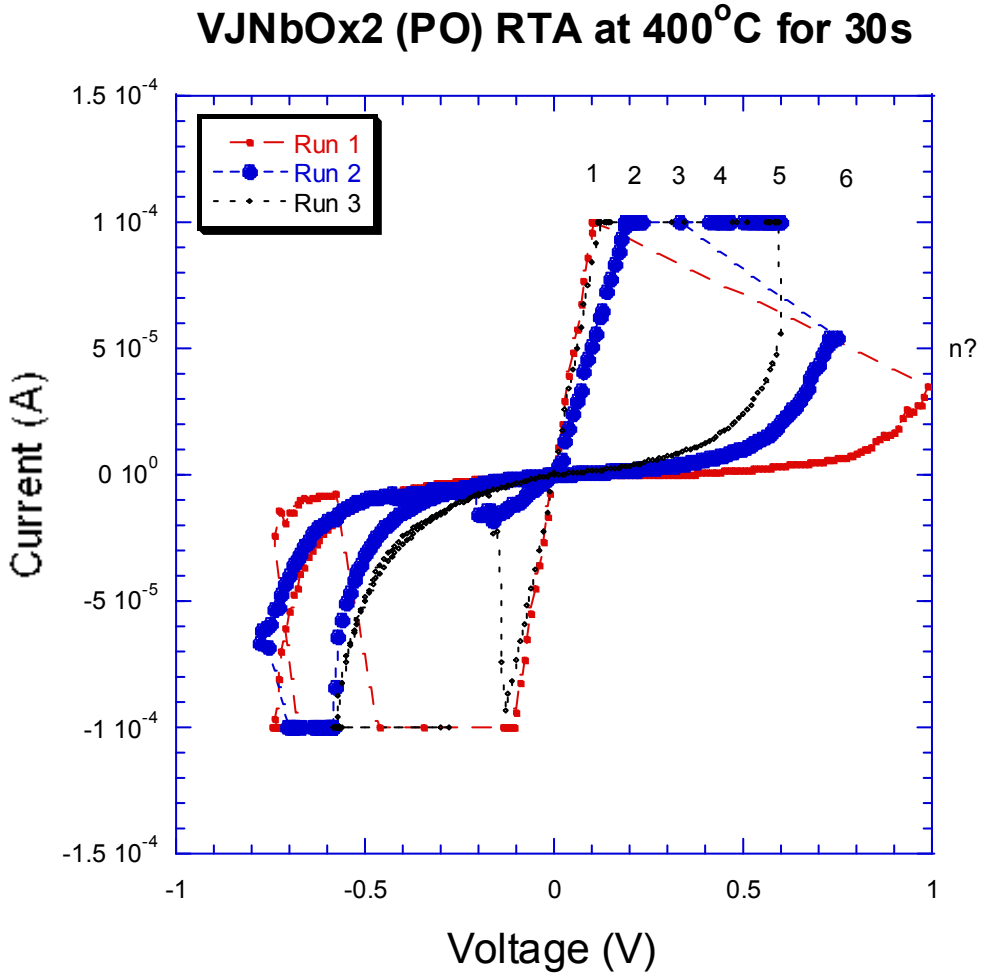


Figure 3.9 Multi-level switching of a junction from wafer VJNbOx2 after RTA.

An attempt to improve the situation by the further increase of rf plasma power (wafer VJNbOx4) has given junctions with typical Schottky-barrier *I-V* curves (Figure 3.10), without observable hysteresis.

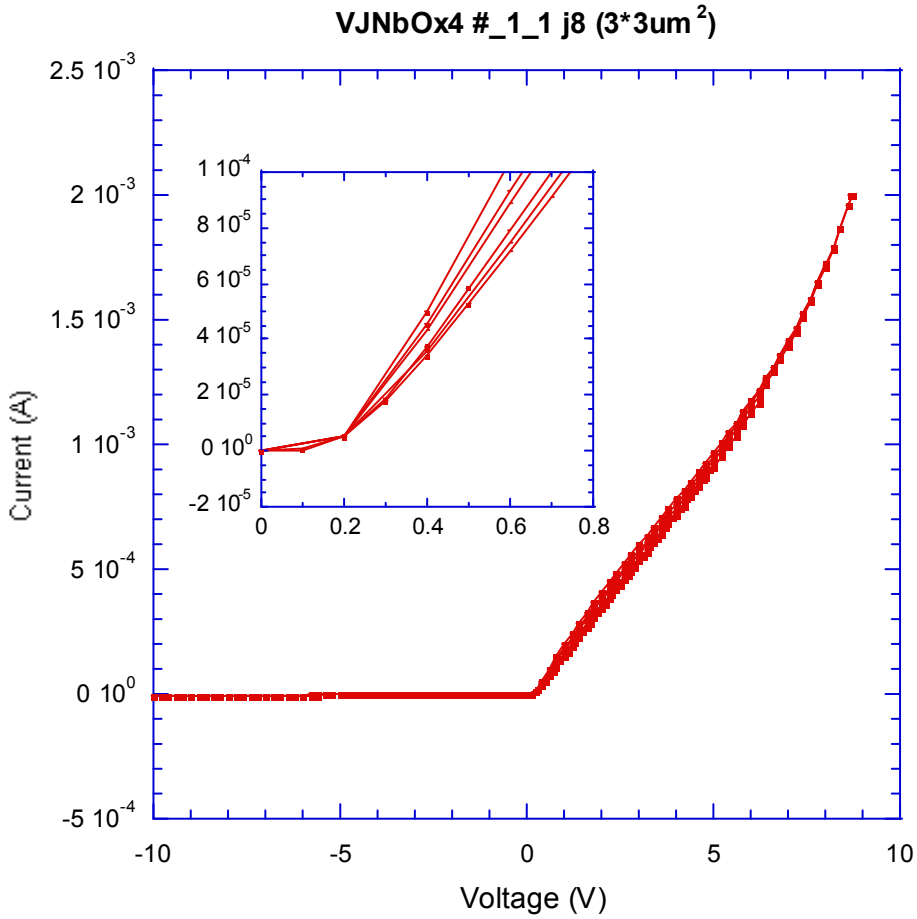


Figure 3.10 Schottky *I-V* curves of a junction from wafer VJNbOx4.

The schottky *I-V* curve indicates a metal-semiconductor contact which is dominant in the electron transport behavior through the tunnel barrier.

Since by that time, we had reached more promising results with CuO_x devices, we decided not to pursue the niobium oxide option any longer.

3.4 CuO_x-based junctions

Experiments with copper oxides (Table 3.4) were also started with thermal oxidation – see wafer VJCuOx3 and 4. The results from these wafers were not pleasant either, especially with a wide distribution of initial resistance not scaled to junction areas (see Figure 3.11 for resistance distribution of wafer VJCuOx3. The electrical measurements have shown low conductance ratio, and similarly poor yield, like previous TO NbO_x wafer.

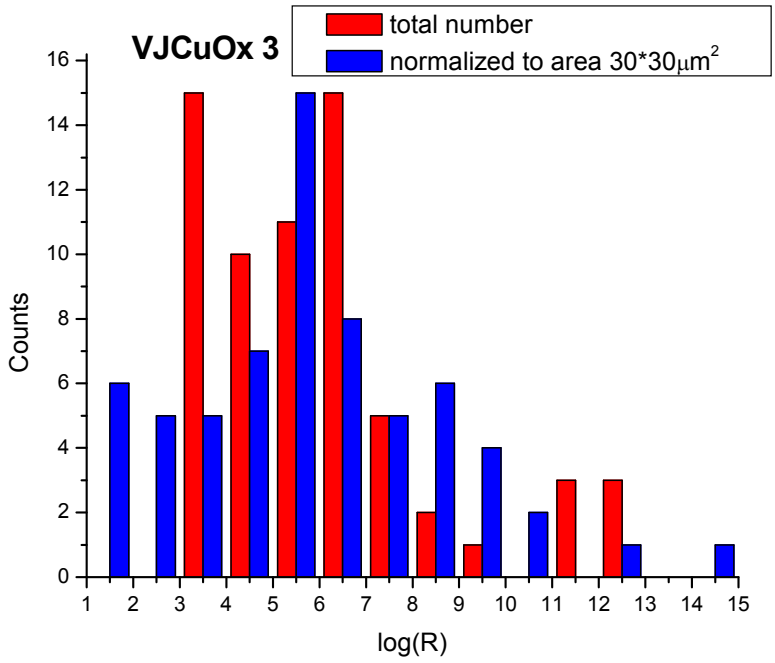


Figure 3.11 Resistance distributions of junctions from wafer VJCuOx3.

Table 3.4 Parameters and properties of CuO_x samples.

Wafers Inte	**rlayer formation**	**Stack**	**RTA**	**Bistability/ Properties**	
VJCuOx3	thermal oxidation: 100 Torr O_2, 40 min	$Cu/CuO_x/Nb$	400˚C, 180 s	Y	yield <5% R_{OFF}/R_{ON} <5
VJCuOx4				Y	
VJCuOx5	plasma oxidation: 10 W, 15 mTorr O_2, 10 min	$Cu/CuO_x/Nb$	200 to 800˚C, 30 to 180 s	Y	yield ~50% R_{OFF}/R_{ON}~2 (at 100 W; RTA 800˚C, 30 s)
VJCuOx6	plasma oxidation: 50 W, 15 mTorr O_2, 10 min			Y	
VJCuOx7	plasma oxidation:100W, 15 mTorr O_2, 10 min			Y	
VJCuOx13	plasma oxidation:100W, 25 mTorr O_2, 10 min	$Cu/CuO_x/Nb$	400˚C, 30 s	Y	yield <20% R_{OFF}/R_{ON}~10
VJCuOx15	plasma oxidation:300W, 25 mTorr O_2, 10 min			Y	
VJCuOx17	plasma oxidation:300W, 25 mTorr O_2, 10 min			Y	

Our first few attempts (wafers VJCuOx 5, 6 and 7) with the transfer to plasma oxidation, at modest rf power (10 to 100 W) has helped to narrow down the distribution of initial resistance. Figures 3.12 and 3.13 show the *I-V* curves of junctions without and with RTA from wafer VJCuOx7. The current compliance is set at a few mA and $|V_t|$ and $|V'_t|$ are around 1 to 2 V. To maximize yield, we have tried RTA at a higher temperature, e.g. 800ºC, and the average yield rises to ~50% (Figure 3.14) for wafer VJCuOx7. Unfortunately, just like in the case of NbO_x, the yield rise is accompanied by a sharp drop of the OFF/ON resistance ratio to only around 2 (Figure 3.15).

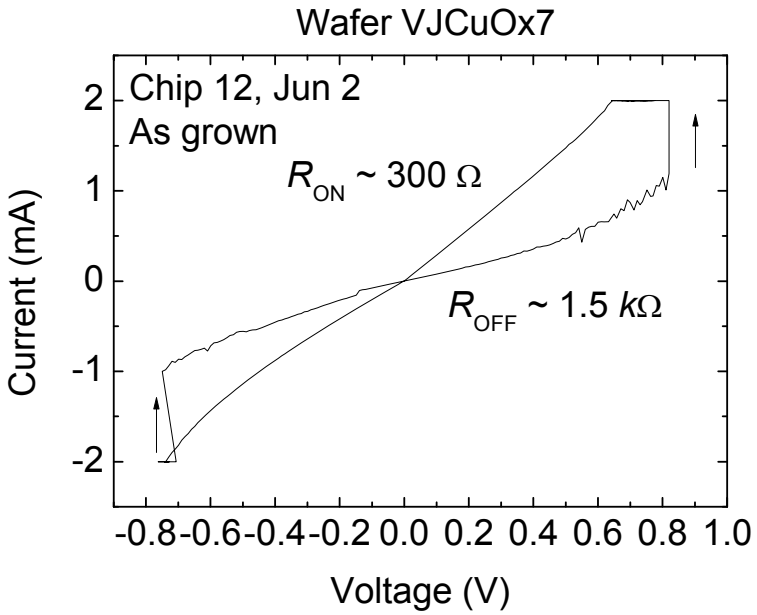


Figure 3.12 Typical dc *I-V* curve of a junction from wafer VJCuOx7.

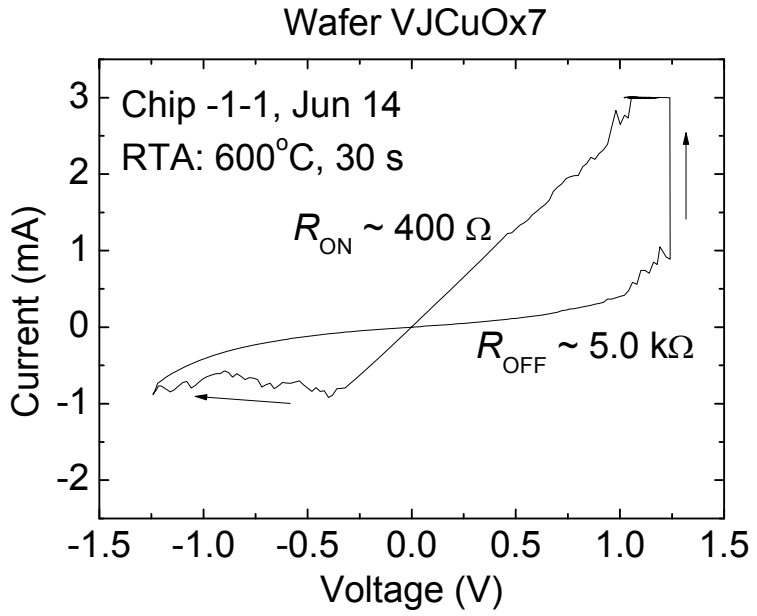


Figure 3.13 Typical dc *I-V* curve of a junction from wafer VJCuOx7 after RTA.

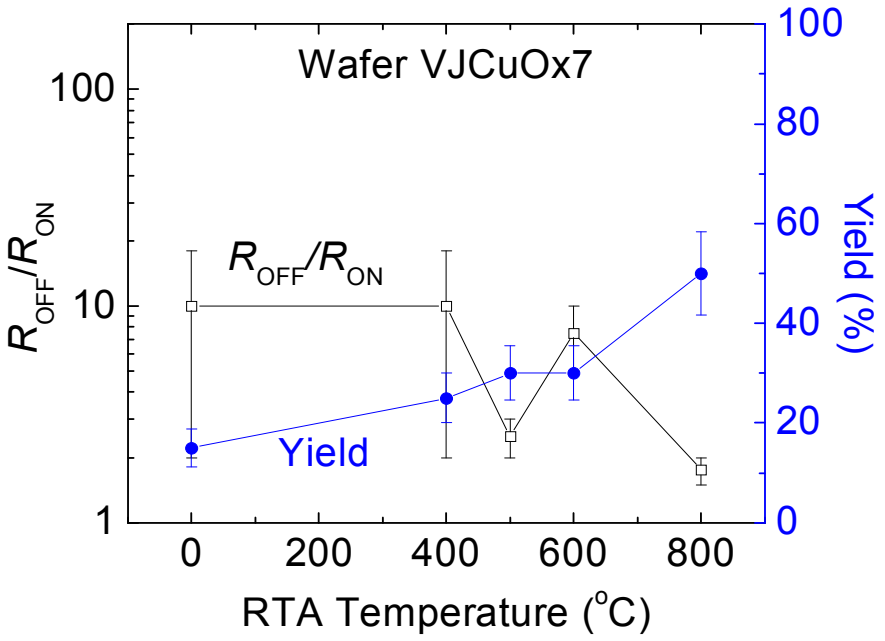


Figure 3.14 Effect of temperature of a 30-second RTA on the OFF/ON resistance ratio and the yield of good devices from wafer VJCuOx7.

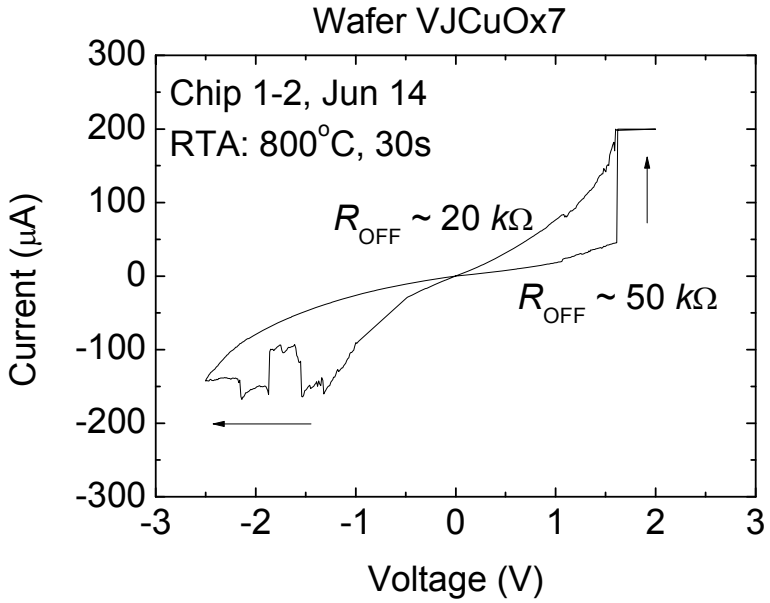


Figure 3.15 One dc *I-V* curve of a junction from wafer VJCuOx7 after RTA, with R_{OFF}/R_{ON}=2.5.

Encouraged by prior work [88], we have explored the option of very high plasma power combined with a higher oxygen pressure (wafers VJCuOx13, 15 and 17). Together with an RTA at 400°C, this has led to an improvement of the resistance ratio (as high as 30, see Figure 3.16), but the yield has dropped to below 20%.

In addition, the switching endurance for all copper-oxide junctions was rather low, with the number N of cycles not exceeding 20 or so.

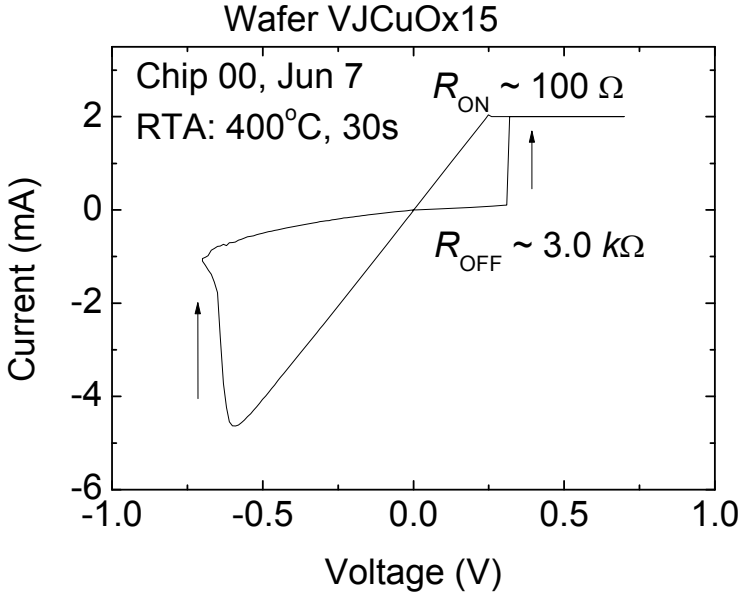


Figure 3.16 One dc *I-V* curve of a junction from wafer VJCuOx15 after RTA, with R_{OFF}/R_{ON}=30.

3.5 Single-layer-TiO_x-based junctions

In the view of recent encouraging publications [65, 81, 89-92], the main focus of our work has moved to devices with titanium oxide interlayer(s) – see Tables 3.5 and 3.6. We will discuss the single layer TiO_x wafers in this section. Just as in the case of other two oxides (NbO_x and CuO_x), we have started with the simplest option of thermal oxidation (wafer VJTiOx1), just to get equally poor results in terms of resistance distribution, ON/OFF conductance ratio, endurance and yield.

Table 3.5 Parameters and properties of single layer TiO_x samples.

Wafer	**Interlayer formation**	**Stack**	**RTA**	**Bistability/ Properties**	
VJTiOx1	thermal oxidation: 100 Torr O_2, 40 min	Ti/TiO_x/Nb	400˚C, 30 s	Y	yield <10% R_{OFF}/R_{ON} <5
VJTiOx2	plasma oxidation: 50 W, 15 mTorr O_2, 10 min	Ti/TiO_x/Nb	400 to 800˚C, 30 s	Y	yield ~50% R_{OFF}/R_{ON}=5-100 (at RTA at 700˚C, 30 s)
VJTiOx3	plasma oxidation: 500 W, 5 Torr O_2, 10 min			Y	
VJTiOx4	deposited TiO_2, thickness ≈ 15 nm	Ti/TiO_x/Ti	400˚C, 30 s	N	metastable junctions (see the text)
VJTiOx7		Pt/TiO_x/Ti		N	
VJTiOx13				N	

In this oxide fabrication, we have tried to use a completely different way of TiO_x formation, by its evaporation deposition from a stoichiometric TiO_2 target (wafers VJTiOx4, 7 and 13). The oxide thickness has been measured to be around 15 nm for all three wafers, by an XTC Film Thickness and Rate Monitor in the evaporation system (refer to Figure 3.1 for details). All junctions with different choices of metal electrodes

(Pt or Ti) have produced apparent *I-V* hysteresis loops, which are very sensitive to temperature and the voltage sweep rate. Figure 3.17 shows temperature dependence of *I-V* sweeps of a junction from wafer VJTiOx4. The electric current at room temperature (RT) is 8 orders of magnitude higher than that at liquid nitrogen temperature (LN). Also, we have noticed the hysteresis loop has vanished in LN. A thermal cycle has also changed the hysteresis loop by two orders of magnitude. A further study has shown considerable current change was happening even at fixed dc bias voltage (Figure 3.18), i.e. the measured states were not stable in time, putting in question the whole body of previously recorded data. All these behaviors were probably due to trap assisted tunneling through TiO_2 tunnel barrier.

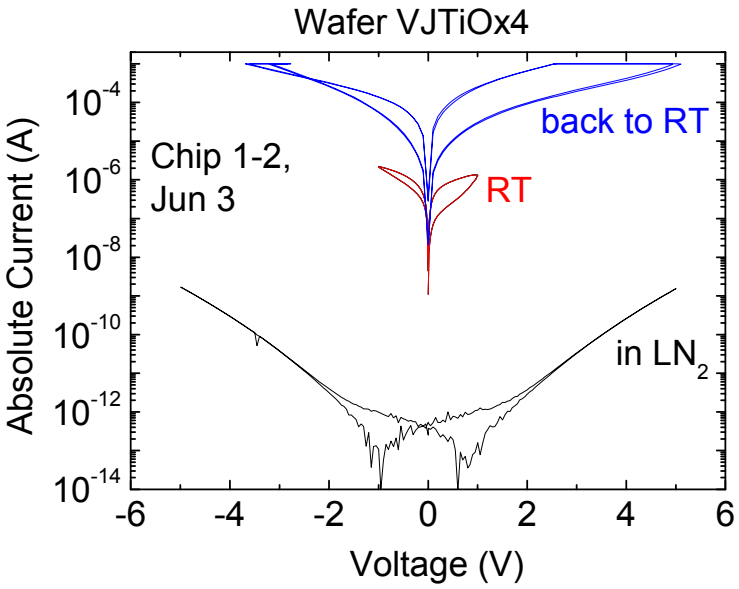


Figure 3.17 Temperature dependence of *I-V* hysteresis loops of a junction from wafer VJTiOx4. *I-V* measurements were taken at room temperature first, followed by cryogenic measurement at liquid nitrogen temperature. The junction was brought back to room temperature to finish this thermal cycle. The shape of *I-V* loop in liquid nitrogen was due to capacitance of the oxide layer and limitation of current resolution.

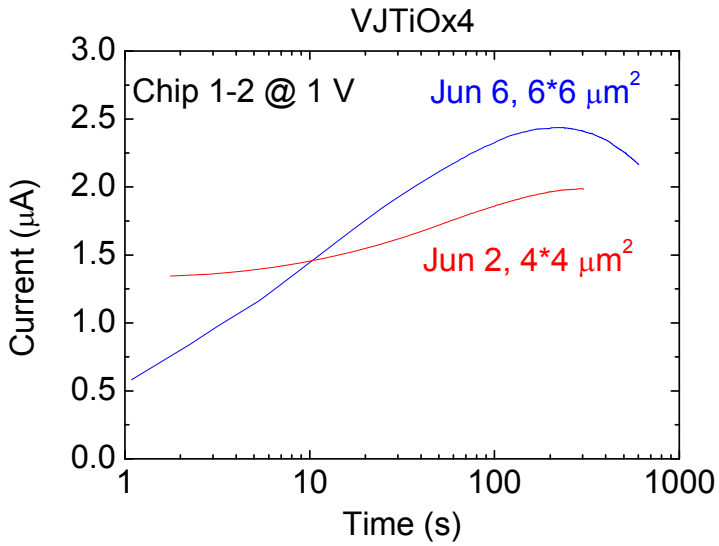


Figure 3.18 Time dependence of current at 1 V at room temperature. Two junctions with different areas are both from wafer VJTiOx4.

Junctions made by plasma oxidation of the base titanium electrode, didn't show resistance bistability until accompanied by post-annealing. Figure 3.19 shows an dc *I-V* curve of a junction from wafer VJTiOx2 at a relatively high annealing temperature, 700°C. Switching *I-V*s (with resistance ratio $R_{OFF}/R_{ON} \approx 10$) have been cycled at current compliance of +3 and -3 mA, and the threshold voltages V_t and V'_t are around +4 and -4 V, respectively. At the same time, the good junction yield has reached 50% - see Figure 3.20 for a detailed study of RTA effect on resistance ratio and yield.

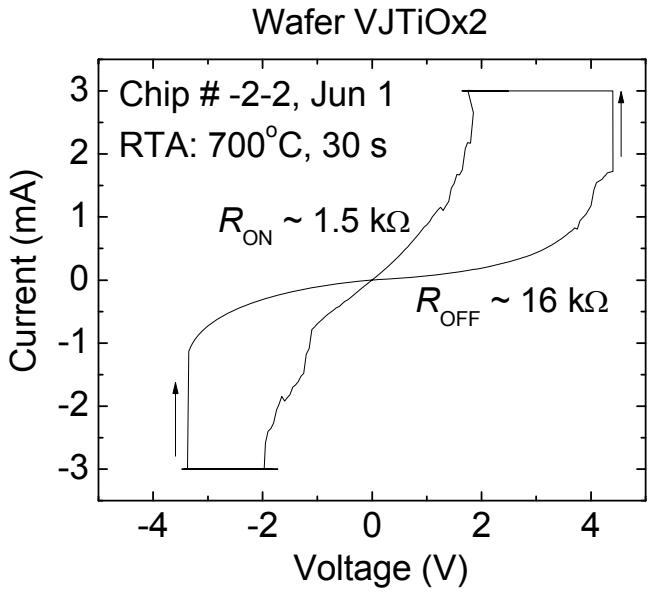


Figure 3.19 Typical dc *I-V* curve of a junction from wafer VJTiOx2 after RTA.

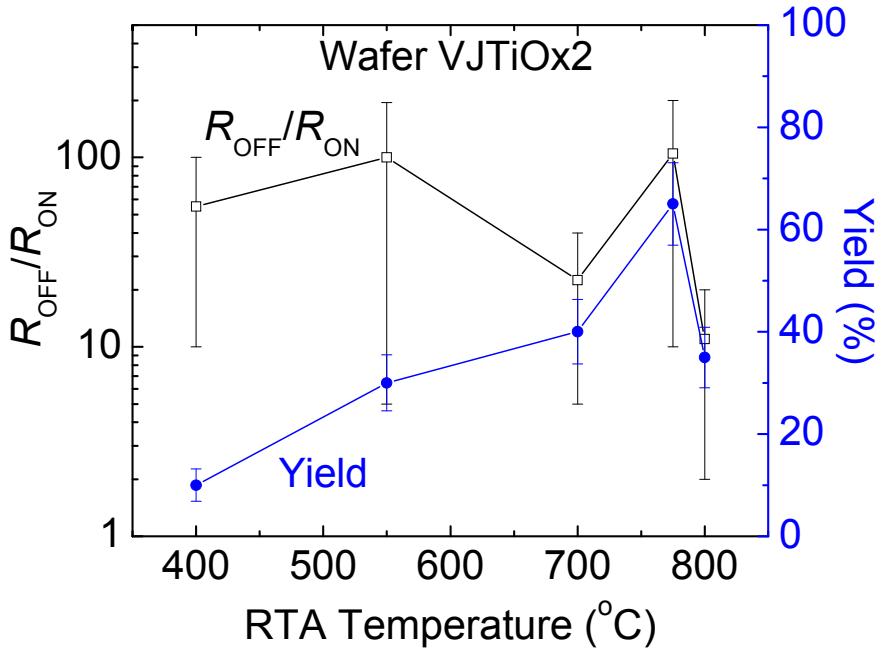


Figure 3.20 Effect of temperature of a 30-second RTA on the OFF/ON resistance ratio and the yield of good devices from wafer VJTiOx2.

Since we have well repeatable switching *I-V* curves of junctions from wafer VJTiOx2 after RTA at 700ºC for 30 seconds, it is possible to perform switching endurance test of these junctions. We have used (dc) voltage pulse sequences (see Figure 3.21 for details) to realize the endurance test, and the switching endurance has been improved to $N \sim 10^3$ (Figure 3.22), while the resistance ratio was not too impressive (see the rows for VJTiOx2 and 3 in Table 3.5), but acceptable for some applications. [64] Further attempts at a higher rf power and RTA temperatures did not help to improve resistance ratio, so that other fabrication methods were clearly needed.

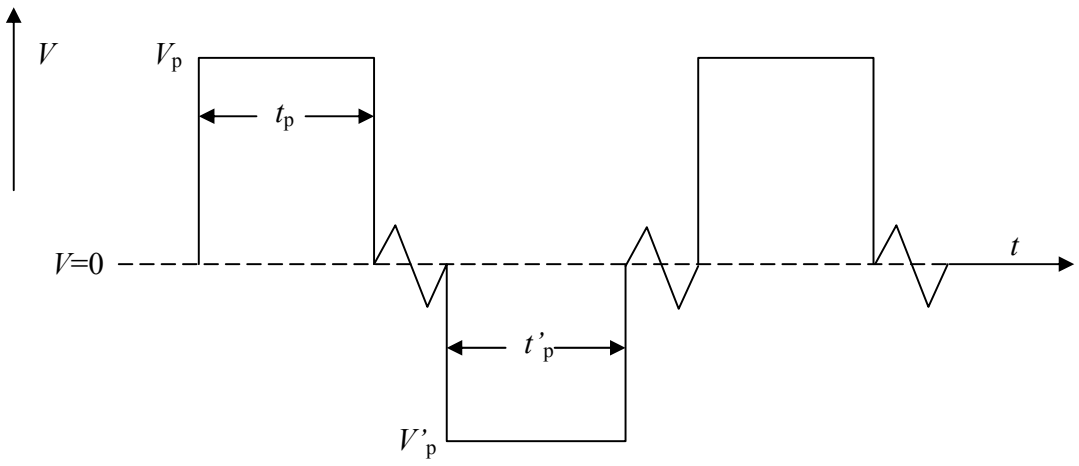


Figure 3.21 Schematic illustration of voltage pulses used in endurance test. V_p, t_p and V'_p, t'_p are the amplitude and duration of positive and negative applied voltage pulses, respectively. After each successful voltage pulse, a small and quick voltage sweep (with amplitude of 50 mV and time scale of 1 s) has been performed to obtain the resistive state of the junction.

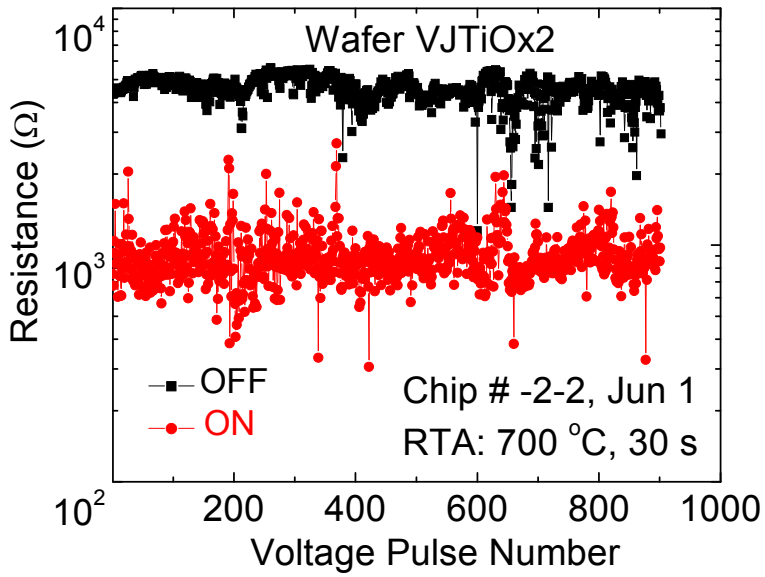


Figure 3.22 Results of the "endurance test" (repeated ON/OFF cycling) of a junction from wafer VJTiOx2 after RTA.

3.6 Multi-layer-TiO_x-based junctions

In hope to improve the results even further, and inspired by a recent publication [81], we have explored in detail the option of several sequential cycles, each consisting of deposition of a very thin (1.5 nm) Ti layer, followed by its plasma oxidation (wafers VJTiOx6, 8, 9, 12, 14, 16, and 17). Table 3.6 lists fabrication parameters and some major properties of junctions from these wafers.

Table 3.6 Parameters and properties of multi-layer TiO_x samples.

Wafer Inte	rlayer formation	Stack	RTA	Bistability/Properties	
VJTiOx6	plasma oxidation of 1.5 nm Ti (1 cycle)	Pt/TiO_x/Ti	400 to 700˚C, 30 s	Y	yield <30% R_{OFF}/R_{ON} <30
VJTiOx12				Y	
VJTiOx8	plasma oxidation of 1.5 nm Ti (5 cycles)		200 to 700˚C, 30 s	Y	yield ~70% R_{OFF}/R_{ON} = 30 - 10^3
VJTiOx14				Y	
VJTiOx16				Y	
VJTiOx17	plasma oxidation of 1.5 nm Ti (7 cycles)		300˚C, 30 s	Y	yield <40% R_{OFF}/R_{ON} = 50 - 10^3
VJTiOx9	plasma oxidation of 1.5 nm Ti (10 cycles)		400˚C, 30 s	Y	yield <15% R_{OFF}/R_{ON} >200 V_t >5 V

Such thin individual layers are hardly continuous (as partly confirmed by their HR TEM images like the one shown in Figure 3.3), and their sequential deposition and thorough oxidation are just a good way to produce a relatively thick, virtually uniform layer of TiO_x. For example, Figure 3.3 shows the ADF-STEM image of a sample from

wafer VJTiOx8, with 5 layers forming 13 nm of oxide. A detailed electron energy loss spectroscopy (EELS) study (Figures 3.23, 3.24 and 3.25) has shown that through this layer, the titanium-to-oxygen atomic ratio changed little, with the average value higher than 0.5, indicating some oxygen deficiency in comparison with the stoichiometric TiO_2. The study has also shown a certain fraction of Pt atoms in the oxide layer, gradually decreasing toward the counter-electrode, apparently due to some re-sputtering of the base electrode material in the oxidizing rf plasma, probably responsible for the layer non-uniformity visible in Figure 3.3.

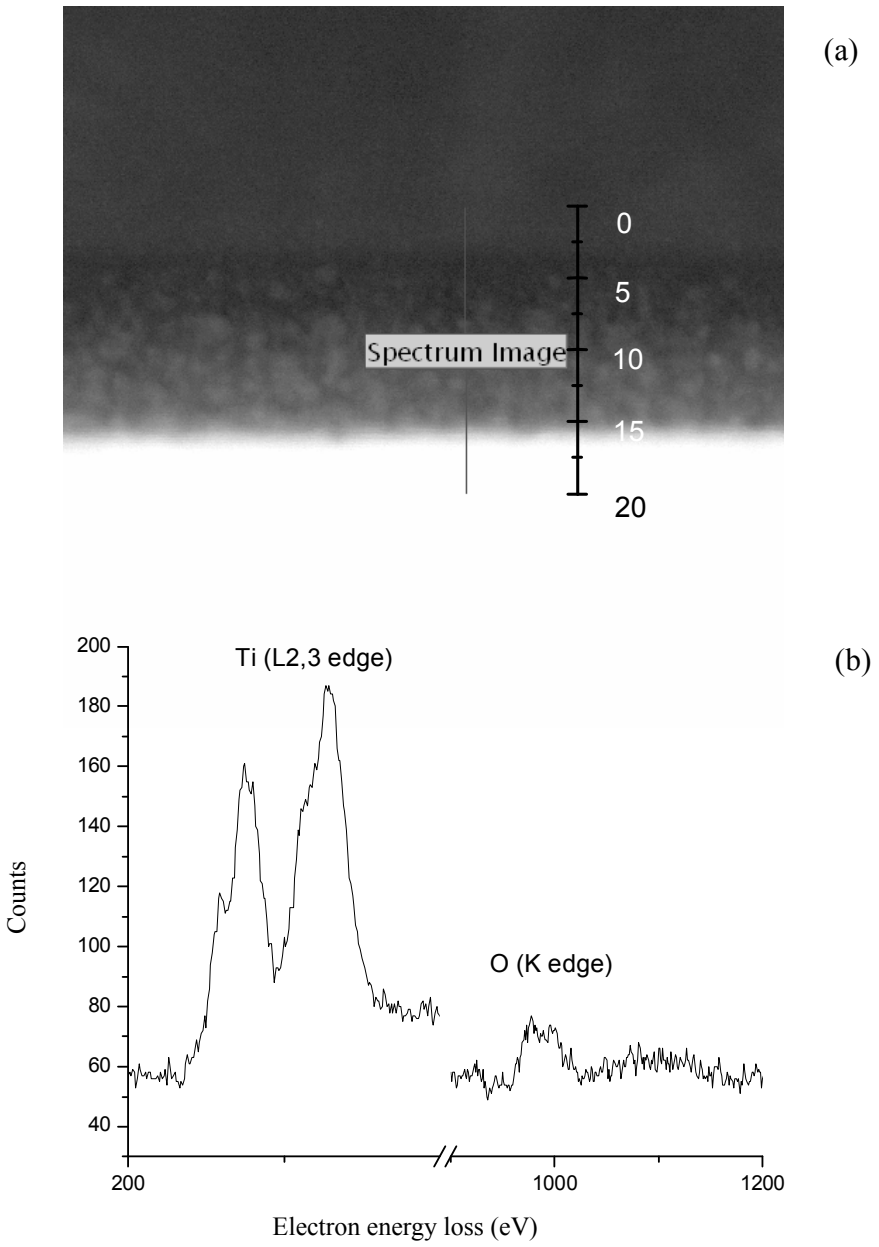


Figure 3.23 (a) EELS spectrum location references in an ADF-STEM image. Scale bar is in nanometers. (b) Typical electron energy loss peaks of titanium and oxygen in an EELS spectrum.

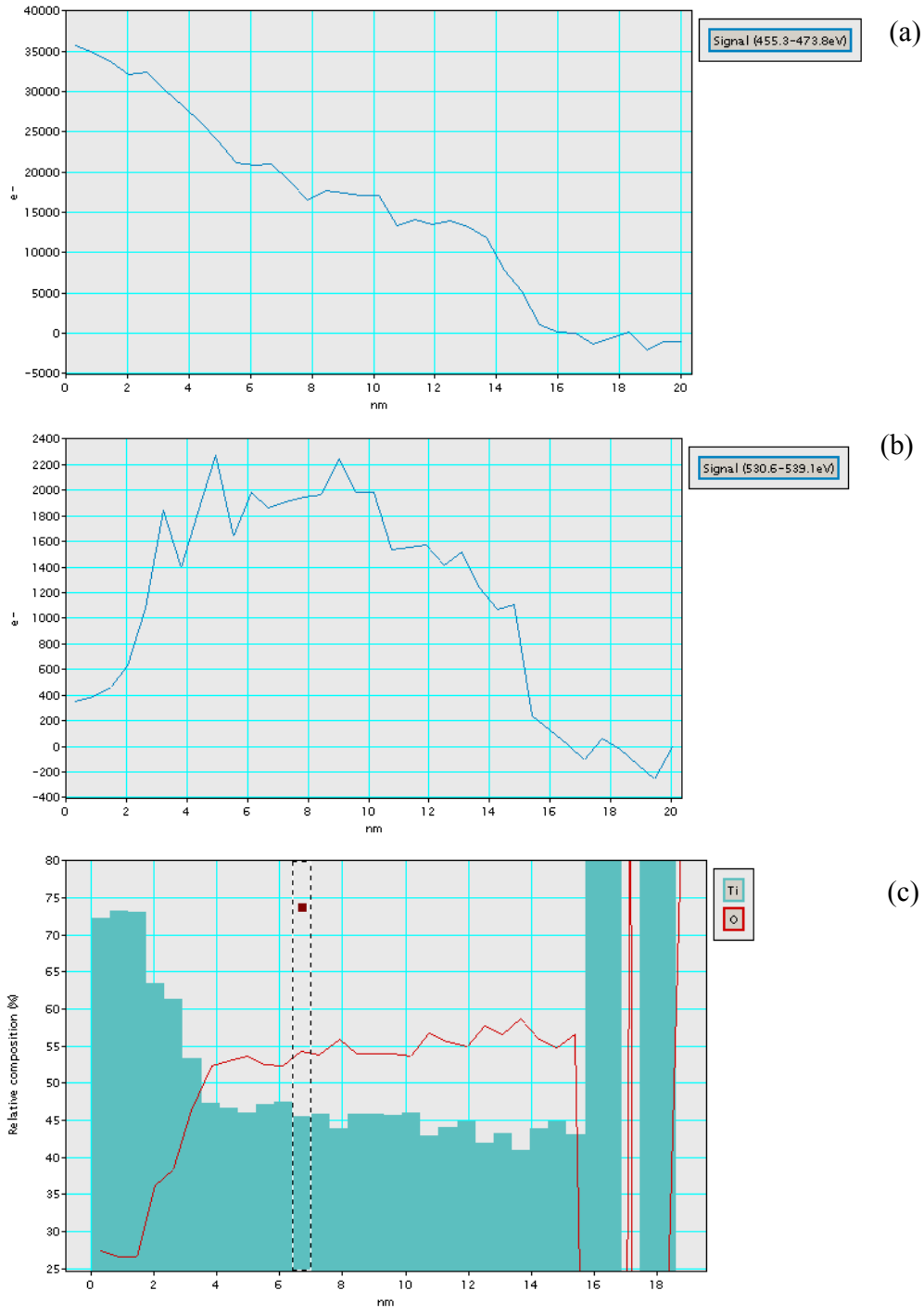


Figure 3.24 (a) EELS signal profile of titanium, (b) EELS signal profile of oxygen and (c) the relative concentration of titanium and oxygen of a device from wafer VJTiOx8.

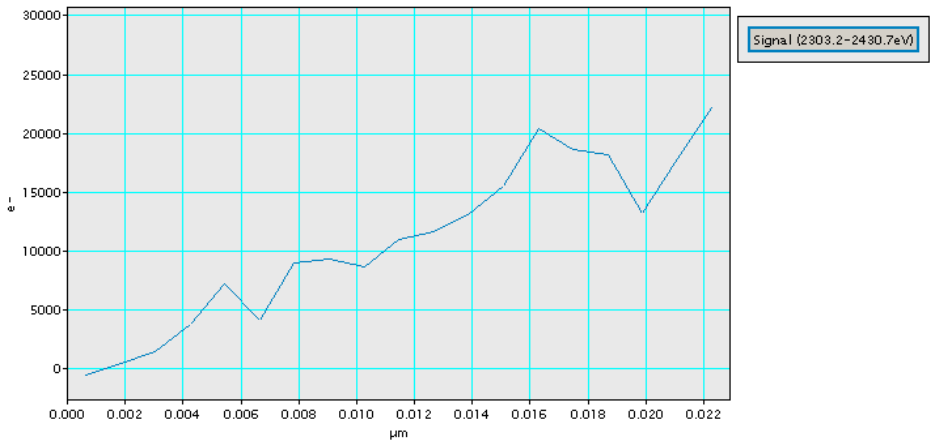


Figure 3.25 EELS signal profile of platinum of a device from wafer VJTiOx8.

Our further STEM study of 7 layers TiO_x samples from wafer VJTiOx17 (with total oxide thickness ~16 nm) has confirmed the oxygen deficiency and platinum re-sputtering phenomenon. (See Figures 3.26 and 3.27 for details.)

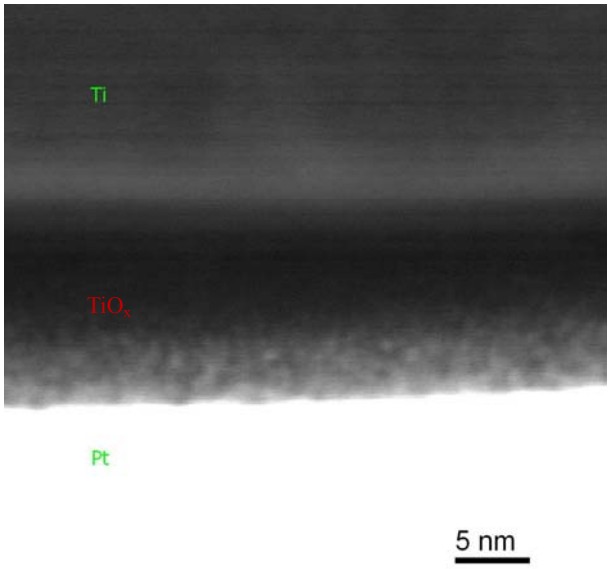


Figure 3.26 An ADF-STEM image of a junction from wafer VJTiOx17 (7 cycles).

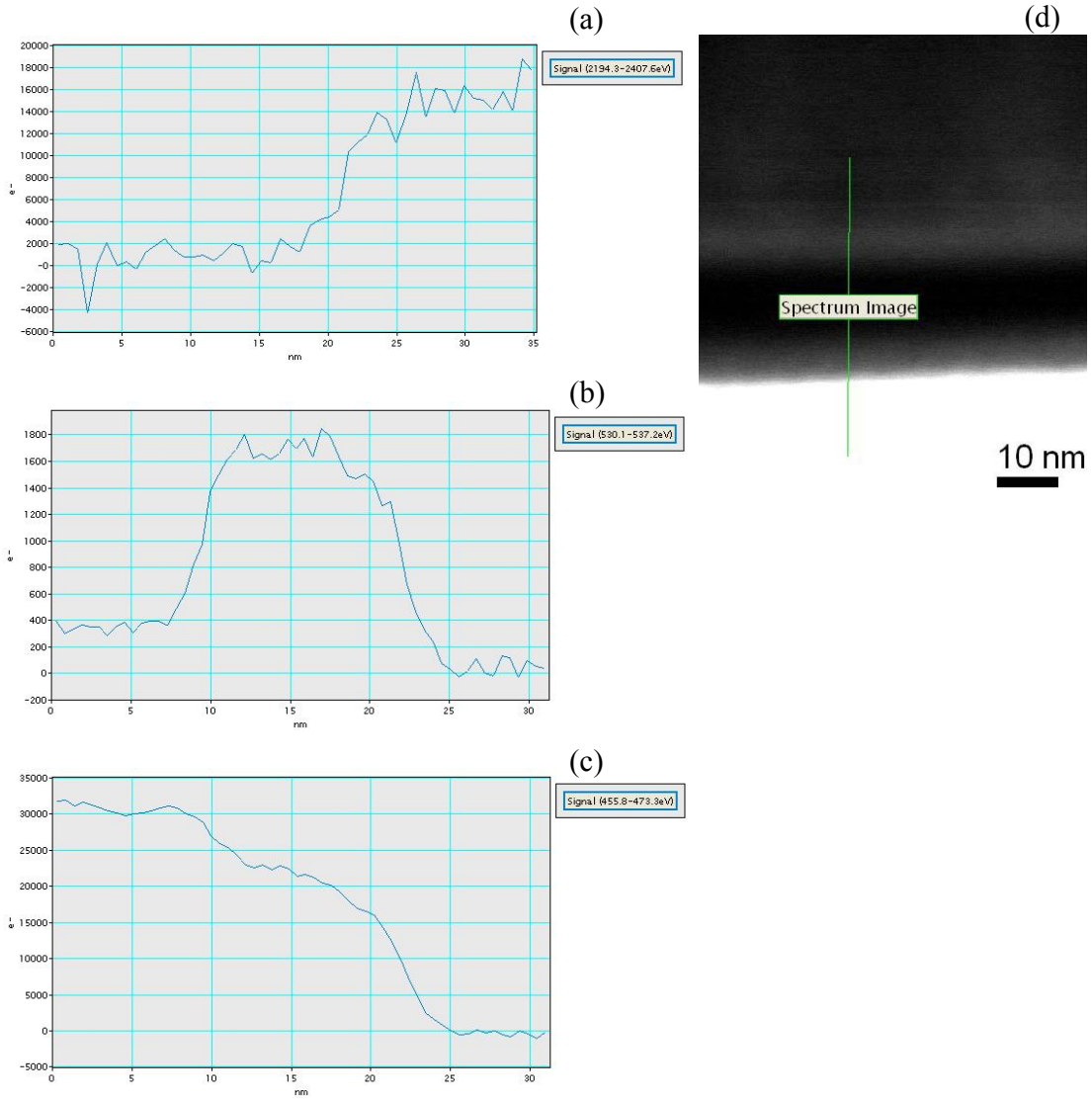


Figure 3.27 EELS signal profiles of (a) platinum, (b) oxygen and (c) titanium of a device from wafer VJTiOx8. Spectrum location references are given in (d).

The electrical measurements showed that such multi-cycle deposition gave us junctions with the best reproducibility to date, with ~70% junction yield without annealing. Figure 3.28 shows close similarity of dc *I-V* curves of good junctions from wafer VJTiOx8 (with $|V_t|$ and $|V'_t|$ ~1 V, current compliance at 2 mA and R_{OFF}/R_{ON} ~30).

Further endurance test showed the switching cycles can be repeated for $N \sim$ a few hundred times. The high yield obtained on our best wafer VJTiOx8, with 5 sequentially oxidized Ti layers, have allowed us to perform a more quantitative test of the sample-to-sample reproducibility, namely the measurements of switching threshold voltage statistics. The results are shown in Figure 3.29. One can see a clear gap between the histogram peaks corresponding to V_t and V'_t. Values of both threshold voltages can be obtained from Figure 3.29 as $V_t = 0.9 \pm 0.3$ V and $V'_t = 0.6 \pm 0.2$ V.

The high yield, small threshold voltage, low current and relatively high resistance ratio do partially fulfill the requirements for nonvolatile memory applications listed in Chapter 1.

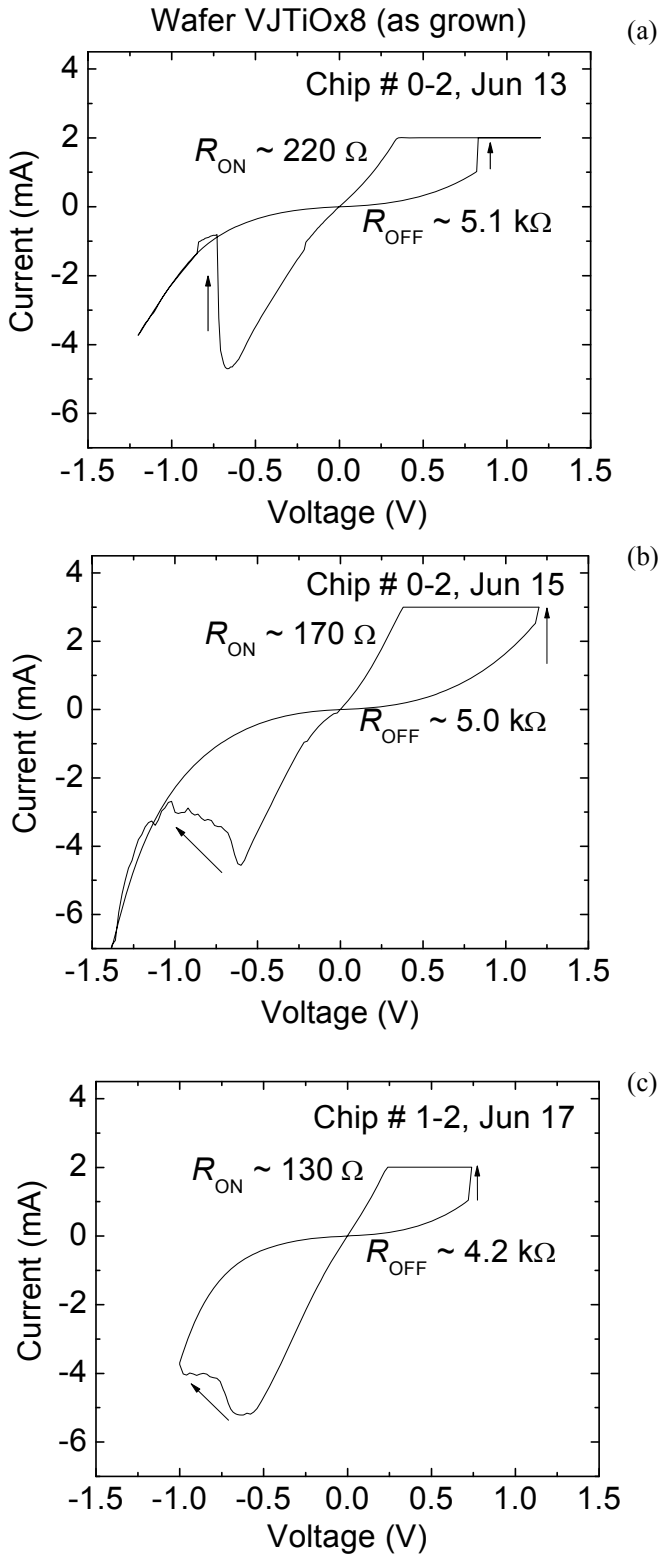


Figure 3.28 DC *I-V* curves of three different devices from wafer VJTiOx8 before the RTA.

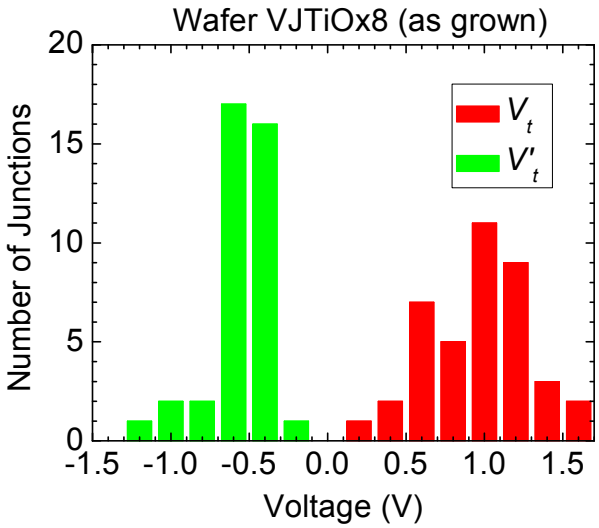


Figure 3.29 Statistics of the switching thresholds V_t and V'_t for "as grown" devices (i.e. before the RTA) from wafer VJTiOx8.

For further improvement of junction performance, selected chips were subjected to RTA at temperature from 200 to 700ºC for 30 seconds. Unfortunately, the RTA, while increasing the resistance ratio to as high as ~10^3 with annealing temperatures above 300ºC, and sustaining similarly high switching endurance, reduces the yield continuously to below 20% – see Figure 3.31. Figure 3.30 shows an *I*-V curve of a junction from wafer VJTiOx8 at an optimized annealing condition (i.e. 300ºC, 30 seconds) when resistance ratio is ~10^3 and yield is still good (around 50%). One should also notice the slight increase of threshold voltage V_t (~ 2 V) which keeps rising with higher annealing temperatures.

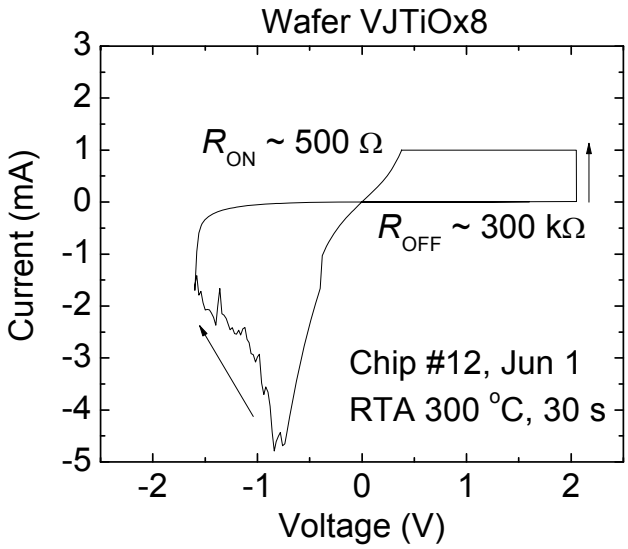


Figure 3.30 Typical dc *I-V* curve of a junction from wafer VJTiOx8 after the RTA.

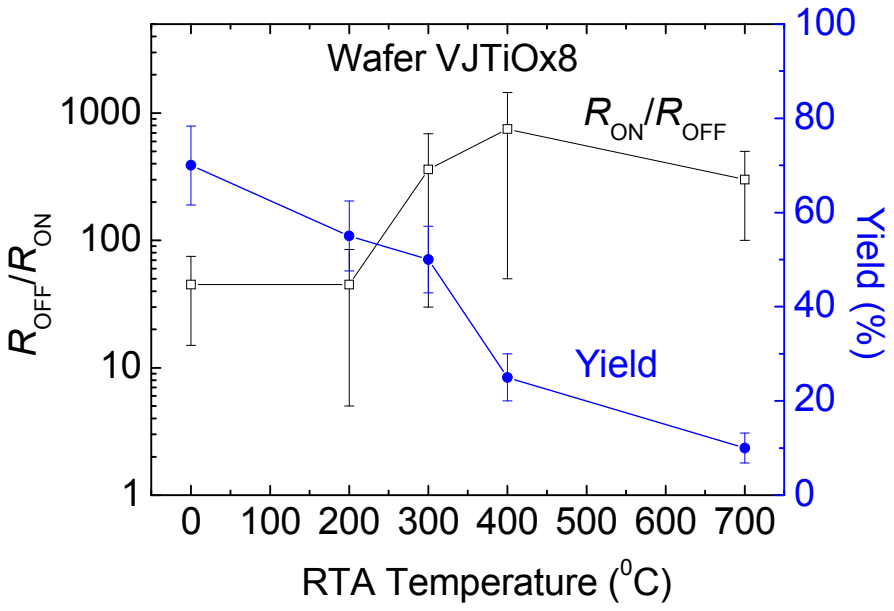


Figure 3.31 Effect of temperature of a 30-second RTA on the OFF/ON resistance ratio and the yield of good devices from that wafer.

Our attempts at more deposition-oxidation cycles to increase the oxide thickness (wafers VJTiOx9 and 17) gave a certain resistance ratio increase, but continuously reduced the good device yield, with much higher threshold voltages V_t and V'_t. Figure 3.32 shows a typical *I-V* curve of a junction from wafer VJTiOx17, with $V_t \sim 3.8$ V and $R_{OFF}/R_{ON} \sim 1000$. Post annealing kept reducing yield and raising threshold voltages.

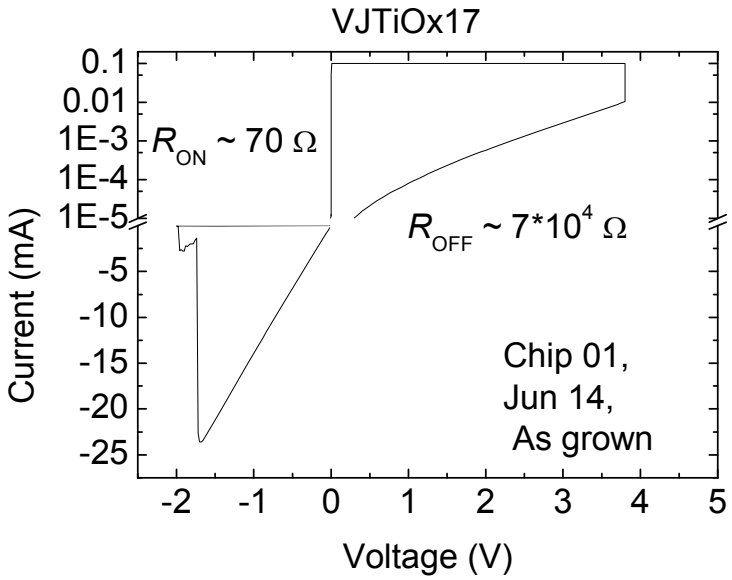


Figure 3.32 Typical dc *I-V* curve of a junction from wafer VJTiOx17. (7 cycles) Positive current is set in log scale to be visible in the plot.

3.7 Conclusions and other possible approaches

To summarize, we have explored the effect of resistive bistability in junctions with interlayers of three metal oxides, NbO_x, CuO_x, and TiO_x, formed by several techniques, within a broad range of fabrication and post-processing conditions – see Tables 3.3-3.6. The results indicate that the problem of reproducible resistive bistability is much harder than implied by most publications in the field. Namely, while the mere demonstration of the bistability is pretty straightforward with any of those oxides (and, by literature data, with many other materials), the implementation of device-to-device reproducibility, with high yield of good devices, is much harder.

So far, our best reproducibility results, with the yield close to 70%, and a clear separation of histogram peaks for two switching thresholds (Figure 3.29), have been obtained for TiO_x junctions with ~13 nm oxide layer formed by 5 sequential deposition-oxidation cycles, without post-annealing. While such reproducibility is on a par with the best results reported for metal oxide devices in the literature [66, 67, 73], it is only sufficient for simple hybrid circuit demonstrations [65, 89, 93, 94], rather for real large-scale integration. We see the following reserves available for the further improvement of the reproducibility and other device parameters (such as the R_{OFF}/R_{ON} ratio, switching endurance, and switching speed).

1. Using junctions of much smaller area.

Indeed, most interesting applications require much smaller (10-nm-scale) crosspoint devices [64], and the apparent mechanism of bistability (see Figure 1.3b-d and its

discussion) may actually give more reproducible results for smaller junctions – the conclusion partly confirmed in Reference 67.

Our next few wafers of TiO_x samples will be accompanied with electron beam lithography (EBL) for a good definition of smaller junction areas, e.g. 100×100 nm^2. We are also trying to use different chip configurations such as a crossbar structure (Figure 1.5) to avoid unnecessary overlaps of top and bottom electrodes and thus reduce the leakage current. The new crossbar configuration also enables us to demonstrate the idea of CMOS/nanoelectronic circuits. (See section 3.8 for details.)

2. Forming junctions with short voltage pulses (or their sequences), rather than the dc voltage used in our experiments.

Such method may prevent local heating effects which may mask, or even reverse the field-induced ion drift.

The initial setup of electrical measurements using short voltage pulses is schematically shown in Figure 3.33.

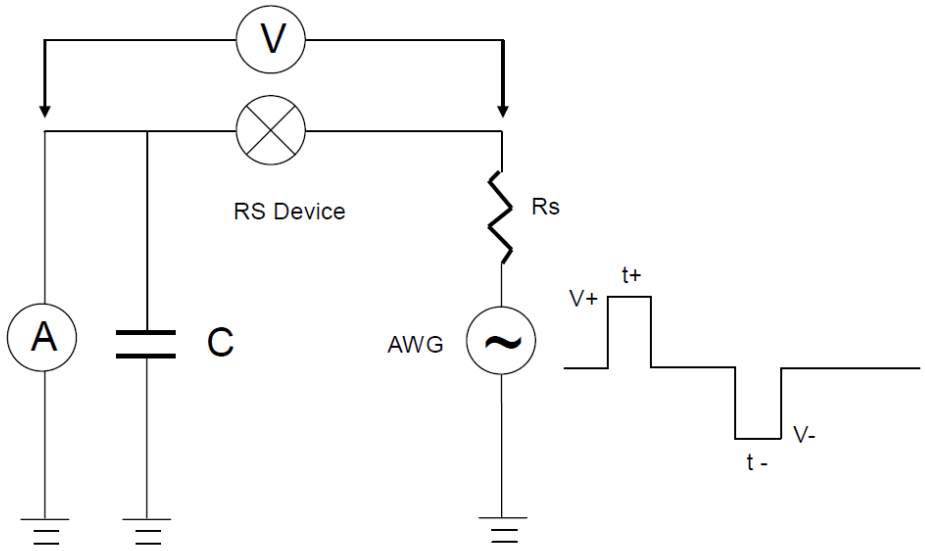


Figure 3.33 Diagram of setup for short voltage pulses measurements.

In Figure 3.3, an Arbitrary Waveform Generator (AWG) generates both positive and negative voltage pulses with corresponding amplitudes and durations V_+, t_+ and V_-, t_-. A series resistor R_s is using to limit the current and a capacitor C to ground high frequency components during the current measurements. After each successful voltage pulse, a small reading voltage V_{rd} is applied for sufficient time to obtain the state of the junction. Some typical values of these parameters are listed below:

$|V_+|, |V_-| \sim 1$ to 10 V

$t_+, t_- \sim 1\ \mu$s to 1 ms

$R_s \sim 1$ to 10 kΩ

$C \sim 1$ to 100 nF

$V_{rd} \sim 5$ mV

Our first attempts of using short voltage pulses didn't show great improvement of junction performance, and it was probably due to the complicated combination of the parameters listed above. The capacitance and inductance of other circuit components might also affect the results.

3. Using different materials and/or different fabrication conditions. (such as amorphous-silicon [79] or polymer interlayers [82])

We have fabricated 5 wafers with the same *p*-Si/a-Si/Ag stack described in Reference 79. The fabrication process is slightly different from metal oxide wafers in that it uses the bare *p*-type silicon substrate as the base electrode (after a standard industry procedure of RCA clean). The substrate has been loaded in an evaporation system (Pb system) to perform pre-cleaning in argon plasma, followed by electron beam evaporation of a 50-nm amorphous silicon (a-Si) layer. It has been sealed by a 100-nm-thick silver top electrode after sufficient time for substrate cooling down. The chip configuration and junction patterning are similar to those of metal oxide processes.

Figure 3.34 shows a dc *I-V* curve of a junction from wafer VJa-SiAg1. One can immediately notice the large OFF/ON resistance ratio ~1000 which is comparable to our best results of multi-layer TiO_x samples. Unfortunately, junctions from all 5 wafers have shown very poor yield (<5%) and endurance (<10 cycles). We believe the reasons include the a-Si thin film stress (since there is only one controllable parameter, deposition rate) and the large overlaps of the top and bottom electrodes.

We are also exploring the polymer thin film option, and the synthesis of WPF-oxy-F

[82] is conducted by Professor Andreas Mayr of the SBU Chemistry Department. It is also an obvious option for further integration study since the polymer memory layer deposition is only a simple step of spin-coating.

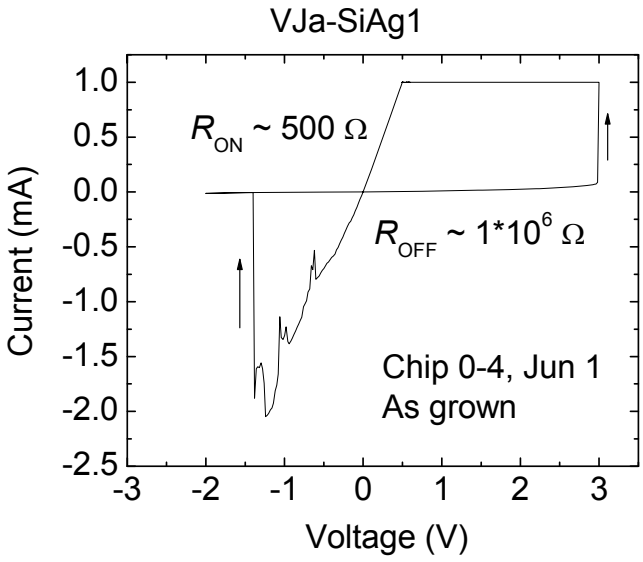


Figure 3.34 One dc *I-V* curve of a junction from wafer VJa-SiAg1.

It is our feeling that the task of reaching the ~90% device yield necessary for VLSI applications [64] is by no means hopeless, though it may require a large-scale industrial effort. We hope that our results will be useful for such effort.

3.8 Integration attempts

Inspired by the idea of CMOS/nanoelectronic circuits, we have ordered commercial CMOS chips from MOSIS using IBM 7RF 180nm process. The chip layout is shown in Figure 3.35, while Figure 3.36 shows microphotographs of fabricated chip fragments.

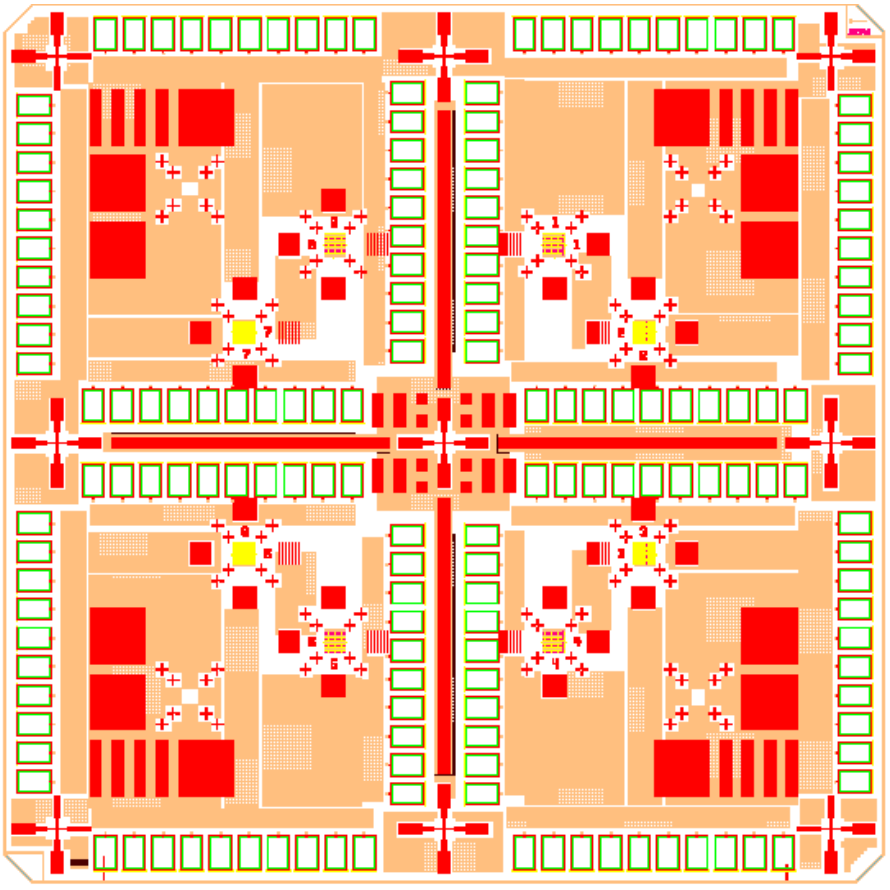


Figure 3.35 Layout of one CMOS chip.

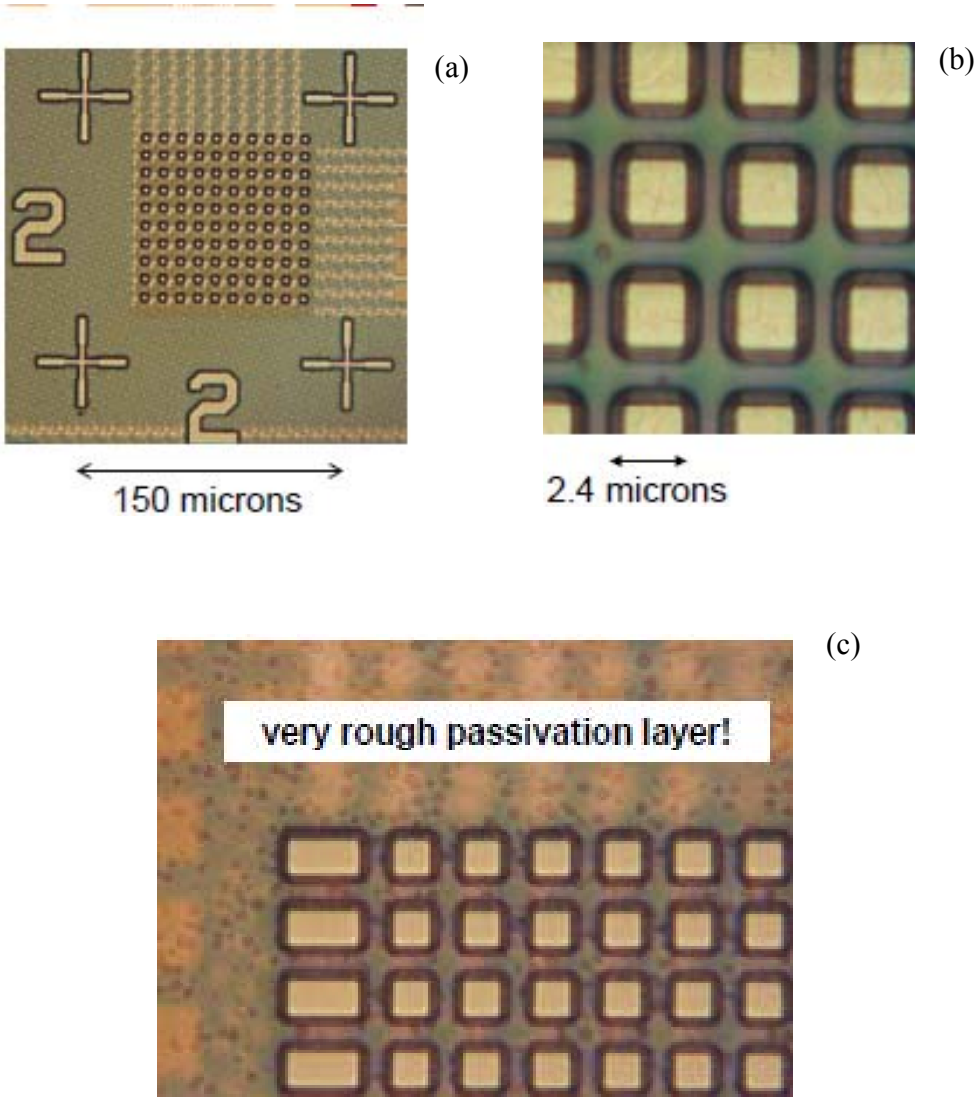


Figure 3.36 Actual microphotographs of CMOS chip surface.

Figure 3.15 shows the configuration of a 4×4 mm^2 CMOS chip assembly which contains 4 identical chips. Each chip has 200 transistors on it with their 40 leads (for Sources and Gates) spreading on it. The leads of drains are confined in the yellow areas with a set of align marks surrounding them.

Figure 3.16 shows images of actual CMOS chip surfaces with emphasis on "active areas" which mean the areas where the leads of drains (as contacts with nanowires of a crossbar) locate. One can immediately see that the size of the lead is ~ 2.4 μm which is virtually small to keep the high density of a crossbar, but sufficient for a good optical alignment. The very rough surface shown in panel (c) is due to silicon nitride passivation layer. Its removal is the first task of the integration process (Figure 3.37). After the passivation layer has been removed by either the chemical mechanical polishing (CMP) or the reactive ion etch (RIE), we will deposit and pattern the contact pin metals to make a good electrical contact with Drains of CMOS circuits. An insulating layer of SiO_2 will be then deposited and polished, followed by deposition and patterning of base metal nanowires, as well as the additional metal of contact pins for top nanowires. After all processes above have been done, the sample will go through similar steps of metal oxidation, insulator deposition, top metal deposition and their corresponding patterning as described in Chapter 3.2, i.e. wafer VJTiOx8, Pt/TiO_x/Ti stack with multi-layer TiO_x. It serves as a demonstration of CMOS/nanoelectronic circuits with a crossbar add-on on top of CMOS circuits (Figures 1.5 and 1.6).

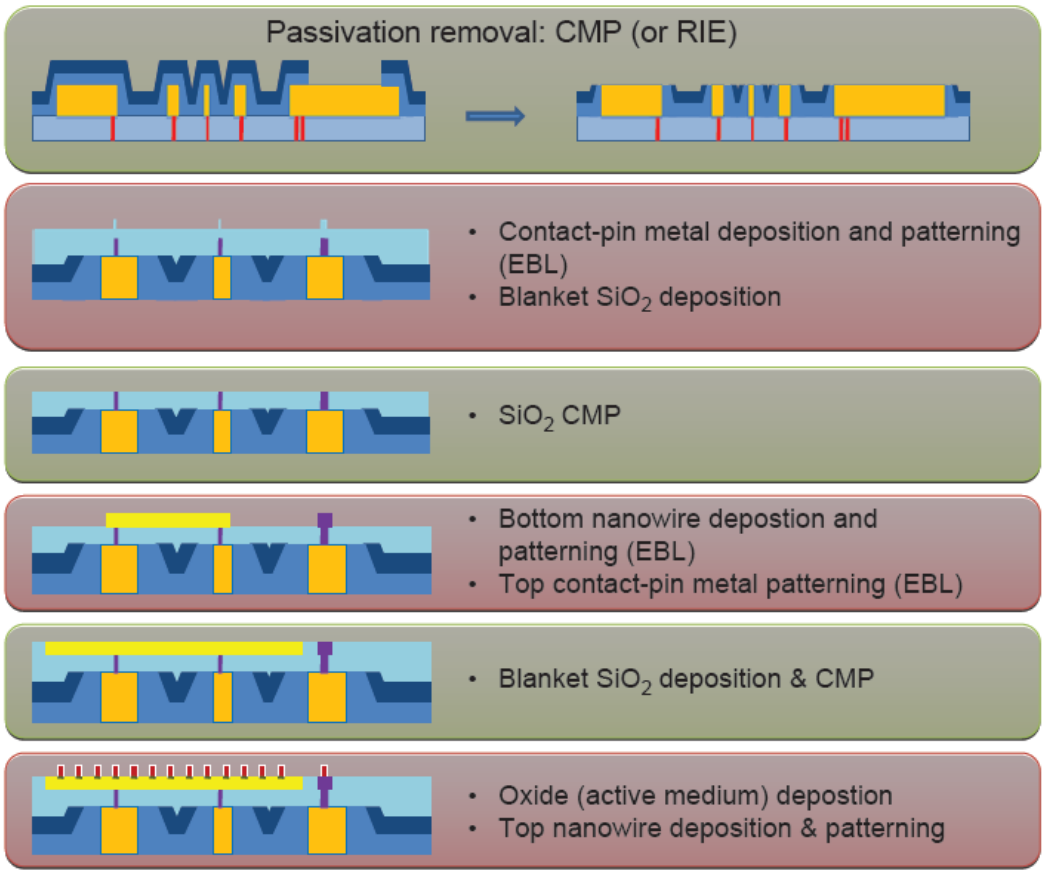


Figure 3.37 Integration steps for demonstration of CMOS/nanoelectronic circuits.

We are currently working on chemical mechanical polishing (CMP) for removing the passivation layer to expose the contact metal for further steps of integration. With the progress of device performance improvements and the new (small area) crosswire configuration in parallel, we can soon achieve the goal of a demonstration of hybrid CMOS/nanoelectronic circuits with a resistive memory device at each crosspoint. (See Figures 1.4 and 1.5.)

Chapter 4
Conclusions

We have studied electron transport properties of metal oxide junction of two types:

1. Aluminum oxide tunnel junctions for floating gate memory applications.

We have measured transport properties of all-metallic tunnel junctions with Nb/Al/Nb stack, fabricated using thermal oxidation or rf-plasma oxidation at various conditions. Rapid thermal post-annealing has been done to improve transport and endurance performance, in particular their endurance in electric fields in excess of 10 MV/cm. The results indicate that such junctions may combine high field endurance (corresponding to at least 10^{10} write/erase cycles in floating-gate memories) and high current density (corresponding to 30-ns-scale write/erase time) at high voltages, with very low conductance (corresponding to ~0.1s-scale retention time) at low voltages. The largest remaining problem with the application of these junctions in FGRAM is the "perturb effect" [27] , i.e. a substantial (by ~2 orders of magnitude) rise of their conductance at semi-selected conditions, i.e. at applied voltages close to 50% of the write/erase value, clearly visible in Figures 2.5 and 2.6. This issue should be addressed by the further improvement of the junctions, or altering the memory architecture, or both.

2. Resistive bistability for hybrid CMOS/nanoelectronic circuits.

We have studied resistive bistability (memory) effects in junctions based on metal

oxides, with a focus on sample-to-sample reproducibility which is necessary for the use of such junctions as crosspoint devices of hybrid CMOS/nanoelectronic circuits. Few-nm-thick layers of NbO_x, CuO_x and TiO_x have been formed by thermal and plasma oxidation, at various deposition and oxidation conditions, both with or without rapid thermal post-annealing (RTA). The resistive bistability effect has been observed for all these materials, with particularly high endurance (over 10^3 switching cycles) obtained for single-layer TiO_2 junctions, and the best reproducibility reached for multi-layer junctions of the same material. Fabrication optimization has allowed us to improve the OFF/ON resistance ratio to about 10^3, but the sample-to-sample reproducibility is so far lower than that required for large scale integration.

We hope that our results will give important clues for our further work in these directions, and to other research groups in pursuit of the goal of integrable nanodevice development.

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Appendix:

Process sheet of wafer VJTiOx2

(All parts with underlines have been filled after each fabrication step.

X indicates a specific step has been done.)

1. **Base electrode patterning** **Date 3/6/08** **Temp.72F** **R.H. 34 %**

X Spin Negative Resist UVN-30 (@3000 rpm, 60 s). [5000 Å]

X Soft Bake: (Temp 90^{o}C, Time 1 min)

X Expose: (JBA) Intensity **A**= 1.58 mW/cm^2 , **B** = 0.48 mW/cm^2 , Time 4.5 sec.

C.Vac. 0

X Post Exposure Bake: (Temp 90^{o}C, Time 1 min)

X Develop: (Microposit CD-26 : DI water 2:1) Temp 20.5^{o}C , Time 1:00 min

Clear @ 45 s

X Inspect, Comments:

clean, contact not good during exposure, edges rounded and marks not clear.

X Plasma Ash (@50W, 1Torr), 40s.

Resist Thickness: 4925 Å.

2. Metal Deposition **Date 3/7/08** **Run # 1203**

Process	B.P. (10^{-7} Torr)	Current (A)	Outgas (A)	Thickness (Å)	Time (min)	Rate (Å/sec)
Ti	6.4	0.68	80	900	15	1

Metal Lift-off

X Soak Acetone: 0.5 hrs.

X Ultrasonic in Acetone: 15 + 10 min.

X Inspect/Comments:

clean but due to poor CV edges rounded & alignment marks did not come out.

X Plasma ash: 1:40 min @50 W and 1 Torr.

Metal Thickness: 890 Å.

3. Oxidation & Nb CE Deposition **Date 3/10/08** **Run # 1568**

Process	B.P. $*10^{-7}$ (Torr)	Stage	Ar/O_2 Pr. (mTorr)	Power (W)	Current (A)	Voltage (V)	Time (min)	Stage Water
Sp. Clean	1.2	Down (Al)	9.5	150	46/40	606	1:00	ON
Oxidation	1.6	UP (Al)	15.0	50	51/33	305	10:10	ON
Nb Presp.	1.6	UP (Al)	10.5	600	2.03	297	2:00	ON
Nb CE	-	Down (Nb)	10.5	600	2.03	297	1:00	ON

Comments: Plasma oxidation at rf power 50 W, O_2 pressure 15 mTorr.

3. Junction Patterning

Mask _CREST M3_ Date _3/10/08_ Temp. 72F_ R.H. _34_ %

_X_ Spin 6% PMMA (@ 3000 rpm, 60 s). [10000 Å]

_X_ Bake: (Temp 140^{o}C, Time 5 min)

_X_ Expose: (JBA) Intensity **A**= 1.58 mW/cm^2 , **B** = 0.48 mW/cm^2 Time

_994_ sec. C.Vac. -3”

_X_ Develop: (MIBK : IPA 1:1) Temp _20.5 ^{o}C , Time _1:00 min + Buzz _0:45 sec

_X_ Inspect, Comments:

OK, few defects, sharp.

_X_ Plasma Ash (@50W, 1Torr), 40s

Surface Clean

Soak in DI water: 0.5 min, and check contact angle.

Wet Etch (15% Phosphoric Acid @ 50 ^{0}C): 20 sec

PLASMA ETCH Nb CE Date: _3/10/08_ Run _2567_

Gas	BP (10^{-5} Torr)	Flow rate (ccm)	Gas Pres. (mTorr)	Power (W)	V_b (V)	Time (min)	End-point @
SF_6	2.6	11.2	25	20	-1.2	2:00	1:30

_X_ Inspect/Comments: _Ok._

4. SiO_2 (Quartz) Deposition **Date 3/17/08** **Run # 798**

B.P. (10^{-7} Torr)	Ar Press. (mTorr)	Power (W)	V_{bias} (V)	V_{p-p} (V)	Deposition Time (min)	Wait Time (min)
2.46	2.5	400	-931	1540	2:30	6:00
					2:30	

Quartz Liftoff

X Stripper (Acetone) – Soak: >12 hrs.

X Ultrasonic in Acetone: 10 min Q-tip scrub? yes + Buzz: 10 min

X Inspect, Comments:

top left corner chipped off (was cracked in quartz system).

X Thickness: I2 above M3 630 Å

X Plasma Ash @50W, 1Torr, 2:00 min

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5. M4 Wiring Mask CREST M4 Date 3/18 /08 Temp. 72F R.H 35 %

X Spin 6% PMMA (@ 4000 rpm, 60 s). [8000 Å]

X Bake: (Temp 140°C, Time 5 min)

X Expose (JBA): Intensity **A**= 1.56 mW/cm^2, **B** = 0.47 mW/cm^2 Time 994 sec.

C.Vac. -2"

X Develop (MIBK : IPA 1:1): Temp 20 °C , Time 1:00 min + Buzz 0:45 sec

X Inspect, Comments: Ok.

X Plasma Ash (@50W, 1Torr): 40s

X Resist Thickness: 8100 Å

6. Nb Wiring Layer Deposition **Date 3/20/08** **Run # 1575**

Process	B.P. (10^{-7} Torr)	Stage	Ar Pr. (mTorr)	Power (W)	Current (A)	Voltage (V)	Time (min)
Sp. Clean	3.0	UP (Out)	9.5	150	48/41	615	2:00
Nb Presp.	2.8	UP (Al)	10.5	600	2.03	297	2:00
Nb CE	-	Down (Nb)	10.5	600	2.03	297	2:00

Nb Liftoff

X Soak in Stripper (Acetone): 60 min.

X Ultrasonic in Acetone: 5 min.

X Inspect, Comments: Ok.