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Front-End Read-Out System for Radiation Scintillation Detector

A Dissertation Presented

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Abstract of the Dissertation

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Detection of various nuclear radiation sources is increasingly important for security issues. A novel three-dimensional (3D) integration of scintillation-type semiconductor radiation detector pixels has been proposed. This dissertation presents a design methodology of a low-power low-noise integrated front-end readout solution suitable for the proposed detector.

The low-power low-noise front-end readout system contains a charge sensitive amplifier (CSA), a analog signal processing unit and an analog-to-digital converter (ADC). The CSA isolates big parasitic capacitor of the detector, and allows the electrons generated from detector to integrate on a smaller capacitor. The signal processing unit contains a high order semi-Gaussian pulse shaping filter and a peak detector. The shaping filter filters the output signal from CSA and maximizes the signal to noise ratio. The peak detector captures the peak amplitude from shaping filter, which is proportional to the number of input electrons. Noise model of

the readout system is constructed, and several noise optimization techniques are discussed to minimize the equivalent noise charge (ENC).

The analog-to-digital converter required in the readout system needs to be low power, high absolute accuracy and tones-free. Extended counting analog-to-digital converter combines the accuracy of delta-sigma modulation and the speed of algorithmic conversion. This conversion architecture is shown to be useful in applications with multiple sensory channels, where both resolution and speed are demanded. A design of a 13 bit extended counting ADC is presented.

This dissertation provides detail discussion on design and simulation of each building block, comparison between different architectures, and experimental results of prototype ASICs, which are implemented through 0.5um CMOS process.

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Part I

Introduction

Chapter 1

Introduction

1.1 Integrated Sensory Microsystems

Design of integrated microsystems and system-on-a-chip solutions combined with advances in MEMS technology leads to significant miniaturization of sensor devices. Such microsystems have a significant and pervasive impact on a large number of applications, including radiation detection [1, 2, 3].

While not every application shares the same requirements, a common system framework can be shared and it provides a basis for defining the design procedures to be followed for development of these systems. The realization of such microsystems requires them to be small, portable, low-power, highly accurate sensing modules capable of bidirectional communication. These solutions should also allow for the integration of the sensors and the electronic interface on the same substrate. Another important constraint posed on these systems would require them to have the ability to perform in distributed instrumentation systems collecting data over a broad physical area leading to multichannel design that would interface distributed sensor arrays. The result of this combination is a smart sensor array.

The interface and processing circuitry has to be placed close to the sensor array for integration and needs to provide sufficient signal processing to extract a limited number of essential features to reduce signal bandwidth before further transmission of information. The limited available power makes a single-chip solution inevitable and its design a challenging task. This solution significantly reduces the size and increases the reliability of complete system. Adaptive solutions have to be incorporated in the system to compensate all the limitations of the interface, such as parasitic effects, low sensitivity and nonlinearities [4].

This work presents an example of such microsystems using common design principles and architectures in radiation detection application.

1.2 Radiation Detection

Lately, nuclear threat has been an increasingly important security issues. The detection of nuclear radiation is important part of prevention of terrorist threats. There is great need to develop, deploy and enhance nuclear and radiological detection capabilities to prevent illicit use of nuclear devices or materials. Great efforts have been made to enhance the effective integration of nuclear and radiological detection capabilities. Figure 1.1 shows a current monitor portal installed at a highway entry port.

However, current portal monitors susceptible to false alarms caused by legitimate radioactive materials, e.g. Bananas, kitty litter, medical isotopes, ceramic tiles, fertilizer. False alarms create undesirable operational burdens on customs and border personnel and costly delays in commercial flow of goods. Therefore, an innovative radiation detector with high sensitivity is required. Plus, handheld or backpack identifier is also in demand to allow flexible and convenient detection. Power and weigh need to be reduced to allow such features to be included.

Figure 1.1: Current portal monitors

Radiation detection techniques for threat reduction application can also transform to other programs of research and development in detection technologies. The radiation of interest may include charged particles (e.g., fast electrons and heavy charged particles), and uncharged particles (e.g., neutrons, X- and gamma-rays). In all cases, the radiation energy must be high enough to cause ionization in the sensing material. The resulting free charges can be single polarity ones, like electrons (e.g., gas sensors), or of dual polarity like electron-hole pairs (e.g., semiconductor sensors).

1.3 Radiation Detector

There are two large groups of solid-state radiation detectors, which dominate the area of ionizing radiation measurements, scintillation detectors and semiconductor diodes [1]. Semiconductor diodes employ reverse biased junctions where

the absorbed radiation creates electrons and holes. The scintillators detect high-energy radiation through generation of light which is subsequently registered by a photo-detector that converts light into an electrical signal. The first type of detector suffers from high voltages and low speed. The second type of detector, though having advantage of low cost and large detection volume, traditionally suffers from low efficiency of converting the high-energy radiation into light, thus low resolution.

Fundamental reason for poor resolution in dielectric scintillators is that the luminescent yield is controlled by reactions that are nonlinear in the density of generated electron-hole pairs, leading to non-proportionality response in radiation events. A new monolithic scintillation-type multilayer detector, in which high-energy radiation produces electron-hole pairs in a direct-gap semiconductor material that subsequently recombine producing infrared light to be registered by photo-detectors located on the surface of each semiconductor layer, is proposed.

The key issue in implementing a semiconductor scintillator is how to make the material transmit its own infrared luminescence [5]. The first attempt is to use Burstein shift technique to improves efficiency of radiation to infrared light. However, semiconductor materials based on extremely high radiative efficiency of high-quality direct-gap, such as InP, prove to be an excellent candidate for radiation detection. Figure 1.2 shows the proposed semiconductor scintillator with a InP scintillator body and an integrated photodiode on its surface.

Another innovative feature of the proposed detector is that it enables monolithic three-dimensional (3D) integration of standard semiconductor wafers, each provided with a pixellated epitaxial photosensitive layer on its surface as well as amplifying and analog-to-digital electronic circuits. The 3D pixellation of the scintillator response enables a novel scheme for high-resolution angular discrimination using compton telescope technique [6, 7, 8, 9]. Therefore, direction of the radiation source can be determined simultaneously. Figure 1.3 shows the 3D scheme of the

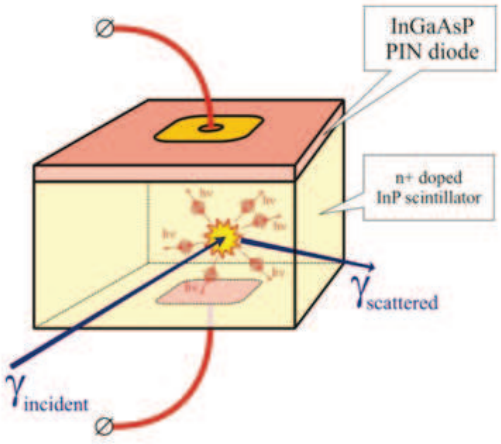

Figure 1.2: Semiconductor scintillator comprising a scintillator body and an integrated photodiode (top plate) on its surface.

proposed system. Figure 1.4 displays the mechanism of compton telescope. The diagram illustrates the track of a gamma photon of diminishing energy upon several successive compton interactions producing a cluster of firing voxels.

The proposed low-power high-resolution detector makes it amenable to applications where the power source is a microbattery. Its ability to integrate large volume under conventional, fully matured CMOS process makes it low-cost and reliable. In addition, the sensor probes can be fabricated on the same substrate as the front-end read-out circuitry and interfaced create fully integrated stand-alone portable detection device capable of sensing, processing and transmitting radiation signals.

1.4 Organization

The remainder of the proposal describes the theory, design procedures and implementation in detail. Part II Analog Section describes design of the analog section of a front-end readout system, which includes charge sensitive amplifier (CSA), shaper and peak detector. Chapter 2 first presents a general problem forming and

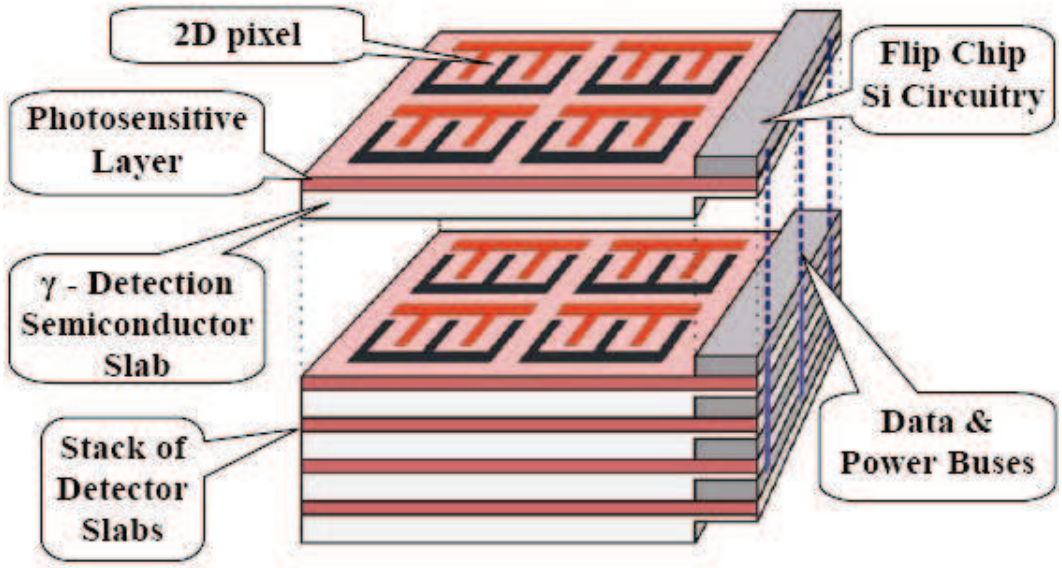

Figure 1.3: 3D pixellation of scintillator

system overview. Chapter 3 presents design and optimization theories of CSA. Chapter 4 presents the theory and design of a analog signal processing unit, including a semi-Gaussian pulse shaper and a peak detector. Chapter 5 describes the implemented ASIC under 0.5um CMOS process. Part III Analog-to-Digital Conversion describes the proposed extended counting ADC for multi-channel readout system. Chapter 6 describes the design and implementation of a 13 bit extended counting analog-to-digital converter. Part IV Conclusions summarizes the dissertation.

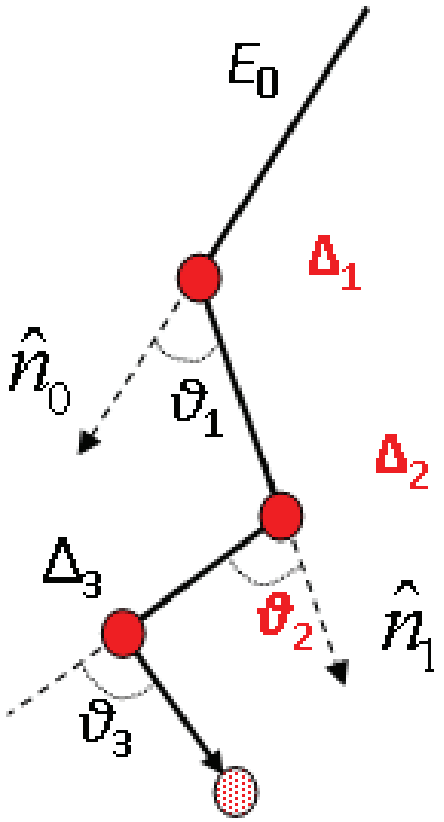

Figure 1.4: Diagram of compton telescope.

Part II

Analog Section

Chapter 2

System Overview

This chapter introduces the problem of reading out signal produced by radiation detector. An integrated front-end readout solution is provided, with brief descriptions of each building blocks. Concept of equivalent noise charge (ENC) is introduced.

2.1 Problem Forming

The proposed three-dimensional (3D) integration of scintillation-type semiconductor detector pixels provides accurate spectroscopic resolution for isotope discrimination and an accurate determination of the direction to source at the same time. In this novel scintillation-type semiconductor detector, high energy radiation produces electron-hole pairs in a direct-gap semiconductor material that subsequently undergo interband recombination, producing infrared light to be registered by a photo-detector.

To measure the optical response of pixelized detector, an application specific integrated circuit has to be designed. The integrated circuit should also be pixilated,

where each of the active pixels would sense the weak and short analog pulse as electrical signal produced by the photo-detector and convert it to digital signal. The digital value should be proportional to the charge produced by the detector and it should be communicated to the digital processing unit, as well as the coordinates of the pixel in which the activity occurred.

The detector can be modeled as a capacitor in parallel with a current source. The current source represents the signal generated by the detector, and it is a small current AC pulse, which has a time period in the nano-second range, on top of a constant DC leakage current. The magnitude of the AC current pulse is determined by number of electrons produced by the detector, which is normally a few thousand or hundreds of thousand, depending on the specific detector and the radiation sources. The constant DC detector leakage current for most radiation detector is measured to be between 10 pA and 100 nA. The capacitor represents the parasitic capacitance to ground of the detector, which imposes the most stringent constraint in the design. The value of parasitic capacitance, for the pixel size of $1mm$ by $1mm$ is estimated to be 50 pF. Another important design parameter would be the rate at which the pulse is likely to appear at the same pixel and based on the physical considerations, we expect to have a time of 100 ms between two consecutive pulses.

The main function of a front-end readout system is to capture the AC current pulses, and convert it to a voltage signal that represents the number of electrons produced by the detector in case of a event. The voltage signal is then digitized for further processing. The AC current pulses should be isolated from the DC constant leakage current and integrated on a smaller capacitor. Because 100 K electrons integrating on a 50 pF capacitor produces only 320 uV, while 100 nA current integrating on a 50 pF capacitor for a time period of 1 mS produces 2 V. The large parasitic capacitance gives uniqueness to the specifications imposed on the sensing

circuitry and requires development of novel circuit techniques to relax the effect of input parasitic capacitance. The readout system should also be able to self-reset after processing each event for continuous automatic read out. The processing time should be kept within one tenth of the estimated time interval between consecutive pulses to avoid signal pile-up.

2.2 Proposed System

The proposed read out system is shown in figure 2.1. Charge sensitive amplifier (CSA) isolates the big input parasitic capacitance, allows most of the electrons produced by detector to integrate on a smaller capacitor C_f in the feedback loop. The second stage is a analog signal processing unit, which includes a pulse shaper and a peak detector. The unit performs signal conditioning, noise optimization and preprocessing before analog-to-digital conversion. Many studies have been conducted on the pulse shaping filter in terms of signal to noise ratio, and have been concluded that a semi-Gaussian shaper generally give the best noise performance [42]-[47]. The output of the shaper is a semi-Gaussian shape pulse with its peak amplitude proportional to input charge Q. The peak of the pulse is captured by the subsequent peak detector. Finally, the analog-to-digital converter converts analog signal information to digital domain before further processing.

2.2.1 Signal Path

The input signal due to one electron charge generated from the detector can be modeled as a Dirac current pulse, whose integral is around q, charge of one electron. The output signal of CSA can be shown as an exponential rise voltage step, with a steady state amplitude of q/C_f. The rise time constant is inversely proportional

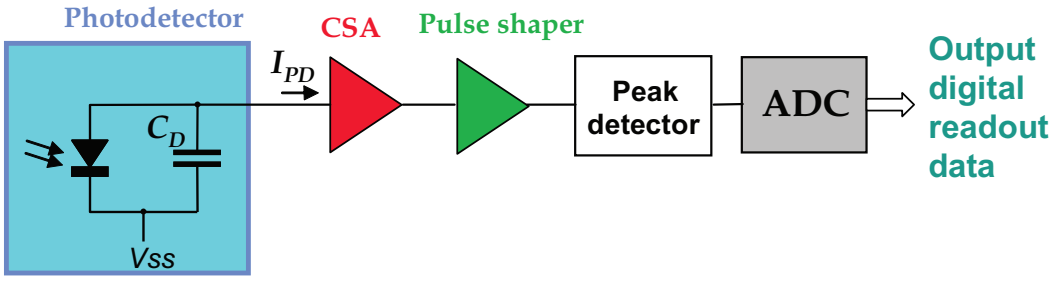

Figure 2.1: Proposed Readout System Block Diagram

to the gain bandwidth of the amplifier and proportional to the detector capacitance. However, it is usually made of only a couple of nanoseconds. Thus, it is reasonable to assume the output of CSA is an ideal voltage step with an amplitude of q/C_f.

The transfer function of a n-th order semi-Gaussian pulse shaper can be expressed as:

$$H(s) = [\frac{s\tau}{1+s\tau}][\frac{1}{1+s\tau}]^n \tag{2.1}$$

where the pulse shaper consists of one differentiator and n integrators, both with the same time constant τ. The output of signal of the pulse shaper is calculated as:

$$V_{out,CSA}(s) = \frac{q}{sC_f}$$

$$V_{out}(s) = V_{out,CSA} \cdot H(s)$$

$$V_{out}(t) = \frac{qn^n}{C_f n!}(\frac{t}{n\tau})^n e^{-t/\tau} \tag{2.2}$$

Equation 2.2 is a semi-Gaussian alike pulse and has a peak at time $n\tau$. The peak amplitude is derived as:

$$V_{out,max} = \frac{qn^n}{C_f n! e^n} \tag{2.3}$$

Thus, the peak amplitude of the output signal is proportional with the generated charge. By measuring the peak value of output signal, the amount of electrons that are generated from detector can be determined.

2.2.2 Noise Path

From the noise point of view, the charge pulse from photodiode first passes low-noise amplification stage that is designed to contribute a minimal amount of intrinsic circuitry noise. The contribution of noise from the further processing stages is in that way significantly reduced since, when referenced to the input, it will be divided by the gain of preamplifier. After the pre-amplification of the signal, a filtering or pulse-shaping is performed for boosting the signal-to-noise ratio. The pulse-shaping processing block utilizes the fact that the noise in this case is broad-band signal, while the signal is narrow-band. If the filtering would match the spectral density of the signal, maximum signal-to-noise ratio could be achieved and at the same time minimal sensitivity.

The dominant noise sources of a detector readout system are shown in figure 2.2. V_n is the total input referred noise of CSA, which contains thermal noise and 1/f flicker noise components. I_n is the shot noise from detector leakage current. The noise contributions from the following stages are relatively small because of the gain of CSA, and are ignored. V_n and I_n can be expressed as:

The total noise power at the output of CSA is then calculated as:

$$V_{n,out}(s)^2 = (\frac{C_{in} + C_f}{C_f})^2 V_n^2 + (\frac{1}{sC_f})^2 I_n^2 \tag{2.4}$$

where C_{in} is the capacitance seen at the input of CSA and is composed with the parasitic capacitance of detector and the input capacitance of CSA.

The total noise power spectrum at the output of pulse shaper is then calculated

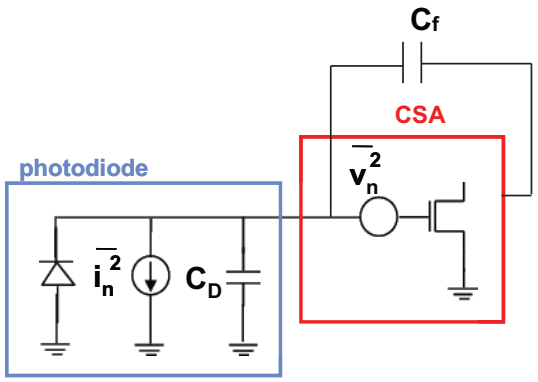

Figure 2.2: Simplified noise model for detector system

as:

$$V_{n,tot}^2 = \int_0^\infty |V_{n,out}(j2\pi f)|^2 |H(j2\pi f)|^2 df \tag{2.5}$$

where $H(s)$ is the transfer function of pulse shaper.

2.3 Equivalent Noise Charge

The measure of sensitivity of the front-end readout system is normally characterized as equivalent noise charge (ENC). The ENC is defined as the ratio of the total integrated rms noise at the output of the pulse shaper to the signal amplitude due to one electron charge q [13]. ENC can be calculated by dividing equation 2.5 and 2.3. It is summarized as following:

$$ENC_{ws}^2 = a_{ws}\frac{\gamma}{g_m}(C_p + C_g)^2\frac{1}{\tau} \tag{2.6}$$

$$ENC_{wp}^2 = a_{wp} I_{det} \tau \tag{2.7}$$

$$ENC_{1/f}^2 = a_f K_F (C_p + C_g)^2 \tag{2.8}$$

where ENC_{ws}, ENC_{wp} and $ENC_{1/f}$ represent the three main noise components, namely the white series noise, originating from input MOS thermal noise, the flicker noise, and the white parallel noise, due to the detector leakage current; a_{ws}, a_{wp} and a_f are the constant shaping factors that depend on the order of pulse shaper; γ is the thermal noise coefficient that depends on the operation region of transistor; g_m and C_g are the transconductance and gate capacitance of input MOS transistor; C_p is the load capacitance at the CSA input, which is the summation of the detector parasitic capacitance C_d, feedback capacitor C_f and other parasitic capacitance resulting from bonding; τ is the time constant of the pulse shaper; I_{det} is the detector leakage current and K_F is integrated flicker noise contribution of input transistor.

It can be seen that the thermal noise component is proportional to input capacitance and inversely proportional to the time constant of pulse shaper; the shot noise component is proportional to the time constant while independent to the input capacitance; the 1/f noise component is proportional to input parasitic capacitance while independent to the time constant of pulse shaper. Thus, the ENC is optimized in respect to both the pre-amplifier and the pulse shaper. Details of noise optimization techniques are described in Chapter 3.

2.4 Conclusion

This chapter presents a proposed solution for front-end readout system. It includes a charge sensitive amplifier, a pulse shaper and a peak detector. Equations for calculating the equivalent noise charge are derived.

Chapter 3

Charge Sensitive Amplifier

The charge pulse has to be pre-amplified before any processing that is necessary for increased sensitivity and signal-to-noise ratio could take place. The input pre-amplification can be performed in two ways. The charge can be directly integrated on the detector capacitance and this voltage can be readout with high-input impedance voltage amplifier. However, with the signal strength of our specific detector and its large parasitic capacitance, this method would lead to undetectable voltage signal and is hardly possible. The other way is to use a low input impedance amplifier, using either charge or current amplifier. With charge sensitive amplifier the charge is integrated on a smaller feedback capacitance and voltage step is observed at the output. With the current amplifier, the current is buffered and can be integrated on the smaller capacitor at the output of amplifier. This work focuses mainly on CSA, as it is the dominant structure in detector readout system.

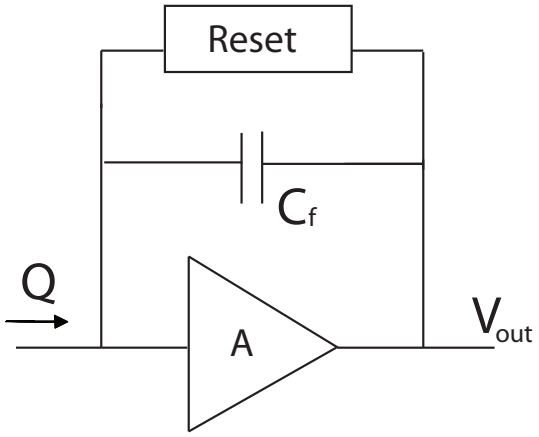

Figure 3.1: Charge Sensitive Amplifier (CSA)

3.1 Circuit Overview

A Charge Sensitive Amplifier or CSA converts input charge signal into voltage signal [10]-[15]. A model of CSA is shown in figure 3.1. The amplifier used in CSA generally has a large input impedance, moderate small signal gain and moderate bandwidth. Due to Miller effect, the current pulse generated by detector mainly flows through the feedback capacitor C_f, as long as $C_p << C_f A_0$, where A_0 is the small signal gain of amplifier. A source follower is used as buffer to drive the output and isolate the sensitive node from large load capacitance. The reset network has three main functions: 1. it resets the output signal of preamplifier after a current pulse is processed; 2. it has to provide the necessary DC feedback for proper operation of amplifier; 3. it has to absorb the DC leakage current of the detector.

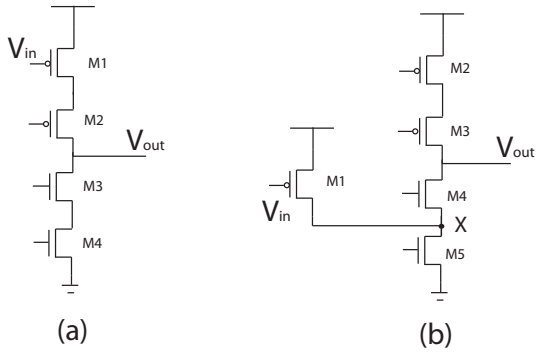

Figure 3.2: Two implementations of amplifier

3.1.1 Amplifier

There are two basic configurations to implement the amplifier, shown in figure 3.2. The first configuration is called as a telescopic amplifier. In figure 3.2(a), all transistors are working in the saturation region. By virtue of its transconductance, the input transistor M1 converts variations in its gate-source voltage to a small-signal drain current [18, 19], which pass through the output resistance seen at the output node to generate an output voltage. The cascode transistors M2, M3 boost the output resistance, thus boost overall gain.

The second configuration is called as a folded-cascode amplifier. As shown in figure 3.2(b), the small-signal current created by the input transistor, M1, is folded up. Cascode transistors are also adopted in this configuration. The advantage of the folded-cascode amplifier is, unlike the telescopic amplifier, the biasing current of output transistors doesn't need to be the same as that of the input transistor. Therefore, the input transistor can be biased under a higher current to achieve a higher transconductance, while the output transistors can be biased under a lower current to achieve a higher output resistance [2]. Because transconductance is proportional to the biasing current, to which output resistance is inversely proportional. The

disadvantage of the folded-cascode amplifier is, a) it obviously consumes more current, b) additional pole is created at node X. More variation of the folded-cascode amplifier can be found in [20].

3.1.2 Reset Network

The simplest way to implement the reset network is to use a very large resistor, R_f. However, it has several major drawbacks. Firstly, the noise contributed from R_f added to the white parallel noise component from last chapter. In order to make such contribution negligible, the following relation has to be held:

$$\frac{4kT}{R_f} << 2qI_{det} \tag{3.1}$$

where I_{det} is the detector leakage current. Assuming the leakage current to be $100pA$, the feedback resistor R_f has to be much larger than $0.5G$ ohms, which is impossible to integrate on-chip due to limited silicon area.

Secondly, large resistance leads to large voltage drop across the resistor. Assuming values of leakage current and resistance from above, the voltage drop across the resistor is about hundred millivolts, which might be too much for small voltage supply technology. Thirdly, the feedback resistor solution adapts poorly to variation of detector leakage current.

An alternative is to use clocked reset switch, implemented by one single transistor. The reset is established by closing the reset switch that connects input and output of CSA. The disadvantage of this option is that 1) there is no dc path for the leakage current, so it will also integrate on the feedback capacitor, which leads to frequent reset to avoid saturation of the amplifier; 2) fast digital clock signal is a major interference for high-sensitive systems.

Adaptive reset can be achieved by using a MOSFET biased in saturation shown

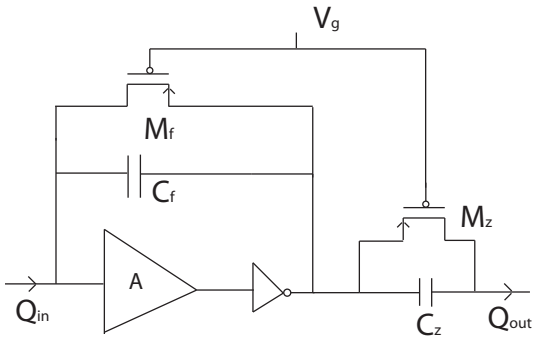

Figure 3.3: Adaptive reset network

in figure 3.3 [16], [17]. Transistor M_f is connected between amplifier's output and input, its gate is connected to a fixed biasing voltage. In this configuration, for small changes in V_{gs}, the transistor absorbs a wide range of values of leakage current, from sub-pA to hundreds of nA. Allowing the transistor to be biased in saturation ensures that the drain current is not effect by changes at the amplifier's input. The transistor should also be selected with a length much larger than width so that it is biased in strong inversion. The reason for that is for the same amount of drain current, transistor in strong inversion has less noise contribution than it is in weak inversion.

One problem for this solution is the discharge is not linear due to the non-linear dependence of drain current on V_{gs}. A compensation network composed with C_z and M_z is included to ensure linearity. C_z and M_z are N times replicas of C_f and M_f, therefore cancels the additional zero produced by the adaptive reset network. A charge gain of N is also provided by the compensation network, $Q_{out} = NQ_{in}$. The noise contribution from M_z is negligible as long as $N >> 1$.

3.2 Noise Analysis

The ENC equations for three main components are provided in previous chapter, and they are relisted here.

$$ENC_{ws}^2 = a_{ws}\frac{\gamma}{g_m}(C_p + C_g)^2\frac{1}{\tau} \tag{3.2}$$

$$ENC_{wp}^2 = a_{wp}I_{det}\tau \tag{3.3}$$

$$ENC_{1/f}^2 = a_f K_F(C_p + C_g)^2 \tag{3.4}$$

where ENC_{ws}, ENC_{wp} and $ENC_{1/f}$ represent the three main noise components, the white series noise, the flicker noise, and the white parallel noise.

The transconductance of transistor biased in strong inversion can be expressed as:

$$g_{m,strong} = \sqrt{2I\mu C_{ox}W/L} \tag{3.5}$$

and that biased in weak inversion can be expressed as:

$$g_{m,weak} = \frac{I}{nU_T} \tag{3.6}$$

where n is the subthreshold slope coefficient, U_T is the thermal voltage, μ is the mobility of holes in a specific process, C_{ox} is the gate oxide capacitance per unit area, I W and L is the biasing current, width and length of input transistor.

The flicker noise of MOS transistor has two different origins [21, 22]. The δN model assumes the drain noise current is a result of fluctuation of charge carriers. The $\delta\mu$ model assumes that the fluctuation of charge carriers mobility generates the noise. Studies have shown that p-MOSFET generally follows the δN model when biased in weak inversion, and the $\delta\mu$ model when biased in strong inversion.

Therefore, the 1/f flicker noise voltage spectral density S_F can be expressed as:

$$S_{F,\delta N} = (\frac{q^2 nkTN_T}{2\beta C_{ox}^2})\frac{1}{WL}\frac{1}{f} \tag{3.7}$$

$$S_{F,\delta\mu} = (\frac{nq\alpha_H}{\sqrt{2\mu C_{ox}^3}})(\frac{1}{\sqrt{W^3 L}})\sqrt{I}\frac{1}{f} \tag{3.8}$$

where k is the Boltzman constant, T is the absolute temperature, α_H is the Hooge constant, N_T is the oxide/interface trap density per unit volume and energy at the quasi Fermi level, β is the tunneling parameter of the traps. It is seen that the $\delta\mu$ model predicts the noise increases with the root square of biasing current I, while the δN model predicts that the noise is independent of I.

As of these reasons, optimization is formulated under two different conditions, strong inversion and weak inversion of input transistor region of operation.

3.2.1 Strong inversion

By inserting value of transconductance of transistor biased in strong inversion in (3.2) and spectral density model of $1/f$ noise in (3.4), we obtain

$$ENC_{ws}^2 = (\frac{a_{ws}}{\tau}\frac{\gamma L}{q^2\sqrt{2\mu/n}})\frac{(C_p + C_g)^2}{\sqrt{C_g}}\frac{1}{\sqrt{I}} \tag{3.9}$$

$$ENC_{1/f}^2 = (a_f\frac{nq\alpha_H L}{\sqrt{2\mu}})\frac{(C_p + C_g)^2}{\sqrt{C_g^3}}\sqrt{I} \tag{3.10}$$

The total ENC can be expressed as:

$$ENC_{tot,strong}^2 = A_1\frac{(C_p + C_g)^2}{\sqrt{C_g}}\frac{1}{\sqrt{I}}\frac{1}{\tau} + A_2\frac{(C_p + C_g)^2}{\sqrt{C_g^3}}\sqrt{I} + A_3\tau \tag{3.11}$$

where A_1, A_2 and A_3 are constants that can be derived from previous equations.

Thus, the total ENC is expressed in terms of three design variables: biasing current I, gate capacitance of input transistor C_g and shaping constant τ.

Optimum I exists as ENC_{ws} decreases with I while $ENC_{1/f}$ increases with I. Optimum τ exists as ENC_{ws} and ENC_{wp} share the same relation. For a fixed current, it is derived that minimum thermal noise would be achieved for $C_g = 1/3C_p$, while the minimum flicker noise is achieved for $C_g = 3C_p$, if thermal and flicker noise would be independently optimized.

Inserting equation 3.5 into (3.2) and spectral density model of $1/f$ noise in (3.4), we obtain

$$ENC_{ws}^2 = (\frac{a_{ws}}{\tau}\frac{\gamma L}{q^2\sqrt{2\mu/n}})\frac{(C_p+C_g)^2}{\sqrt{C_g}}\frac{1}{\sqrt{I}} \tag{3.12}$$

$$ENC_{1/f}^2 = (a_f\frac{nq\alpha_H L}{\sqrt{2\mu}})\frac{(C_p+C_g)^2}{\sqrt{C_g^3}}\sqrt{I} \tag{3.13}$$

The total ENC can be expressed as:

$$ENC_{tot,strong}^2 = A_1\frac{(C_p+C_g)^2}{\sqrt{C_g}}\frac{1}{\sqrt{I}}\frac{1}{\tau} + A_2\frac{(C_p+C_g)^2}{\sqrt{C_g^3}}\sqrt{I} + A_3\tau \tag{3.14}$$

where A_1, A_2 and A_3 are constants that can be derived from previous equations.

Thus, the total ENC is expressed in terms of three design variables: biasing current I, gate capacitance of input transistor C_g and shaping constant τ.

Optimum I exists as ENC_{ws} decreases with I while $ENC_{1/f}$ increases with I. Optimum τ exists as ENC_{ws} and ENC_{wp} share the same relation. For a fixed current, it is derived that minimum thermal noise would be achieved for $C_g = 1/3C_p$, while the minimum flicker noise is achieved for $C_g = 3C_p$, if thermal and flicker noise would be independently optimized.

Unconstraint optimization

Absolute minimum can be derived by calculating partial derivatives with respect to I, C_g and τ of equation 3.14, and equating them to zero. The results are written as:

$$
\begin{aligned}
C_{g,opt} &= C_p \\
I_{opt} &= \sqrt[3]{\frac{{A_1}^2 {A_3}^2 C_p}{16 {A_2}^5}} \\
\tau_{opt} &= \sqrt[3]{\frac{16 A_1 A_2}{{A_3}^2} C_p^2}
\end{aligned}
\tag{3.15}
$$

When the above optimum is feasible, $ENC_{ws} = ENC_{wp} = ENC_{1/f}$ and

$$
min[ENC_{tot,strong}^2] = 3\sqrt[3]{16 A_1 A_2 A_3}\sqrt[3]{C_p^2} \tag{3.16}
$$

The above analysis has to be kept within the assumption that the input transistor is in strong inversion, therefore the following equations has to be held.

$$
I > 5 I_S, \tag{3.17}
$$

with

$$
I_s = 2 n \mu C_{ox} U_T^2 \frac{W}{L}, \tag{3.18}
$$

This leads to upper bound on size of transistor

$$
C_g < \frac{I L^2}{10 n \mu U_T^2}. \tag{3.19}
$$

For our detector with $50pF$ parasitic capacitance and $10pA$ leakage current, unconstraint optimization leads to minimum ENC of $128e^-$ at a biasing current of $22mA$, which is significantly over the power consumption limit of our system.

Constraint optimization

The constraints on the optimization of ENC originate from rate of the events, that presents the upper bound on the choice of τ, total power consumption of CSA, that constraints the biasing current and the chip area, that presents constraint for

choice of C_g. There is also additional constraint that links choice of biasing current and gate capacitance, related to the operation region of the input transistor, which is expressed in (3.19).

As derived in [22], when the biasing current is higher than I_{opt}, the suboptimum capacitive ratio tends toward $C_g/C_p = 3$ as 1/f noise becomes dominant; when the biasing current is lower than I_{opt}, the suboptimum capacitive ratio moves to $C_g/C_p = 1/3$ as thermal noise becomes dominant. If the biasing current is further lowering to a point that even $C_g/C_p = 1/3$ cannot holds the input transistor in strong inversion, the suboptimum point is reached at $C_g/C_p = 1/3$.

If the shaping time constant is limited by the event rate, and must be shorter than τ_{opt}, then the suboptimum biasing current is higher than I_{opt} and suboptimum capacitive ratio is moving toward $C_g/C_p = 1/3$ since shorter shaping time constant results in larger thermal noise component.

3.2.2 Weak Inversion

Transistor biased in weak inversion has the highest g_m/I_d ratio, therefore it is desired to bias the transistor in weak inversion for applications that have tight power budget. ENC for the case of input transistor operating in weak inversion can be obtained by inserting the transconductance in (3.6)into (3.2) and δN model for 1/f noise in (3.4)

$$ENC_{ws}^2 = \frac{a_{ws}\gamma nkT}{Iq}(C_p + C_g)^2\frac{1}{\tau} \tag{3.20}$$

$$ENC_{1/f}^2 = a_f(\frac{q^2 nkTN_T}{2\beta C_{ox}})\frac{(C_p + C_g)^2}{C_g} \tag{3.21}$$

The total ENC can be expressed as:

$$ENC_{tot,weak}^2 = B_1\frac{(C_p + C_g)^2}{I}\frac{1}{\tau} + B_2\frac{(C_p + C_g)^2}{C_g} + B_3\tau \tag{3.22}$$

where B_1, B_2 and B_3 are constants that can be derived from previous equations.

Optimum τ still exists. For a given C_g, $ENC_{tot,weak}$ decreases continuously as the biasing current I is increased. If other parameters are fixed, the minimum thermal noise is achieved at lowest C_g while $C_g = C_p$ is minimum for flicker noise.

Unconstraint optimization

In order to keep the input transistor biased in weak inversion, the following relationships have to be held:

$$I < 0.01 I_S, \tag{3.23}$$

and leading to

$$I < \frac{C_g n \mu U_T^2}{50 L^2} \tag{3.24}$$

Therefore, optimum I is chosen as the largest current that keeps the input transistor in weak inversion.

$$I_{opt} = \frac{C_g n \mu U_T^2}{50 L^2} \tag{3.25}$$

Optimum C_g and τ can be calculated as the solutions for the following equations:

$$\begin{aligned} \frac{\partial ENC_{tot,weak}}{\partial C_g} &= 0 \\ \frac{\partial ENC_{tot,weak}}{\partial \tau} &= 0 \end{aligned} \tag{3.26}$$

which gives the unconstraint optimum point at weak inversion as:

$$\begin{aligned} C_{g,opt} &= C_p \\ I_{opt} &= \chi C_p \\ \tau_{opt} &= 2\sqrt{\frac{B_1}{B_3 \chi} C_p} \end{aligned} \tag{3.27}$$

where $\chi = \frac{n \mu U_T^2}{50 L^2}$.

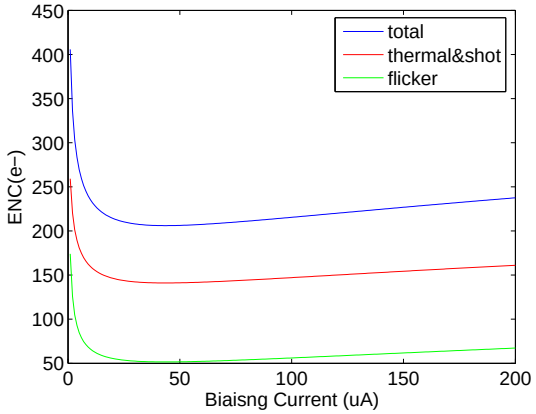

Figure 3.4: Optimized ENC with different biasing currents at weak inversion

When the above optimum point is feasible to implement, the absolute minimum ENC in weak inversion is

$$min[ENC^2_{tot,weak}] = 4\sqrt{\frac{B_1 B_3}{\chi} C_p} + 4B_2 C_p \tag{3.28}$$

With our specific sensor, unconstraint optimization leads to minimum ENC of $206e^-$ at a biasing current of $44\mu A$. Therefore, the ENC is increased less than two times while the power consumption can be reduced by about 500 times.

Constraint optimization

The conditions where the three design variables are limited are considered respectively. If biasing current I is fixed. Optimum τ is calculated as $\tau_{subopt1} = \sqrt{\frac{B_1}{B_3 I}}(C_p + C_g)$. After insert the optimum time constant into (3.22), it is observed that for thermal noise, the optimum C_g is chosen as the smallest value to keep the transistor in weak inversion; for flicker noise, the optimum C_g is at C_p. Figure 3.4 shows a simulation with different biasing currents. ENC worsens about 10% for biasing current drops to 30% of its optimum value.

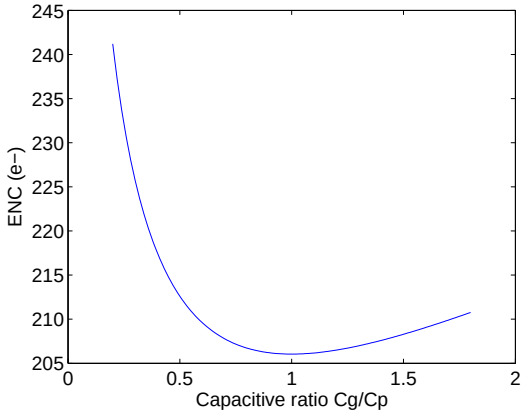

Figure 3.5: Optimized ENC with different capacitive ratio at weak inversion

If C_g is limited due to area constraint, optimum biasing current has to be chosen as the largest value to keep the transistor in weak inversion, or $I_{subopt2} = \chi C_g$. Optimum τ can still be calculated as

$$\tau_{subopt2} = \sqrt{\frac{B_1}{B_3\chi}}\frac{C_p + C_g}{\sqrt{C_g}} \tag{3.29}$$

which gives suboptimum ENC to be

$$ENC_{subopt2} = 2\sqrt{\frac{B_1 B_3}{\chi}}\frac{C_p + C_g}{\sqrt{C_g}} + B_2\frac{(C_p + C_g)^2}{C_g} \tag{3.30}$$

Figure 3.5 shows a simulation with different capacitive ratio between C_g and C_p. ENC worsens about 10% for input transistor size drops to 30% of its optimum value.

If the shaping time constant is fixed due to event rate, the same optimization process results in $I_{subopt3} = \chi C_p$, $C_{g,subopt3} = C_p$. The suboptimum ENC is calculated as

$$ENC_{subopt3} = \frac{4B_1 C_p}{\chi}\frac{1}{\tau} + 4B_2 C_p + B_3\tau \tag{3.31}$$

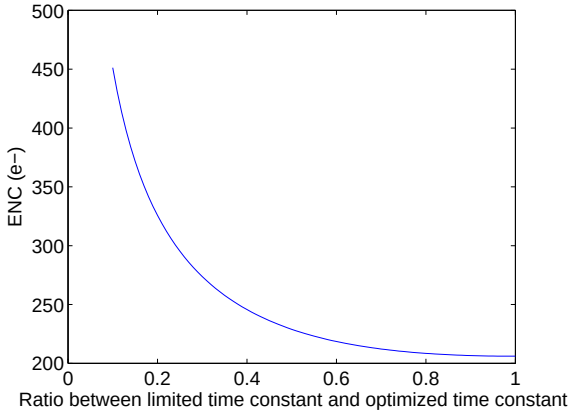

Figure 3.6: Optimized ENC with different time constant

Figure 3.6 shows a simulation with different limited time constant. ENC worsens about 10% for time constant drops to 50% of its optimum value.

3.2.3 Comparison and discussion

When absolute minimum noise is desired, the transistor would be biased in strong inversion. However, in circumstances where the biasing current of input transistor is fixed in a low range due to limited power budget, the optimization process is modified and choice of region of operation of the transistor depends on the required power consumption. The optimum point also varies with different sensor specs and noise requirements.

For our specific design, we have relatively flexible choices over time constant and input transistor size, while power consumption is our main concern. Figure 3.7 shows a simulation with biasing current below $1mA$, which is a reasonable current range most readout system adopt. The X-axis is biasing current, and Y-axis is the minimum achievable ENC for the fixed biasing current if the transistor operates in strong inversion or weak inversion, assuming optimum point of C_g and τ are

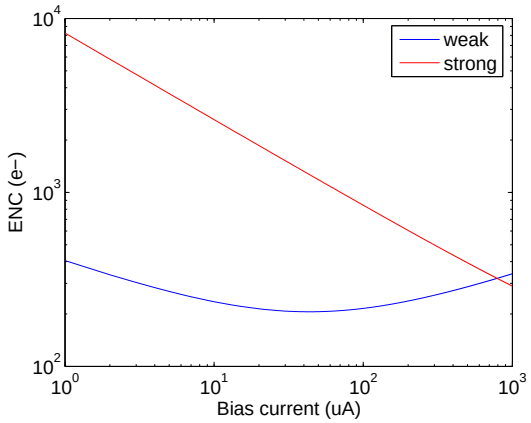

Figure 3.7: Optimized ENC as a function of biasing current under strong and weak inversion.

feasible.

In strong inversion, ENC monotonically decreases as current increases. Since the input transistor cannot be large enough to be equal to C_p, due to the relative small biasing current, the minimum ENC is always achieved when C_g is the largest value that keeps the input transistor in strong inversion. In weak inversion, a minimum ENC exists at point where $C_g = C_p$, and biasing current equals to the largest value that can keep input transistor in weak inversion.

As can be seen from the figure, when biasing current around hundreds of μA, weak inversion is advantageous over strong inversion; when biasing current moves to above $1mA$, strong inversion becomes more preferred. However, the above conclusion ignores the moderate inversion, the biasing region between weak inversion and strong inversion. In the region between $100\mu A$ and $1mA$, moderate inversion is better than weak inversion. Because in moderate inversion, the transistor can biased at capacitive matching point, $C_g = C_p$; while in weak inversion, the transistor has to be moved away from the capacitive matching point to keep weak inversion biasing.

The problem for moderate inversion is that there are no accurate flicker noise model in moderate inversion, measurement data of single transistor is required to construct models in moderate inversion. In lack of actual measurement result of our targeted process, we constructed moderate inversion flicker noise model with the help of weak inversion and strong inversion models, assuming that in moderate inversion the two origins of flicker have a combined role, which depends on the inversion coefficient. The inversion coefficient can be calculated as I/I_s, where I_s is described in equation 3.18. In our design, we choose biasing current of $100\mu A$ and $C_g = C_p$. The input transistor is biased in the moderate inversion.

3.3 Design and Simulation

Figure 3.8 shows the design of implemented CSA. A separate supply is used for the sensitive input transistor for better noise performance. Several design issues are described in this section.

3.3.1 Noise contributions from other transistors

The additional noise contributions from M_2, M_3 and M_5 can be approximated as:

$$V_{n,add}^2 = (V_{n2}^2 g_{m2}^2 + V_{n5}^2 g_{m5}^2)/g_{m1}^2 + V_{n3}^2 (\frac{C_{gd1}}{C_{gd1} + C_{gs1} + C_p})^2 \tag{3.32}$$

where V_{n2}, V_{n5} and V_{n3} are input referred noise at the gate of M_2, M_5 and M_3 respectively.

The input referred voltage noise from M_2 and M_5 is scaled by the transconductance of M_1. Because M_2 and M_1 have similar biasing current, and NMOS normally has at least order of magnitude higher flicker noise coefficient than PMOS,

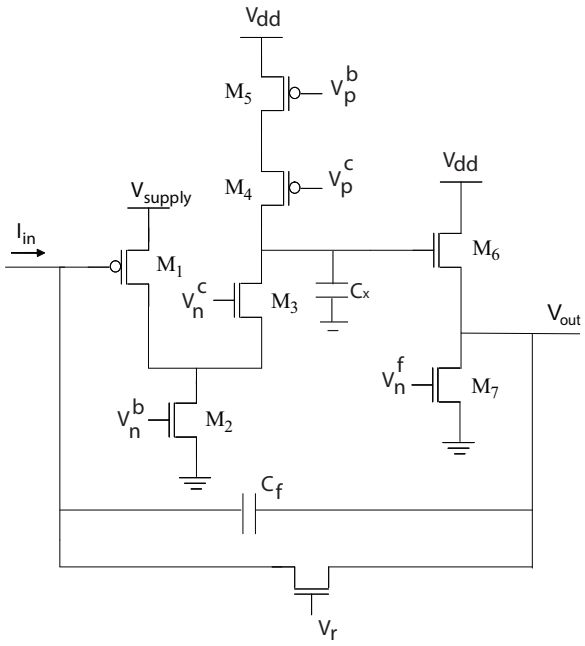

Figure 3.8: Schematic of implemented CSA

the noise contribution from M_2 can not be neglected. To reduce the thermal noise from M_2, g_{m2} has to be small, which leads to more voltage headroom for fixed biasing current. To reduce the flicker noise from M_2, the transistor has to be made big, which leads to stability problem that will be discussed in the next section. Therefore, it is also advantageous to bias M_1 in weak inversion and M_2 in strong inversion, so that the noise contribution from M_2 can be efficiently scaled down.

The noise from M_3 is coupled through C_{gd1} to the input of CSA. Since M_1 is normally very large, this component is not negligible. Considering the additional noise sources from (3.32), the optimization process has been modified, and the optimum point is slightly different.

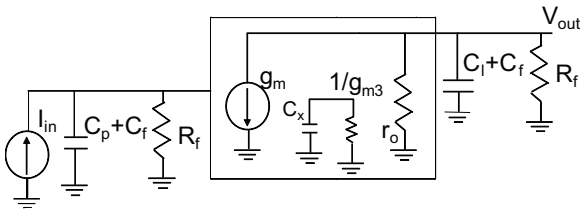

Figure 3.9: Open circuit schematic after breaking the loop

3.3.2 Stability analysis

The large input transistor makes the non-dominant pole of CSA amplifier closer to its dominant pole, thus the stability of CSA requires careful examination.

Assuming that the source follower is an ideal buffer and the reset MOS transistor has a very large equivalent resistance R_f, the small signal model of open loop circuit is shown in Figure 3.9. g_{m3} is the transconductance of M_3, r_o is the equivalent output resistance of CSA amplifier, $C_x = C_{gd1} + C_{db1} + C_{gd2} + C_{db2} + C_{gs3} + C_{sb3}$ is the total capacitance at the folding node and C_l is the capacitance at the CSA output. The feedback network is C_f in parallel with R_f. Thus, the loop gain can be derived as:

$$A(s)\beta = \frac{V_{out}(s)}{I_{in}(s)}\beta = \frac{g_m(r_o||R_f)(\frac{s}{Z_1}+1)}{(\frac{s}{P_1}+1)(\frac{s}{P_2}+1)(\frac{s}{P_3}+1)} \tag{3.33}$$

where zero is at $z_1 = 1/(R_f C_f)$ and poles are at $p_1 = 1/[R_f(C_f + C_p)]$, $p_2 = 1/[(r_o||R_f)(C_f + C_l)]$ and $p_3 = g_{m3}/C_x$. p_1 is attributed to the capacitive load at the input node, p_2 and p_3 are the two poles associated from CSA amplifier. The feed-forward zero comes from the RC network in feedback.

The pole and zero locations are shown in Figure 3.10. The unity frequency gain f_u can be approximated as:

$$f_u = \frac{g_m C_f}{(C_f + C_l)(C_p + C_f)} \tag{3.34}$$

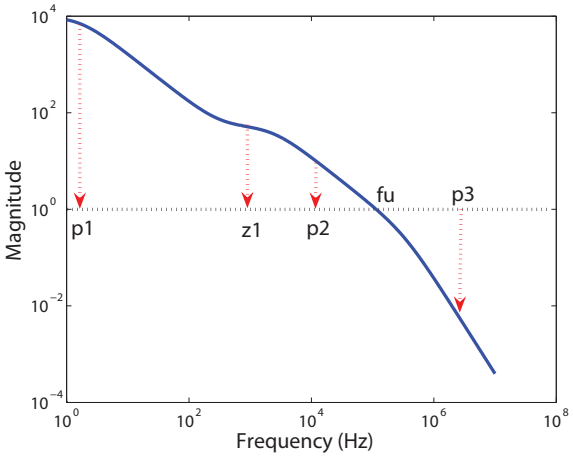

Figure 3.10: Pole zero location of CSA

The first pole and zero occurs at relatively low frequency, their phase contribution can be approximately canceled. Therefore, the first non-dominant pole appears after f_u is critical and ultimately determines the phase margin of the loop. It is reasonable to assume that the CSA amplifier's non-dominant pole is fixed, thus it is desired to place f_u far away from p_3.

Smaller C_f makes CSA more stable, however large amplifier gain is required due to high C_p/C_f ratio. Thus, adding compensation capacitive load C_l is the only feasible option. For these reasons, for our design the chosen values for C_l and C_f are $2pF$ and $500fF$ respectively, and achieved phase margin is over 70^o.

Figure 3.11 shows a simulation of the designed CSA with different compensation capacitors C_l. The effectiveness of previous stability model is proven. Though the added compensation capacitor slows down the circuit's step response to over $3us$, a large time constant of following shaper makes the overall readout system unaffected.

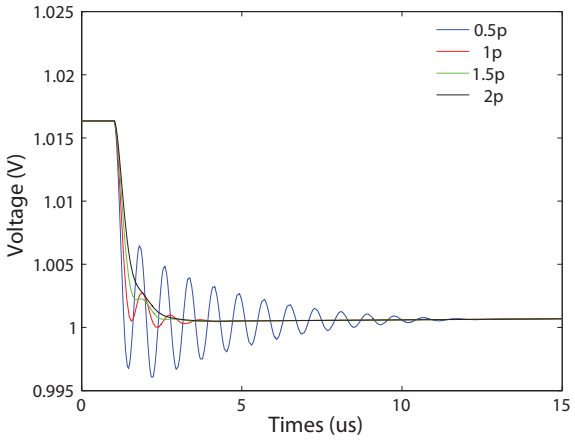

Figure 3.11: Simulation of CSA with different compensation capacitors

3.3.3 Cascade CSA stages

In order to increase the overall gain provided from pre-amplification stage, thus reduces the noise contribution from the subsequent shaper, a second CSA stage is added as shown in figure 3.12. Pole-zero compensation networks are formed by a parallel connection of N-replica of C_{f1}, M_{f1} and C_{f2}, M_{f2}. A second CSA stage increase the overall gain by another factor N_2. The compensation network forces the second amplifier has the same DC point as the first amplifier. Since the input capacitance of second amplifier is not as large as first amplifier, the second amplifier was designed as a scaled-down version of the first amplifier. Also, the additional compensation capacitor is not required for the second amplifier. In our design, we have used $N_1 = N_2 = 10$, $C_{f1} = C_{f2} = 500fF$.

3.3.4 Simulation

The circuit is designed under AMI $0.5\mu m$ CMOS process. Selection of transistor sizes and capacitor values are listed in table 3.1. The amplifier used in the

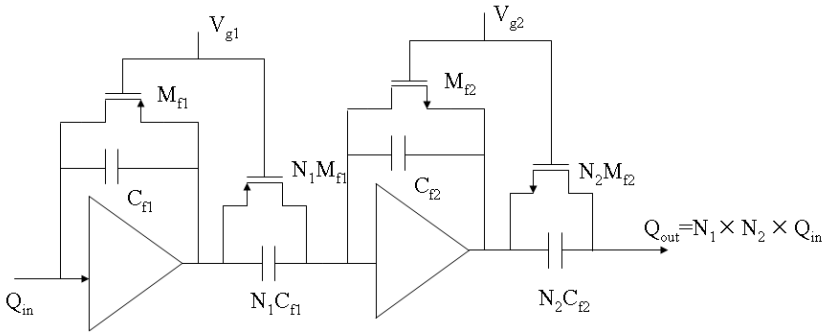

Figure 3.12: Cascading two CSAs as input stage

Table 3.1: Transistor sizes and capacitor values of designed CSA

M_1	$54k\lambda/4\lambda$
M_2	$700\lambda/16\lambda$
M_3	$400\lambda/16\lambda$
M_4	$600\lambda/16\lambda$
M_5	$600\lambda/16\lambda$
M_{f1}	$6\lambda/200\lambda$
C_{f1}	$500fF$
C_x	$2pF$

seconde CSA stage is a five-times scaled down version of the one used in the first CSA.

The circuit was simulated using Cadence SpectreS simulator and BSIM3 version 3.1 transistor models. Figure 3.13 shows a simulation result of $10K$ input electrons.

3.4 Current-mode preamplifier

A current mode preamplifier suitable for the readout system is also worth mentioning. With the current amplifier, the current is buffered and can be integrated on the smaller capacitor at the output of the amplifier. This approach provides a solu-

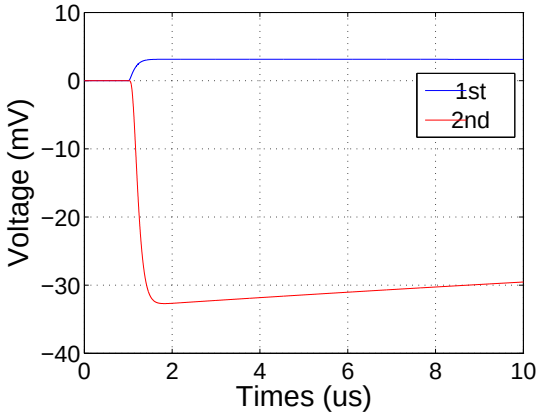

Figure 3.13: Simulation of cascade CSAs with 10K input electrons

tion without using feedback, thus allows faster response time to radiation event, but the theoretical noise sensitivity is higher in this case. The current-mode preamplifier is not the main focus of this dissertation, thus its design and implementation are briefly discussed in this section.

The basic concept is to use a current buffer to isolate the large input parasitic capacitance associated with detector, and direct the generated charge into a small capacitor [24, 25, 26, 27]. The current mode preamplifier avoids charging and discharging of the parasitic capacitors to high-voltage levels and keeps the internal nodes at low-impedance values [28]. The current buffer should have low input impedance, high bandwidth and low noise [29]-[35]. A simple structure of current buffer is the common gate current buffer (CG) [36, 37], shown in figure 3.14(a). The input impedance is derived to be $1/gm_1$. As long as the impedance seen into the input of current buffer is greatly smaller than the parasitic capacitance within signal bandwidth, the current pulse created by the detector will flow into the current buffer. However, since the parasitic capacitance is fairly large in our design, the transconductance of input transistor must be large to have enough bandwidth. It

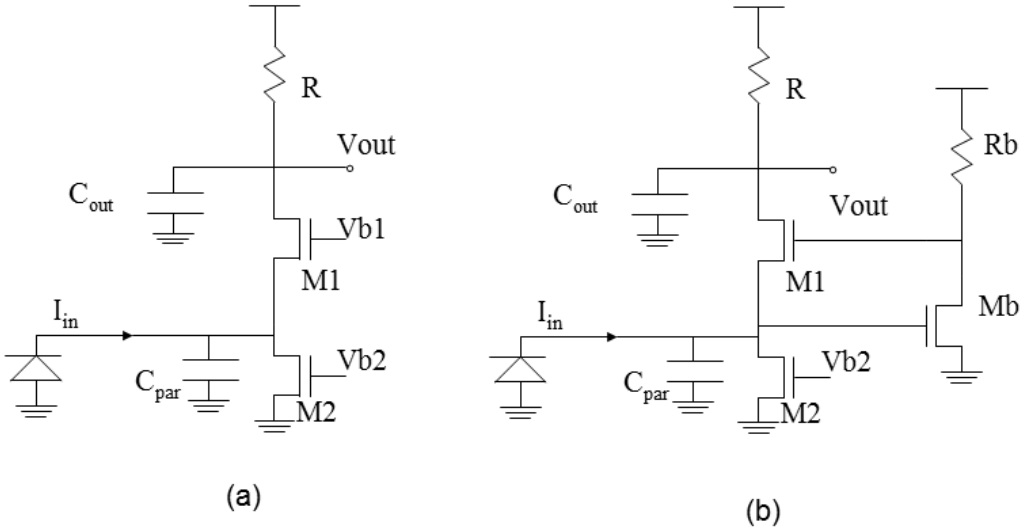

Figure 3.14: Current-mode preamplifier implementations

leads to large power consumption, because the transconductance is proportional to biasing current.

An alternative option for current buffer is the regulated cascode structure (RGC) [38]. Figure 3.14(b) shows schematic of RGC. The input impedance is boosted to $1/gm_1(1+Rbgm_b)$. It greatly relaxes the input transistor and thus reduces power consumption. While decreasing the input impedance, the local feedback stage inherently produces a zero, which causes a peaking in the frequency response. In order to avoid this peaking from the bandwidth, tradeoff in the resistance R_b or the gate width W_1 of $M1$ has to be considered. The choice of R_b is related to the voltage gain of the feedback loop and it is setting the biasing current of Mb. Reducing W_1 may lead to the increase of the channel thermal noise contribution from $M1$ due to smaller gm_1.

3.4.1 Small Signal Analysis

Similar to the analysis shown above, the input transistor can be modeled as a transconductor. A small signal analysis shows its input impedance is calculated as:

$$Z_{in,CG} = \frac{1}{g_{m1}} \tag{3.35}$$

And RGC's input impedance is calculated as:

$$Z_{in,RGC} = \frac{1}{g_{m1}(g_{mb}R_b + 1)} \tag{3.36}$$

For simplicity, the circuit can be modeled as a two poles system, with one pole at the input node, the other at the output. Transfer functions can be described as follows:

$$H_{CG}(s) = \frac{Vout(s)}{Iin(s)} = \frac{R}{(\frac{C_{in}}{g_{m1}}s + 1)(RC_{out}s + 1)} \tag{3.37}$$

$$H_{RGC}(s) = \frac{Vout(s)}{Iin(s)} = \frac{R}{(\frac{C_{in}}{g_{m1}(g_{mb}Rb+1)}s + 1)(RC_{out}s + 1)} \tag{3.38}$$

where gm is the input transconductance of M1. Assuming the input pole is much greater than the output pole, and R is very large, signal outputs in response to a single electron in both configurations can be expressed approximately as:

$$V_{s,out} = \frac{q}{C_{out}} \tag{3.39}$$

where q is the charge of a single electron. If C_{out} is equal to C_f, it is a same result as voltage mode preamplifier.

3.4.2 Noise Analysis

The noise models of both CG and RGC structures are shown in figure 3.15. The input-referred noise current per unit bandwidth for CG structure is:

$$\begin{aligned} I_n^2 &= \frac{8}{3}kT\frac{1}{g_{m1}}(C_{in}s)^2 \\ &\quad + \frac{8}{3}kTg_{m2} + 4kT\frac{1}{R} \end{aligned} \tag{3.40}$$

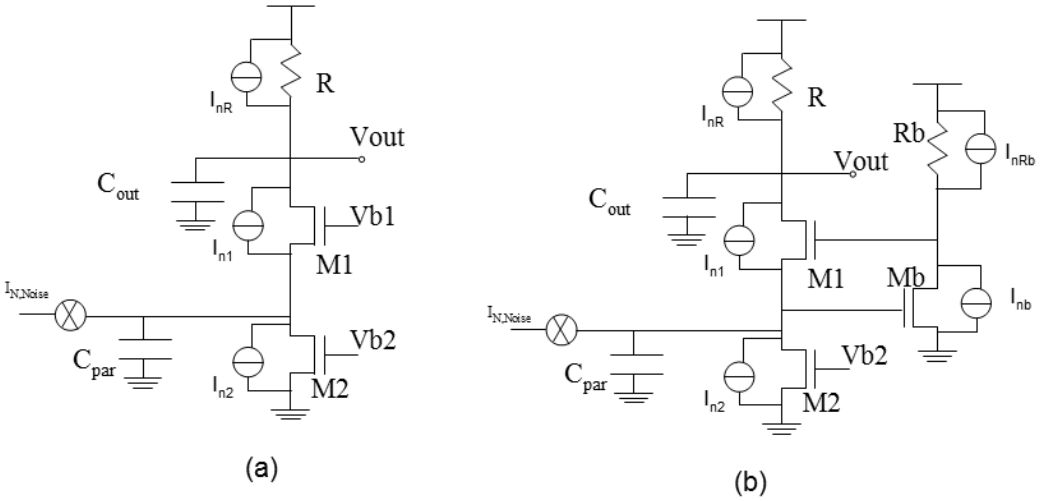

Figure 3.15: Noise models of CG and RGC

The input-referred noise current per unit bandwidth for RGC structure is:

$$\begin{aligned} I_n^2 &= \frac{C_{in}s^2(\frac{8}{3}kTg_{mb} + 4kT\frac{1}{R_b})}{g_{mb} + 1/R_b} \\ &+ \frac{8}{3}kT\frac{1}{g_{m1}}(C_{gs1} + C_{gdb})s^2 \\ &+ \frac{8}{3}kTg_{m2} + 4kT\frac{1}{R} \end{aligned} \tag{3.41}$$

The CG noise equation reveals two problems of the structure. First, it requires a relatively large gm_1. This is a direct impact of the large input capacitance, since a smaller gm1 limits the bandwidth of the current buffer, and fewer charges is integrated on the output capacitance. A large gm_1 can be achieved with either wider transistor or larger biasing current. The former increases the gate capacitance of $M1$, which in turn, adds up to the input capacitance. The latter obviously leads to higher power consumption. Second, it shows little flexibility in the design of CG preamplifier. The only parameter under control is gm_2. However, for a fixed bias current, gm_2 is reduced only at the cost of voltage headroom.

Compared to CG structure, the RGC structure greatly relaxes the requirement of gm_1, and thus reduces power consumption. The contribution from $M2$ can be reduced as, in RGC, it has a smaller biasing current which leads to smaller gm_2. It is observed that noise contributed from $M1$ is now related with a much smaller capacitance $C_{gs1} + C_{gdb}$, and high frequency noise associated with the large input capacitance is now related with Mb.

However, the current buffer preamplifier generally displays disadvantage in noise performance over CSA. The noise contributions from $M2$ and R are related with the input node directly. While in the voltage preamplifier, the noise contributed by current sources is scaled by the input transistor.

3.4.3 Design and Simulation

Since the large input parasitic capacitance, a current buffer based on regulated cascode structure is designed under AMI 0.6μm CMOS process. Several design issues are described following.

A larger R and a smaller C_{out} is in favored in the preamplifier design. However, large R leads to large voltage headroom, which is directly related with power consumption. An additional current mirror is added in figure 3.16 to divert part of the biasing current. Also a feedback loop is applied to control the additional current mirror. The feedback loop also makes the preamplifier adaptable to different leakage current. The amplifier in the loop has a very low bandwidth so that it won't effect the output signal.

However, two problems remain. The parasitic capacitance of $M4$ increases C_{out} significantly. Because $M4$ suffers from low mobility and must be quite wide to carry a large current. This issue is combated with another cascode transistor $M3$. With a smaller biasing current, $M3$ can be sized small. Noise analysis shows its

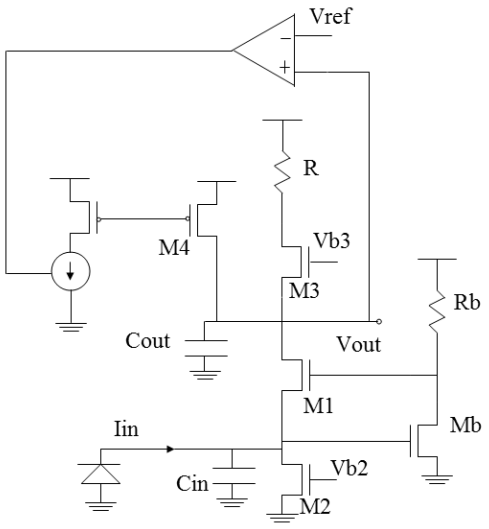

Figure 3.16: Schematic with added current mirror

noise contribution is negligible.

Another problem is that the added current mirror produces more noise. A comparison between smaller R without additional current mirror and larger R with additional current mirror is provided in [39]. It is derived that the added current mirror has about $\alpha(2\gamma - 1)$ times more noise, where $I_{d4} = \alpha I_{d1}$ and γ is the thermal noise factor. Fortunately, the noise contribution from R in equation (8) is much smaller than the other terms. Therefore, the added noise can be ignored.

The biasing current in this design is chosen as $1mA$ for the main branch, and $0.5mA$ for the RGC branch. The transistor sizes and their noise contributions are listed in table 3.2.

The circuit was simulated using Cadence SpectreS simulator and BSIM3 version 3.1 transistor models. Figure 3.17 shows the simulated transient response. The gain of the preamplifier is about 250 mV/fC.

Table 3.2: Transistor sizes of current buffer and their noise contribution

Transistors	W/L ratio	Noise contribution
M1	68	0.003%
Mb	136	82%
M2	40	18%
M3	5.6	0.04%
M4	60	0.06%

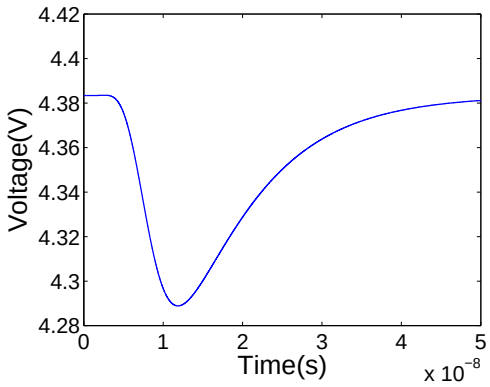

Figure 3.17: Current buffer simulated transient response

3.4.4 Measurement Result

The designed chip was fabricated through 0.5μm CMOS process with 2 poly and 3 metal layers. The chip works with a single 5-V supply and has an overall power consumption of $7mW$.

The fabricated chip is tested with a custom designed general purpose mixed-signal test station equipped with PC interface and FPGA development board. Test station is interfaced to PC through data acquisition card NI-6259 for characterization and to FPGA development board, built around a Xilinx Spartan 3E FPGA, for real-time measurements. Test station is comprised of motherboard, that contains interface circuitry to PC and FPGA, digital-to-analog converters for providing biasing voltages and power regulators, and daughter card, that contains ASIC and enables flexible connections to motherboard through wire-up. Figure 3.18 shows a picture of test station.

The input current pulse was generated by applying voltage step with rise time of 5 ns through function generator to input of the chip. That input was connected to virtual ground of input amplifier through capacitor Ctest, implemented on chip, with value of 1 pF. Capacitance Cdet is inserted at the input node of amplifier and has value of 50 pF, same as parasitic capacitance of photo-detector.

Although the test station has problems with high parasitic and environment interference, it provides a convenient and fast way to do preliminary test for ASICs. For more precise testing, a specific designed printed custom board (PCB) needs to be designed.

Figure 3.19 shows a picture of the output signal where the input current pulse corresponds to charge of 100,000 electrons. The input pulse was simulated as a voltage step with 5ns rise time passing through a 1pF capacitor connected serially to the input.

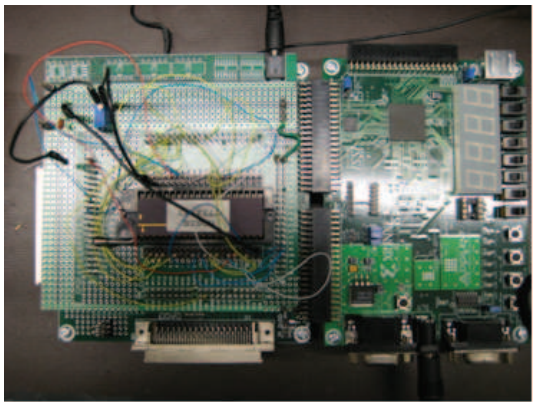

Figure 3.18: Custom designed test station

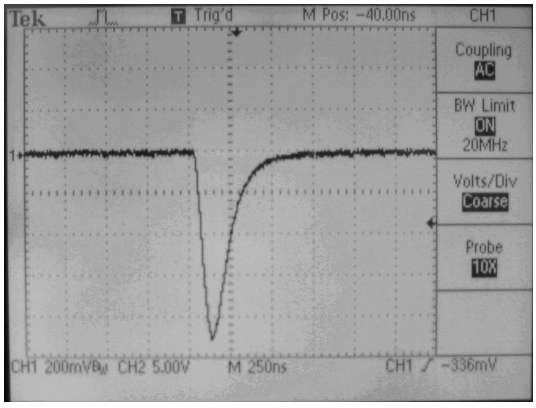

Figure 3.19: Measurement of current buffer

3.5 Conclusion

A design of low-noise charge sensitive amplifier (CSA) for measurement of optical response of photo-detector registering light produced by semiconductor scintillator is presented. Detailed analysis of the CSA suitable for large parasitic detector capacitance is provided, regarding noise, power and stability. Two scenarios where input transistor is biased in strong inversion and weak inversion are compared, with included accurate 1/f noise modeling. Current-mode preamplifier is also investigated and implemented with CMOS process. Measurement result of designed current-mode preamplifier is presented.

Chapter 4

Analog Signal Processing

As stated in part I, analog signal processing is essential in building smart sensing system. In this chapter, design theories and issues regarding the pulse shaping filter and the peak detector are presented.

4.1 Semi-Gaussian Pulse Shaping Filter

The output signal from preamplifier is further processed by a pulse shaping filter to maximize signal to noise ratio. Many literatures [42]-[47] have already proven that a semi-Gaussian shaper is the optimum choice of pulse shaper for radiation detection application. Before we take further analysis, it is worth to see how the pulse shaper filters noise. Figure 4.1 displays Matlab simulation results with a first order semi-Gaussian pulse shaper and other conventional design parameters. As seen from the figures, the semi-Gaussian pulse shaper has a cusp shape transfer function. It filters both the low frequency noise and the high frequency noise. However, for different noise components, the pulse shaper has different aspects. The thermal noise passes the pulse shaper directly and is filtered both at high frequency and low

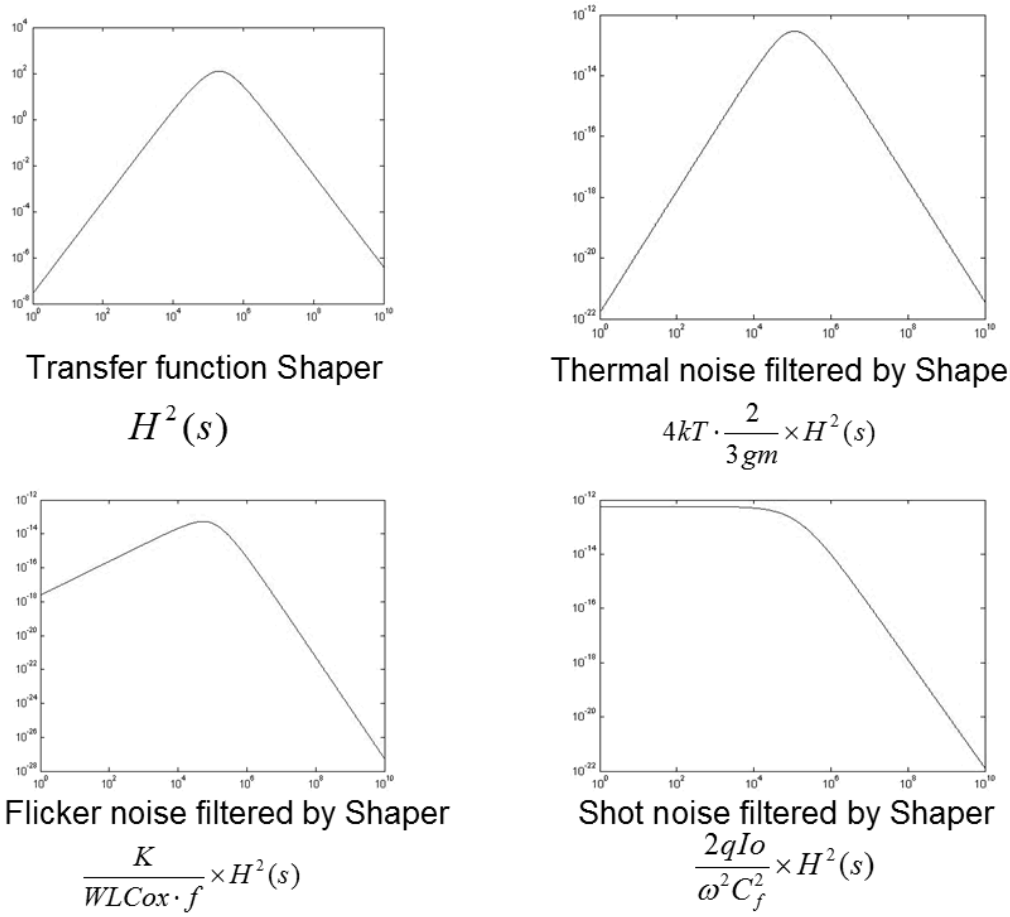

Figure 4.1: Pulse shaper for different noise components

frequency. The 1/f noise is filtered in a similar way, except at low frequency 1/f noise is higher than thermal noise. The shot noise is filtered only at high frequency because it passes the feedback capacitor before it reaches pulse shaper.

It is clear that the pulse shaper has an optimized design to balance the filtering among the three components. In chapter 3, the equation to calculate optimum τ, the time constant, is provided. However, since our specific detector has a fairly low leakage current (about $10pA$) the optimum shaping time is as large as $100us$. Luckily the application we target has a low event rate, we have the luxury to imple-

ment long shaping time to further reduce the noise. However, due to constraints in technology and layout, the resistor and capacitor values required to implement such long shaping time are far from practical in integrated circuit design. A structure called R-lens filter [48], [50] has been selected to implement the shaper.

A significant design challenge for the ASIC is to minimize the noise, so as to get the minimum possible signal detected. However, the design parameters for minimum noise are greatly effected by the variability in the parameters of the detector, such as the parasitic capacitance and the leakage current. This section also provides an adaptive solution that can be incorporated in the system to compensate for the variations of the detector and readout circuitry.

4.1.1 Optimum number of shaper order

The order of shaping filter depends on the number of integrator it includes. Higher order of shaper leads to lower noise, but at a price of more power consumption and area. The order of shaper in our design is determined through a simulation shown in figure 4.2, where ENC is plotted with order of shaper. It is seen that the most noise reduction happens between 1st order and 2nd order. Thus, we designed a 2nd order shaper to compromise between noise, power and area.

4.1.2 Design of Shaper with large time constant

The schematic of a single RC cell used in the shaping filter along with the schematic of the ICON cell are shown in figure 4.3 and figure 4.4. The ICON cell is essentially a current mirror with ratio of M [49], [51]. The current mirror makes the equivalent resistor M times higher than the integrated physical resistance. The ICON cell has the ability to accept current of either polarity. The quiescent of the ICON cell, which is set by $V_{nref} - V_{pref}$, can be very low, thus reducing noise

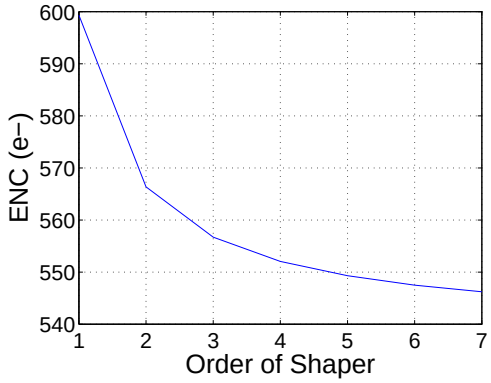

Figure 4.2: ENC versus order of shaper

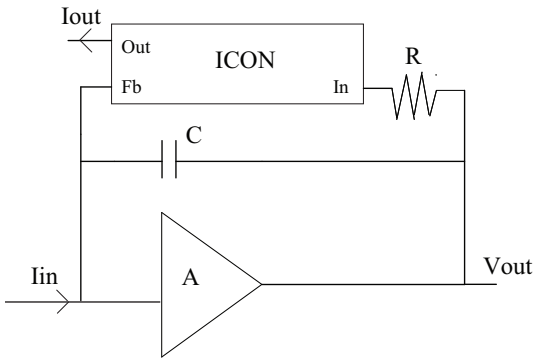

Figure 4.3: Schematic of single RC cell

contribution from the shaper. Assuming the ICON cell has a ratio of M, the transfer function of a single RC cell shown in figure 4.3 is:

$$\frac{I_{out}(s)}{I_{in}(s)} = \frac{1}{MRCs + 1} \tag{4.1}$$

Therefore, multiple ICON cell can be cascaded to form different order of shaping filter. The amplifier in the single RC cell again needs to be a scaled down version of the amplifier in CSA so that the same DC level can be kept.

The final design of the 2nd order shaping filter is shown in figure 4.5. The ratio

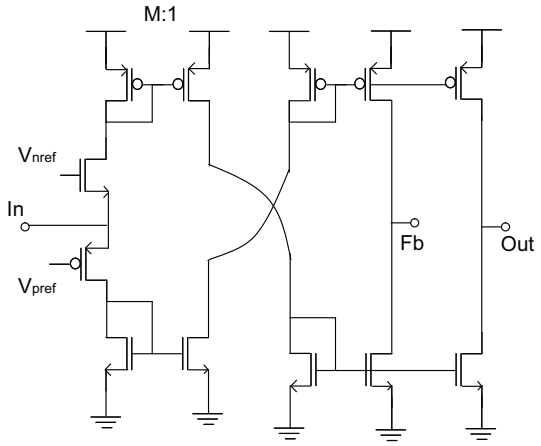

Figure 4.4: Schematic of ICON cell

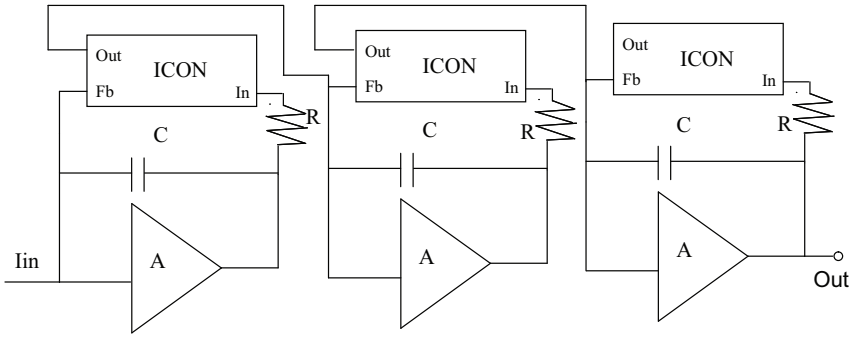

Figure 4.5: Schematic of 2nd order shaping filter

M in ICON cell is selected to be 100. A current gain of 12 is added in the last RC cell to fully utilize the output swing.

4.1.3 Simulation

The circuit is designed under AMI $0.5\mu m$ CMOS process. R and C in the ICON cell are selected as $80k$ ohms and $5pF$. With the help of ICON cell, a peaking time of $80\mu s$ is achieved. The biasing current of ICON cell is only $20nA$. The amplifier used in the pulse shaper is again a five-times scaled down version of the one used

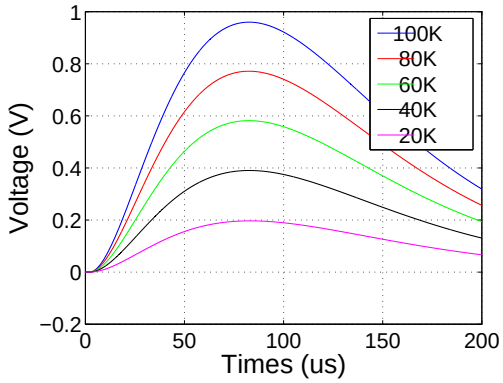

Figure 4.6: Simulation of pulse shaping filter

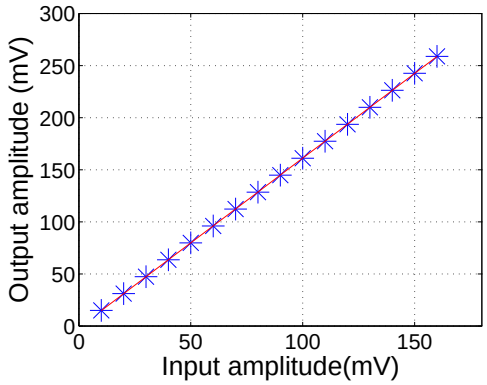

Figure 4.7: Linearity plot of designed pulse shaper

in the first CSA.

A simulation result of the output of shaper is shown in figure 4.6. The input signal is swept from 20K electrons to 100K electrons.

Figure 4.7 shows a linearity plot of designed pulse shaper. X-axis is the input amplitude, and Y-axis the output peak amplitude. Excellent linearity is achieved.

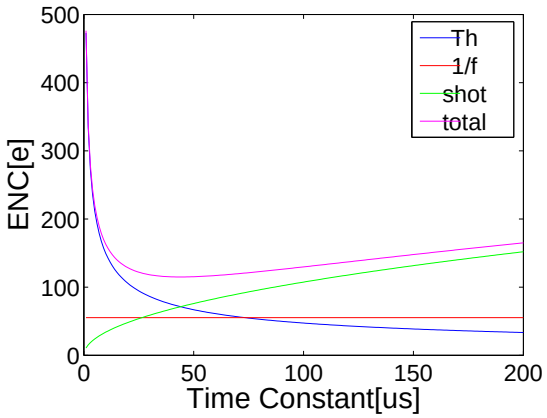

Figure 4.8: ENC versus time constant

4.2 Adaptive shaping filter

Previous analysis shows that an optimum time constant is available for any set of detector parasitic capacitance and leakage current. Figure 4.8 shows the calculated total ENC as well as three different components based on $50p$ input capacitance and $10p$ leakage current. Figure 4.9 shows the total ENC under different detector specifications. In this section, a potential improvement of the designed pulse shaper is proposed and briefly discussed.

Optimum filtering varies according to parameters of detector. To adaptively filter the output signal of CSA, a system shown in figure 4.10 is proposed. The system of single readout channel consists almost the same things except the adaptive control block. The adaptive control block produces threshold level for discrimination of radiation event, it also adaptively adjusts the time constant for the shaper, optimized for minimum output noise and increased sensitivity of the system [52].

In order to adaptively adjust the time constant, a Gm-C filter is proposed to implement the pulse shaper, as shown in figure 4.11. It is a first order differentiator cascaded with a first order integrator. The transfer function can be expressed as

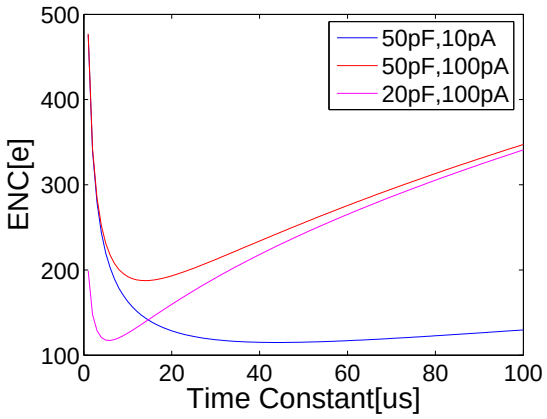

Figure 4.9: ENC versus different specs

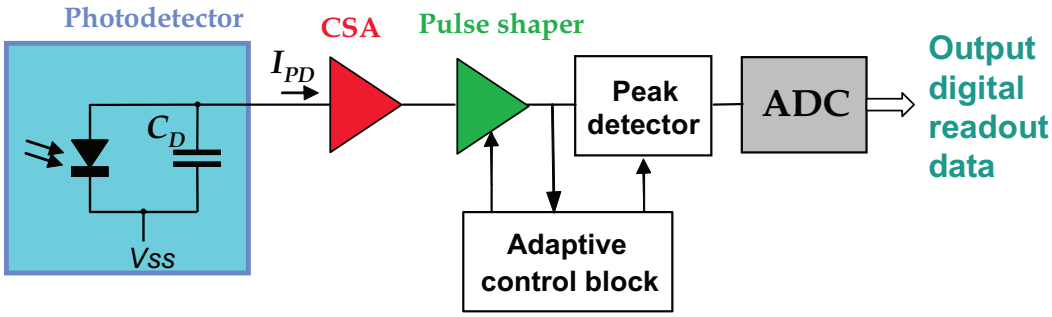

Figure 4.10: Block diagram of proposed system for adaptive filtering

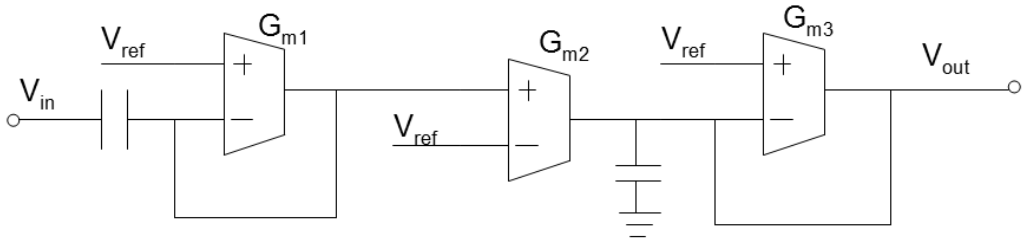

Figure 4.11: Continuous-time Gm-C filter implementation of shaper

$$H(s) = \frac{G_{m2}}{G_{m3}}[\frac{sC_1/G_{m1}}{1 + sC_1/G_{m1}}][\frac{1}{1 + sC_2/G_{m3}}] \tag{4.2}$$

G_{m1} and G_{m3} are nominally set equal. G_{m1}/C sets the time constant. The ratio of G_{m2} and G_{m3} can be used to set the gain. By changing the biasing current, the transconductance changes, therefore changes the time constant of pulse shaper. The simulated frequency response of the designed filter for pulse shaping is shown in figure 4.12. It shows hot time constant of shaper can be changed by change in the biasing voltage. The biasing voltage of OTA is varied from 3.8V to 4.2V in steps of 200mV. The time constant of the filter is changed from $1\mu s$ to $50\mu s$.

The adaptive control block is used for optimization of noise performance of system through control of biasing current of Gm cell in shaper and optimally setting the threshold value for comparison with peak detector signal for detection of radiation event and triggering of analog-to-digital conversion. Block diagram is shown in figure 4.13.

The variations in the leakage current of the photodiode can be significant, as well as the parameters of the input transistor. These variations affect the optimal performance of the pulse shaper, as shown in Figure 4.9. As derived before, the amplitude of pulse shaper signal does not depend on time constant of shaper. The minimization of ENC with respect to time constant can than be achieved by min-

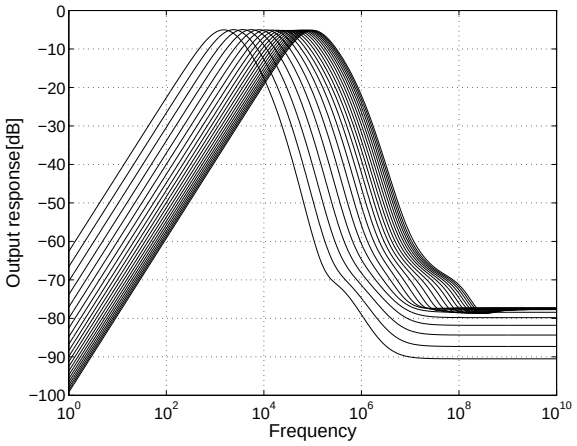

Figure 4.12: Frequency response of the designed pulse shaper for variation of biasing voltage of OTA.

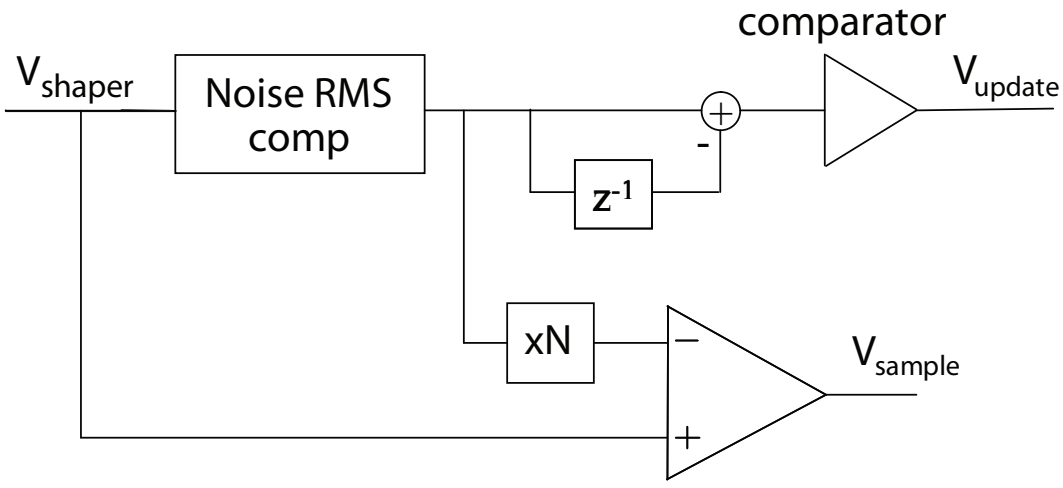

Figure 4.13: Block diagram of adaptive noise processing

imization of the standard deviation of the output noise signal of the shaper. The output noise signal dependance on time constant of shaper can be written as

$$V_{n,tot}^2 = A/\tau + B\tau + C \tag{4.3}$$

where A, B and C are constants that depend on the parameters of the diode and readout circuitry.

To optimize the time constant of shaper, we propose adaptation based on stochastic perturbation technique [53]. An noise RMS computation block senses the RMS level of output signal from pulse shaper, $V_n(t)$. Based on the sign of the gradient of $V_n(t)$, obtained as difference between $V_n(t+T)$ and $V_n(t)$, a small increment of biasing current is performed, where the sign of constant increment depends on the sign of gradient. To demonstrate the algorithm, we have constructed an artificial output noise signal, which includes 1/f noise, thermal noise and shot noise components, in time domain. The thermal and shot noise are white and follow a Gaussian distribution in the time-domain. The time-domain 1/f noise is generated as described in [54]. Figure 4.14 shows a simulation of the proposed system. The red curve is the calculated ENC versus time constant, and the blue curve shows how the algorithm helps the Gm-C filter to find the best time constant to minimize noise.

Figure 4.15 shows a typical recorded radiation signal in time domain. In order to be power efficient, only the informative data needs to be transmitted. Therefore, the following pulse processing unit needs only to be triggered when the output signal is up certain threshold.

[67] shows that in systems with limited computational resources, taking the absolute value of the neural signal before applying a threshold is just as effective for detecting spikes as applying more elaborate energy-based detectors using digital signal processing techniques. Figure 4.16 presents a proposed block diagram for

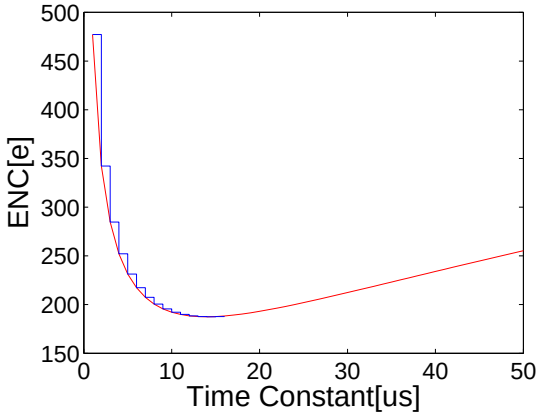

Figure 4.14: Simulation of adaptive noise processing

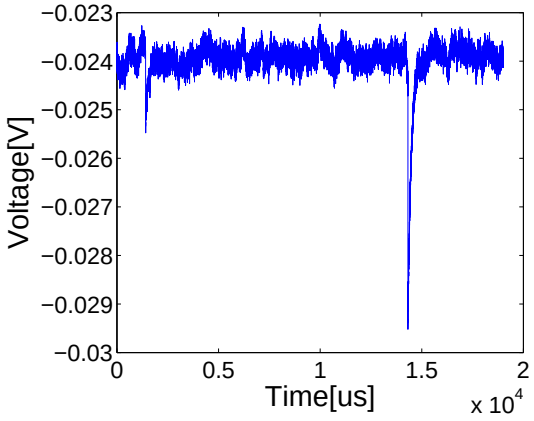

Figure 4.15: Recorded radiation signal

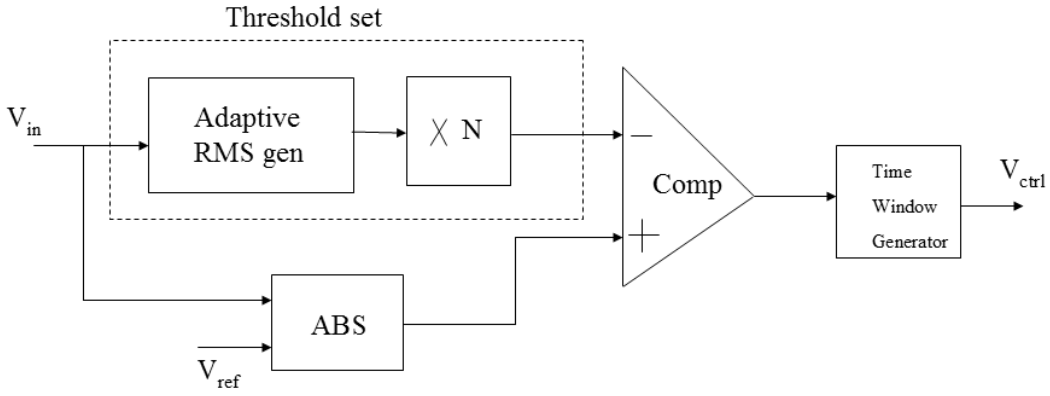

Figure 4.16: Block diagram of adaptive spike detector with absolute value algorithm

an analog spike detector using an absolute value algorithm. It is similar as shown in [68], which is used in a biomedical application. The adaptive real-time threshold set block [69], [70] performs spike detection using a specified multiple (N in figure 4.16, usually 3 to 7) of the background noise rms value. ABS block generates absolute value with respect to common mode reference for input signal. The time window generator block produces 1-bit digital enable signals for a period of time, which is required for successful recording of an active spike signal.

Figure 4.17 shows implemented adaptive spike detector with the ABS. $V_{1\delta}$ is set to the rms level of the input waveform by comparator A and the feedback loop. This voltage is amplified by a constant level, which is set by the ratio of R_1 and R_2. The voltage, $V_{threshold}$, sets the adaptive threshold voltage. Absolute value circuit consists of two identical operational transconductance amplifiers (OTA) and two identical PMOS cascode mirrors, rather than one OTA with one PMOS current source and one NMOS current sink introduced in [71], to reduce a current mismatch error between NMOS and PMOS.

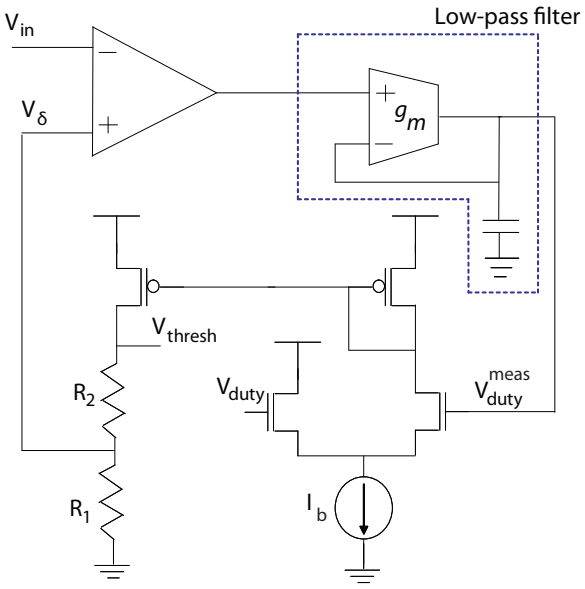

Figure 4.17: Schematic of the adaptive spike detector using absolute value. Adaptive threshold set scheme was from [69], [70].

4.3 Peak Detector

The peak value of the output pulse from pulse shaper should be sampled before it is sent to analog-to-digital conversion. Some literatures suggest using a large analog memory cell to sample the output signal from pulse shaper at a relatively high frequency [41]. This solution requires large on-chip area and consumes a large amount of power as well. We adopt the solution with peak detector.

Peak detectors are a key element in nuclear electronics signal processing; it captures the peak amplitude of a pulse [55]-[58]. In CMOS design, the peak detector uses an MOS current source as the rectifying unit inside a feedback loop of a high-gain amplifier. A simplified schematic of the classical CMOS peak detector circuit for positive voltage pulses is shown in figure 4.18. The principle operation is similar as in the case of negative voltage pulses.

Transistor M_1 acts as a charging and also as a switching element. Before the

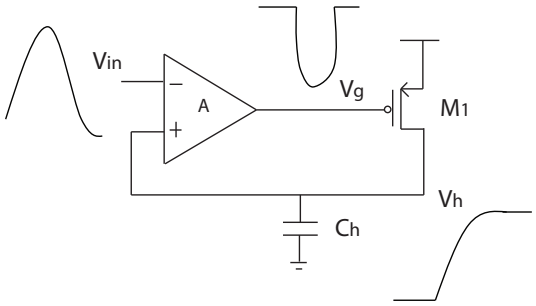

Figure 4.18: Simplified version of pulse shaper

pulse comes at the input V_{in}, the hold voltage V_h tracks the input voltage. When the input voltage V_{in} starts to increase, the gate voltage of M_1 is decreasing sharply. M_1 then turns on, allows C_h to be charged up, and V_h follows V_{in} as the pulse increases. After the pulse is over, V_{in} decreases. The gate voltage of M_1 increases, and turns off M_1. Then C_h has no charging and discharging path. Therefore, V_h holds the peak value of input pulse.

A two-phase peak detector is proposed in [57] that cancels offset and common mode gain, which are the major error sources of the classical CMOS peak detectors. Figure 4.19 shows the schematic of proposed two-phase peak detector. During $\phi 1$ the circuit functions as the classical version. After the peak value is captured, $\phi 2$ is active, which closes the unity feedback loop around the opamp. The voltage stored at C_h is read out through the unity gain buffer. Since the same amplifier is used in both phases, the offset is canceled. Figure 4.20 shows simplified schematics of the peak detector in two phases separately.

Figure 4.21 shows the schematic of designed OTA. The biasing current is selected to be around $70uA$. C_h is selected to be $5pF$ to reduce offset error. [56], [57] explains a design criteria for OTA to keep the peak detector stable. Since the rise time of shaper output signal is rather slow, the criteria is easily met.

Figure 4.22 shows a simulation result of designed peak detector. The blue curve

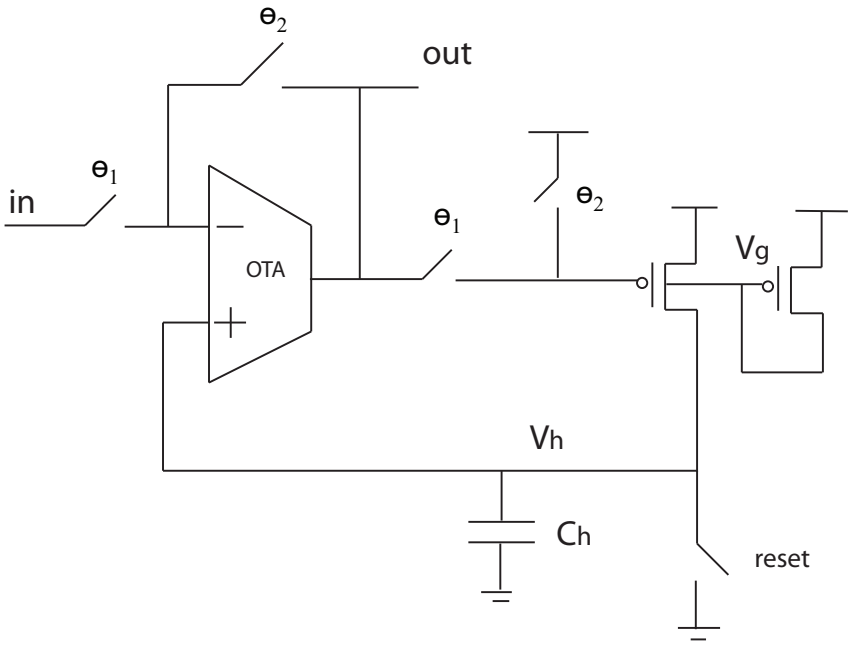

Figure 4.19: Schematic of two phase peak detector

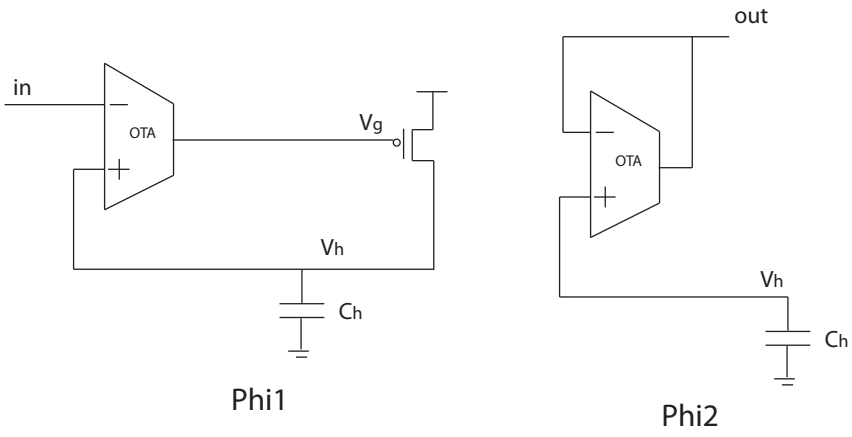

Figure 4.20: Simplified schematic of peak detector in two phases

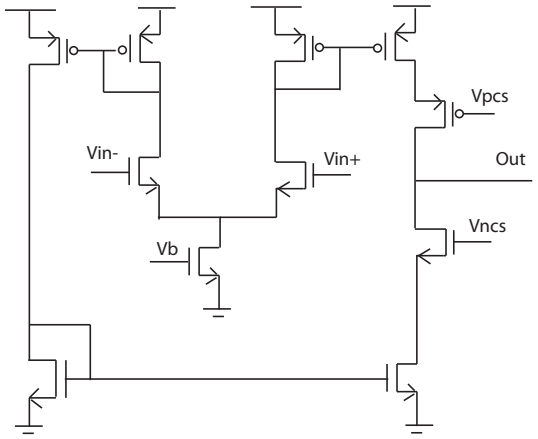

Figure 4.21: Schematic of OTA

is the input semi-Gaussian pulse signal, the red curve is the voltage stored at C_h, the green curve is the final output voltage after $\phi 2$ is activate. It is seen that output voltage is only available after input pulse starts to decrease.

Figure 4.23 shows a linearity plot of designed peak detector. X-axis is the input pulse peak amplitude, and Y-axis the output signal of peak detector. Excellent linearity is achieved.

4.4 Conclusion

This chapter describes the design of a pulse shaper and peak detector. The pulse shaper employs ICON cell, which amplifies the implemented resistance by means of current mirror. Thus, high time constant pulse shaper is built with minimum silicon area. A two-phase peak detector is designed and simulated. The designed peak detector cancels offset errors from operational amplifier. A possible improvement of pulse shaper is also discussed. The proposed adaptive shaping filter has the ability to adjust its time constant according to detectors with different specs.

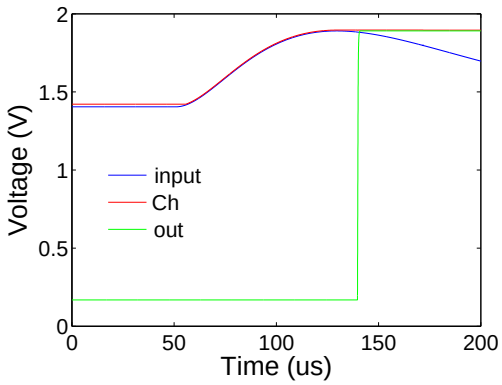

Figure 4.22: Simulation result of peak detector

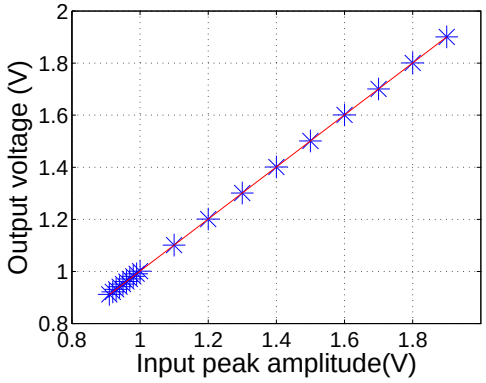

Figure 4.23: Linearity plot of designed peak detector

Chapter 5

Implemented ASIC

In previous chapters, we described the analog building blocks to readout signal from radiation detector. This chapter presents an ASIC implementation of the analog section of the front-end readout system.

5.1 Implemented ASIC

The implemented ASICs are fabricated through AMI CMOS 0.5um process [72]. The process employs 3 metal and 2 poly with high-resistance option. The first version employs one single CSA and Figure 6.15 shows a micro-photo of implemented ASIC. Four channels of readout system are integrated into an area of $1.3mm$ by $1.6mm$. Each channel consists of a CSA, pulse shaper and a peak detector. The input node of CSA is placed as close to the pads as possible to minimize parasitic. Biasing and signal routing are placed on the right side of the chip, which are not shown.

The last channel is implemented with on-chip characterizing circuitry. An external tunable current source is added at the input node of CSA to simulate detector

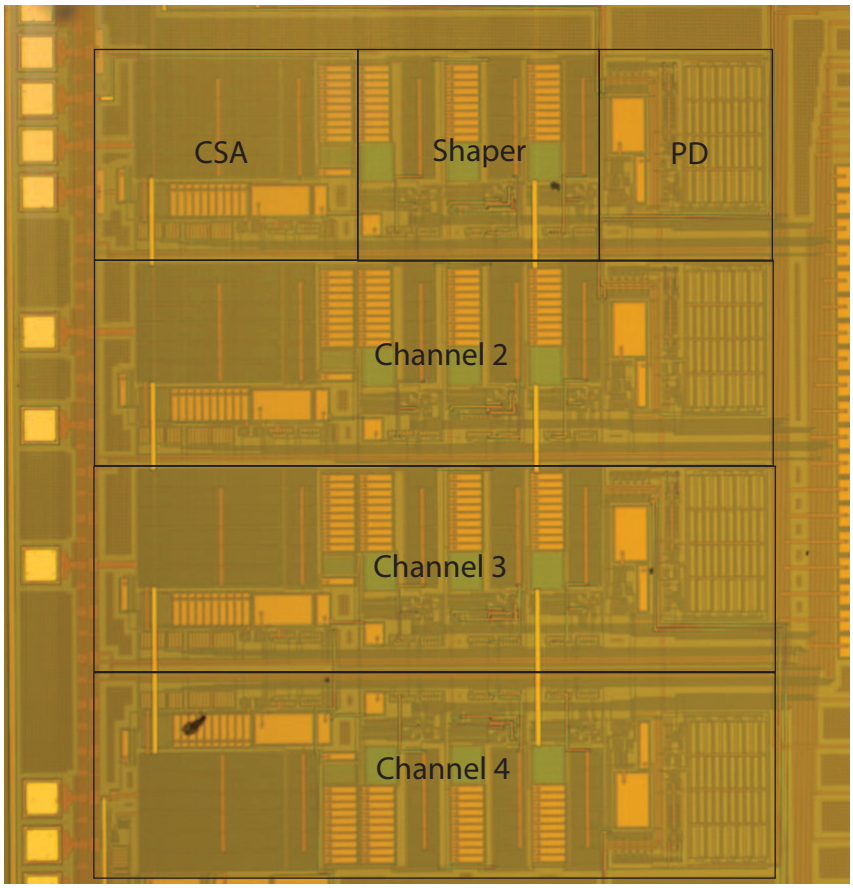

Figure 5.1: Micro-photo of implemented ASIC

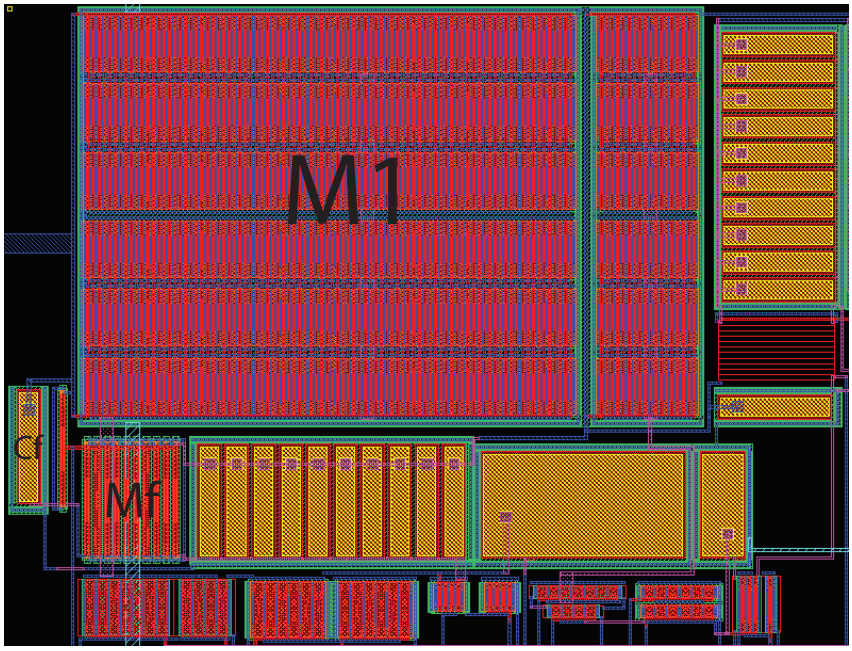

Figure 5.2: Layout of CSA

leakage current. Different values of capacitors are also added at the input node to simulate detector parasitic capacitance through control of switches.

Figure 5.2 displays the layout of CSA. The input transistor M_1 takes up to half of the total area. C_f and M_f are placed at the left bottom corner to reduce the routing distance for input node. It can be also seen that the amplifier in second CSA is about 5 times smaller.

Figure 5.3 displays the layout of pulse shaper. Note that the amplifier used in pulse shaper is again a 5 times scaled down copy.

Figure 5.4 displays the layout of peak detector. The digital blocks of peak detector are shielded from analog blocks with a guard ring. Separate power supply is used to power the digital blocks.

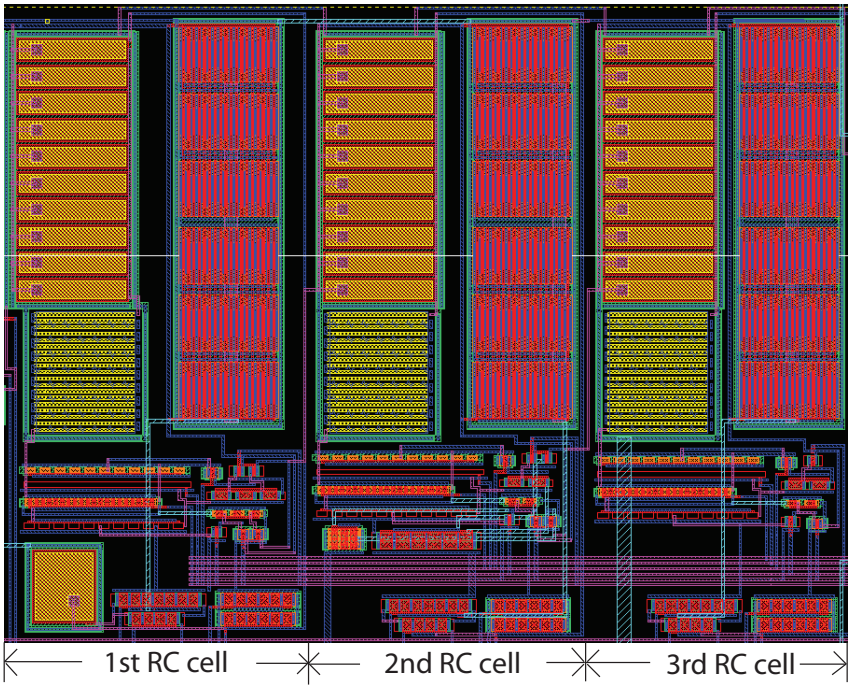

Figure 5.3: Layout of pulse shaper

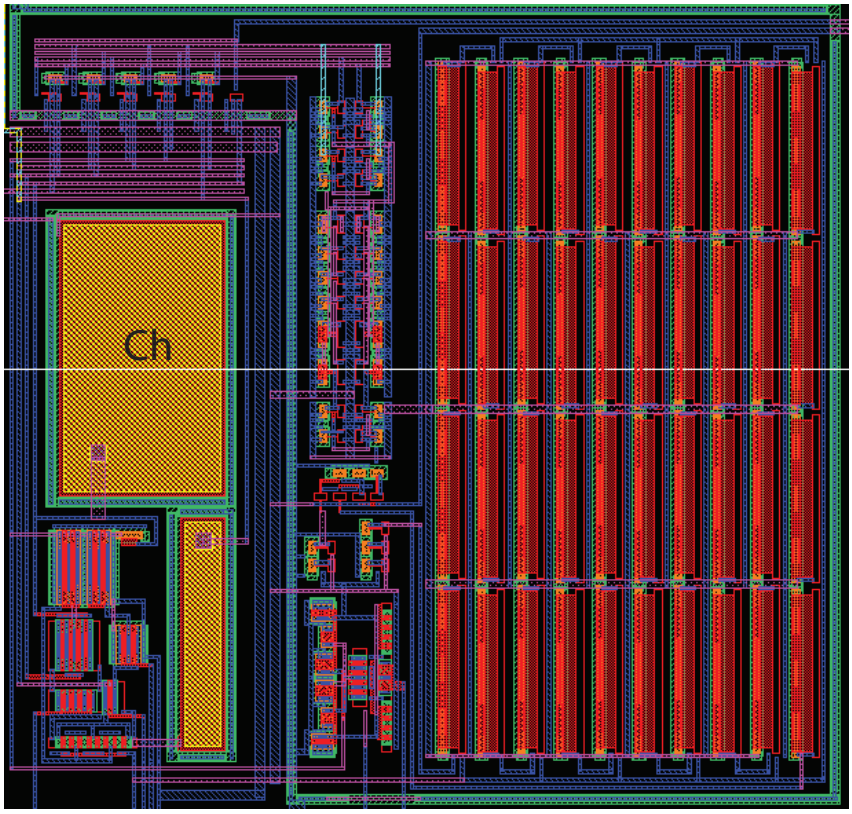

Figure 5.4: Layout of peak detector

5.2 Test setup

An interface board has been designed and fabricated, which will allow for the test of the ASIC. The board provides connections with a data acquisition card NI-PCI 6259, which is installed in a PC. The acquisition card provides analog input and analog output with 16 bits resolution, and up to 48 ports of digital I/Os, which provide digital control signal for the testing chip and also control on-board commercial DACs to generate biasing. Three regulators are used to provide power supplies for the chip: $3.3V$ analog supply, $3.3V$ digital supply and a $2.5V$ supply for the input transistor of CSA to reduce noise.

Figure 6.17 shows a photo shot of the designed interface board. The chip is placed in the black square box in the middle of board. To minimize parasitic effect, chip-on-board technique is employed. The bare die of chip is wire-bonded directly on the board, and fully encapsulated with epoxy. Plug-in sockets provide access with the radiation detector. However, this configuration leads to increased noise. More advanced techniques, such as wire-bonding, bump bonding flip-chip technology, should be applied in the future for more precise test.

When testing without detector, a $1Gohm$ resistor is plug into the sockets to simulate the leakage current. Different capacitors can be soldered serially with the input node to simulate the parasitic capacitance of detector, and also provide input charge by passing a voltage step through the serially connected capacitor.

PC-based supervision of the whole system has been realized by means of MATLAB programs.

Figure 5.6 shows a setup to test the ASIC with sensor. Enclosure covered with aluminum foil is used to shield excess environment interfaces. A prototype of the proposed scintillation radiation detector is mounted on the board. A movable holder that holds radiation source and has the ability to control distance between source

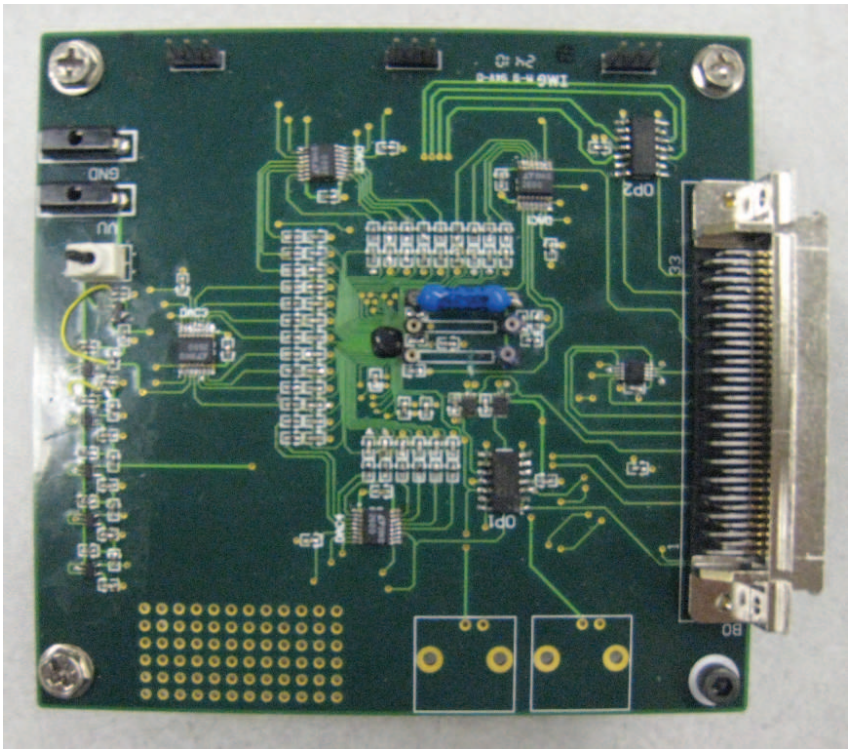

Figure 5.5: Photo of the interface test board

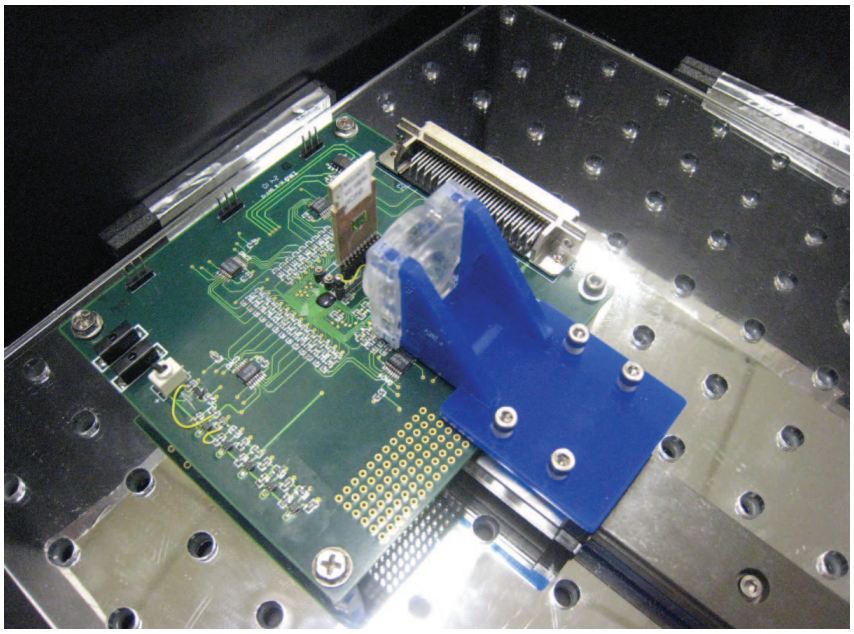

Figure 5.6: Setup to test ASIC with sensor

and detector is designed.

5.3 Measurement results

The ASIC is first characterized without detector. Figure 5.7 shows a measurement result of output signal of CSA. The input charge is simulated with a voltage step passed through a $1pF$ capacitor connected serially with the input node. The input charge is $5K$ electron, $10K$ electron and $20K$ electron, respectively.

Figure 5.8 shows a measured output voltages of CSA as a function of input charge. Good linearity is achieved.

Figure 5.9 shows a measurement result of output signal of shaper. The input charge is simulated the same way as previous test. The input charge is $5K$ electron, $10K$ electron, $15K$ electron, $20K$ electron and $25K$ electron, respectively. A

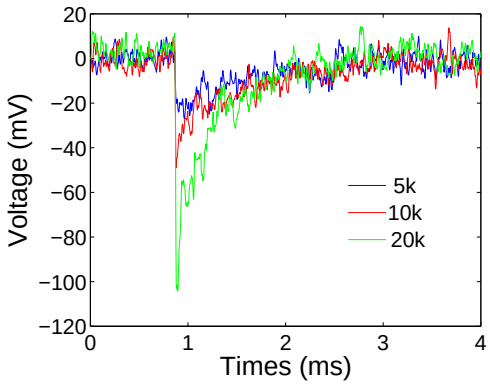

Figure 5.7: Output of CSA for different input signals

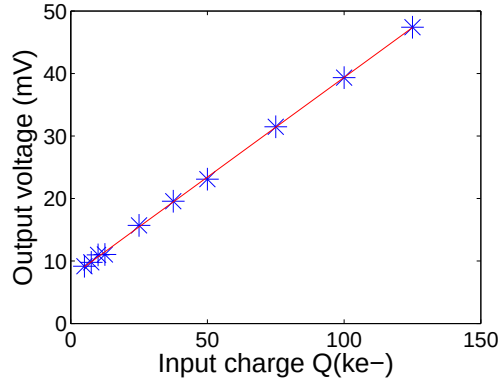

Figure 5.8: Measured output voltage of CSA as a function of input charge.

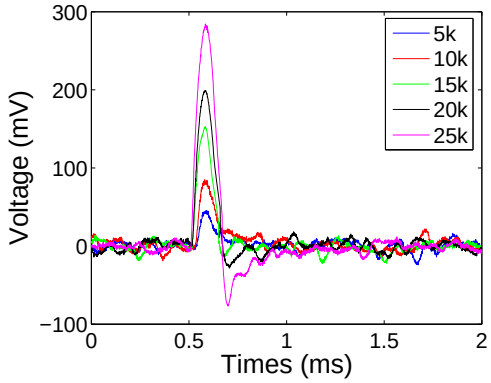

Figure 5.9: Output of pulse shaper for different input signals

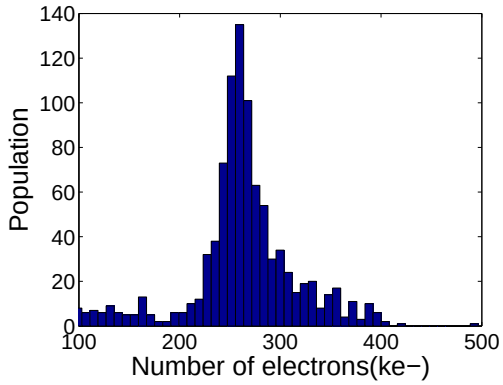

Figure 5.10: Experiment result with americium source.

charge gain of approximately $71mV/fC$ is measured.

Figure 5.10 shows a experiment test result of a real radiation source, americium, placed very closely to the detector. The readout system registers about one thousand events. Based on the readout number of electrons, the registered events are sorted into 50 bins. The plot is a histogram of recorded signal, the X-axis is the number of readout electrons, the Y-axis is the population of each bin.

5.4 Conclusion

This chapter presents the implemented front-end readout ASIC. The designed chip layout, test interface board, and some experimental measurement results are displayed.

Part III

Analog-to-Digital Conversion

Chapter 6

Analog-to-Digital Conversion

Comparing to off-chip analog-to-digital conversion, the design of a sensor system with on-chip analog-to-digital conversion would reduce noise introduced by interconnections between analog and digital modules, and provide a high-throughput recording systems that can provide ability to configure data collection mechanism for reliable data logging [59].

The main constraint in the design of proposed multi-channel system is power and size of analog-to-digital converters. The size constraint leads to channel multiplexing which results in increased data rate of converter and increased power. We propose the use of extended counting technique, that represents combination of incremental and algorithmic ADC, providing resolution of the interest, and on the other hand small form factor.

In this chapter, design of a 13 bit extended counting analog-to-digital converter is presented.

6.1 Extended Counting Analog-to-Digital Conversion

Traditionally, two widely used candidate architectures are available. Delta-sigma modulation achieves a high resolution by means of oversampling. This normally leads to an increased power consumption. Moreover, these implementations require digital decimation filters that may occupy several square millimeters of silicon area [60]. Algorithmic ADC [61, 62] has much smaller power consumption and can operated at higher speed. However, the linearity is limited by component matching. In standard CMOS process, only 8-10 bits of resolution can be achieved. Extended counting converter combines the advantages of delta-sigma modulation and algorithmic A/D conversion [60], [63]-[66]. It achieves a good trade-off between accuracy and speed.

The extended counting conversion contains two conversion modes. The converter passes two modes one after the other in time, and each mode needs several clock cycles to complete. Hence, one sample is converted through several clock cycles. A block diagram of the architecture is shown in Figure 6.1. The first mode, which is called "counting conversion", is a resettable first-order delta-sigma modulator. It converts the most significant bits (MSB). Then the residue of the first mode, V_{count}, is fed into the second mode, called "extended counting conversion", which is generally implemented as an algorithmic conversion. The least significant bits (LSB) are obtained in the second mode.

Normally, LSB is set to 10 bits, the limit of algorithmic conversion. The MSBs is determined by the system resolution requirement. For the design example which is shown in this chapter, 13 bits is required. Therefore, we acquired 3 bits from the counting stage and 10 bits from the extended counting stage. So, the first stage needs $2^n = 8$ clock cycles, where $n = 3$ is the number of MSBs. The second stage needs $(n + 2)/2$ clock cycles to ensure that the component mismatches limit the

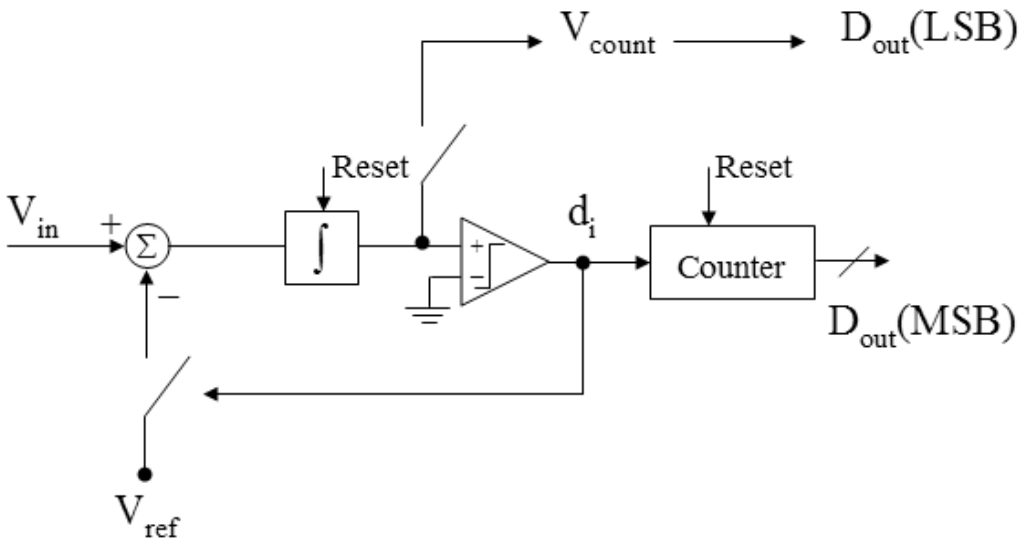

Figure 6.1: Block diagram of extended counting A/D conversion

LSB resolution to 10 bits, where $n = 10$ is the number of LSBs. Two additional clock cycles are required in the transition between stages, leading to a total 16 clock cycles needed for one conversion.

The designed switched capacitor implementation of ECADC is described as follow. The operation of counting conversion is illustrated in Figure 6.2. An initial reset is performed before each conversion. Each step includes two phases. In the first phase, the input voltage V_{in} is sampled and the output of op-amp is held constant for the comparator to decide the digital output bits D_i. In the second phase, a reference voltage V_{ref} depending on the sign of D_{i-1} from last phase is fed back to the input. C_2 is designed to be two times of C_1. Therefore a first-order delta-sigma modulation is performed. The operation can be expressed in the following equation:

$$V_i = V_{i-1} + \frac{C_1}{C_2}(V_{in} - D_{i-1}V_{ref}) \tag{6.1}$$

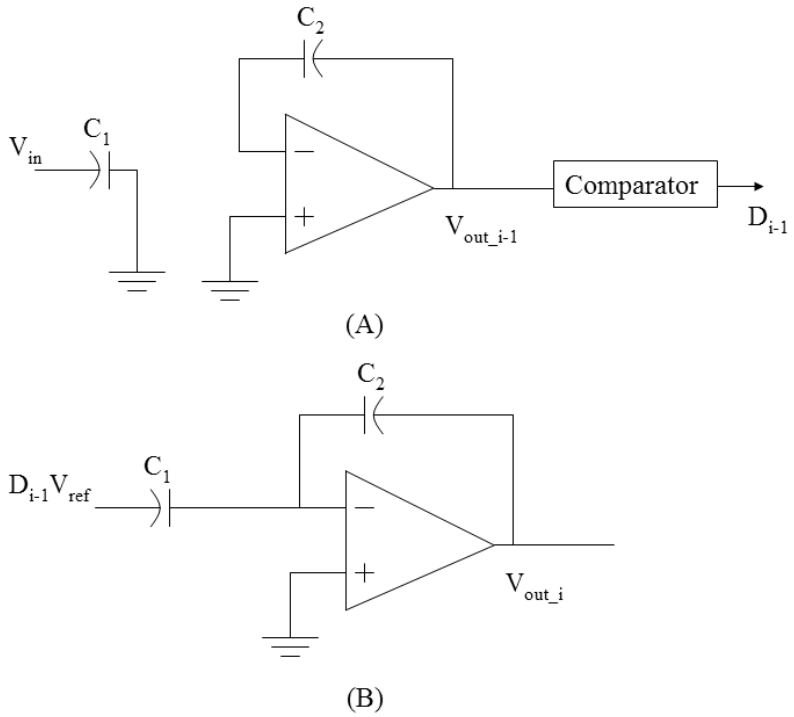

Figure 6.2: Counting stage

The operation of extended counting conversion is illustrated in Figure 6.3. Similar circuit operations take place in the extended counting stage, except that two digital bits are generated in one clock cycle. In order to loose the requirement for OPAMP's output voltage range, all capacitors except are set nominally equal. For better linearity, an amplification with the factor of 2 is performed to initialize the second stage [60]. The operation can be expressed in the following equation:

$$V_i = (1 + \frac{C_3}{C_1})V_{i-1} - D_{i-1}\frac{C_3}{C_1}V_{ref} \tag{6.2}$$

Figure 6.4 shows a single-ended schematic of the designed ADC. The implemented fully differential structure is not shown here for simplicity. Compared with the reported architecture [60], three capacitors are used instead of four. All capac-

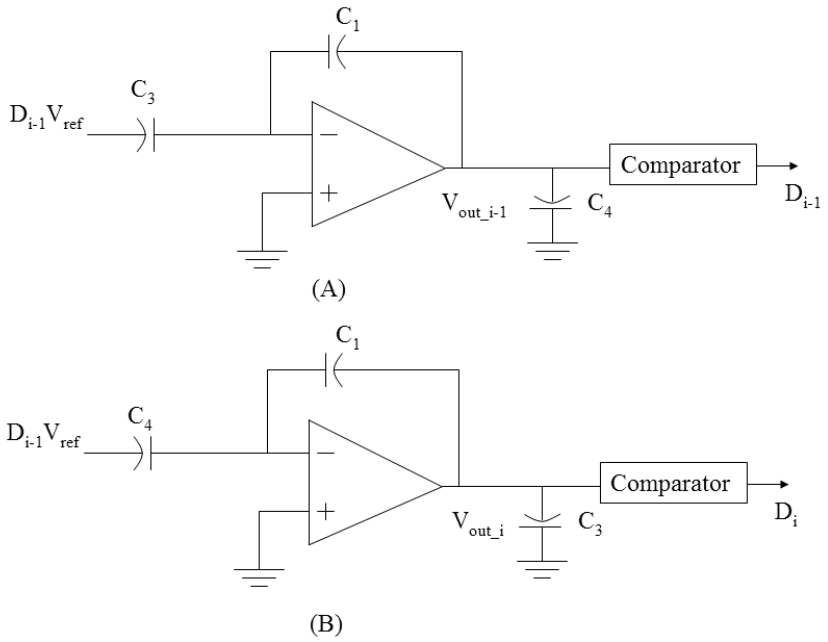

Figure 6.3: Extended counting stage

itors are nominally equal, and C_2 and C_3 are connected together in the first stage to provide a larger feedback capacitor. The switches in blue are mostly activated in the counting stage, while the switches in red are mostly activated in the extended counting stage. Figure 6.5 shows the clock scheme of one conversion.

6.1.1 Design of operational amplifier

The most important building block of the ADC is the operational amplifier (OPAMP). Non-ideality of OPAMP effects the overall performance of the ADC. In our design, we have considered the infinite gain o OPAMP, mismatch between nominally equal capacitors, input parasitic capacitance of OPAMP and offset of comparator and OPAMP. Behavior model is constructed in MATLAB to simulate such affects. Figure 6.6 shows the MATLAB simulation result, which is simulated

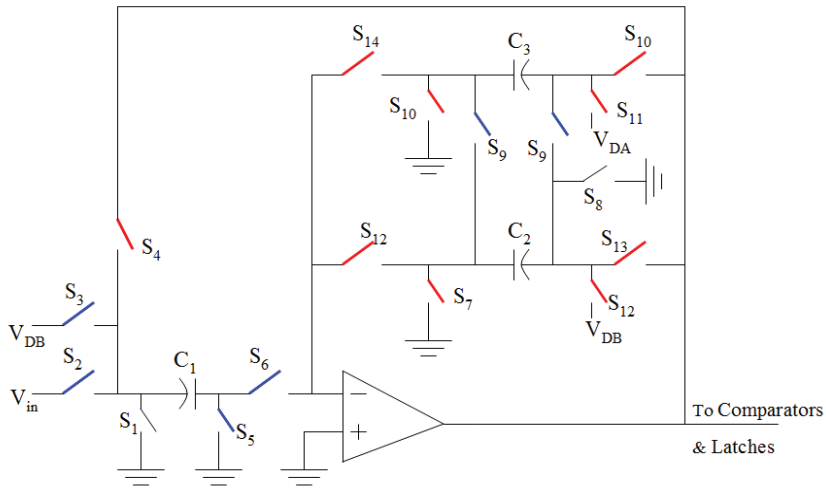

Figure 6.4: Designed schematic of ECADC

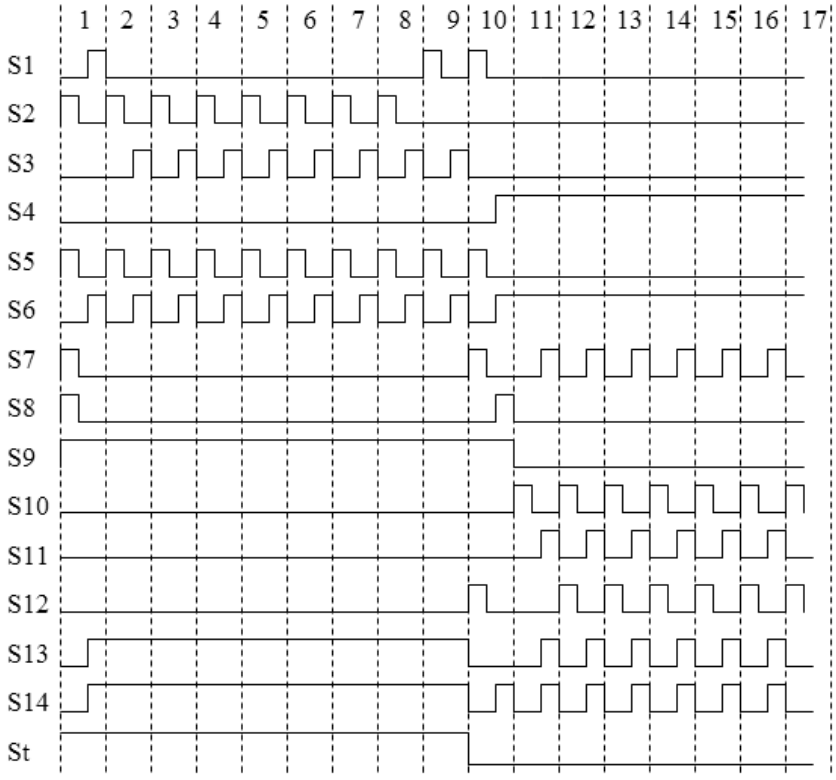

Figure 6.5: Clock scheme of one conversion

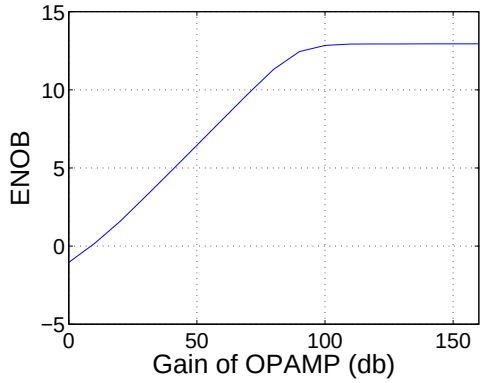

Figure 6.6: Behavior simulation to determine gain requirement of OPAMP

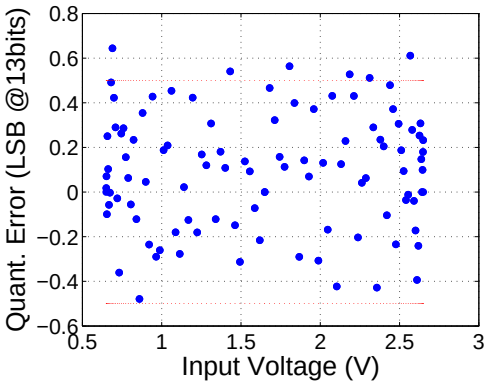

Figure 6.7: Behavior simulation of the targeted OPAMP gain

under the following assumptions: 1. 0.1% mismatch between caps, 2. $3mV$ offset of comparator and OPAMP, 3. $0.5pF$ input parasitic capacitance of OPAMP. The simulation indicates a gain of over $100db$ is required to achieve the target resolution. Figure 6.7 shows a simulation of the worst case scenario, when mismatches and offsets are at their maximum. The red line is $1/2$LSB. The input voltage is a sine wave of $2V$ peak-to-peak amplitude sampled with a frequency of $500KHz$. The Y-axis shows the quantization error of the simulated ADC. A effective number of bits (ENOB) of 13.051 is achieved with $100db$ gain of OPAMP.

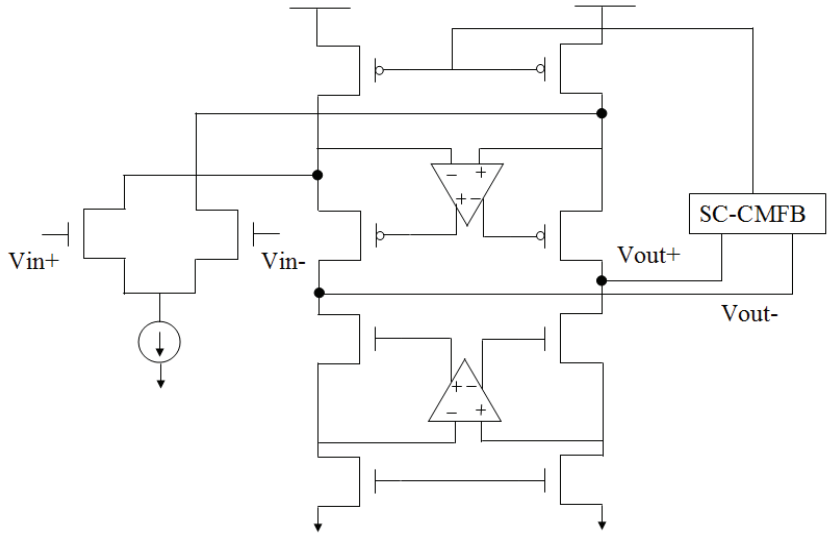

Figure 6.8: Schematic of designed OPAMP

The target sampling rate of our design is $512kHz$. 16 clock cycles are required for each conversion, which leads to $8MHz$ of clock frequency. The gain-bandwidth (GBW) of OPAMP should be 5 times greater than the clock frequency to ensure proper settling. OPAMP should be able to settle in half of the clock period. Thus, a GBW over $100MHz$ is desired.

Considering gain and GBW along with output swing, input capacitance and other requirements, a folded-cascode structure with gain-boosting is selected. Figure 6.8 shows the schematic of designed OPAMP. The gain-boosted amplifiers are also implemented with folded-cascode structure to achieve large output swing. Switch-capacitor common mode feedback is implemented for the OPAMP.

The additional pole which comes with the gain-boosted amplifier affects the overall settling behavior. [73] provides a classic analysis, and the following relationship must hold to maintain fast settling:

$$\frac{1}{\beta}\omega_1 < \omega_3 < \omega_2 \tag{6.3}$$

where β is the closed loop gain, ω_1 and ω_2 are the dominant and first non-dominant poles of the original amplifier, ω_3 is the dominant pole of the gain-boosted amplifier.

The designed OPAMP is simulated to have gain of $106db$ and $230MHz$ gain-bandwidth.

6.1.2 Design of Switches

Switches used in our design is implemented with CMOS transmission gate. Careful design of switches is required in high speed application. Smaller switches suffer from low conductance, thus the charging or discharging current is not strong enough to meet the speed requirement. Larger switches suffer from large parasitic capacitance.

In our design, proper size of switches are determined through simulation. In most critical path, switches are sized 10 times of the minimal size switches.

6.1.3 Design of Comparator

To reduce the kick-back noise from comparator, the comparator is designed with a two stage structure: pre-amplifier and latch. Figure 6.9 shows the single-ended schematic of preamplifier. The amplifier used in the preamplifier is implemented with a simple high-gain common-source cascode amplifier. Figure 6.10 shows the schematic of designed latch.

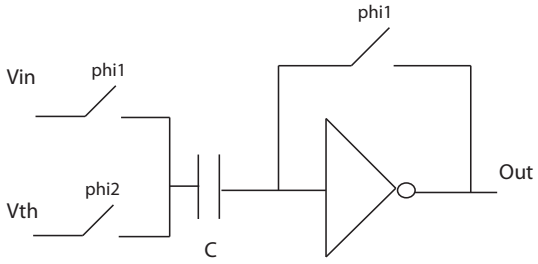

Figure 6.9: Schematic of designed preamplifier for comparator

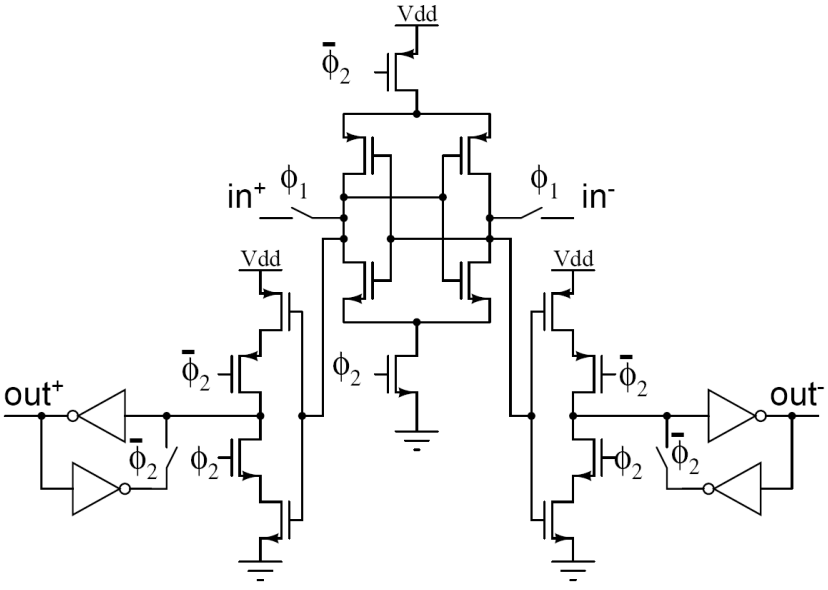

Figure 6.10: Schematic of designed latch for comparator

6.2 Optimization Techniques

This section presents several optimization techniques of designing the extended-counting ADC.

6.2.1 Optimizing the Number of ADC

The power consumption of ADC is mainly determined by the sampling speed, and the sampling speed is limited by the settling time of OPAMP used in the ADC. To minimize core size, only one ADC is usually chosen. Signals from multiple channels are multiplexed before fed into the ADC. However, this results in a high sampling frequency ADC, which leads to increased power consumption. To achieve an optimum point between size and power, a detail analysis is required.

The settling time is controlled by two parts: slew rate (SR) and gain bandwidth (GBW) of the OPAMP. If one third of the settling time is assigned to slew rate [74], and a single-pole model of OPAMP is used, two equations can be derived:

$$I_D = 3 \cdot f \cdot V_{pp,diff} \cdot C_{L,eff} \tag{6.4}$$

$$I_D \cdot \frac{W}{L} = \frac{9ln^2 2}{2\mu_0 C_{ox}} \cdot (N+1)^2 f^2 \cdot (\frac{C_{L,eff}}{m})^2 \tag{6.5}$$

where f is the sampling frequency, I_D is the drain current of the OPAMP input differential pair, $V_{pp,diff}$ is the largest differential full scale slewing, $C_{L,eff}$ is the effective load presented at the output of the OPAMP, N is the resolution, and m is the feedback factor. The first equation gives the SR limited current requirement, and the second equation gives the GBW limited current requirement. It is clear that when the SR limitation is dominant, the drain current is linear with frequency, when the GBW limitation is dominant, the drain current follows a square law. Hence, the optimum point between size and power lies when the biasing current of OPAMP is

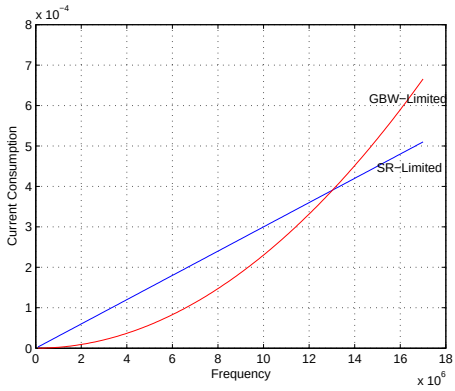

Figure 6.11: Current consumption versus clock frequency

selected at the SR limited region, but as close as to the GBW limited region.

With the design process parameters and the unit capacitance used in our design, MATLAB simulations are performed to find the optimum number of ADCs. Figure 6.11 plots the current consumption of the OPAMP as a function of sampling frequency f. Based on such plot, the optimum number of ADC and optimum number of channels multiplexed into one ADC are determined.

6.2.2 Different Settling Behaviors in Two Stages

Figure 6.12 shows a typical circuit scheme in ECADC architecture and its equivalent small signal model. Assuming the output impedance of OPAMP R_o is very large and the input parasitic capacitance C_{in} is small, a small-signal analysis indicates that the transfer function is:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{C_S(sC_F - G_m)}{C_F G_m + s(C_{out}C_S + C_F C_S + C_F C_{out})} \tag{6.6}$$

Assuming the input voltage is a unit step, the voltage step in both time and frequency domain is

$$V_{in}(t) = U(t), V_{in}(s) = 1/s. \tag{6.7}$$

Thus the output voltage in both domain is

$$V_{out}(t) = \frac{C_S}{C_F}U(t) - \frac{C_S}{C_F}[1 + \frac{b}{a}]e^{-bt}U(t), \tag{6.8}$$

$$V_{out}(s) = \frac{1}{s}\frac{C_S(sC_F - G_m)}{C_F G_m + s(C_{out}C_S + C_F C_S + C_F C_{out})}, \tag{6.9}$$

where

$$a = \frac{G_m}{C_F}, b = \frac{G_m C_F}{C_{out}C_S + C_F C_S + C_F C_{out}}. \tag{6.10}$$

The time constant τ of the output voltage is then derived to be

$$\tau = \frac{1}{b} = \frac{C_{out}C_S + C_F C_S + C_F C_{out}}{G_m C_F}. \tag{6.11}$$

Figure 6.13 shows a simulation result of OPAMP outputs in one conversion. The solid line is the positive output of OPAMP, and the dashed line is the negative output of OPAMP. The fastest settling happens in the first few clock cycles, where the converter works in counting stage. In this stage, C_S=1p, C_F=2p, C_{out} equals to the parasitic output capacitance of OPAMP. In the last few clock cycles, the converter works in extended counting stage, where C_S=1p, C_F=1p, C_{out} equals to 1p plus the parasitic output capacitance of OPAMP. In the transition between stages, where the amplification required to initialize extended counting stage is performed, C_S=2p, C_F=1p, C_{out} equals to the parasitic output capacitance of OPAMP. If the output parasitic capacitance of OPAMP is assumed to be 300f, then

$$\tau_{counting} = \frac{1.45}{G_m}, \tau_{extended} = \frac{3.6}{G_m}, \tau_{transition} = \frac{2.9}{G_m}. \tag{6.12}$$

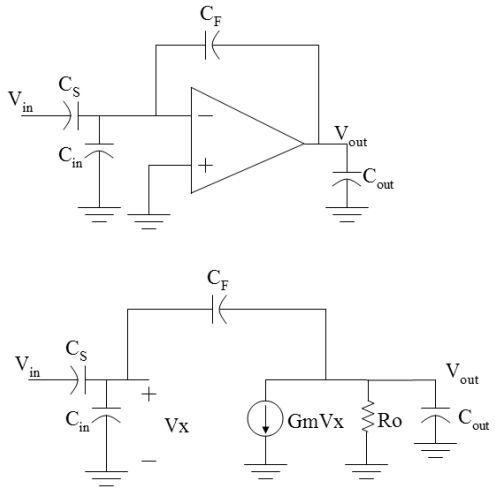

Figure 6.12: Typical circuit scheme in ECADC and its equivalent small signal model

From the above equation, the settling time in extended counting stage is almost 2.5 times than that in counting stage, and the time constant in extended counting stage and transition are fairly the same. Thus, the small-signal analysis does a good prediction of the circuit behavior, and the calculation results approximately match the simulation. Therefore, it is clear that power is wasted if the same OPAMP is used in the whole conversion.

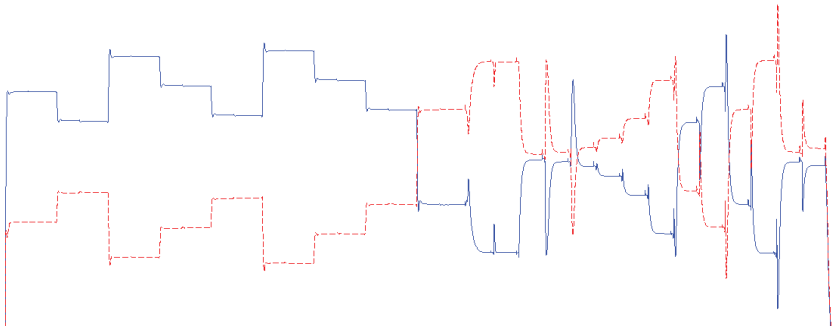

Figure 6.13: Different settling behaviors

Two methods are developed to combat this problem. Firstly, different clocks can be used in conversion. Shorter time period can be assigned to counting stage to take advantage of its shorter time constant. Hence, faster speed can be achieved while consuming the same amount of power, or in other word, lower power is consumed while maintaining the same conversion speed.

Instead of using clocks with different periods, we implemented a reconfigurable OPAMP with adjustable biasing current. Smaller biasing current is needed when the time constant is lower. Hence, the OPAMP is switched to a higher biasing when counting stage is finished. It is a similar concept described in [75]. In figure 6.4, $Ibias1$ and $Ibias2$ are two different biasing currents for counting stage and extended counting stage, respectively. In figure 6.5, St is the clock controlling biasing current of OPAMP, and Stc is a complementary clock of St. The switching is performed in the first phase of 10th clock, when the OPAMP is not operating. Thus, additional clock cycle penalty is avoided to reconfigure the OPAMP.

Since G_m^2 is proportional with the drain current of OPAMP, and 8 clock cycles from counting stage can benefit from this technique, the total power reduction is about 40% for our design. If more bits resolution are required from counting stage, the reduction is even greater. Using the same conditions as above, and assume 10 bits resolution is provided from extended counting stage, the power consumed in one conversion with two different structures is plotted in Figure 6.14.

6.3 Implemented ASIC

6.3.1 Chip layout

The implemented ASIC is fabricated through AMI CMOS 0.5um process. The process employs 3 metal and 2 poly with high-resistance option. Figure 6.15 shows

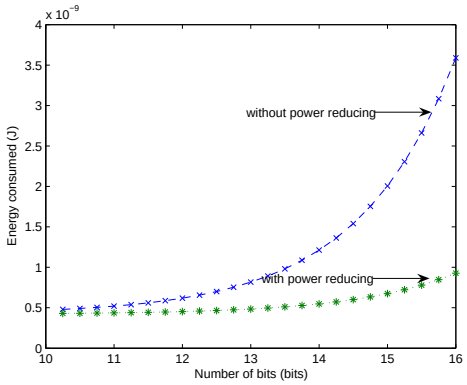

Figure 6.14: Power reduction versus number of bits

Table 6.1: Summary of designed ADC

Resolution	13bit
Power Supply	3.3V
Sample Freq.	512k Hz
Power Cons.	7mW
Input Range	2V
Core Area	0.7mm by 0.8mm

a micro-photo of implemented ASIC. The ASIC was originally designed for a 32 channels neural recording system [76]. The ASIC consists 32 low-noise low-power neural recording front-end channels, and two 13 bit extended counting ADCs. Total system occupies occupies an area of $3mm$ by $3mm$. The performance of the ADC is summarized in table 6.1.

Figure 6.16 displays the layout of CSA. The digital parts and the analog parts are carefully separated to avoid interference. The most sensitive analog part, the OPAMP, is laid out in the bottom, with its biasing routed at its top. The capacitor arrays, which consists multiple identical unit capacitor cells, are laid out in the middle. Common-centroid structure is used to improve matching. The switches are laid out at the top, with their digital control signals routed at its top. Thus, the

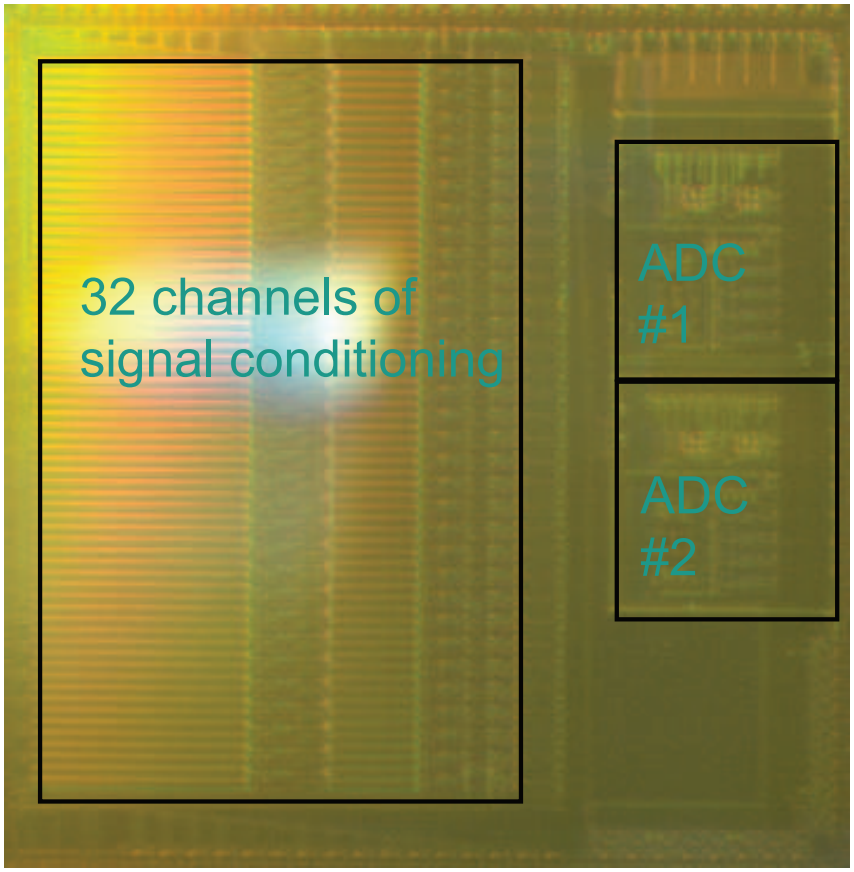

Figure 6.15: Micro-photo of implemented ASIC

digital signal lines are placed far from the analog signal lines. Besides, the routings of digital signals are shielded with a poly layer, which is connected to a fix voltage, to avoid interference on the substrate. Guard rings are also applied to protect the sensitive analog circuits.

6.3.2 Test setup

An interface board has been designed and fabricated to test the implemented ASIC. Figure 6.17 shows a photo shot of the designed interface board. The board provides connections with the same data acquisition card NI-PCI 6259 as described in chapter 5. On-board commercial DACs and regulators were also used to generate biasing and provide clean supply. Several level shifters were employed to transfer $5V$ DIOs from NI 6259 to $3.3V$, as the NI 6259 only provides $5V$ DIO and the chip was designed under $3.3V$. Chip is mounted on a zero-insert-force (ZIF) socket for easy accessibility. PC-based supervision of the whole system has been realized by means of custom MATLAB programs.

6.3.3 Measurement results

Figure 6.18 shows a measurement result of the designed ADC.

The measurement result doesn't meet design criteria for the following reasons. First, the maximum frequency of NI 6259 data acquisition card's DIOs is limited to around $100KHz$, which is much less than the designed clock frequency $32MHz$. This leads to offset to the common-mode feedback circuitry in OPAMP. Because of the nature of the switched capacitor common mode feedback circuitry, leakage current through open switches discharges the small capacitor that stores the common-mode voltage level. If the small capacitor is not frequently recharged, the common-mode voltage is drifted. In our design the capacitor in common-mode

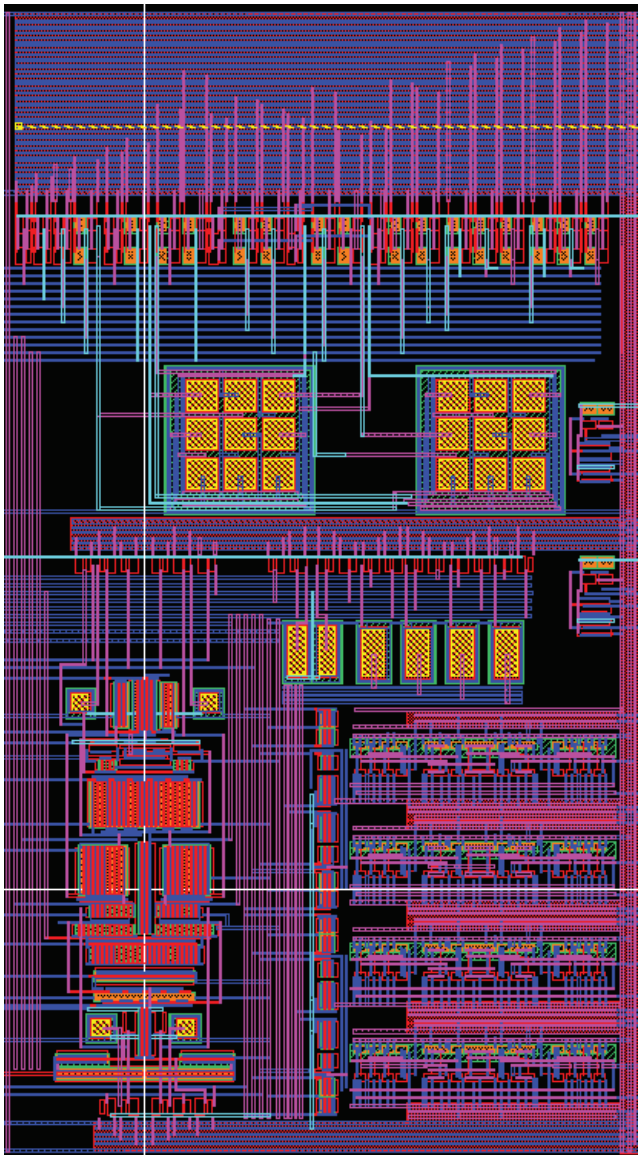

Figure 6.16: Layout of ADC

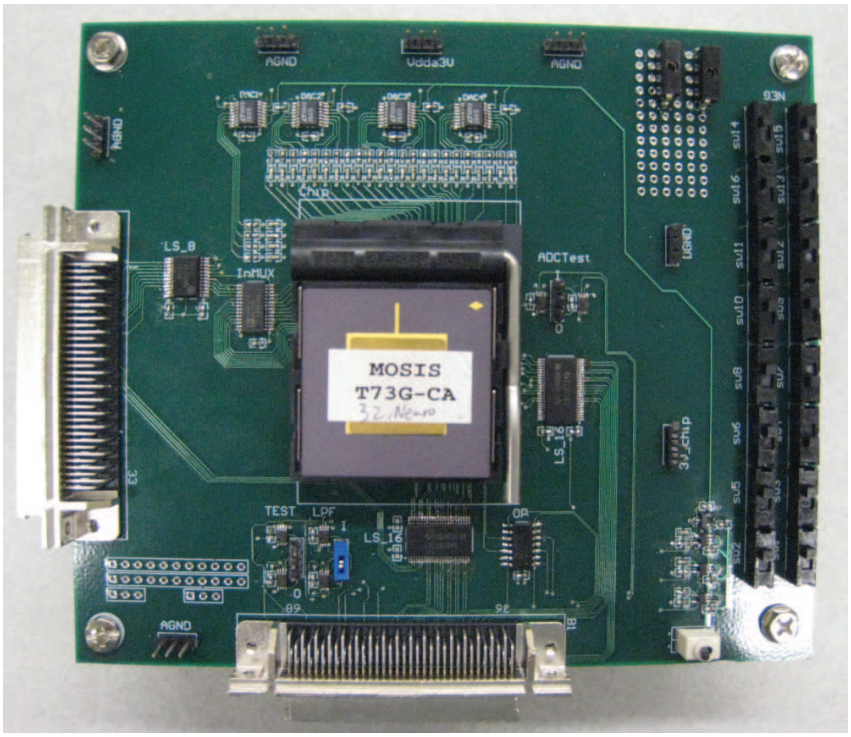

Figure 6.17: Photo of the interface test board

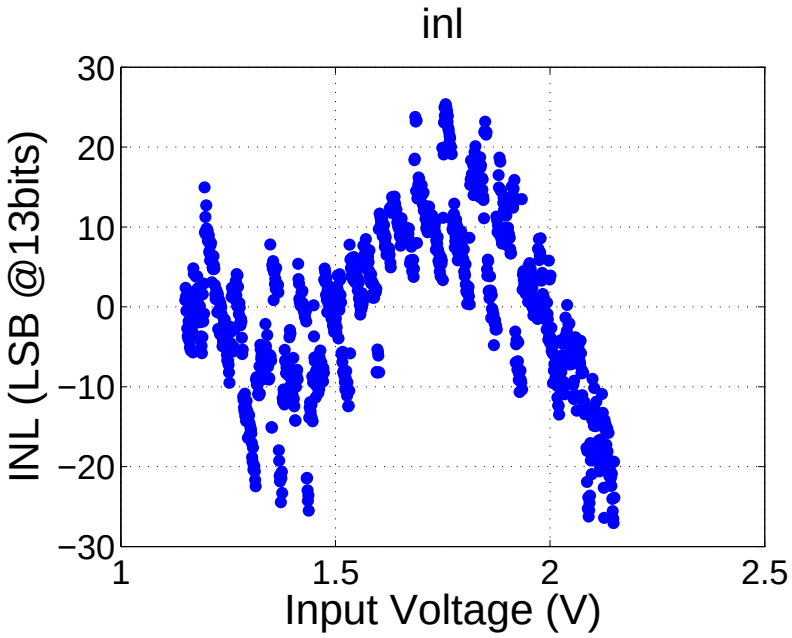

Figure 6.18: Measured INL of designed ADC

feedback circuit is selected to be $100fF$ for speed consideration. Assuming $1pA$ of leakage current, the common-mode voltage is drifted for $1.6mV$ in 16 cycles of $100KHz$ clock, which is over 13 LSBs under 13 bits resolution.

Second, the design assumed 10 bits resolution from the extended counting stage, which greatly relies on component matching. With careful layout consideration, the CMOS technology can achieve $8-10$ bits matching between capacitors. In our design, the capacitor arrays are laid out with identical unit capacitors with common-centroid structure. However, parasitic capacitance originates from routing metals that pass through the capacitor are not considered [40]. Dummy capacitor cells are also not employed, therefore the middle capacitor in the common-centroid structure experiences offset with those in the outer layer. The lack of consideration in layout along with technology limits might affect the measurement result.

6.4 Conclusion

Extended counting analog-to-digital converter (ECADC) combines the accuracy of delta-sigma modulation and the speed of algorithmic conversion. This conversion architecture is shown to be useful in multi-channel sensory applications, where both resolution and speed are demanded. This chapter presents a design of a 13 bit ECADC for 32 neural recording channels. Several power optimizing methods are described. The designed converter achieves a resolution of 13 bits and a sampling frequency of $512kHz$. With $3.3V$ supply, the total power consumption is estimated to be $7mW$. The designed ADC is fabricated through AMI $0.5um$ CMOS process. Fabricated chip is characterized with custom designed test setup. Measurement result is provided and discussed. The proposed extended counting ADC structure displays its advantage in integrating with the front-end readout system described in the previous part.

Part IV

Conclusions

Chapter 7

Conclusions and Future Plans

7.1 Conclusions

Front-end readout system for a innovative semiconductor scintillator radiation detector is designed and implemented. The novel detector produces high energy radiation electron-hole pairs in a direct-gap semiconductor material that subsequently undergo interband recombination, producing infrared light to be registered by a photo-detector. To measure the optical response of pixelized detector, an application specific integrated circuit has to be integrated with the array of detectors.

The system includes a charge sensitive amplifier (CSA), a semi-Gaussian pulse shaping filter and a peak detector. CSA integrates the charge signal from photo-detector into a small capacitor, thus converts charge signal into voltage signal. Semi-Gaussian pulse shaping filter conditions output signal from CSA, increases signal-to-noise ratio of the overall system. The pulse shaping filter converts output signal of CSA into a semi-Gaussian shape pulse with its amplitude proportional to input charge. Peak detector captures the peak amplitude of the output pulse from shaping filter.

This work presents a design of a low-noise charge sensitive amplifier. Design challenges when facing large parasitic capacitance are discussed and analyzed. For optimization of the performance and increased sensitivity of readout circuitry, we have devised an optimization technique that incorporates accurate flicker noise model. Designed CSA achieves high sensitivity at low power consumption. In addition, a current-mode preamplifier designed based on trans-impedance amplifier is also presented. The current-mode preamplifier doesn't use feedback, thus it can be used in applications with fast event rate. However, its noise performance is worse than CSA.

Design of a large time constant semi-Gaussian pulse shaper is presented. Use of current mirror ICON cell alleviates the requirement of large RC, which take large silicon area to integrate on-chip. A two-phase peak detector is also designed and simulated. This work also presents a design of an adaptive front-end readout system. The proposed system provides ability to minimize noise with variability in the photodiode and readout electronics. The adaptive control block automatically adjusts read out threshold based on the output noise level, thus gives the system potential for further programmability.

The designed front-end readout system was implemented with AMI 0.5 μm CMOS process through MOSIS. The fabricated chip was characterized with custom designed test interface board. Several experimental measurement results are presented.

For analog-to-digital conversion, which is the last component of the front-end readout system, this work presents a design of extended counting analog-to-digital converter (ECADC). The ADC was originally designed for a 32-channel low-noise low-power neural recording system. However, its ability to compromise among speed, power and resolution makes it a suitable candidate for multi-channel sensory application. Several design issues regarding power consumption and size are

proposed. An interesting technique that reduces power consumption by about 40% is developed. The preliminary prototype of the ADC along with 32 neural recording channels are implemented using AMI 0.5μm CMOS technology. Its functionality has been tested, measurement results are reported and discussed.

In summary, a front-end readout system for novel semiconductor scintillator radiation detector is proposed and designed. The designed readout system is implemented with CMOS process. Fabricated ASICs are characterized and measurement results are reported.

7.2 Future plans

Since the proposed detector employs several innovative techniques, the characteristic of the detector needs to be fully studied. More experiment tests should be conducted to provide more general information of the scintillation detector. Noise parameters can also be extracted from these experiments to optimize noise performance in design of integrated read out system.

A significant improvement in the detector side is that it is possible to further reduce the parasitic capacitance into 0.5 pf by reducing the pixel size to $0.1mm$ x $0.1mm$. In the theoretical analysis, we are using approximation that the noise will be dominated by the detector noise and the input MOS transistor noise. While, the detector noise is independent of the detector capacitor, noise contribution of input MOS transistor is scaled by the detector capacitance. By reducing the size of the pixel, the leakage current and detector capacitance will be scaled directly with the area. This will reduce both terms in the equivalent noise charge, and theoretical limit for 50 pF input capacitance ($1mm$ x $1mm$ pixel) can be reduced from 1000 electrons to 20 electrons in the case of 0.5 pF detector capacitance($0.1mm$ x $0.1mm$ pixel). The pixelation of the detector would therefore lead to significantly lower

detectable charge.

In the same time, further experiment test of fabricated integrated read out system needs to be conducted. Based on the test results, design should be iteratively revised until it meets both accuracy and speed requirements. Actual noise measurement results of a single transistor from the targeted need to obtained, so that CSA can be optimized with a more accurate noise model. The current test interface board has problems when testing detector with readout ASIC together. Better solution of connecting detector with readout system needs to be investigated. ASIC implementation of the proposed adaptive filtering system is needed to prove effectiveness of the concept. Effort is also required to integrate ADC with multiple channels of analog section of readout system on the same die.

The extended counting ADC needs to be re-optimized for better measured resolution result. Layout techniques to reduce mismatches need to be employed as much as possible. Switch capacitor configurations which help to reduce offset effect of OPAMP also required to be implemented. A better test structure should be designed to incorporate high frequency clock.

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