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Defect studies in 4H- Silicon Carbide PVT grown bulk crystals, CVD grown epilayers and devices

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Abstract of the dissertation

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Silicon Carbide [SiC]which exists as more than 200 different polytypes is known for superior high temperature and high power applications in comparison to conventional semiconductor materials like Silicon and Germanium. The material finds plethora of applications in a diverse fields due to its unique properties like large energy bandgap, high thermal conductivity and high electric breakdown field. Though inundated with superior properties the potential of this material has not been utilized fully due to impeding factors such as defects especially the crystalline ones which limit their performance greatly. Lots of research has been going on for decades to reduce these defects and there has been subsequent improvement in the quality as the diameter of SiC commercial wafers has reached 150mm from 25mm since its inception.

The main focus of this thesis has been to study yield limitingdefect structures in conjunction with several leading companies and national labs using advanced characterization tools especially the Synchrotron source. The in depth analysis of SiC has led to development of strategies to reduce or eliminate the density of defects by studying how the defects nucleate, replicate and interact in the material. The strategies discussed to reduce defects were proposed after careful deliberation and analysis of PVT grown bulk crystals and CVD grown epilayers. Following are some of the results of the study:

[1] Macrostep overgrowth mechanism in SiC was used to study the deflection of threading defects onto the basal plane resulting in stacking faults. Four types of stacking faults associated with deflection of c/c+a threading defectshave been observed to be present in 76mm, 100mm and 150mm diameter wafers. The PVT grown bulk crystals and CVD grown epilayers in study were subjected to contrast studies using synchrotron white beam X- ray topography [SWBXT]. The SWBXT image contrast studies of these stacking faults with comparison of calculated phase shifts for postulated fault vectors by macrostep overgrowth of surface outcrops,

has revealed faults to be of four types of which one of the following are discussed in detail: (a) Shockley faults

The fault vector were determined by taking into account the contrast from stacking faults in SWBXT undergoing phase shift as the X-ray wave fields cross the fault plane. The deflected dislocations onto the basal plane were responsible for the stacking faults and were observed to be detrimental to the devices grown on them as they replicate to the epilayer. In the wafers studied at different stages of the SiC crystal boule resulted in reduction of threading defects as they at certain stage get deflected out of the crystal causing drop of defects density.

[2] A novel technique known as the Ray Tracing Simulation was used to determine the sense of c/c+a dislocations obtained via Grazing- Incidence X-ray Topography. Determination of the complete sense and burgers vector of these dislocations was very important to augment our proposed models on stacking faults associated with these defects. Orientation contrast mechanism in X- ray diffraction topography was previously determined to be the dominant factor in SiC by our group and the same principles were used for the simulation. The results were surmised after extensive comparison between experimental and simulation images for the c+2a defects.

[3] With the BPD density down to a record level of few hundred per square centimeter in several wafers in multiple regions made it possible to observe the conversion of sessile Threading Edge Dislocations [TED] to glissile BPDs with this repeating multiple times. Previously the high density of Basal Plane Dislocations [BPD] prevented from discerning the details accurately in the SiC images taken by SWBXT. The contribution of SWBXT in accurately categorizing the nature of dislocations in SiC has enabled the crystal growth community to incorporate strategies to mitigate their influence. One of them has been recognizing BPDs as deformation induced defects which have led to the development of strategies to reduce stress imperative for the motion of BPDs to levels below critical resolved shear stress. This in turn has provided an opportunity for last five years to resolve important defect interactions in the crystals with one of them being the operation of single- ended Frank Read source for the first time in SiC.

[4] Failure analysis of SiC bipolar devices using SWBXT and correlation with defect density has been studied to determine how the defect density affect breakdown voltage of high power junction diodes. It was observed that the screw dislocation density unlike in failure analysis studies performed previously did not affect the breakdown voltage for these Junction Barrier Schottky (JBS) rectifiers. The defects that were detrimental were the triangular defects, stacking faults and micropipes in bipolar devices observed on 4H- SiC patterned wafers.

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List of Acronyms

XRT	X- ray Topography
SiC	Silicon Carbide
AFM	Atomic force microscope
BPD	Basal Plane Dislocations
CVD	Chemical Vapor Deposition
FWHM	Full Width at Half Maximum
HRXRD	High- resolution X- ray Diffraction
MP	Micropipe
PD	Partial Dislocations
PVT	Physical Vapor Transport
REDG	Recombination enhanced dislocation glide
SEM	Scanning Electron Microscope
SF	Stacking Faults
SWBXT	Synchrotron white beam X- ray Topography
TED	Threading Edge Dislocation
TEM	Transmission Electron Microscope
TSD	Threading Screw Dislocation
JBS Rectifiers	Junction Barrier Schottky Rectifiers
NIC	Nomarski Interference Contrast

List of Symbols

μ	shear modulus (J/m^2)
γ	surface energy, or stacking fault energy (J/m^2)
ν	Poisson's ratio
χ_h	electrical susceptibility
ξ_h	extinction length
σ	stress (N/m^2)
ε	strain
b	Burgers vector (m)
u	displacement vector (m)
s	wave vector (m^{-1})
n	plane normal
l	line direction of the dislocation
g	reflection vector
R	stacking fault vector (m)
(uvw)	factional coordinates of atom in the unit cell
(hkl)	miller indices
F_{hkl}	structure factor of (hkl) reflection
f	atomic scattering factor
Φ_0	incident angle (angle between incidence beam and sample surface)
Φ_h	exit angle (angle between exit beam and sample surface)
r_e	classical electron radius (m)
λ	wavelength (m)
V	unit cell volume (m^3)
K	equilibrium coefficient

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Dedicated To
My Parents and Brother

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Publications:

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- H. Wang, F. Wu, *S. Byrappa*, S. Sun, B. Raghothamachar, M. Dudley, E. K. Sanchez, D. Hansen, R. Drachev, S. G. Mueller, and M. J. Loboda, *Basal plane dislocation multiplication via Hopping Frank- Read source mechanism in 4H- SiC*, in Appl. Phys. Lett., 100, 172105 (2012); doi: 10.1063/1.4704679
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- M. Dudley, *S. Byrappa*, H. Wang, F. Wu, G. Choi, B. Raghothamachar, E.K. Sanchez, D. Hansen, R. Drachev and M.J. Loboda, *Analysis of Dislocation Behavior in Low Dislocation Density, PVT- grown, Four- Inch SiC single Crystals*, in Mater. Res. Soc. Symp. Proc. 1246, 1246-B02-02.
- M. Dudley, H. Wang, F. Wu, *S. Byrappa,* S. Shun, B. Raghothamachar, E.K. Sanchez, G. Chung, D. Hansen, S.G. Mueller, and M.J. Loboda, *Synchrotron X- ray Topography Studies of the Evolution of the Defect Microstructure in Physical Vapor Transport Grown 4H- SiC Single Crystals*, in *ECS Trans. (*2013), 58(4): 315-324; doi:10.1149/05804.0315ecst
- M. Dudley, *S. Byrappa*, H. Wang, F. Wu, B. Raghothamachar, G. Choi, S. Sun, E. K. Sanchez, D. Hansen, R. Drachev, S. Mueller, and M. J. Loboda, *Formation Mechanism of Stacking Faults in PVT 4H- SiC Created by Deflection of Threading Dislocation of Threading Dislocations with Burgers Vector c+a*, in Silicon Carbide, III-Nitrides, and Related Materials (2010), Mater. Sci. Forum, 679-680, 269-272.
- H. Wang, *S. Byrappa*, F. Wu, B. Raghothamachar, M. Dudley, E. K. Sanchez, D. Hansen, R. Drachev, S. G. Mueller and M. J. Loboda, *Basal Plane Dislocation Multiplication via the Hopping Frank- Read Source Mechanism and Observations of Prismatic Glide in 4H- SiC*, in Silicon Carbide and Related Materials (2012), Mater. Sci. Forum, 717-720, 327-330.
- F. Wu, H. Wang, *S. Byrappa*, B. Raghothamachar, M. Dudley, P. Wu, X. Xu, I. Zwieback, *Characterization and Formation Mechanism of Six Pointed Star- Type Stacking Faults in 4H- SiC*, in Journal of Electronic Materials 2013, DOI: 10.1007/s11664-012-2379-9.
- F. Wu, *S. Byrappa,* H. Wang, Y. Chen, B. Raghothamachar, M. Dudley, E.K. Sanchez, G. Chung, D. Hansen, S.G. Mueller, and M.J. Loboda, *Simulation of Grazing- Incidence Synchrotron X- ray Topographic Images of Threading Dislocations in 4H- SiC*, in Mater. Res. Soc. Symp. Proc. 1433(2012), DOI: 10.1557/opl.2012.1050.

- H. Wang, F. Wu, *S. Byrappa*, S. Shun, B. Raghothamachar, M. Dudley, E.K. Sanchez, G. Chung, D. Hansen, S.G. Mueller, and M.J. Loboda, *Combined Application of Section and Projection Topography to Defect Analysis in PVT- Grown 4H- SiC*, in Mater. Res. Soc. Symp. Proc. 1433 (2012), DOI: 10.1557/opl.2012.1142.
- H. Wang, S. Shun, *S. Byrappa*, S. Shun, B. Raghothamachar, M. Dudley, E.K. Sanchez, G. Chung, D. Hansen, S.G. Mueller, and M.J. Loboda, *Quantitative Comparison Between Dislocation Densities in Offcut 4H- SiC Wafers Measured Using Synchrotron X- ray Topography and Molten KOH Etching*, in Journal of Electronic Materials 2013, DOI: 10.1007/s11664-013-2527-X.
- M. Dudley, H. Wang, F. Wu, *S. Byrappa,* S. Shun, B. Raghothamachar, E.K. Sanchez, G. Chung, D. Hansen, S.G. Mueller, and M.J. Loboda, *Synchrotron Topography Studies of Growth and Deformation- Induced Dislocations in 4H- SiC*, in Mater. Res. Soc. Symp. Proc. 1433 (2012), DOI: 10.1557/opl.2012.1141.
- F. Wu, H. Wang, *S. Byrappa*, B. Raghothamachar, M. Dudley, E.K. Sanchez,.D. Hansen, R. Drachev, S.G. Mueller and M.J. Loboda, *Synchrotron X- ray Topography Studies of Propogration and Post- Growth Mutual Interaction of Threading Growth Dislocations with c-component of Burgers Vector in PVT- Grown 4H- SiC*, in Silicon Carbide and Related Materials 2011, Materials Science Forum, 717-720, 343-346.
- N. Zhang, Y. Zhang, B. Raghothamachar, *S. Byrappa*, G. Choi, E.K. Sanchez, D. Hansen, R. Drachev, and M.J. Loboda, *Characterization of 100 mm Diameter 4H- SiC crystals With Extremely Low Basal Plane Dislocation Density,* in Materials Science Forum, 645-648, pp.291-294.
- H. Wang, *S. Byrappa,* F. Wu, B. Raghothamachar, M. Dudley, P. Wu, I. Zwieback, A. Souzis, G. Ruland, and T. Anderson, in Jour. of Appl. Phys., 2013(to be submitted).

Fields of Study

This section summarizes my major research accomplishments. Many aspects of the defect structures in silicon carbide bulk crystals, epilayers and devices have been studied in depth. Based on the numerous results obtained during my research, the most significant accomplishments which are expected to have the biggest impact on the crystal growth process and the quest for defect density reduction as well as those constituting major contributions to techniques for characterization are summarized below.

1. Studies on both horizontally cut SiC wafers and axially slices cut parallel to the growth direction have revealed the existence of nc+ma (n, m are integers) type threading defects in SiC. The deflection of these threading defects by macrostep overgrowth mechanism causes two partials to be separated by the height of step riser. Depending on the direction of stress only one of the partials is able to glide while the other is sessile which causes large stacking faults in SiC. The contrast analysis studies of these faults on multiple reflections have revealed the fault vector to be of the type 1/3[01-10] type and are associated with the c+a defects.

2. Ray- Tracing simulation has been successfully used to simulate c+2a type defect in grazing topography geometry. This novel technique takes into account orientation contrast mechanism and enables to get both the sense of dislocation and Burgers vector magnitude. The c+2a defect has been identified accurately in axial cut slices and Burgers vector is of the type 1/3[2-423].

3. Single- Ended Frank Read mechanism for defect multiplication has been identified for the first time in SiC. The Basal Plane Dislocation converts to a Threading Edge Dislocation which reconverts back and this process repeats itself several times acting as a Single- Ended Frank Read source. The low density of BPDs in the recent wafers enabled one to discern these kinds of features for the first time in SiC which will definitely aid in reduction of defects in SiC.

4. Failure analysis of high performance and high voltage diodes has been carried out in SiC using SWBXT studies. Both bare and patterned wafers were studied to figure out how the defects density affected the breakdown voltage of these devices. The studies carried out in more than 150 devices revealed that the screw dislocation density did not have significant impact on the device performance of Junction Barrier Schottky (JBS) rectifiers unlike Triangular defects or Stacking faults which caused the devices to fail immediately.

1. Introduction

Single crystal SiC is one of the most promising semiconductor materials among others such as Gallium Arsenide (GaAs), Gallium Nitride (GaN), Silicon (Si) etc. due to excellent mechanical, chemical, thermal and electrical properties compared to conventional ones. Where Silicon cannot be used at temperature above 200^0C and GaAs at above 150^0C, SiC can be used at temperatures above 1000^0C making it the most widely used material for realizing high temperature and high power applications.

An interesting phenomenon of this material which was discovered nearly many decades ago was the one- dimensional disorder resulting in many structures of different stacking sequence [1]. This came to be known as 'Polytypism' and ever since has fascinated material scientists in delving into this field of study. Since its discovery [2], more than 200 different polytypes of SiC have been determined [3] finding plethora of different applications. The first structure which was discovered was 15R where same Si-C double layers repeat every 15 layers, which was labeled to be type I. The second was the hexagonal structure with six- layer repetition labeled as type II. Third was again hexagonal structure with four- layer repetition labeled as type III and the fourth was cubic structure labeled as type IV. Many scientists have given different notations for representing the polytypes but the most commonly used notation for many decades has been that of Ramsdell [4] which makes no distinction between layers consisting of untwinned tetrahedra and those with twinned tetrahedra. In this type of representation at first Si-C double layers is taken into consideration and the polytype is differentiated giving the order of periodicity, n, together with the Bravais lattice of the crystal. For example if we consider Wurtzite structure which has the sequence αAϒC…, the order of periodicity, n, is 2 and the periodicity will be $c=2d_{0002}$, where d_{0002} is the interlayer spacing. The Bravais lattice for Wurtzite structure is hexagonal (H), this will be represented as 2H in Ramsdell notation. 3C-SiC is the only polytype out of infinite variations which shows cubic symmetry, so this is known as β-SiC. All the other polytypes which have non-cubic symmetry are collectively known as α-SiC.

Silicon Carbide like other semiconducting materials, such as Si, Ge, GaAs, Diamond etc is made up of corner sharing tetrahedral [1,3] i.e. tetrahedral bonding between the Silicon and Carbon atoms with a Carbon atom at the centroid of four Silicon atoms as shown in fig. 1.

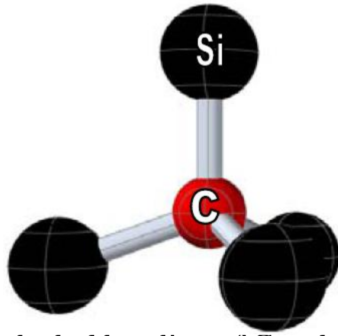


Figure 1: Tetrahedral bonding of C and Si atoms in SiC.

In the SiC tetrahedral C-axis coincides with one of the Si-C bonds, the triangular base of the tetrahedron opposite to this bond is normal to the C-axis and defines a C-plane. The Carbon-Silicon bonds are very strong, with 88% being covalent bonds and the remaining 12% ionic. Like any other biatomic semiconductor materials, Silicon Carbide has two distinct polar faces, Si-face(0001) and C- face(000-1), and several non- polar faces with the most common being a-plane(11-20) and m- plane(1-100) as shown in figure 2.

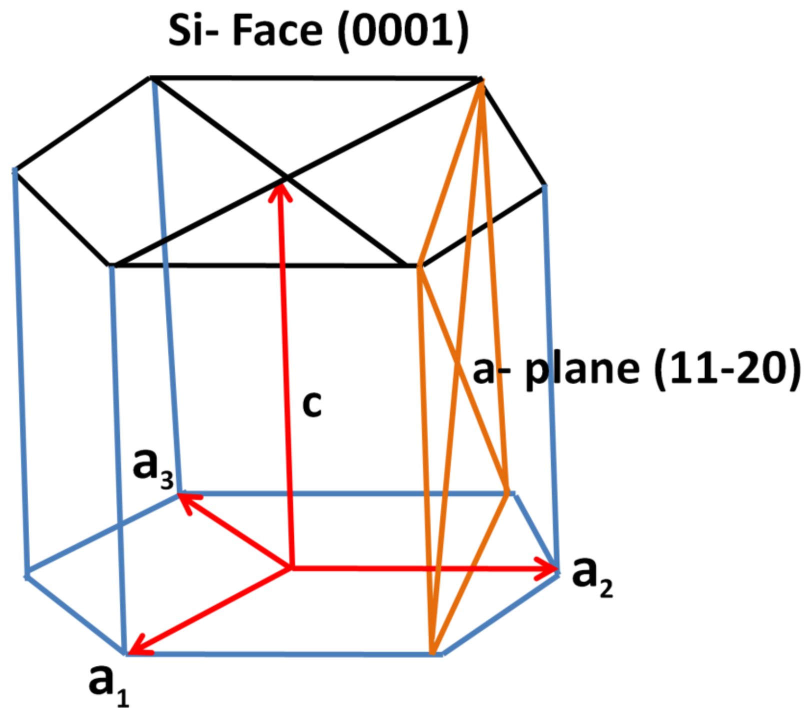


Figure 2: Hexagonal structure of a unit cell for 4H-SiC and 6H-SiC

The carbon atom at the center of the tetrahedron divides the height in a 3:1 ratio, i.e. the distance from top Silicon atom is almost three times larger than its distance from the base triangle. The edges of the base triangle in the SiC tetrahedron are along the <11-20> directions. The stacking of these corning sharing tetrahedra on one top of another is strictly based on two rules-

(a) A tetrahedron is followed by another one of the same variant but with the preceding subscript
(b) A tetrahedron is followed by the twinned variant of a preceding subscript

Keeping these two rules in mind an infinite arrangement of SiC tetrahedrons can be stacked on one top of another with each one forming a different polytype [4]. Thus, in an assembly of corner- sharing tetrahedrons they can occupy one of the three sites indicated by A, B and C. The tetrahedron shown in Figure 1 where a C atom is bonded to four other Si atoms has three- fold symmetry about the c- axis. Therefore one can get a different variant by rotating the tetrahedron by 180^0 around c- axis as shown in Figure 3 (a) - (b). By doing the rotation we get different variants denoted by A', B' and C' which are twinned as compared to untwinned tetrahedrons denoted by A, B and C. Figure 4 and 5 shows the stacking sequence of 4H- and 6H- SiC which have been arranged based on the two stacking rules showing both twinned and untwinned tetrahedrons which are rotated by 180^0 around the c- axis.

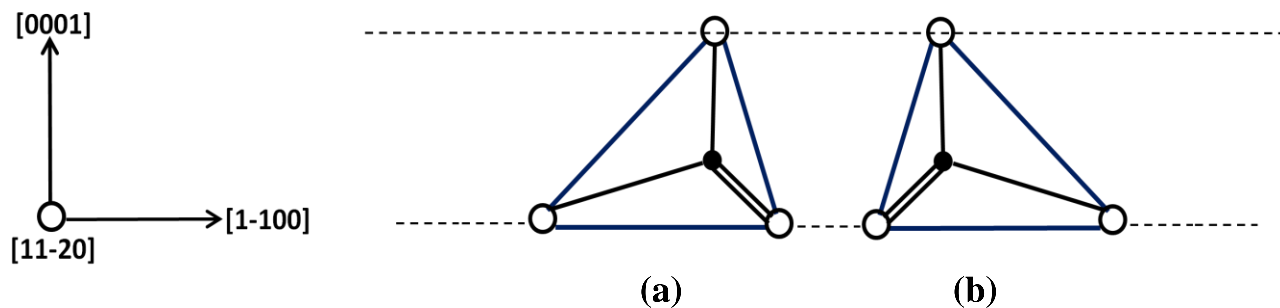


Figure 3. (a) shows projection of twinned tetrahedron on {11-20} plane and (b) shows untwinned tetrahedron that is rotated 180^0 about the c- axis.

The tetrahedron in in SiC has trigonal symmetry about the c- axis, Miller- Bravais indices are used to represent the planes and directions in discussing SiC polytypes. Thus, the c- axis is set parallel to the [0001] direction making the c- plane parallel to (0001). Usually two

tetrahedrons (twinned and untwinned) are related to each other by mirror symmetry in the {1-100} plane.

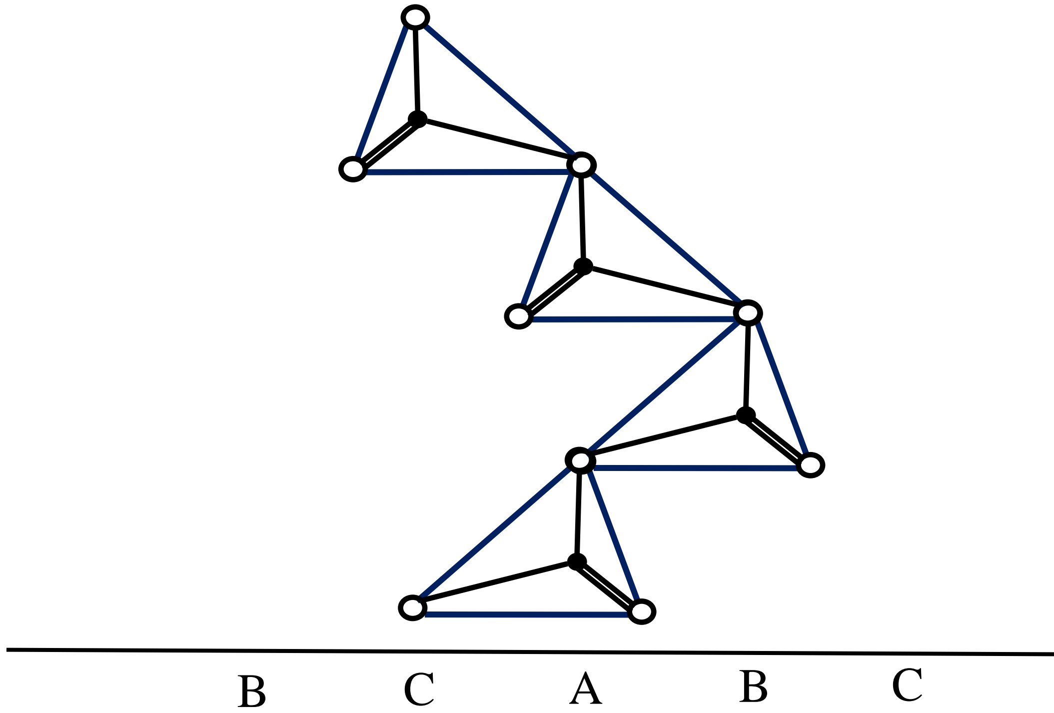


Figure 4: shows the projection of 4H- SiC on (11-20) plane, the Si- C bonds are shown in each tetrahedron.

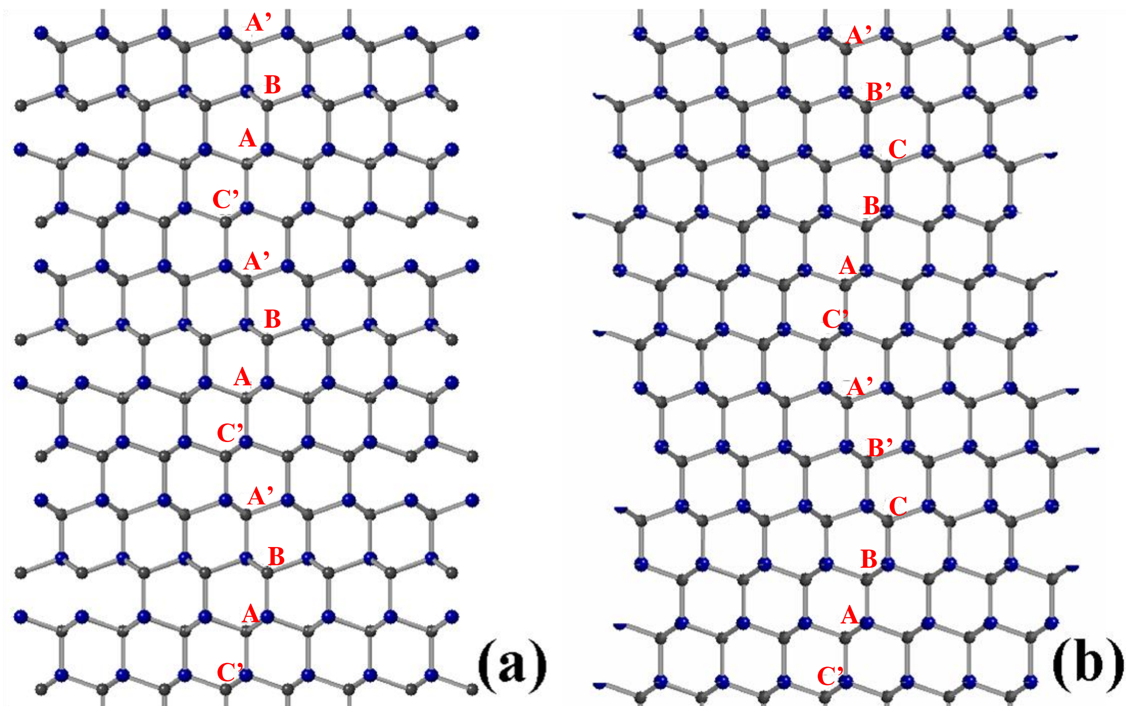


Figure 5 Projection of 4H-SiC (a) and 6H-SiC (b) structure into (11-20) plane. Small and large balls indicate C and Si atoms, respectively. The stacking sequences are "ABA'C'…" and "ABCB'A'C'…" for 4H and 6H-SiC, respectively

1.1. Crystal Growth of Silicon Carbide

1.1.1. Substrate growth by Physical Vapor Transport (PVT)

Silicon Carbide crystal growth is different compared to other conventional semiconductor crystals, as melt growth techniques used for others cannot be incorporated in SiC. It is not easy to melt SiC under achievable process conditions and because of the phase equilibria in SiC, it rather sublimes before melting. The calculated values show that stiochiometric SiC would melt only at above 10000 atm and 3200^0C [5]. Because of these reasons SiC bulk crystals are usually grown by physical vapor methods which were developed during 1950s but modified and commercially used to grow crystals only in 1980s. High growth temperatures are required for these sublimation techniques, they are easy to implement but over large substrate areas it becomes difficult to control the process. To grow SiC bulk commercially three vapor techniques have been used:

(a) Acheson process[6]
(b) Lely process[7]
(c) Modified Lely process[8,9]

In the physical vapor methods the SiC source placed in hot zone of the growth furnace undergoes sublimation. By diffusion and advection the vapor species is transported to cooler region of the furnace housing the SiC seed crystal. Source materials is usually composed of SiC powder, Si or C powders mechanically mixed or crystalline SiC. Single crystal SiC is formed by the deposition of supersaturated vapor species, growth proceeds by vapor transport of C- or Si-bearing species from source. The growth parameters for bulk SiC by sublimation methods is usually between 2100- 2400^0C, growth pressure less than 20 Torr, and temperature gradient between the source and seed ranges from 20-35^0C/cm. Typical growth rates for SiC is 0.5-5mm/hr [10]. At this moment the largest commercially available 4H-SiC and 6H-SiC is 100mm which are grown by many companies like Dow Corning, Cree Inc., II-VI etc. Figure 6 shows how the size of SiC wafers have evolved over the years with 25mm grown in 1992 to the current

one which is 150mm. Efforts are being made to grow bulk crystals larger than 150mm so as to increase the active area to incorporate more devices onto it.

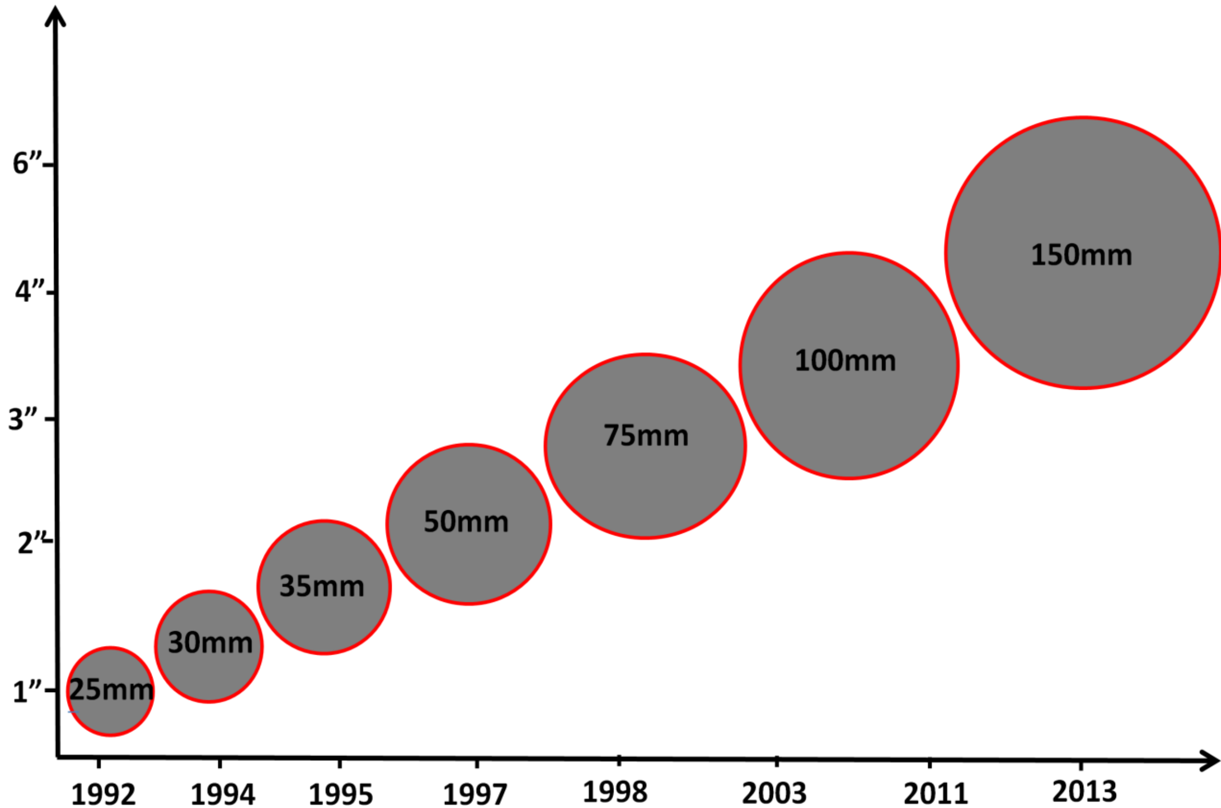


Figure 6: Increase in 4H-SiC commercial wafer diameter versus the year.

1.1.2. Epilayer growth of SiC by Chemical Vapor deposition

Chemical vapor deposition is the most popular technique for the epitaxial growth in Silicon Carbide crystals. Thin crystalline layers from the gas phase are deposited onto the substrate to improve the quality of bulk material and grow complicated devices on it. Mixture of gases are injected into the growth chamber housing the SiC substrate at temperatures around 1300^0C. Generally as source gases for Silicon, Silane is injected and a hydrocarbon such as Propane or Methane is used as the source for Carbon. Nucleation is typically favored at steps, crevices or defects on the surface of the substrate, because these sites have the lowest potential, allowing the nucleated species to attain minimum energy. Epitaxial films grown on on- axis

substrates can convert nearly all micropipes and basal plane dislocations into threading edge and screw dislocations, which are detrimental to devices, whereas on large misorientations, tilted 3^0-8^0 toward a-axis, substrate defects are propogated into the epitaxial layer [11, 12]. There are various Chemical Vapor Deposition methods available, in this report only Homoepitaxial growth is discussed. Homoepitaxial growth is usually carried out on α-SiC (4H-, 6H-, 15R-, 21R-SiC) using off-oriented Silicon Carbide because the quality of films obtained by growing on (0001) face is poor and this technique is called Step- Controlled Epitaxial growth. In this the epitaxial layer will replicate the stacking order of the substrate and the wafer is usually misoriented by 3-8^0 from the basal plane to control the morphology of the deposited layer. In the conventional CVD techniques higher growth rates cannot be obtained due to which boule production becomes difficult, to overcome this problem high- temperature CVD (HTCVD) process is used which is an improved version and yields in thicker films and also higher growth rates. The setup of high temperature CVD is similar to that of modified Lely method, that it has the similar crucible used in Lely method with holes at the bottom. SiC substrate is placed at the top in the susceptor and the gaseous reactants by diffusion and advection is passed to the top from bottom through the holes. One of the main advantages of this method is the homogeneity of epitaxial films grown on the substrates and longetivity of the growth due to which maximum deposition of the gaseous components becomes possible. Temperature also plays a very important role as it greatly affects the quality, growth rate and also polytype of the epitaxial film. Deposition of 3C- SiC polytype is usually at the temperature range 1300-1500^0C, irrespective of the substrate polytype used. This is due to the low surface mobility which prevents the reactants from reaching step edges. This is the single main reason, growth temperatures for 4H-SiC and 6H-SiC epitaxy typically ranges from 1500-1800^0C, because temperatures above 1600^0C make the 3C- SiC polytype unstable and shift the equilibrium toward 4H-SiC and 6H- SiC [13]. The temperature again plays an important role on the growth rate of the epitaxial film, higher growth rates are usually achieved at higher temperatures, the quality of the film, for temperatures greater than 1750^0C, degrades toward producing polycrystalline SiC [14].

1.2. SiC Properties

SiC is a wide bandgap semiconductor (2.2- 3.4 eV) that exists in a wide variety of polytypes and was one of the first materials to be investigated for electronic applications. The importance of SiC is based upon its durability and performance at high temperatures (>300^0 C).

SiC as a semiconducting material finds application in multiple sectors in the market especially as a substrate for fabricating Light Emitting Diodes (LEDs) because of smaller lattice mismatch (~ 3.4%) compared to other materials such as Sapphire (~ 16%). The semiconducting properties of SiC were realized by William Shockley himself many decades ago. As Si- based power devices especially in high- power and high efficiency applications are approaching material limits, this has prompted lot of research to find alternatives of which SiC has been confirmed to be a promising material.

SiC as a material has several advantages because of very important properties such as high- operating electric field, high- operating temperature, high- saturated electron drift velocity, high- switching frequency, high- breakdown voltage, high- thermal conductivity and low losses which make it an ideal material for high- temperature, high- power and high- frequency applications. In addition to these interesting properties it is easy to dope this material and grow Silicon dioxide (SiO_2) layer. Some of the important properties of SiC are discussed below:

Mechanical and Chemical Properties: SiC is one of the hardest materials known with a Young's modulus of 424 GPa [15]. It is chemically a very inert material and does not usually react with other materials at room temperature. Only efficient etching material known to react with SiC is KOH at really high temperature (~400- 600^0 C). It is very difficult to diffuse dopants into the material like Si therefore one needs to either grow or implant dopants into SiC. It sublimes at temperature above 1800^0 C.

Bandgap: It is known as a wide bandgap material because the bandgap varies between 2.39eV to 3.4 eV [15]. The most commonly used polytypes in the market are 4H- and 6H- SiC and the wide bandgap makes it a material of choice for high- temperature, high- power and high-frequency applications. A limitation in Si- based devices is the thermal ionization of electrons from valence to conduction band which is not a problem in SiC- based devices because of the bandgap advantage which again helps in high- temperature applications.

Critical Field: This property explains the larger breakdown field in SiC as compared to Si. The high breakdown electric field strength of SiC explains the high critical field due to which the devices fabricated from this material has high breakdown field making it an ideal material for several applications. The critical electrical field of SiC is around eight times higher than that of

Si, which makes SiC an excellent choice for power semiconductor devices. A SiC semiconductor die is much thinner due to its high dielectric strength and is doped to a much higher level, leading to lower losses.

Saturated Drift Velocity: For high- frequency devices it is the high saturated drift velocity that is more important as compared to breakdown electric field strength, which is almost twice that in Si. Due to the high drift velocity it is very useful in obtaining high channel currents especially for microwave devices, and this makes it an ideal material for high- gain solid- state devices.

Thermal Conductivity: This is another very important property for high- power and high-frequency applications. Increase in temperature affects the device properties by causing changes to physical properties of a device such as carrier mobility which decreases with increase in temperature. The thermal conductivity of SiC is higher than even materials such as Copper and many other metals at room temperature. Due to this property of SiC the heat generated during operation must be conducted away from the device and into the package. SiC has thermal conductivity about three times higher than that of Si. Therefore, heat dissipation by the losses can be conducted from within the semiconductor with a much lower temperature drop across the semiconductor material.

1.3. Applications of SiC

High- temperature, high- power and high- frequency applications: SiC is an ideal material for all these applications because of wide bandgap, high thermal conductivity and melting point. SiC material are compatible with many other materials such as AlN, GaN, TiC, GaAs etc. which makes many devices feasible when fabricated. SiC has been used in fabrication of many powerful devices such JFETs, MESFETs, MOSFETs, pn junction rectifiers, and storage capacitors. Several companies such as Cree Inc., GeneSiC and Infineon in the market provide most of these high performance devices. To improve the efficiency of devices fabricated on SiC it is important to reduce the defects density in SiC and increase the commercially available size of wafers in the market.

Optoelectronics: The wide bandgap of SiC makes them ideal candidates for far UV radiation detection. Commercially available devices include UV photodetectors, blue and violet

light emitting diodes. SiC can also be used as a laser material, it is potential waveguide substrates for nitride based optoelectronics. SiC is successfully utilized as a substrate for growth of several nitrides with potential usefulness for UV optoelectronics. A wide variety of optoelectronic devices can be fabricated by growing GaN on AlN as buffer layer to avoid cracks, which in turn is grown on SiC as the substrate material [15].

Gas, Chemical and Pressure Sensors: Due to large piezoelectric coefficients materials such as Si have been extremely useful for pressure and strain sensors. The current available operational range for these semiconductor pressure sensors is up to 500^0 C and the demand for sensors that can operate at temperatures above this for automotive and avionic applications make SiC one of the most promising materials. SiC is also a very well-known refractory material and the combination of semiconducting properties makes it a suitable material to integrate micro sensors, microactuators and integrated circuits on the same SiC substrate by using several methods simultaneously. SiC can be used as a pressure sensor because it can take advantage of SiC's thermal indifference and hardness that could operate in extreme temperature and pressure conditions such as inside an engine or turbine. Molecular species such as hydrogen, hydrogen sulfide and ethanol can be detected with thick, continuous catalytic metal gates on MOS capacitors. Certain reactions, such as, dissolution of saturated hydrocarbons occur at temperature above 350^0 C. The high temperature required for these reactions make SiC a likely candidate for semiconductor portion of the MOS structure comprising such as gas detectors.

Telecommunications: SiC finds application in manufacturing of antennas of low volume, low profile and low mass that are generally very useful for spacecrafts because of size and mass. SiC acts as a supporting material where the antennas operate at temperatures above 500- 800^0 C and SiC can operate in rugged conditions. Using SiC as the dielectric and support as well as the transmission material will eliminate any chance of buckling as there will be no thermal expansion mismatch. The robust nature of SiC makes it possible to make these thin, self-supporting, monolithic antennas of varying thickness. My modifying the surface of SiC substrates to create insulation regions of porous SiC, the material may be used in transmission lines. It is usually modified by photo- electrochemical technique in which porous- SiC is made electrochemically under illumination with light more energetic than the bandgap. The resolution

of a photo- electrochemical processing technique is around 0.5 μm, therefore antennas that are in wavelengths in the range of GHz or THz range maybe constructed using this technique [15].

1.4. Defects in SiC substrates and epilayers

Silicon Carbide being a much superior material compared to other conventional semiconductors is still not being used commercially on a large scale as others because of one single reason- high dislocation density which is affecting Silicon Carbide power electronics. For the grown-in defects, for example growth dislocations, their origins can usually be attributed to (a) the replication of pre-existing dislocations which thread the growth surface of the seed; (b) dislocation nucleation on either the seed interface or the moving growth interface through incorporation of inclusions or impurity; or (c) dislocation nucleation accompanying growth accidents (fluctuations in growth temperature or pressure or mechanical disturbance). For those defects which are created following growth, these typically arise due to the presence of thermal gradients which can generate shear stresses on active slip planes. In 4H and 6H-SiC the active slip planes are the basal planes and the shear stresses, which are associated with non-linear axial thermal gradients, can force basal plane dislocations (which can be readily nucleated at the boule edges or, in the case of PVT-grown SiC, at the interface between the polycrystalline periphery and the inner single crystal) to glide into the interior of the boule where they encounter a variety of obstacles including threading screw and edge dislocations, and grain boundaries.

Despite its high breakdown electric field, high thermal conductivity and wide bandgap its performance when used in making conventional power devices like MOS-based diodes, bipolar-mode diodes and thyristors and Schottkey contact based devices fails to achieve the desired limits at high temperatures, due to the presence of defects in the substrate which replicates into the epilayer [16]. Therefore understanding the defects present in Silicon Carbide right from its growth becomes imperative for the reduction of these dislocations which otherwise affect the performance of SiC crystals in different ways. Frequently observed dislocations in Silicon Carbide are screw dislocations (SDs) with different Burgers vector, basal plane dislocations (BPDs), threading edge dislocations (TEDs), stacking faults (SFs), low angle grain boundaries (LAGBs) etc. Some of the defects which nucleate into the epilayer as extended defects are micropipes, elementary screw dislocations, basal plane dislocations and stacking faults, each of which affect the device performance grown on the active areas of the substrate.

For the first time in 1992 it was realized that the presence of micropipes (MPs) reduces breakdown voltage of p-n junction diodes because of their hollow core nature by Koga et al. [17]. MPs were given the term “device killing defects”. After this lot of research was done on MPs focusing on how they affect the various devices and ways to get rid of them during growth. After this P.G. Neudeck et al. found pre- avalanche reverse- bias point failures in epitaxially grown p-n junction devices of 1mm^2 or larger in area [18]. The device performance can also be adversely affected by elementary SDs in substrate, Neudeck et al. observed this in 4H-SiC in which even the presence of one single SD reduced the breakdown voltage by 5-35%. The locations of these breakdown microplasms were exactly at the locations of these elementary screws and this was correlated by Synchrotron white beam X-ray Topography (SWBXT) studies [19]. The defect density of MPs have gone down considerably and the commercial substrates that companies like Dow Corning, Cree sell in the market are zero- micropipe density wafers. Though these defects have gone down, one more planar defect which is very detrimental to the device performance is the generation and expansion of stacking faults which has been reported to cause breakdown of voltage bringing down the efficiency of devices [20, 21]. Some of these common defects present in SiC will be reviewed in detail in the following paragraphs showing images from Synchrotron X-ray Topography, which is by far the most useful non-destructive characterization technique to study defects in semiconductor crystals. It is interesting to note that some of these defects interact with each other which also will be explained in detail in results section and the proceeding paragraphs.

1.4.1. Threading Screw Dislocations (TSDs)

The screw dislocations in SiC can be divided into two types: closed core screw dislocations and hollow core dislocations [also known as Micropipes or giant screw dislocations]. They have their line directions along the [0001] growth axis with Burgers vector being equal to nc where c is the lattice parameter along growth axis and n being an integer. Recent improvements in PVT grown methods have enabled the elimination of hollow core screws but the closed core screws exist in higher density. TSDs affect the performance of SiC devices greatly as they can replicate through the crystal boule to the epi affecting devices grown on them. Although KOH chemical etching is an effective way to determine the density of these screws in SiC, it is destructive and cannot reveal complete information of the dislocations like the SWBXT. Back reflection X- ray topography and Grazing Incidence X- ray Topography are

two important geometries that is commonly used for studying TSDs in SiC. Figure 7 (a) shows a back reflection image which consists several white dots of different diameters, b analysis showed the white dot marked M to be a micropipe and the ones in the vicinity to be closed core TSDs. Figure 7 (b) Shows a topograph taken from the same area by Transmission Geometry which also reveals the black curved lines corresponding to the BPDs.

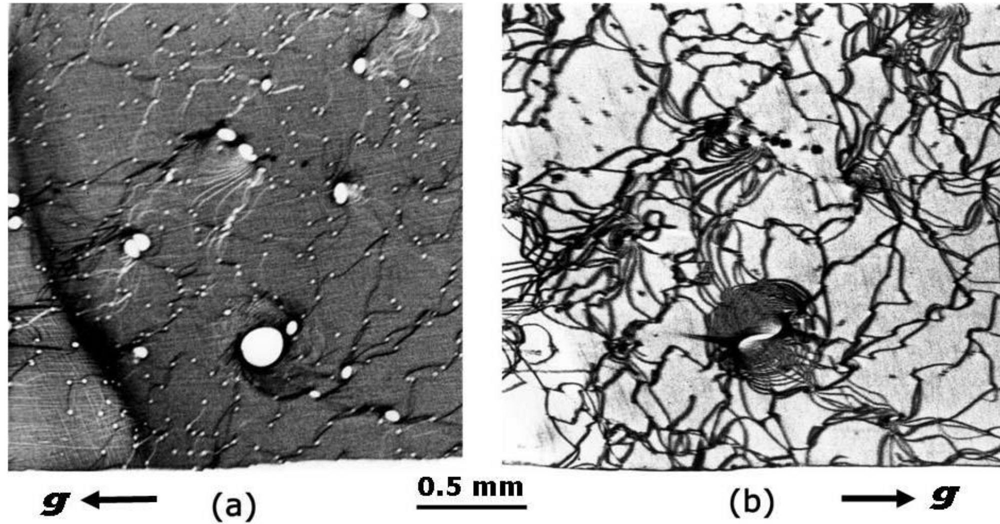


Figure 7 Typical back reflection X-ray topograph (a) and transmission X-ray topograph (b) showing SDs. Small white dots are elementary TSDs and large white dots are MPs. (after Vetter[22- 25])

There are various reasons for the nucleation of screw dislocations, Dudley et al. [23- 28] reported that incorporation of inclusions resulted in a pair of micropipes with opposite Burgers vector and this is one of the reasons for nucleation of screw dislocations. Also Sanchez et al. [23- 28] found, on on-axis epitaxy the density of SDs are a factor of 300 higher than that grown on off-axis epitaxy. This phenomenon was interpreted to be result of 2D nucleation as islands expand and coalesce with the neighboring ones, some of the bounding dislocations can have Burgers vector along c axis and are possible sites for nucleation of SDs. Based on this the density of SDs can be effectively reduced by incorporating step flow growth compared to conventional 2D nucleation growth. Step flow growth occurs at misoriented C-cut seeds resulting in nucleation of SDs. While in the off- axis growth the presence of large number of kinks provide energetically stable sites for adatoms and the growth is going on by expanding at these terraces.

When two SDs of the same sign are present very close to each other, their spirals spin without intersecting each other, known as cooperative spirals. Meanwhile when two SDs of opposite sign pair are in close proximity they annihilate and form a closed loop.

1.4.2. Micropipes

Micropipes also known as thegiant screw dislocations lying parallel to (0001) axis is given the term device killing defects as it completely negates the performance of device grown on them. The line directions along [0001] and for the value of $n \geq 2$ for 6H- SiC and $n \geq 3$ for 4H- SiC are immediately classified as micropipes. Figure 8 shows an image of a micropipe taken by back reflection X-ray topography which has been compared with an optical image in which the crystal has been etched using molten potassium hydroxide (KOH). They are hollow core in nature and this can be understood by Frank's theory that predicted their existence back in 1951 but was observed only in 90s. According to Frank a screw dislocation whose Burgers vector exceeds a critical value in crystals with large shear modulus will have a hollow core nature instead of regular closed core SDs. The equilibrium diameter D of these dislocations related to the magnitude of the Burgers vector b is given by

$$d = \frac{\mu \mathbf{b}^2}{\mathbf{4}\boldsymbol{\Pi}^2 \boldsymbol{\Upsilon}}$$

Where μ is the shear modulus and ϒ is the specific surface energy.

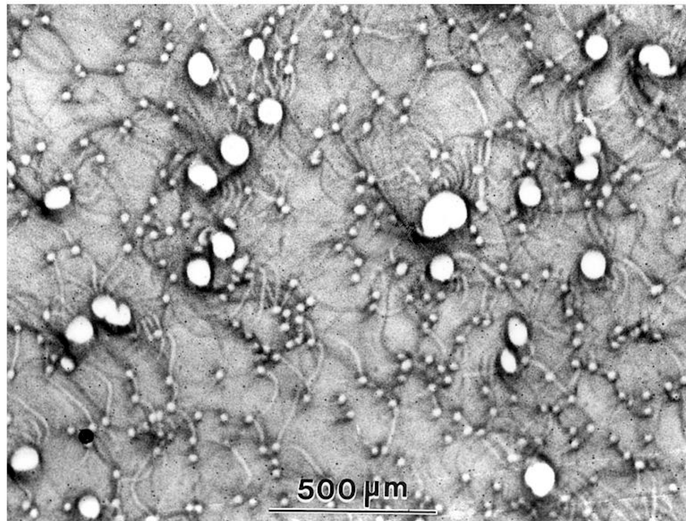


Figure 8 Back reflection topograph of (0001) 6H-SiC showing the circular images of Micropipes [25].

Various reasons have been predicted for the existence and nucleation of this hollow- core SDs, one of them due is to the incorporation of inclusions which results in imperfect lattice closure, around an inclusion resulting in their nucleation [23]. Other nucleation mechanisms include heterogeneous phase [26] and hexagonal voids [27]. There is no unanimous interpretation for their formation mechanism and the above predictions do not conflict with each other either.

These MPs can be observed and their Burgers vector experimentally can be calculated by various techniques such as AFM, SEM, TEM and most effectively and easily by X-ray diffraction topography. The first topographic observation of the presence of these dislocations was made by Dudley et al. [28]. The critical Burgers vector for a hollow core screw dislocations are 2c and 3c for 6H- and 4H- SiC respectively [25]. Their Burgers vector can be directly calculated by back reflection X-ray topography by measuring their diameter [25] which appear as circular white spot in the figure 8.The physical shape of MPs is not round but usually hexagonal or elongated hexagonal shape. Ray tracing principle can be used successfully to simulate both SDs and MPs, Grazing- reflection geometry can also be used to directly observe SDs and MPs. Yi chen et al used this technique effectively along with ray- tracing principle to simulate these dislocations and find out their dislocation sense i.e. their Burgers vector direction.

Recent progress made in PVT growth has enabled the complete elimination of Micropipes in the crystal boule. Various ways have been developed by companies selling SiC commercial wafers and they are not discussed here as they are propriety information for the companies who do not reveal their strategies adopted.

1.4.3. Threading Edge Dislocations

These dislocations are due to the extra half (1-100) habit plane introduced into the crystal during growth. They are pure edge type dislocations with Burgers vector of the type 1/3(11-20) on {0001} wafers, and line directions roughly parallel to the growth axis while Burgers vector lie in the c-plane. TEDs have been recently observed to cause premature breakdown voltage and cause leakage of current [29]. TEDs are mostly inherited from the substrate or converted from

bent BPDs due to image force [30]. Ha et al. [31] proposed the formation of TEDs due to prismatic plane slip. The TEDs are the reason for prismatic plane tilt and they are visible in KOH etching and can be seen aligning along the grain boundary and are major components of low angle grain boundries [LAGB]. Figure 9 (a) shows an X-ray topograph image where TEDs can be seen aligning along the grain boundary. Chen et al has done Burgers vector analysis for the TEDs and have been determined to be of six different types [32] as shown in Figure 9 (b). Six different directions [-1-120], [12-10], [2-1-10], [11-20], [1-2-10] and [2-1-10] of the TED Burgers vector has been determined, with magnitude of Burgers vector being same in all directions.

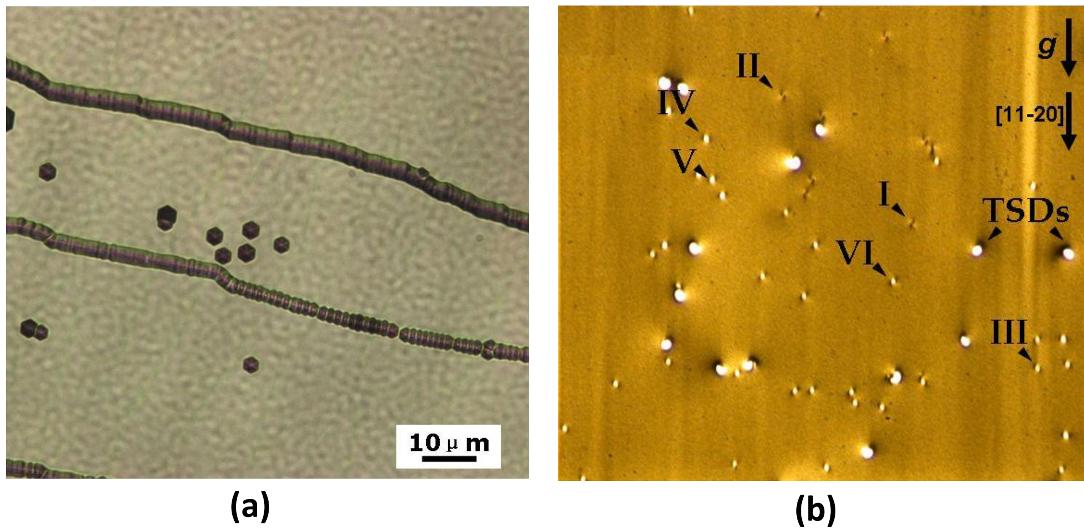


Figure 9 shows a X-ray topograph in which the big white spots are TSDs as marked and the small roughly white circles are TEDs, from more than fifty different topographs they examined they were able to find six different types of TEDs as shown. The experimental results were simulated by ray- tracing method to generate the six types of TEDs observed.

1.4.4. Basal Plane Dislocations

BPDs have burgers vector of the type 1/3(11-20), they have both line direction and burgers vector on the basal plane. They can be pure edge, pure screw or a combination of these two making them mixed type. SWBXT can be conveniently used to image these dislocations and also calculate their density which is the total line length of BPDs divided by the volume of the sample being considered. It was recently reported by our group that the BPD density obtained via SWBXT showed values by almost two to three orders of magnitude than by KOH etching [33]. Figure 10 shows a SWBXT image taken by Transmission geometry which reveals black curved

lines corresponding to the BPDs. Transmission SWBXT is the best technique to study BPDs because of their nature to image the entire volume of material unlike in Grazing or Back reflection geometry which does not reveal information beyond certain penetration depth. The main reason for their formation is due to relaxation of stress caused by temperature gradients during cooling down from growth temperature to room temperature. Due to recent advancements in the growth technology replication of BPDs from substrate to epilayer has been almost 97% eliminated [34].

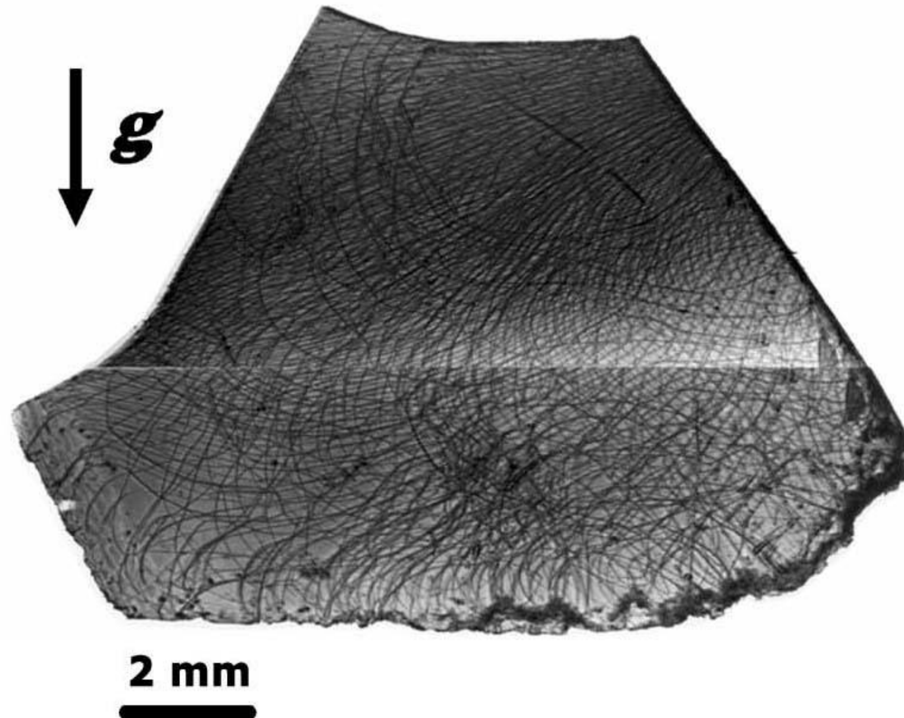


Figure 10. $[11\bar{2}0]$ transmission topograph of a 6H Lely seed showing BPDs as black curved lines.

It was observed that BPDs usually dissociate into two Shockley partials with a ribbon of stacking fault between them and they expand in p-n diodes which caused drop in forward voltage. The reason why SiC dislocations are dissociated into partials is because they have very low stacking fault energy [35]. Electron- hole pair recombination was interpreted to provide the energy needed for dissociation and expansion [36]. Si- core partials are more mobile than C-core partials due to lower bond energy and below brittle to ductile transition temperature (BDTT) only Si- core partial moves and C-core partial is sessile or immobile.

Due to recent strides in growth technology the density of BPDs have gone down by almost two to three orders of magnitude which provides an outstanding opportunity to discern details of their core structure, behavior and interaction with other growth dislocations. In the crystals that were studied for last five years the BPD density in certain areas have dropped to few hundred per square centimeter and overall wafer average density is almost down to few thousands per square centimeter on a regular basis. The reason for these changes can be attributed to the stress strategies incorporated during growth for example reducing thermal shear stress to levels below critical resolved shear stress of 1 MPa [37]. Figure 11 shows simulation geometry of “High Stress” growth process that resulted in shear stresses of 11.5 MPa during growth, while the “Low” stress condition results in shear stresses of only 0.5 MPa shown in 11 (b), which is well below the critical resolved shear stress of 1MPa for the generation of basal plane dislocations as expected [38].

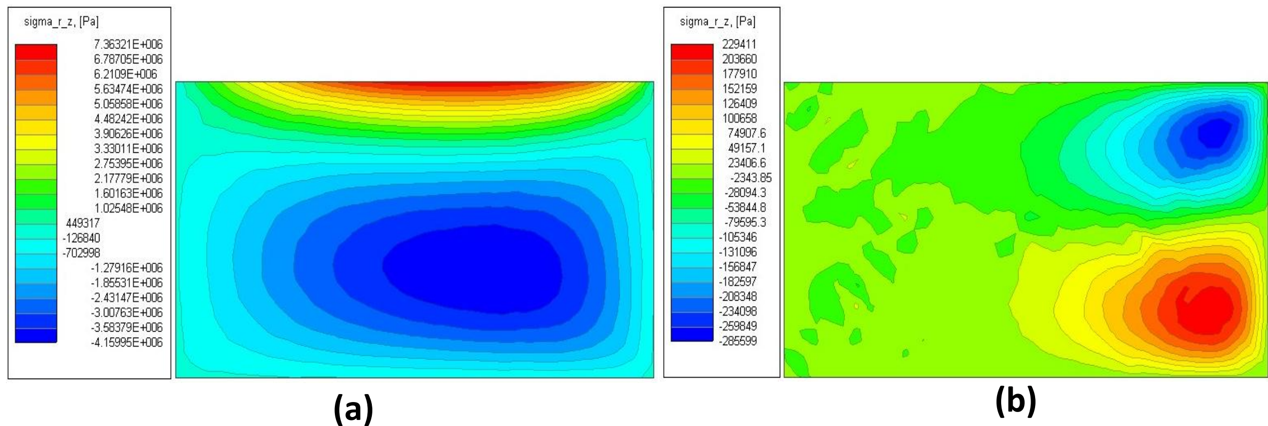
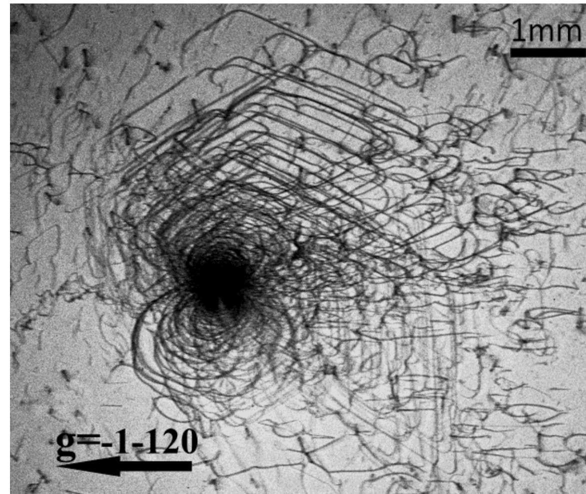


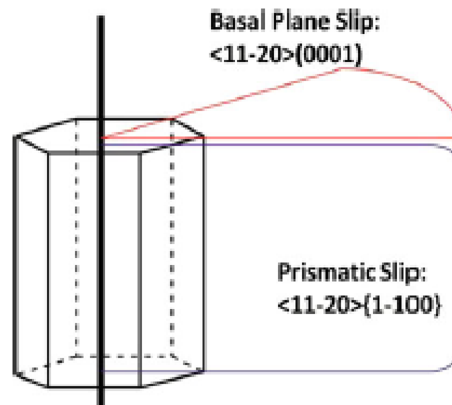
Figure 11 (a) shows simulation geometry of shear stress distribution in the boule grown under high stress condition and (b) is the boule grown under low stress condition.

Micropipes in SiC can act as nucleation sites for dislocation half- loops as shown in figure 12 (a) belonging to the primary 1/3<11-20>(0001) slip system [22] and to the secondary 1/3<11-20> (1-100) prismatic slip system [31]. Both types of loop are thought to nucleate at steps on the inner surface of the hollow cores of the micropipes and are thought to subsequently expand under thermal stress either immediately after growth or during post- growth cooling as shown in figure 12 (b). Half loops emanating in both the slip systems look different on topograph images, the basal plane half- loops anchored to the micropipe are very clearly visible since the basal plane is only slightly inclined to the wafer surface and the basal plane loops exhibit weak contrast on one of the {1-100} reflections according to the g.b criterion. On the

other hand the prismatic slip bands might appear as linear trail of TEDs or may intersect long screw or mixed component dislocations, they will again exhibit weak contrast on one of the {1-100} reflections.



(a)



(b)

Figure 12 (a) shows Transmission XRT image showing a micropipe from which BPDs are emanating in both slip systems and 12 (b) is an illustration showing the mechanism of BPD generation in both slips system [42].

1.4.5. Defects introduced due to interaction of common defects in SiC

1.4.5.1. Interactions between threading dislocations in 4H- SiC

Recently SWBXT group at State Univ. of New York at Stony Brook have consistently observed threading defects which is a combination of c and a defects resulting in c+a burgers vector [39]. These defects were postulated to exist in SiC in theory by many groups including SWBXT team at Stony Brook until recently when they were confirmed by studying numerous axial slices shown in Figure 13 i.e. samples cut parallel to the [0001] growth axis. The c+a defects are also threading defects in which the two extra half planes associated with 'a'

component are anchored together with the surface step associated with the ‘c’ component as shown in figure 14. These c+a defects were observed to deflect out of the crystal system at various stages of growth facilitating in the reduction of overall threading density.

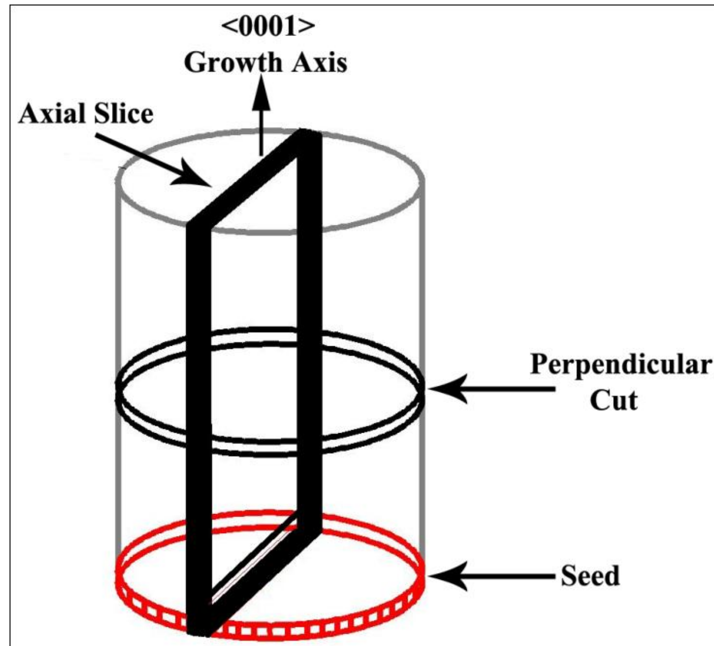


Figure 13. Illustration showing horizontally wafers cut perpendicular to growth axis and the axial slices cut parallel to [0001] growth axis. Axial slices help study defects that replicate from seed to the top of the boule.

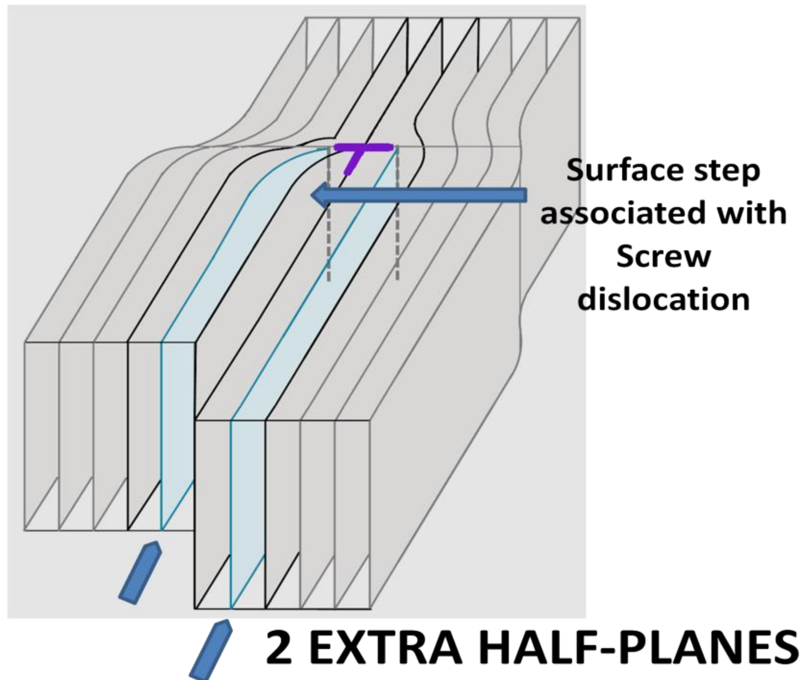
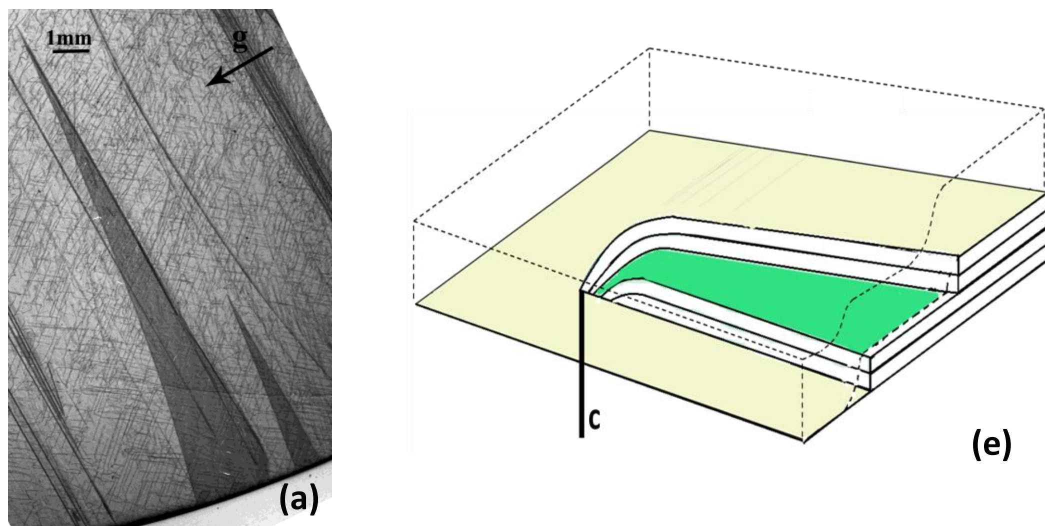


Figure 14. Shows typical c+a defects in which the defect core has both the c- and a- component associated with screw and edge dislocations respectively. In this case c- height screw has bisected the two extra half planes.

These c+a dislocations were observed consistently in numerous axial slices, in many cases replicating right from the crystal seed interface to the top of the boule and also several times getting deflected out of the crystal.

1.4.5.2. Deflection of threading defects resulting in stacking faults:

Four types of stacking faults have been observed recently by the SWBXT group at Stony Brook consistently in 76mm, 100mm and 150mm commercial wafers. These stacking faults were confirmed to have been associated with deflection of threading defects onto the basal plane and subsequent creation of stacking faults with four fault vectors. The SWBXT image contrast studies of these stacking faults with comparison of calculated phase shifts for postulated fault vectors by macrostep overgrowth of surface outcrops, has revealed faults to be of the following types: (a) Shockley faults; (b) Frank faults; (c) Combined Shockley + Frank faults with fault vector s+c/2; (d) Combined Shockley + Frank faults with fault vector s+c/4. Figure 15 (a)-(d) shows four types of stacking faults observed lately associated with the deflection of threading defects with fault vector 1/3(-1100) for Shockley fault; ½(0001) for Frank faults; 1/6(20-23) for a combination of Shockley plus c/2 Frank fault; and 1/12[-4043] for a combination of Shockley plus c/4 Frank fault. The four models to explain these phenomena by macrostep overgrowth mechanism in SiC has been shown as illustrations in Figure 15 (e)-(h) [40].



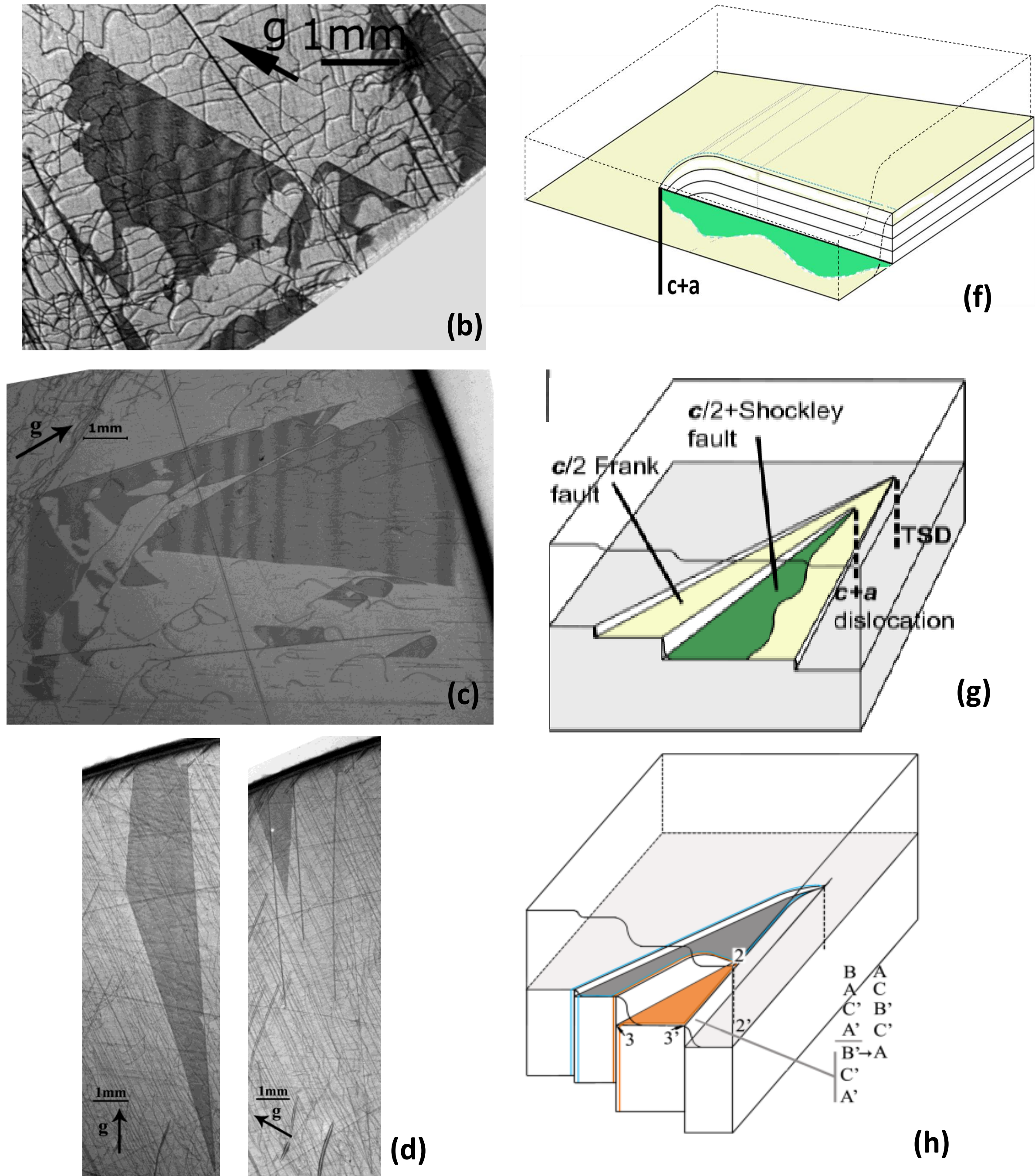


Figure 15. Transmission topographs from 4H-SiC crystals showing stacking faults with fault vector: (a) R = 1/2[0001] (Frank fault); (b) R = 1/3[1-100] (Type I Shockley fault); (c) R = 1/6[20-23] vector (S+c/2 fault); (d) R = 1/12[-4043] (C) & R =1/12[-4403] (D) (vector S+c/4 fault). Illustrations of the stacking faults: (e) Frank type stacking fault (shaded area); (f) Type I Shockley fault with the glissile partial lying below the step and the sessile at the top which is locked; (g) Overgrowth of **c** dislocation and formation of the **c**/2 Frank type fault within which a **c**+**a** dislocation with one sessile Shockley partial and one glissile Shockley partial converts some part of the fault to **c**/2 plus a Shockley type; (h) Overgrowth of **c**+**a**dislocation with a c-height step converting it into a Frank dislocation plus two Shockleys with one sessile and the other

glissile. Overgrowth of **c+a** dislocation 11' with c/4 and 3c/4- height steps which has second 22' with **c**-height spiral step protruding onto the terrace between these two step risers."Interfacial Shockley" converts A layer into B', allowing overgrowth by the A' layer at the bottom of the macrostep. Following overgrowth the Shockley associated with the deflected 22' dislocation located at 23 glides under stress until it reaches the edge of the step 23' creating the fault of type C shown in (d).

These fault vectors were determined by taking into account the contrast from stacking faults in SWBXT undergoing phase shift as the X-ray wavefields cross the fault plane. The deflected dislocations onto the basal plane were responsible for the stacking faults and were observed to be detrimental to the devices grown on them as they replicate to the epilayer. In the wafers studied at different stages of the SiC crystal boule resulted in reduction of threading defects as they at certain stage got deflected out of the crystal causing drop in defects density. [40]

1.4.5.3.Defect multiplication of BPDs involving Hopping Frank- Read source mechanism

The detrimental influence of BPDs on bipolar devices has been reported and under forward voltage acts as recombination centers and dissociate into stacking faults [41]. A new double deflection mechanism for their multiplication was proposed in 4H- SiC where the BPDs deflect into sessile TEDs to be re- deflected back onto the basal plane [42]. These BPDs which are glissile in nature once on the basal plane can act like single ended Frank- Read source [37]. Figure 16 (a) shows SWBXT image taken in transmission geometry showing diamond shaped loops which are the result of hopping Frank- Read mechanism and figure 16 (b)- (e) shows the illustration of the double deflection taking place to create such a kind of hopping.

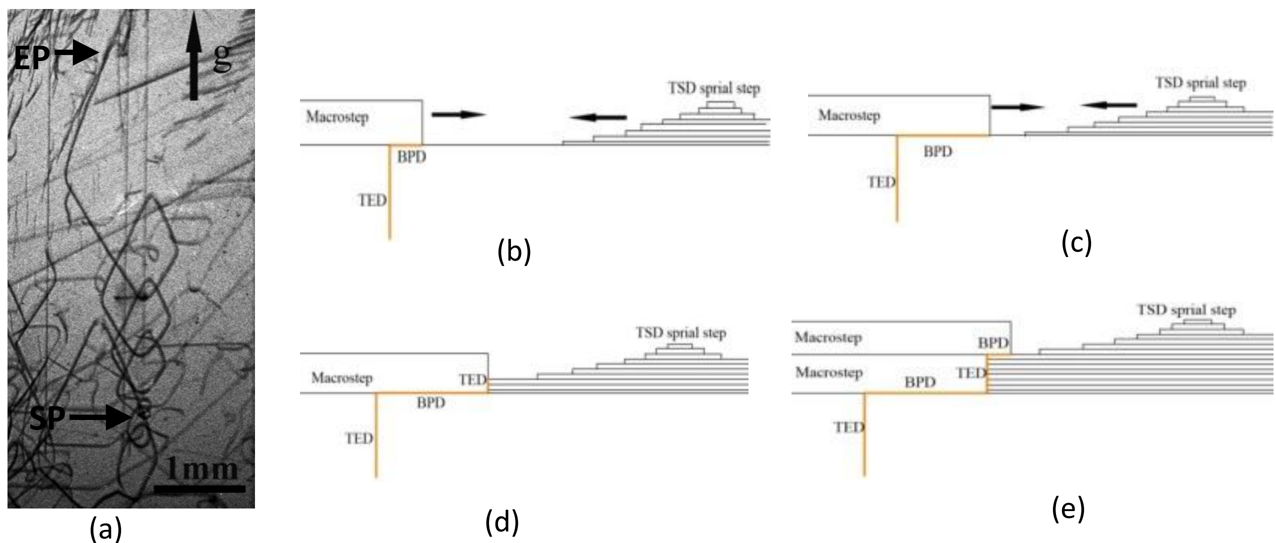


Figure 16. Transmission X-ray topograph ($g=1\bar{1}\bar{2}0$) showing a diamond shaped BPD loop (SP – starting point; EP – ending point).(b)-(e) Schematic cross-sectional view of the deflection of a TED onto the basal plane by a macrostep followed by re-deflection into threading orientation through the encounter between macrostep and a TSD spiral advancing in the opposite direction.

The generation of such dislocations lead to further multiplication of BPDs in the crystals, the mechanism of their formation involves a TED surface outcrop getting deflected onto the basal plane by macrostep overgrowth as shown in figure 16 (b)- (e) created by step bunching or obstacles they encounter which cannot admit the sessile TEDs into them. The TED on the basal plane starts to advance in the direction of step flow as a BPD but the advancing macrostep and BPD can be encountered by obstacles at this time in the opposite direction. This opposite step might be a spiral screw dislocation in the down step direction as shown in the figure 17 on the adjacent terrace and at this juncture the BPD is re- deflected back into a TED segment.

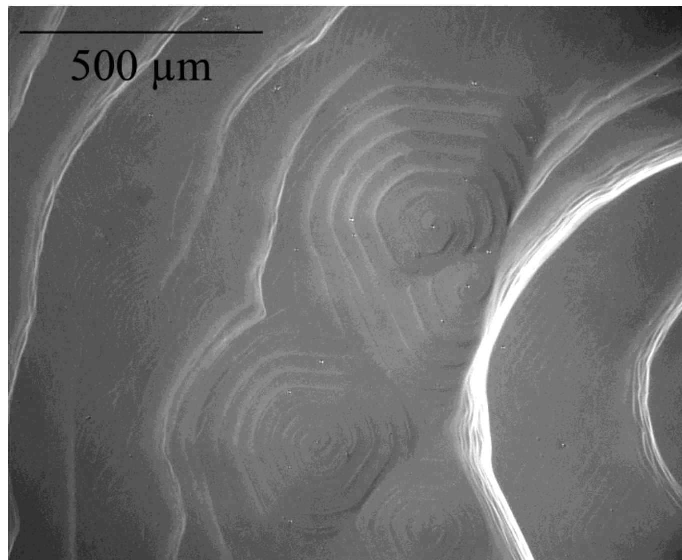


Figure 17 is an optical image taken from a 4H- SiC boule. One can clearly see the large macrosteps on the surface of boule with opposite pair screw dislocations on the terrace which is the reason for the conversion process resulting in Hopping mechanism.

1.4.6. Defect behavior in 4H- SiC Epitaxial Layers

The progress of SiC devices is closely related to high quality epitaxial growth and the problem of defect replication from substrate to epi creates huge problems for device groups working with SiC power electronics. Epitaxial film growth is imperative for SiC wafers as direct ion implantation into substrates like in the case of Si is not possible for SiC because it results in inferior electrical properties. SiC devices are mostly fabricated using homoepitaxial films as they

are known to provide superior electrical properties and are achieved using vapor phase epitaxy (VPE), liquid phase epitaxy (LPE) and vapor- liquid- solid (VLS) epitaxy. SiC industry mainly uses VPE under which CVD is most matured and commercial success has been achieved using this technique with lot of modifications.

The defects that are present in substrate or the ones introduced during film growth all play a major role in device performance which will be discussed in in chapter 6. It is important to study and discuss few of the most common extended defects behavior in SiC epitaxial layers:

1.4.6.2.Conversion of BPDs to TEDs

BPDs are one of the major defects affecting performance of SiC power electronics especially causing a reduction in voltage across *p- i- n* diodes to increase. BPDs in SiC under forward bias cause the stacking faults to expand which not only results in degradation of performance in SiC bipolar devices but also affects throughput. Dissociation of BPDs into mobile silicon-core (Si-core) partial dislocations and subsequent expansion of Shockley stacking faults (SFs) associated with advancement of these partial dislocations under forward bias causes forward voltage drop and reduced lifetime of silicon carbide (SiC) based bipolar devices [43]. Such expansion of basal SFs is activated by the electron-hole REDG process as shown in figure 18 (a) - (e) [44, 45, and 46].

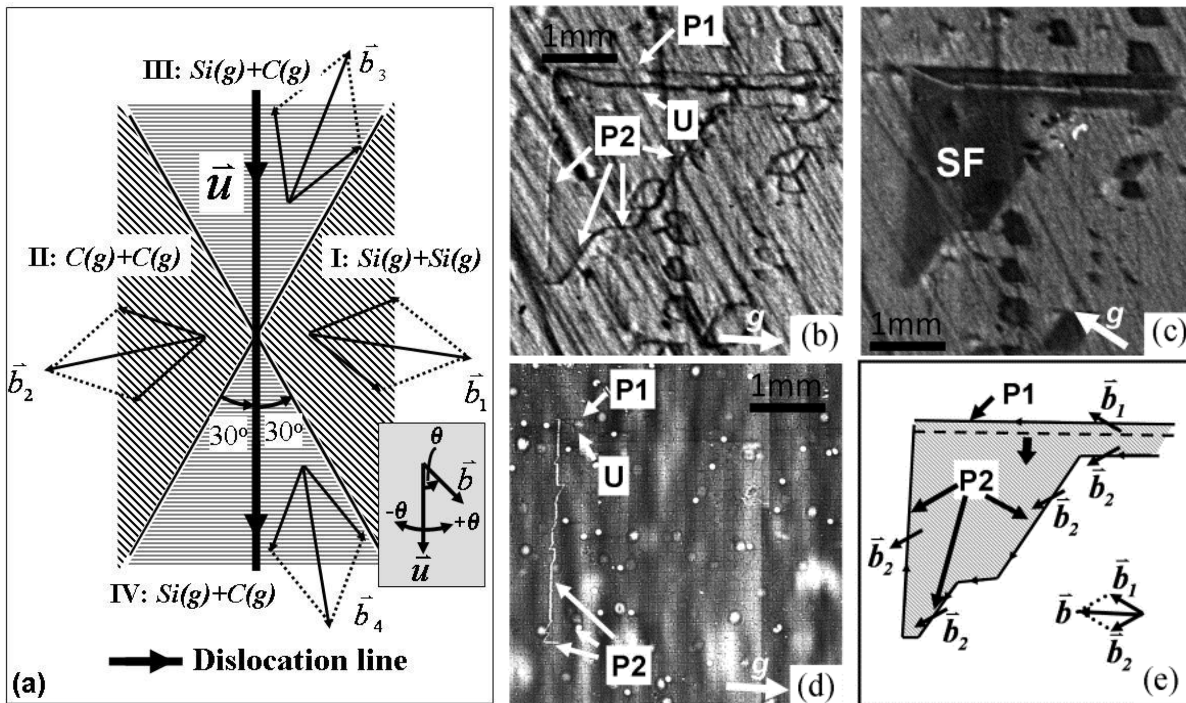


Figure 18(a) Dependency of core structures of Shockley partial dislocations dissociated from a perfect BPD on the direction of Burgers vector with respect to line direction of dislocation (Si-face up): Region I: $30^o<\theta<150^o$ - two Si-core partials; II: $210^o<\theta<330^o$ - two C-core partials; III: $150^o<\theta<210^o$ -one Si-core and one C-core. IV: $-30^o<\theta<30^o$ - one Si-core and one C-core (θ defined in inset of (a)); REDG-activated SF after forward bias from a screw-oriented BPD. (b) (11-20) transmission topograph showing the partials (P1 and P2) bounding the SF; (c) (-1010) transmission topograph showing the SF; (d) (0008) back-reflection topograph showing TSDs; (e) SF configuration. SF is obtained via expansion of Si-core partial toward the bottom edge of the view (dashed line) and interaction with TSDs [47].

Major research has been carried out to reduce the density of these defects in epilayer and one of the best agreed methods by several groups is to increase conversion ratio of BPDs to more benign TEDs. Several ways have been developed to facilitate the process of conversion; one of the ways is to use off- axis substrates which causes BPDs intersecting the substrate/ interface surface to convert into TEDs. Zhang and Sudarshan et al [34] etched the substrate surface prior to epitaxy which resulted in etch pits at BPD sites to facilitate lateral growth over step flow growth within pits causing TED conversion as shown in figure 19. Sumakeries et al [48] have used lithography and dry etching for patterning the SiC substrates before epitaxy. Recently Song et al [49] and SiC industries have used a combination of KOH- NaOH etchant for etching substrates before CVD growth. Tsuchida et al [50] has achieved high conversion rate by annealing at the elevated temperatures. Another method to bolster this process is to include interruptions during growth reported by VanMil et al and Stahlbush et al [51] where conversion has been reported at interrupted interfaces. Although several methods have been used it is still difficult to achieve 100% conversion ratio especially with BPDs in screw orientation.

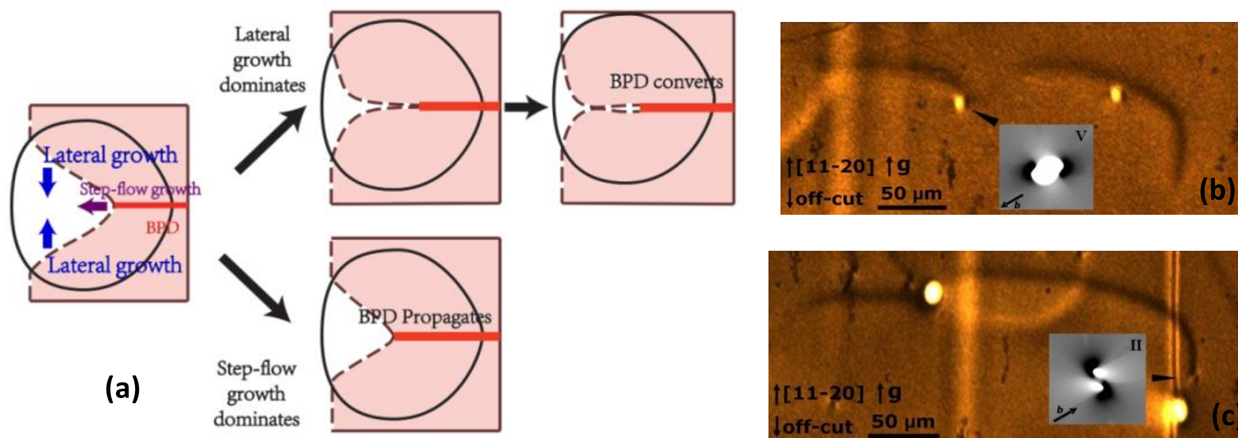


Figure 19(a) Evolution of the basal plane during epitaxy if lateral growth dominates, and if step-flow growth dominates [51]; 11-28 SWBXT topographs showing conversion of BPDs to TEDs – (b) Type V: b=1/3[2-1-10]; (c) Type II: b=1/3[-2110]. Inset images are ray tracing simulations used to determine Burgers vectors of TEDs.

1.4.6.3.Triangular Defects

As discussed previously SiC has more than 200 different polytypes and the most common among them are 3C, 4H, 6H and 15R. One of the major challenges for SiC crystal growth community is the presence of polytype inclusions due to low stacking fault energy which play a significant role in controlling the wafer size and act as nucleation sites for other defects. One of the ways to control these inclusions is to have good control over the thermodynamics and kinetics of the growth process. In addition to these careful deliberation has to be given for factors such as seed surface polarity, supersaturation, vapor phase stoichiometry, impurity levels, facet and off- cut angle of the seed used. One of the most common polytype inclusion is the 3C- SiC which is known as the triangular defects as they exist in triangular shape and usually fan out towards the step flow direction as shown in figure 20. Triangular defects are classified as device killing defects as it has deleterious effect on the devices. In order to achieve high quality CVD growth it becomes extremely important to control 3C- inclusion, one of the ways used is to grow the crystal at high temperatures because 3C- SiC grows at lower temperature unlike hexagonal polytypes like 4H- , 6H- SiC need high growth temperature due to differences in energy of formation. This methodology does not completely reduce the 3C- SiC and when the SiC community had a huge setback in 1980s and 1990s due to these defects, Matsunami et al [52] introduced step controlled epitaxy during this time i.e. using seeds with off- axis. This technology enabled the growth of device quality epilayers in SiC as the surface steps present on the substrates acted as templates for replication of underlying polytype and reduced the terrace width. Sudarshan et al also concluded that in addition to using off- axis substrates, controlling growth parameters it is also important to maintain the cleanliness of the equipment especially that of the susceptor.

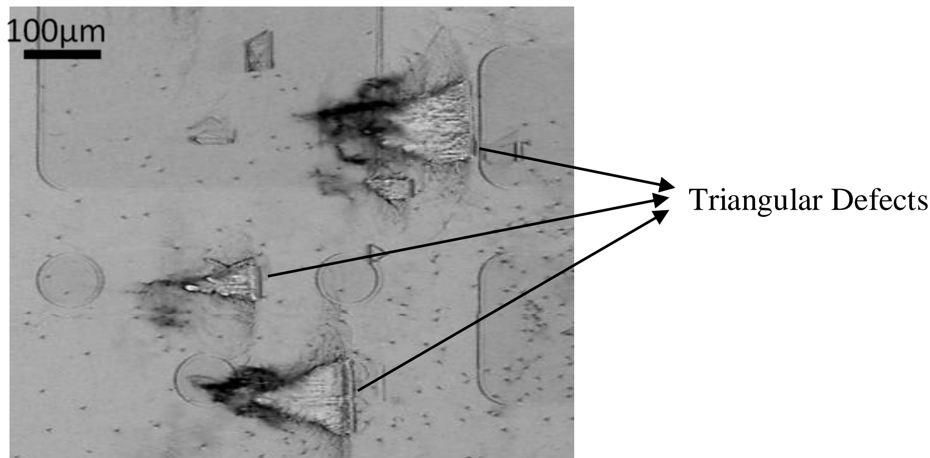


Figure 20 is an [11-28] SWBXT image taken by Grazing geometry showing Triangular Defects that are expanding in the direction of off- cut.

1.4.6.4.Nucleation of TEDs, BPDs and TSDs at substrate surface damage

During epitaxial growth, subsurface damage associated with surface scratches on the substrate, residual from polishing act as nucleation centers for TED-TED pairs, TED-BPD pairs, TSD-TSD pairs and Carrot defects [54]. When scratches are parallel to the off-cut direction (Fig. 21 (a)-(b)), a single, dense row of TEDs is formed. For scratches inclined to the off-cut direction (see Fig. 21 (c)-(f)), in addition to the row of TEDs, BPDs are also nucleated with density of BPDs increasing with the angle between the scratch and off-cut directions.TSDs can also be nucleated along substrate surface scratches as seenin Fig. 21 (g)-(h) which show four pairs of large hexagonal pits (indicated by arrows) that correspond to elementary TSDs. The mechanism for nucleation of pairs of TSDs at scratches is similar to that for nucleation of TSDs at inclusions in SiC [23] where atomic steps that approach the local surface indentations in the scratch groove collapse (Fig. 21 (i)) creating two screw dislocations of opposite signs with Burgers vector magnitude equal to the magnitude of the step disregistry. Such nucleation of defects at subsurface damage associated with substrate surface scratches can be avoided by ensuring that the surface grooves associated with scratches are fully removed prior to growth.

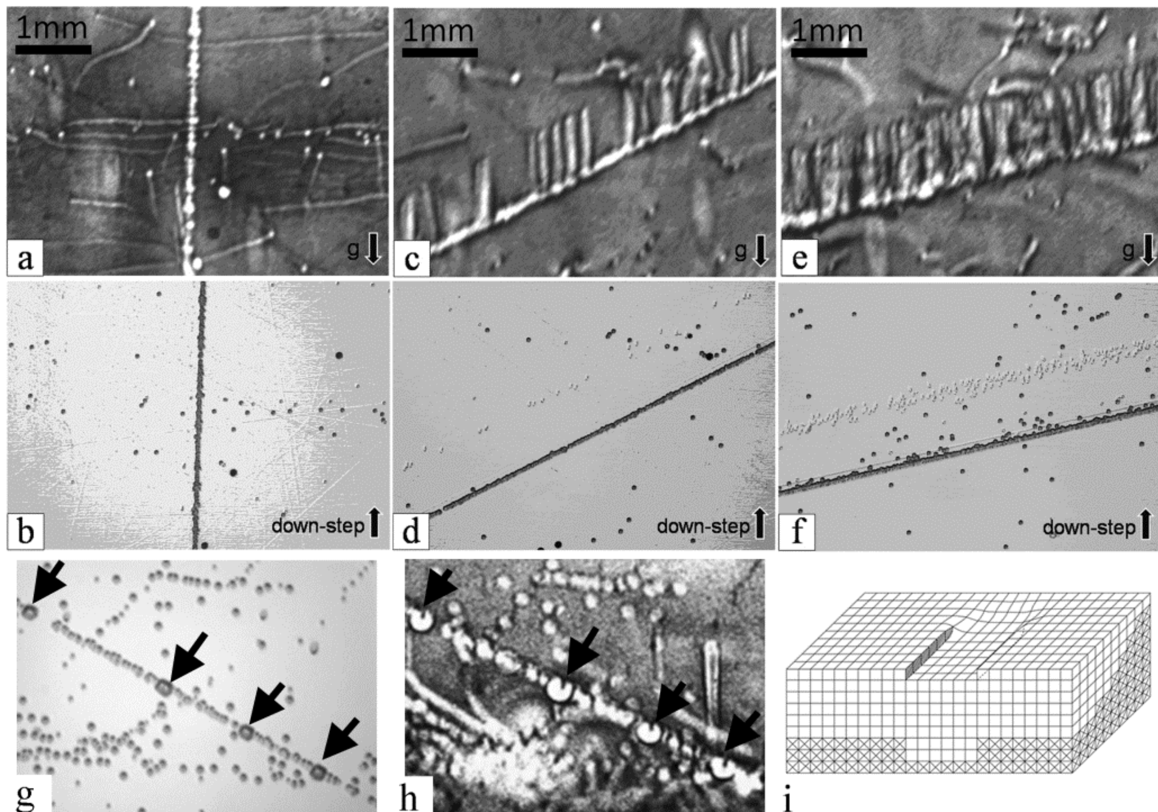


Figure 21 X-ray topographs ((a), (c), (e) (h) and corresponding etch pit patterns ((b), (d) and (f) (g)) recorded from epilayers grown on a scratched substrate surface. (a)-(b) show scratch parallel to off-cut direction while (c)-(f) show scratches inclined to the off-cut direction; (g) &(h)Arrows show four pairs of TSDs which have propagated from the scratch to the epilayer surface. (c) Schematic diagram illustrating the nucleation of a pair of opposite-sign screw dislocations during the process of scratch overgrowth.

1.5. Motivation

As discussed SiC although possesses superior properties in comparison with conventional semiconductors, the high defect density especially the crystallographic defects affects the performance of the material drastically when put to use. The SiC community realizes that it is extremely important to study these defect structures in detail so as to come up with models explaining their occurrence and take steps to negate their influence. My research for last five years has been to study these defect structures in substrates, epilayers and also in devices using advanced tools such as Synchrotron X- ray Topography. Our group has made significant contributions in the reduction of defects in SiC and the low density of defects has enabled us to study interesting phenomena such as the deflection of nc+ma type defects leading to stacking faults of different fault vector [chapter 3], simulation of c+2a type defects [chapter 4], Single-Ended Frank Read source [chapter 5] and failure analysis of high performance diodes in SiC [chapter 6]. Studying defects in SiC using advanced tools and by working with processing teams in industries to bring high quality SiC wafers has been my motivation. This work has aided the companies to increase their commercial wafer size from 76mm during the time I started my PhD to current 150mm wafers.

2. Theory and Experiment

2.1. Synchrotron X-ray Topography

X-ray Topography, a non-destructive characterization technique is the most effective method to look at interior or surfaces of single crystals and get an insight of the defect distribution or lattice misorientation in the crystal by producing images by directing X-rays onto them. Topography being considered is that of the crystal diffracting planes and not just the exterior surface of it. Berg, Barrett, Guinier, Ramachandran and Wooster were the early pioneers of topographic technique who opened up new frontiers of Materials Science. That these methods have such important role in semiconductor industry were realized later on by Klapper, Dudley et al. The emergence of synchrotron sources has resulted in improvement in spatial resolution, experimental procedures and also speed of experimentation which was not possible in the lab techniques.

An X-ray Topograph is simply obtained by projecting X-ray beam onto a single crystal set at the Bragg angle, onto a two- dimensional detector usually a high resolution X-ray film. The defects inside the crystal have a different diffracting power compared to that of more perfect regions leading to local intensity variations on the topograph which are known as X-ray topographic contrast and which constitute 'images' of the defects. It is important to have knowledge about the theory of X-ray Diffraction to study the lattice plane topography of the crystal under investigation. Dynamical or kinematical theories of X-ray diffraction are used for the analysis of these images as the contrast varies differently in perfect and imperfect regions of the crystal [54]. Usually for small crystals with dimensions less than a micrometer in diameter and where the dislocations divide the crystal into a mosaic structure of independently diffracting cells, Kinematical theory of diffraction is employed to study the crystal topography. But for large single crystals which are also highly perfect, where the amplitude of diffracted wave is almost same as that of incident beam, interchange of energy occurs between the beams as they pass through the crystal and in that case kinematical theory cannot be applied. In that case to study what is happening inside the crystal one has to use Dynamical theory of X-ray diffraction [55, 56, and 57].

2.1.1. Brief History of X-ray Topography

The Laue spots obtained by X-ray diffraction of crystals never have uniform contrast throughout but contain a structure that maps variations in lattice planes causing the spots. In 1931, Berg performed experiments on rock salt using monochromatic X-rays from a tube at a certain distance, in which point to point variation of reflecting power from throughout the crystal was recorded onto a photographic plate. The striated images obtained were deduced to be plastic deformation that the crystal had undergone. At around the same time Barrett(1931) concluded that the elastic strains produced by piezoelectric oscillations could alter the reflecting power of quartz crystals, this he demonstrated by photographing the Laue spots similar to that of Berg.

So around this time it was discovered X-rays could be used as a tool to study inhomogeneous strain produced in materials as well as natural imperfections, after this for around ten years not much advances were made in this field. Not much effort was made to use these interesting investigations to study metallurgical specimens in particular, until Barrett in 1945 reported results from single crystals of Silicon Ferrite. With fine grain emulsion plates, the enlarged X-ray micrographs he obtained showed black lines corresponding to regions of high reflecting power on the specimen and white areas that represented non- reflecting regions of the crystal.

It was actually Ramachandran in the year 1944 who first used the term 'Topograph' to describe the appearance of Laue spots that he obtained from polished cleavage planes of diamond using a white X-ray beam from Tungsten target. The Laue spots were identified as topographic map of the crystal plate exhibiting variations in structure. With a source-specimen distance of 30cm and the photographic plate kept at 2.5 cm from the crystal, using a pinhole source of 0.3mm in diameter, Ramachandran achieved a resolution of 25mm. He realized the practical importance of such a technique to detect lattice perfection, as compared to luminescence studies in general. This term 'Topograph' was added into the literature when Wooster and Wooster in 1945 obtained topographs for Diamond but in this case using characteristic copper radiation unlike bulk stone results by Ramachandran.

It was only in 1957 the observation of single dislocations was made by Professor Lang who developed a technique known as section topography, which provides images of a cut through the crystal. Soon afterwards, Lang developed another method called the projection

topography, in which case the whole crystal is imaged by also traversing simultaneously crystal photographic plate, and this method came to be known as traverse topography. These methods were widely used until the introduction of Synchrotron radiation as a source of X-rays [55, 56, and 57].

2.1.2. Fundamental theory of X-ray Diffraction Topography

X-ray diffraction is a combination of physics of X-rays and geometry of crystals developed by German physicist Von Laue. The scattered X-ray waves by planes in crystals give rise to diffraction phenomena where two or more waves in phase undergo constructive interference which mutually reinforces each other. The scattering of X-rays by the planes in crystals need to satisfy the Bragg condition given by,

$$\lambda = 2d \sin \Theta$$

where λ is the wavelength of X-rays, d is the interplanar spacing and Θ is the incident angle of the X-rays.

The X- ray diffraction phenomena in crystals are based on dynamical theory and kinematical theory of diffraction. These two theories are taken into consideration in X-ray diffraction topography for interpreting the contrast of images recorded by different geometries. Laue’s kinematical theory comes into play for thin imperfect crystals whereas Ewald and Darwin’s dynamical theory explains contrast in thick perfect crystals. Rescattering is considered negligible or null in case of kinematical theory but dynamical theory considers its effect.

To predict the diffracted intensities accurately in case of small or heavily deformed crystals where the dislocations can divide the crystal into small independent mosaic structures the theory of kinematical phenomena can be successfully incorporated. When the crystals become thicker diffracted intensity is predicted to become larger than the incident intensity which violates the law of conservation of energy, which causes kinematical theory to fail. Primary extinction phenomena can be used to interpret the discrepancies caused by the breakdown of kinematical theory. In such a case it is necessary to take into consideration all the wave interactions in the crystal, as dynamical theory considers the total wavefield inside crystal where diffraction is taken as one entity. Dynamical theory uses Maxwell’s equations to find solutions in a periodic medium which is the crystal but this can create a problem as these

solutions must match with that of plane waves. The solutions that are provided must relate to periodicity in the crystal and such functions also known as Bloch functions is represented by Fourier series.

To derive the diffraction intensity let us consider a parallelepiped shaped crystal with $N_i$unit cells along a_i axis, where i is 1, 2 or 3. Diffraction intensity is given by:

$$I(\overline{b}) = \left|F(\bar{b})\right| G(\bar{b})$$

Where $F(\bar{b})$ = Structure factor = $\sum f_\alpha e^{-2\pi b r_\alpha}$

and $G(\bar{b})$ is Laue function, $G(\bar{b}) = \frac{\sin^2(\pi h N_1)\sin^2(\pi k N_2)\sin^2(\pi l N_3)}{\sin^2(\pi h)\sin^2(\pi k)\sin^2(\pi l)}$

f_α(b) = atomic scattering factor of αth atom located at $\mathbf{r}_\alpha = x_\alpha\mathbf{a}_1 + y_\alpha\mathbf{a}_2 + z_\alpha\mathbf{a}_3$ and **b** is the scattering vector given as $\mathbf{b} = h\mathbf{a}_1^* + k\mathbf{a}_2^* + l\mathbf{a}_3^*$ where $\mathbf{a}_1^*$, $\mathbf{a}_2^*$ and $\mathbf{a}_3^*$ are reciprocal vector and h, k and l are integers. x_α, y_α and z_α are the coordinates of the αth atom within the unit cell and $\mathbf{a}_1$,$\mathbf{a}_2$ and $\mathbf{a}_3$ are unit cell vectors.

$$I = F_{hkl}^2 \frac{\sin^2(\pi h N_1)\sin^2(\pi k N_2)\sin^2(\pi l N_3)}{\sin^2(\pi h)\sin^2(\pi k)\sin^2(\pi l)}$$

This is the equation used for explaining the diffraction intensity in kinematical theory, which only predicts well for small imperfect crystals but does not work for large perfect crystals. In that instance it is required to use dynamical theory, as in the above equation N_1, N_2, N_3 goes to infinity than Laue function G(b) goes to infinity i.e. diffracted intensity will be infinity which becomes impossible and directly contradicts the conservation of energy principle. Therefore dynamical theory of x-ray diffraction has to be applied in case of nearly perfect large size crystal. However, this equation helps understand the dislocation images arisen from extinction contrast in x-ray topography. Second, the width of the diffraction peak varies inversely with the number of the unit cells according to this equation. Thus, extremely narrow peak is expected for thick crystals. This is contradictory with the experimental observation. For example, assuming a 1 mm-thick defect-free Si wafer, the number of unit cells is 1 mm/ 5.43 Å $\approx 1.84 \times 10^6$, the full width at half maximum should be approximately $1/1.84 \times 10^6$ (radians)=0.11 (arcsec), which is

two orders narrower than the actual rocking curve width. Therefore, dynamical diffraction has to be carried out for nearly perfect crystals. In the diffraction theory, a few concepts which are important in interpreting x-ray diffraction topography are briefly introduced below: rocking curve width, the diffracted intensity and penetration depth [55, 56, 57 and 58].

2.1.3. Resolution

Individual defects can only be distinguishable if there is enough spatial resolution. Since there is no magnification in X-ray diffraction topography, the resolution can only be controlled by geometrical factors. Even though compared to electron microscopy, X-ray diffraction topography has much lower spatial resolution but it is more than sufficient for high quality crystals which are currently grown. In order to understand the resolution of X-ray diffraction topography, consider diffraction due to the Bragg's law $\lambda = 2d\ \mathrm{Sin}\ (\Theta)$. Consider a cone with semi-apex angle (90^0 - Θ) and the axis of which is diffracting planes normal vector or the reciprocal lattice vector ($\bar{g}$) as shown in Figure 22 [58].

Since X-ray source has a finite size, which indicates X-rays received at a point in crystal may have originated at two distinct points in the source. Therefore point P in the crystal shown in figure 22 will receive X-rays with correct Bragg's angle from locus of points in the source defined by the intersection of cone and the X-ray source surface. Consider three such points a, b and c on the surface of the source. X-rays emanating from points a, b and c after diffraction from point P will form an arc onto the detector A, B and C. This arc is generated by the locus of points defined by intersection of detector surface and the Bragg's cone. It can be seen that "image" of point P is spread over the arc A-B-C which gives rise to blurring effect in the image of that point. The plane where incident and diffraction beam vector lies, is defined as the plane of incidence (for example plane bPb'). The source dimension perpendicular to the plane of incidence should be minimized in order to reduce the blurring effect or the effective resolution. The blurring is proportional to specimen to film distance, source size perpendicular in the direction of plane of incidence and inversely proportional to source to specimen distance [58].

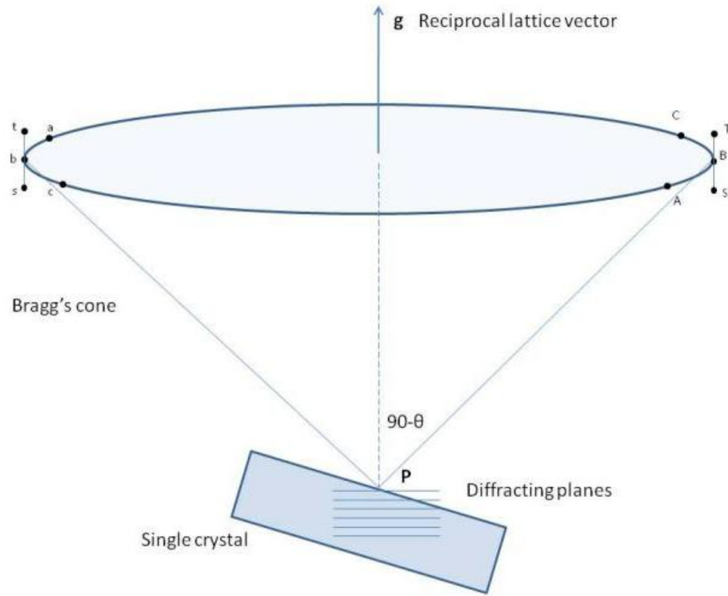


Figure 22 Schematic of diffraction geometry and Bragg's cone showing the effect of source dimension on resolution of topographic image. **g** is the active reciprocal lattice vector, 90-θ is the semi-apex angle of Bragg's cone [58].

The relationship can be mathematically written as:

$$R = \frac{SD}{C}$$

where S is the maximum source dimension perpendicular to the plane of incidence, D is specimen film distance and C is source specimen distance.

Now let us consider the effect of source size in the direction parallel to the plane of incidence. Referring to Figure 22, the point P will accept X-rays (for diffraction) emanating from range of points on the source in the direction parallel to the plane of incidence (t-b-s) determined by the rocking curve width. Higher rocking curve width would mean wider acceptance angle (t-P-s) in the plane of incidence.

It can be shown by simple calculations that source dimension perpendicular to the plane of incidence, D is the specimen film distance and C is the source specimen distance.

We have noted before that spatial resolution depends on specimen to film distance and should be minimized; however there is limitation on resolution of photographic detectors used in topography therefore there is no added benefit in reducing specimen to film distance beyond the

resolution of detector determined by grain size in the emulsion which is around 1μm. In practice specimen to film distance is set such that calculated resolution matches with detector resolution [55, 56, and 57].

The rocking curve width (FWHM) for perfect crystals is given by:

$$2\delta_{hs} = \frac{2r_e\lambda^2}{\pi V \sin 2\theta_B} \frac{1}{\sqrt{|\gamma|}} |C| \sqrt{F_{hkl} F_{\bar{h}\bar{k}\bar{l}}} \quad \text{(Bragg case)}$$

and

$$2\delta_{os} = \frac{2r_e\lambda^2}{\pi V \sin 2\theta_B} \sqrt{|\gamma|} |C| \sqrt{F_{hkl} F_{\bar{h}\bar{k}\bar{l}}} \quad \text{(Laue case),}$$

where r_e is the classical electron radius, λ is the x-ray wavelength, V is the volume of the unit cell, θ_B is the Bragg angle, γ is the asymmetric ratio, C is the polarization factor (C=1 for σ polarization and $C=\cos 2\theta_B$ for π polarization) and F_{hkl} is the structure factor.

One way to determine the crystalline quality is to study the rocking curve width, if the peak is narrow it directly quantifies high quality. In case of peak broadening generally has a proclivity towards low quality of crystal, as it surmises the existence of dislocations, residual strain or mis-orientation.

2.1.4. Penetration Depth

The penetration depth is an important concept and plays a vital role in interpreting X-ray diffraction topograph. It provides the information of the volume from which the image is generated. Penetration depth, defined for a reflection is the depth (t) at which intensity drops to 1/e. Figure 23 shows a reflection with a penetration depth of t [58].

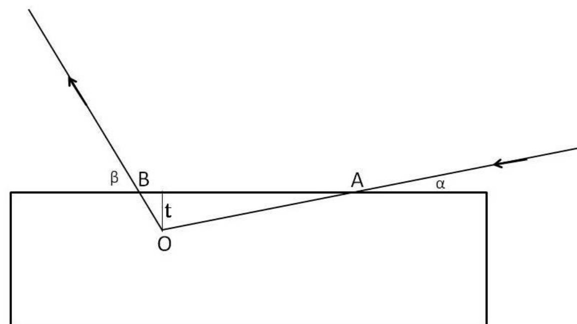


Figure 23 Schematic ray diagram for calculation of penetration depth.

Obtaining penetration depth of x-ray beam is very helpful for interpreting the topographic images. It gives information about the crystal volume imaged and thus helps in the understanding of the defect configurations, especially in epilayers. It can be applied to defective crystals and the photoelectric absorption based penetration depth t is given by

$$t = \frac{1}{\mu\left(\frac{1}{\sin\phi_0} + \frac{1}{\sin\phi_h}\right)},$$

where μ is the absorption coefficient (cm^{-1}), Φ_0 is the incident angle and Φ_h is the exit angle.

However for nearly defect-free crystals, the penetration depth in Bragg geometry is governed by extinction distance. According to the dynamical theory, the extinction distance Λ [55, 56, and 57] is given by

$$\Lambda = \frac{\lambda\sqrt{|\gamma_h\gamma_0|}}{C\sqrt{\chi_h\chi_{\bar{h}}}},$$

where λ is the wavelength, $\gamma_h = cos\psi_h$ (ψ_h is the angle between the diffracted beams with the inward-going surface normal), $\gamma_0 = cos\psi_0$ (ψ_0 is the angle between the incident beams with the inward-going surface normal), C is the polarization factor (C=1 for σ polarization and $cos2\theta_B$ for π polarization) χ_h and $\chi_{\bar{h}}$ are the electric susceptibilities for (*hkl*) and (*-h-k-l*) reflections, respectively and χ_h is defined by equation

$$\chi_h = -\frac{r_e\lambda^2}{\pi V}F_h,$$

where r_e is the classical radius of electrons, V is the volume of the unit cell. The penetration depth is thus given by:

$$z_e = \frac{\Lambda}{2\pi\sqrt{1-\eta^2}},$$

where η is the deviation parameter (the deviation from the rocking curve peak). The minimum penetration depth corresponds to the situation when the incident beam is exactly at the rocking curve center and the penetration depth is $\Lambda/2\pi$.

The dynamical penetration depth is much smaller than the photoelectric absorption penetration depth, this is because when the incident wave vector falls within the rocking curve

width (dynamical diffraction dominates), the scattering from each atomic layer is in phase and the intensity of the forward diffracted beam drops down drastically. Whereas, if the incident wave vector falls outside of the rocking curve, the attenuation of the forward beam is only related to the photoelectric absorption $I=I_0e^{-\mu t}$. In our studies, the photoelectric penetration depth is used because of the relatively high dislocation density.

2.1.5. Contrast formation mechanism in X- ray Diffraction Topography

Defects can be imaged using X-ray diffraction topography where there is measurable difference in diffracted intensity. These defects include those giving rise to localized strain field such as dislocations, subgrain boundary, grain boundary and growth sector boundaries. Contrast in an X-ray diffraction topograph is generally described by two mechanisms: orientation contrast and extinction contrast [55, 56, 57 and 58].

Extinction contrast is due to the difference in scattering power around the defect from rest of the crystal. Extinction contrast is mostly used for understanding and explaining images of dislocation in topographs. Image of a dislocation in a topograph consists of three different types of images: direct, dynamic and intermediary image due to three types of extinction contrast. In transmission geometry, absorption condition (μt) determines the type of image that can be observed. Where μ is the mass absorption coefficient and t is the thickness of the crystal. Near the dislocation core where the lattice is heavily distorted compared to the rest of the crystal, dynamical diffraction breaks down and the core region diffracts kinematically. The reason for rescattering being negligible is because the core region falls outside the full width at half maxima of rocking curve. This is similar to small size crystal diffraction which diffracts kinematically.

Direct dislocation image: This type of image is observed when topograph is recorded under low absorption condition $\mu t<1$. In this case diffracted intensity from dislocation core region is higher than the surrounding matrix resulting in dark dislocation line.

Dynamical dislocation image: This type of image if observed when topograph is recorded under high absorption condition $\mu t>6$. In this case dislocation line will appear as white line due to anomalous absorption also called Borrmann effect.

Intermediary dislocation image: This type of image if observed when topograph is recorded under absorption condition $6> \mu t>1$. In intermediary absorption condition all three components can contribute. Usually these images appear as bead-line contrast along direct image.

Orientation contrast in a X-ray diffraction topograph is the non-uniform distribution of intensity, purely arising from convergence (overlap) or divergence (separation) of diffracted rays. This contrast is seen in crystal containing small angle grain boundary, twin and grain boundary. Misorientation in lattice plane caused by residual stress can also be observed as orientation contrast. Observation of orientation contrast is the result of both the nature of X-ray and the nature of misorientation. If either the beam divergence or the wavelength bandwidth available in the incident X-ray is smaller than the misorientation between two regions, then only one region in the crystal can diffract at a time. Therefore orientation contrast is presence or absence of diffracted intensity in one of the region [58].

Huang et al [23] proved that orientation contrast mechanism dominates and extinction contrast alone is not capable of explaining the contrast in SiC by studying growth defects with large Burgers vector like the superscrew dislocations in X- ray topograph images. Huang et al used Ray- Tracing principle to prove this by studying direct dislocation images of these growth defects. It was shown that this is applicable to other elementary dislocations.

In the orientation contrast model, the mosaic regions around the dislocation is divided into a large number of cubic diffraction units with their local misorientations coinciding with the long- range displacement field of the dislocations. These units diffract X-rays kinematically according to their local lattice orientation. Traces of the inhomogeneously diffracted X- rays are projected onto the recording plate to obtain the direct dislocation image. Thus the direct image here is due to orientation contrast arising from the overlap and separation of inhomogeneously diffracted X- rays with continuously varying directions. Huang et al showed that a good correlation is evident in the case of simulation using orientation contrast mechanism unlike the conventional misorientation contour model which breaks down, that predicts image width much smaller than the observed value. In a similar way what was predicted for micropipes or screw dislocations can be used for other elementary dislocations with smaller burgers vector under low absorption conditions.

2.2. Important analytical tools used for defect studies:

2.2.1. Synchrotron X- ray Diffraction Topography

The X-ray topography experiments were carried out at beamline X-19C located at Brookhaven National Laboratory. The direct white beam from the storage ring is used at the NSLS and the maximum beam size at the sample is approximately 7 × 40 mm^2.The vertical divergence angle is mc^2/E~0.18mrad (where m is the mass of the electron, c is the velocity of light and E is the electron energy). Beamline X-19C has a source with wavelength ranging from 0.2Å to 2Å with peak around 0.8Å. Intensity verses wavelength graph at beamline X-19C is shown in figure 24.

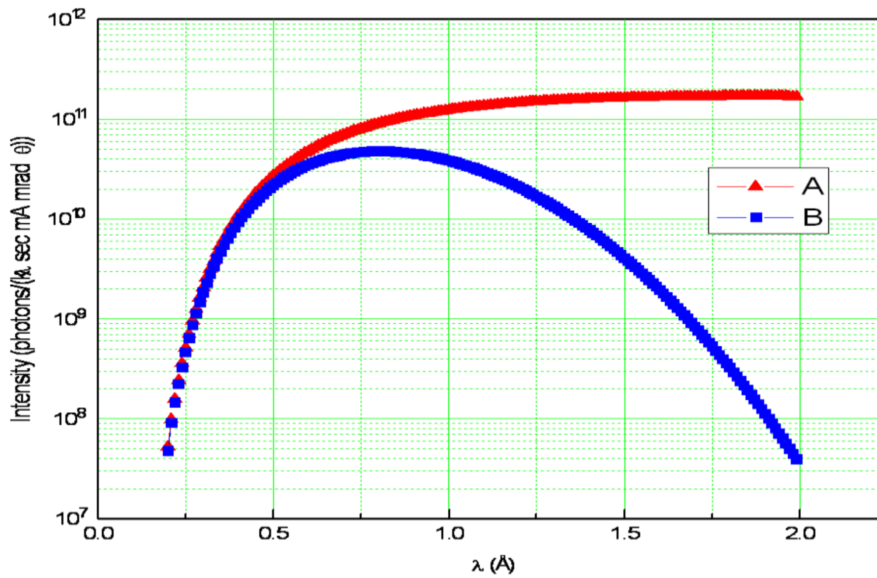
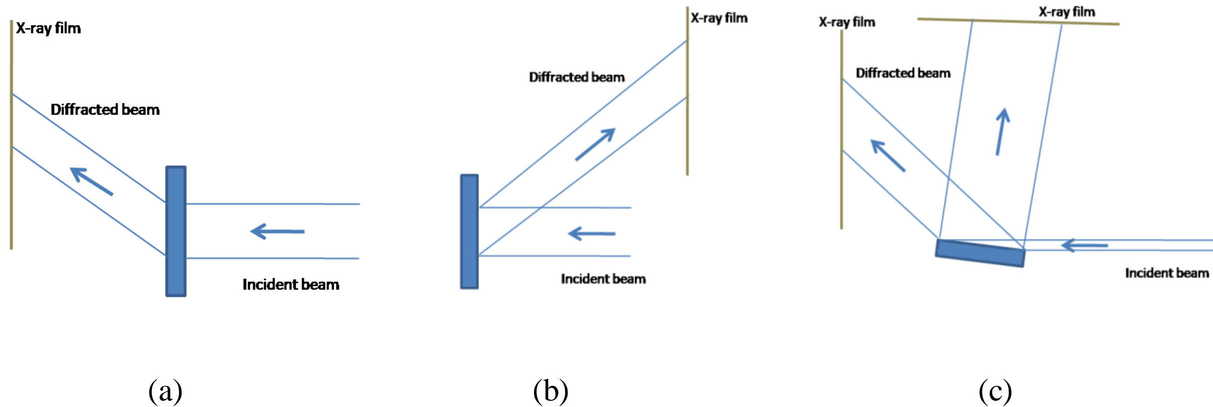


Figure 24 Intensity verses wavelength chart. A. Original beam, no absorption and B. After absorption

Mainly three geometries are used in XRT studies. The schematics of the three geometries are illustrated in Figure 25. The first setup, figure 25 (a) which is Transmission XRT, also called Laue geometry is used to image or record bulk defect information in the crystal. The X-rays completely pass through the sample under investigation. In grazing- incidence reflection (Figure 25 c), a very small incident angle is used (typically 2^0) and the (11-28) or (11-2.12) reflection is recorded. Grazing- incidence is carried out because of the low penetration depth of X-ray beam in such geometry, which is particularly helpful for epilayers studies. The penetration depth can be tuned by rotating the sample along the reflection vector, or by simply adjusting the incident angle (the wavelength should be accordingly adjusted). In back- reflection geometry as shown in

figure 25 (b), a large Bragg angle is used for basal plane reflection (000*l*) [typically 80^0]. The screw dislocations along c- axis and the basal plane dislocations within the penetration depth of X-rays can be clearly recorded.



(a) (b) (c)

Figure 25 Schematics of various geometries used in XRT. (a) Transmission topography. (b) Back- reflection topography and (c) Grazing- incidence topography.

Diffracted images are recorded on AGFA Structurix D3-SC films and KODAK D19 developer and fixer are used to process the exposed emulsions. The resolution of X- ray films is 2 µm which is higher than that of CCD cameras which is about ~ 50 µm; there has been lot of efforts to improve the camera resolution and detection by improving the scintillators. The resolution in films goes down due to photoelectric absorption that limits the grain size which is around ~ 0.2 µm. Another limitation of CCD cameras is the area scanned is much lower than that in films. One major advantage with respect to cameras is there is no chemical processing of images which saves time. An X- ray film dimension is usually 8 inch by 10 inch and always carefully concealed from exposure to light in a box before used for recording SWBXT images.

2.2.2. Transmission Electron Microscopy (TEM)

TEM is a very important tool for analysis of defects and plays a complimentary role to SWBXT especially in studies related to planar defects, twin boundries and understanding material properties down to the scale of atomic resolution. Both the methods are based on X- ray diffraction but the major difference is TEM uses the diffraction phenomena of electrons while SWBXT that of X- rays.

In TEM a beam of highly focused accelerated electrons (few hundreds keV) are passed through an electron transparent specimen which interacts with the specimen as it passes. The complex electron- specimen interactions occurring at this stage results in generation of several signals as shown in figure 26. An image is formed by the interaction of electrons with the specimen and image is magnified onto an imaging device such as photographic film, or most commonly in new TEMs onto a fluorescent screen or CCD camera [59].

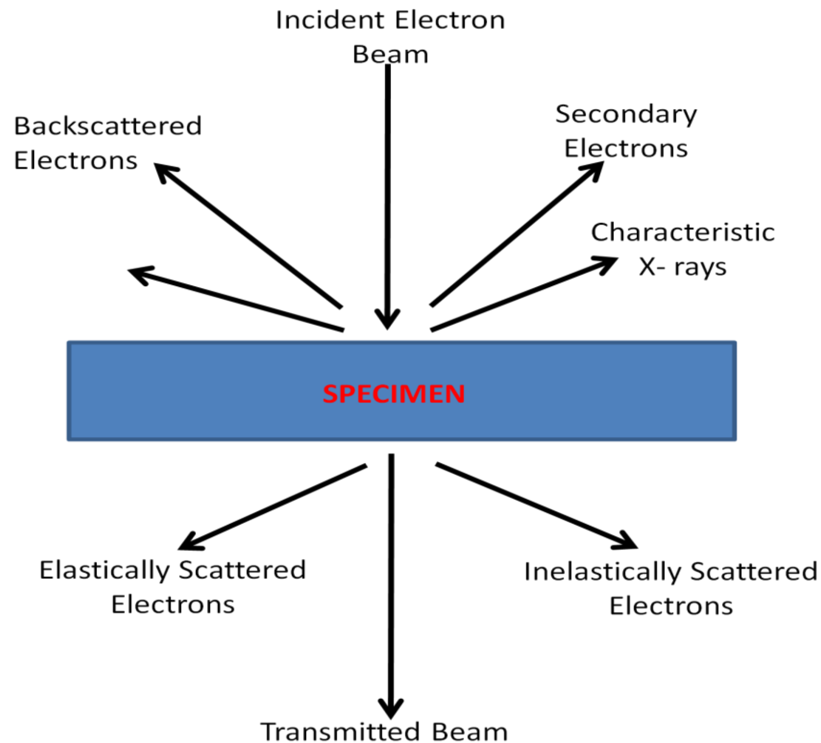


Figure 26 shows the different signals emitted by electron- sample interactions normally observed in TEM.

Operation of TEM can be explained by taking into account two basic modes which are *diffraction patterns and imaging*. In accordance with the Bragg's law the electrons interacting with crystalline specimen is scattered. The electron beams that are scattered at small angles with respect to transmitted beam are focused by the objective lens to form a diffraction pattern at its back focal plane called *selected area diffraction (SAD)*.The scattered beams are than recombined to form an image onto an image plane. It is also possible to obtain the diffraction pattern onto the viewing screen by simply adjusting the imaging system lenses. It is important to study the SAD

pattern in order to determine the zone- axis. The right pattern is obtained on the screen if the zone- axis is adjusted in such a way that it is exactly or almost parallel to the source beam being focused onto the electron transparent specimen.

Once the critical step of obtaining the SAD pattern is complete it is used to form two basic imaging operations: *Bright and Dark field imaging*. In order to form Bright and Dark field images one needs to use the central spot or some or all of scattered electrons respectively as shown in the figure 27 (a) - (b) which is controlled by using an aperture in back focal plane to direct which electrons form the image [59].

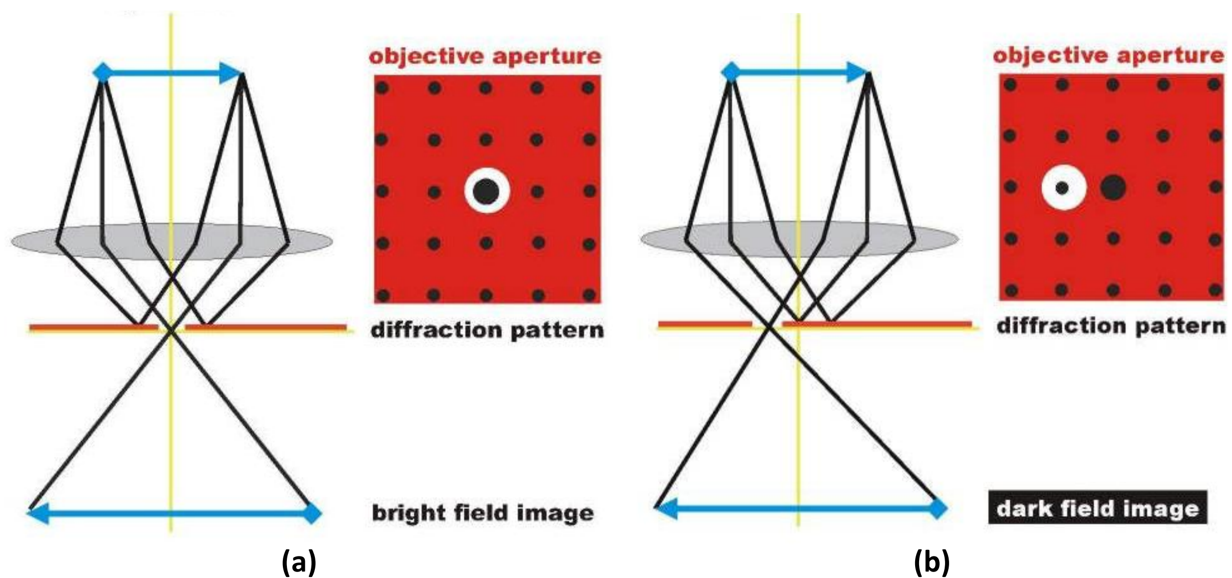


Figure 27 (a) shows the aperture blocking the scattered beam and collecting only the transmitted beam resulting in bright field image. (b) shows the aperture allowing the scattered beam to pass through it to obtain dark field image in TEM [58].

The imaging contrast formation mechanisms is an important aspect of the study and different imaging modes use mainly three types of mechanisms namely:

(a) Mass- thickness contrast
(b) Diffraction contrast (also called amplitude contrast)
(c) Phase contrast and Z- contrast

HR- TEM studies were carried out at Center for Functional Nanomaterials (CFN) situated in Brookhaven National Lab (BNL) for determining the stacking sequence of planar defects

observed in SiC. Wedge shaped sample preparation technique was used to make electron transparent specimen for studies using JEOL- 2100.

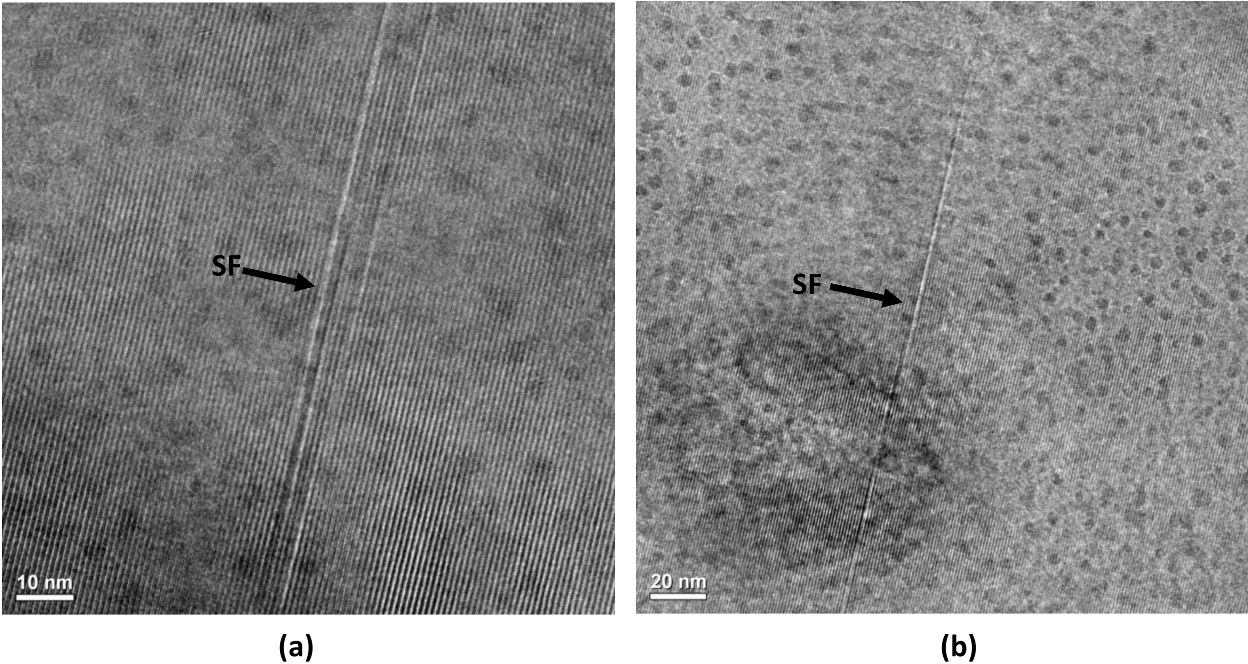


Figure 28 (a) - (b) show HR-TEM images taken using JEOL- 2100 at CFN from two different areas containing stacking faults in 4H- SiC. The stacking faults are marked as SF in both (a)-(b) pointed by the arrows in the images.

2.2.3. Nomarski Phase Contrast Optical Microscopy

This technique is based on the differential intereference contrast (DIC) mechanism and is a powerful optical microscopy tool as it provides a pseudo three- dimensional image. This is helpful in defect density studies especially in counting etch pits due to different defects and also for comparative studies i.e. correlation work of etch pits with defect images obtained by SWBXT. In principle the optical microscope works by amplifying the contrast using phase difference that occurs when light polarized light passes through a material that has different refraction indices (R.I), slope and thickness. The tool consists of two polarizers, two prisms and an objective. The unpolarized light is made polarized by passing through the first polarizer; this light is then split into two beams as it continues through the microscope crossing the first prism. At this stage the polarized light split into two beams are vibrating 90^0 apart to each other (the distance of separation is called the *shear amount*) in the column. These two beams are made to

pass through the specimen having different thickness, slopes and R.I. which causes one of the phase or beam to be delayed. These two beams enter the second prism where two are re-composed and then enter second polarizer that brings them onto the same plane and axis. The interference effect that happens produces a phase contrast which is seen through the objective or can be captured into a computer connected to the microscope. Figure 29 shows an optical image obtained by Nomarski Optical Microscope of etch pits [60].

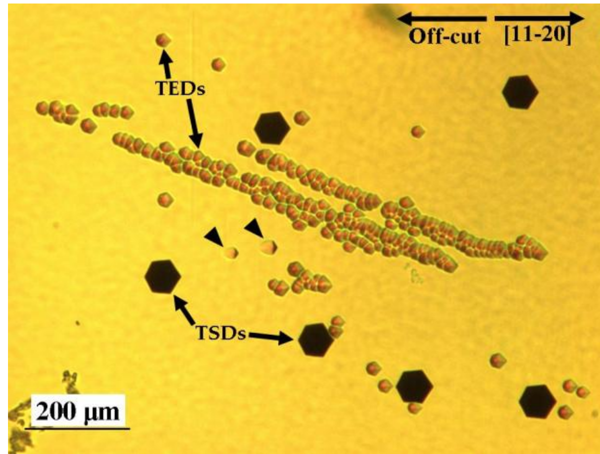


Figure 29 shows a Nomarski optical image of etched surface in 4H- SiC. The hexagonal shaped etch pits correspond to the TSDs and the small pits marked in the image correspond to TEDs showing different contrasts.

2.2.4. Molten Potassium Hydroxide Etching

Etching is an effective method and has several favorable features such as simple and relatively low cost of equipment, no limits to the size of samples to be examined, very quick data acquisition, and the broad range of defects that can be revealed and analyzed makes the technique very attractive for assessment of the quality of single crystals and device structures. Figure 30 and 31 shows etch pit images taken in NIC and SWBXT techniques after KOH etching.

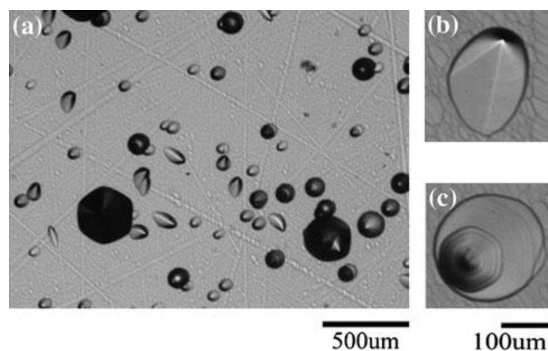


Figure 30 Nomarski intereference contrast optical image showing a selected area on an etched Si- face of a commercial PVT- grown 4^0 offcut 4H- SiC (a). Three type of etch pits are observed: scallop- shell- shaped etch pits corresponding to BPDs (b), large hexagonal etch pits corresponding to TSDs, and small hexagonal etch pits corresponding to TEDs (c).

Etching in our experiments were used as a complementary technique to XRT to compare the etch pit patterns with the results obtained. It was carried out by soaking the SiC crystal surface in molten KOH at 600^0C for 10 min [33].

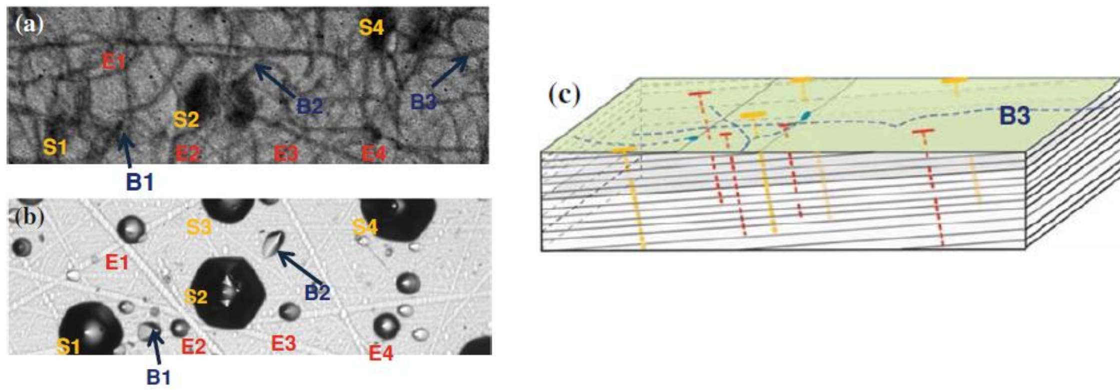


Figure 31 SXRT image (a) and NIC image of etch pits (b) taken in the same area of a preetched 4H- SiC. Illustration (c) demonstrates how threading dislocations (S1 to S4: TSDs; E1 to E4: TEDs and BPDs (B1 to B3) are oriented in the sample [33].

3. Deflection of Threading Dislocations with Burgers vector c/c+a observed in 4H-SiC PVT –Grown Substrates with associated Stacking faults

3.1. Outline

Macrostep overgrowth mechanism in SiC was used to study the deflection of threading defects onto the basal plane resulting in stacking faults. Four types of stacking faults associated with deflection of c/c+a threading defects were observed to be present in 76mm, 100mm and 150mm diameter wafers. The PVT grown bulk crystals and CVD grown epilayers in study were subjected to contrast studies using synchrotron white beam X- ray topography [SWBXT]. The SWBXT image contrast studies of these stacking faults with comparison of calculated phase shifts for postulated fault vectors by macrostep overgrowth of surface outcrops, has revealed faults to be of four types of which one of the following are explained in detail: (a) Shockley faults.

3.2. Introduction

Silicon Carbide as a wide band- gap semiconductor has been a promising material for various high-temperature and high- power electronics technologies since its inception, but the detrimental influence of defects such as dislocations has hampered its device performance [18, 43, 61, and 62]. Over the last two decades SWBXT characterization technique has been an indispensable tool for the SiC crystal growth community as it has played a key role in revealing the detailed configurations of various defects and understanding their origins right from the seed to the devices grown on them. Among the notable contributions are the identification of threading screw dislocations (TSDs) and threading edge dislocations (TEDs) as growth defects [27, 63, 64] and basal plane dislocations (BPDs) as deformation induced defects [65]. Along with these growth and post- growth defects three types of stacking faults have also been observed so far in SiC which are Shockley faults; Frank faults; and third type which is kind of combination of Shockley and Frank. Shockley faults in SiC have been explained to exist because of low stacking fault energy which causes the dislocations on the basal plane to be dissociated into Si- core partials and C- core partials separated by Shockley fault [66]. The partials are separated in the order of 30-70 nm due to which it becomes difficult to resolve in SWBXT though their exact nature can be determined by contrast analysis from multiple reflections. It has been confirmed above the brittle to ductile transition temperature (BDTT) both partials move in tandem with leading partial faulting the plane and trailing partial unfaulting it but below the

BDTT C- core partials become sessile leaving the Si- core partial to glide causing these Shockley faults [67, 68]. Frank faults have been observed in SiC for a long time and they result from the overgrowth of screw dislocation of various step heights [c/4, 3c/4, c/2 height steps] [69].

The development of stress reduction strategies has led to minimizing the driving force for BPD motion behind the growth interface. The reduction of thermal stress during growth to levels below the critical resolved shear stress of 1MPa which has enabled the lowering of BPD densities by up to three orders of magnitude in both 76 and 100mm wafers [37].The lower dislocations density wafers have provided a unique opportunity to perceive various interesting phenomena which among them is the observation of deflection of threading dislocations of Burgers vector c/c+a onto the basal plane which produce various kinds of stacking fault configurations classified into four types. Detailed analysis of these stacking fault configurations on different reflections and their image contrast studies have enabled us to predict the fault vectors to be of four types : (a) Shockley faults with fault vector; (b) Frank faults; (c) Combined Shockley + Frank faults with fault vector s+c/2; (d) Combined Shockley + Frank faults with fault vector s+c/4.

This work mainly focuses on the formation mechanisms of two of these four faults and a lucid understanding of their association with threading deflected dislocations is developed, thereby providing the necessary models. These threading dislocations at some stage of the boule growth get deflected out of the crystal resulting in further reduction of defects density as they are capable of replicating to the epitaxial layer and negate the performance of devices grown on them.

3.3. Experiment

4H- SiC substrates grown by PVT method with 4 degree offcut and homo epitaxial layers grown by CVD were subjected to SWBXT studies using different geometries carried out at Brookhaven National Laboratory, X-19C beamline. For transmission geometry the wafers were scanned at 1"/min and grazing incidence the exposure time was around 10-15 seconds. Multiple axial slices i.e. samples cut parallel to [0001] axis and along [01-10] and [10-10] directions were also studied to confirm the c+a threading dislocations burgers vector. Around 200 different wafers were studied and in some cases from the same boule at different level to understand the stacking faults density as we move from the seed towards the top. The thickness of wafers was in

the range of 300μm to 750μm and for axial slices varied from 300μm to 1mm. Some of the wafers were also etched by molten potassium hydroxide (KOH) for etch pit correlation and in some cases to improve the quality of axial slices for 1, 5, 10 minute intervals. Nomarski differential optical microscopy was used to study the etch pits and other features obtained using the Synchrotron source. The features in the X-ray films recorded were magnified using Nikon camera at different magnifications and developed using chemicals after exposure.

3.4. Results and discussion

PVT grown 4H- SiC of diameter 76mm, 100mm and 150mm were subjected to SWBXT studies to study different defects which were grown at low stress conditions on a 4 degree off-cut angle towards [11-20] direction. Figure 32 shows a SWBXT image recorded under transmission geometry from a region near the wafer edge of 76mm wafer. Several long, mostly straight dislocations can be observed at approximately radial direction, for example at AB and CD. The BPDs seen in the background of the same image appear to be highly curved but these straight dislocations are long and appear to not be running along the growth direction which can be growth dislocations. The measurement of their lengths show that they are on the basal plane and the shorter segments suggest they are connected to the threading segments so that only part of them are on the basal plane. As we know the basal plane is orthogonal to the growth direction, these long straight dislocations might have been deflected from threading orientation onto basal plane due to one plausible reason which is overgrowth of macrosteps, which is not letting these dislocations to continue in threading direction. These dislocations exhibit strong contrast on all reflections belonging to [0001] - zone which suggests these are neither ‘c’ nor ‘a’ dislocation but those between the two (which might be a combination of both i.e. c+a). c+a defects have been predicted by Vetter et al [22] previously but were not able to discern the details in the wafers studied because of high defect density. The low defect density in the wafers studied recently suits well to study these defects as it is possible to differentiate various defects accurately and hence determine the Burgers vector magnitude.

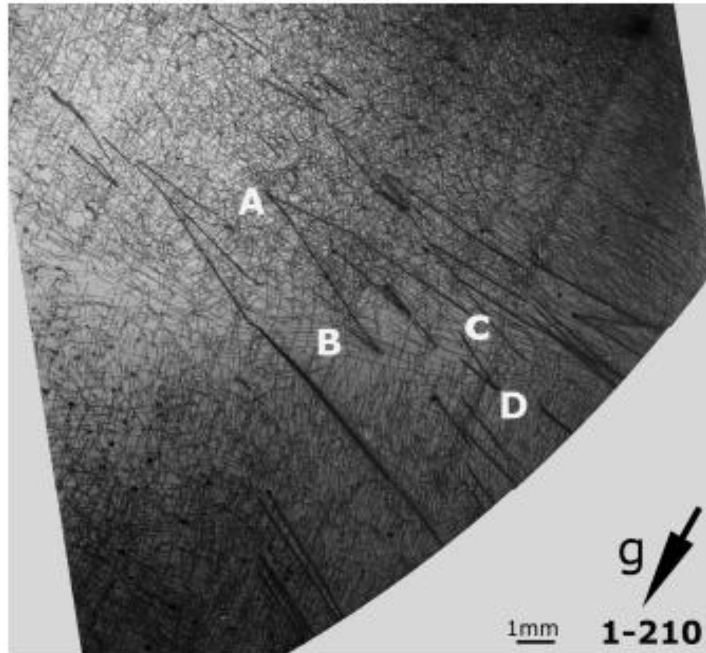


Figure 32 SWBXT Images recorded from a region near the edge of a 75 mm wafer cut (with 4 degrees offcut towards [11-20] from a 1-210 reflection showing long straight dislocations for example at AB andCD. These long dislocations were found in the vicinity of stacking faults in the wafers observed.

Figure 33 (a) - (b) shows SWBXT images of an axial slice cut along [01-10] and [10-10] direction taken by transmission topography geometry. Figure 33 (a) shows an SWBXT image (g=0004) taken in Transmission geometry which show threading defects of both Burgers vector both c and c+a. The dislocations marked a, b, c, d in figure 33 (a) are threading defects which appear to have deflected onto the basal plane. Dislocations d, a and b appear on both (0004) and (-12-10) reflection while c disappears on (-12-10) reflection, g.b extinction contrast analysis proves they are neither c nor a but combination of both i.e. c+a. The contrast analysis for dislocation c proves they are pure c dislocation as g.b= 0. The g.b analysis of axial slice not only confirmed c+a defects but also those threading defects with different $n_1c + n_2a$ (where $n_1$and $n_2$are integers) defects.

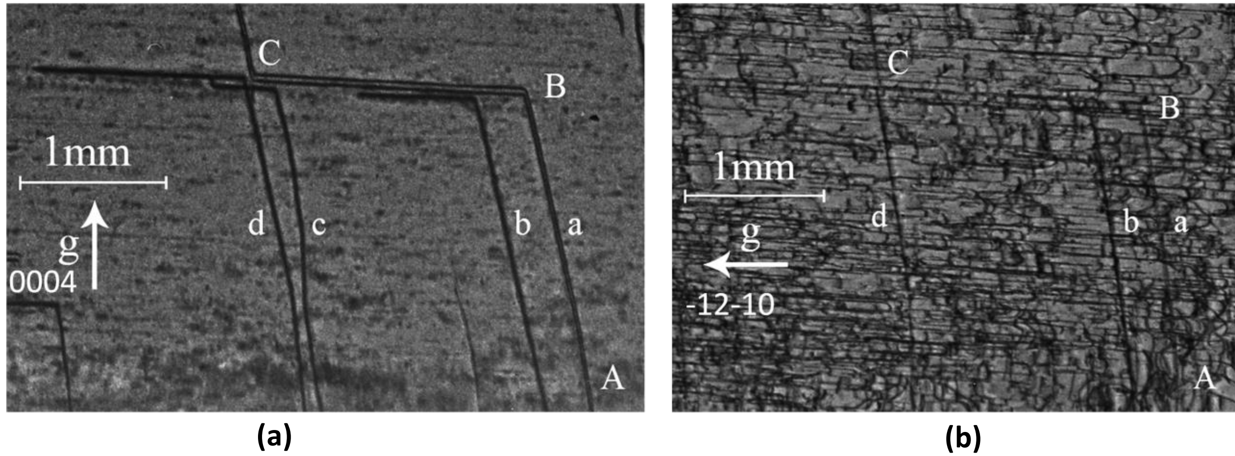


Figure 33 (a) (0004) SWBXT image recorded in transmission geometry from an axial slice showing deflection of dislocations *a-d* during growth; (b) (-12-10) showing dislocations *d, b* and *a* but not *c*.

In all the wafers studied stacking faults was observed in the vicinity of deflected threading dislocations hinting these faults might be associated with threading defects. The contrast from stacking faults in SWBXT arises from the phase shift experienced by the X-ray wavefields as they cross the fault plane [70]. This phase shift has been computed to be equal to $\delta = -2\pi\ g.R$, where g is the active reciprocal lattice vector for the reflection and R is the fault vector. Contrast is expected to disappear δ=0 (corresponding to $g.R = integer$) and is expected to be very weak $\delta = \pm\frac{\pi}{6}$ (corresponding to $g.R = \pm\frac{1}{12}, \pm\frac{11}{12}$). Contrast is very well marked for $\delta = \pm\frac{\pi}{3}, \pm\frac{\pi}{2}$ and $\pm\frac{2\pi}{3}$ (corresponding to $g.R = \pm\frac{1}{6}, \pm\frac{5}{6}, \pm\frac{1}{4}, \pm\frac{3}{4}, \pm\frac{2}{3}$ and $\pm\frac{1}{3}$). Contrast analysis was performed on several wafers with fault areas close to deflected dislocations revealed the fault vector to be of four types.

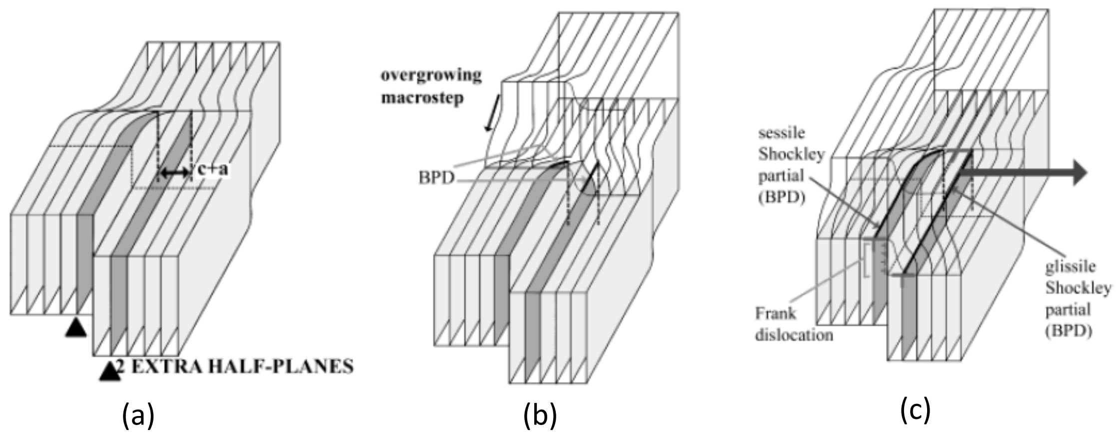


Figure 34 (a)-(c) Overgrowth of c + a dislocation with a c-height step. After deflection, one Shockley is sessile and the other glissile.

The mechanism for the formation of stacking faults associated with deflection of threading dislocations involves the macrostep overgrowth of these threading dislocations. The overgrowth results in c/c+a defects to get deflected onto the basal plane, in case of c+a defects if the step associated with c- component bisects the two extra half planes associated with a-component it results in two partials on basal plane separated by the c- height step. Fig shows schematics to explain this mechanism, in figure 34 (a) - (c) shows a c+a dislocation with the core containing both c- dislocation and two extra half planes associated with a- component anchored together. At this juncture when the macrostep overgrowth happens as shown in figure 34 (b) where a approaching macrostep onto the c+a dislocation cannot let the defect into itself but causes it to get deflected onto the basal plane. In figure 34 (c) shows this macrostep overgrowth to be complete and the c+a dislocation deflected onto basal plane but the partials associated with a- component are no longer on the same surface but are divided by the c- height step. Depending on the direction of stress either one of the partial becomes glissile and other sessile, the latter dislocation which is mobile can glide resulting in faulting of the plane causing large stacking faults as shown in the schematic in figure 35 showing a wafer containing faults. As SiC comprises corner sharing tetrahedral one important aspect to note is for the macrostep to overgrow the tetrahedral bonding of underside of macrostep must maintain the same bonding with top side of terrace i.e. stacking sequence rules must be adhered [71].

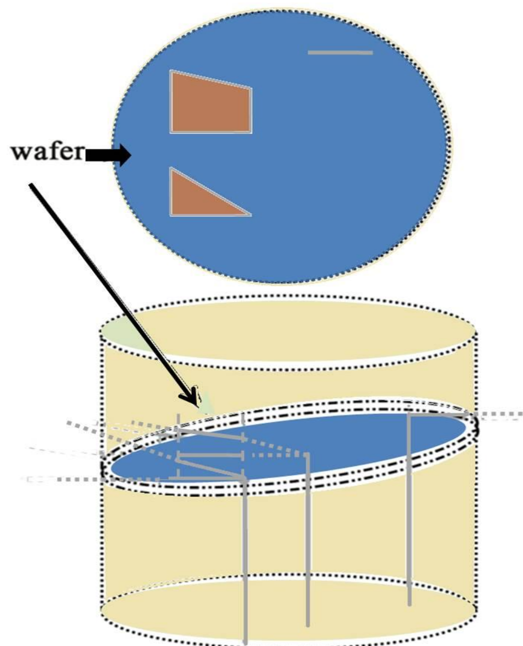


Figure 35 Schematic of deflection of threading dislocations during growth and appearance of the deflected dislocations in the offcut wafer.

Keeping this in mind the deflection of c/c+a threading dislocations can result in four types of stacking faults of which one of the following are explained here in detail:

3.4.1. Shockley fault

In SiC, the presence of Shockley faults as explained is due to the low stacking fault energy due to which it is energetically more favorable for the BPDs on the basal plane dissociate into Si- core and C- core partials in turn separated by a Shockley fault. Above the BDTT the partials move in tandem with leading partial faulting the plane and trailing partial unfaulting it whereas below BDTT only the glissile leading partial glides while the trailing becomes sessile resulting in expansion causing faults. During device operation electron- hole recombination enhanced dislocation glide [REDG] operation takes place where one partial is sessile and other becomes glissile leading to expansion causing Shockley type faults. Both type of partials i.e. c- core and Si- core can become mobile, under high temperature c- core partials are mobile whereas under forward voltage the Si- core partials are mobile causing Shockley faults in SiC bipolar devices.

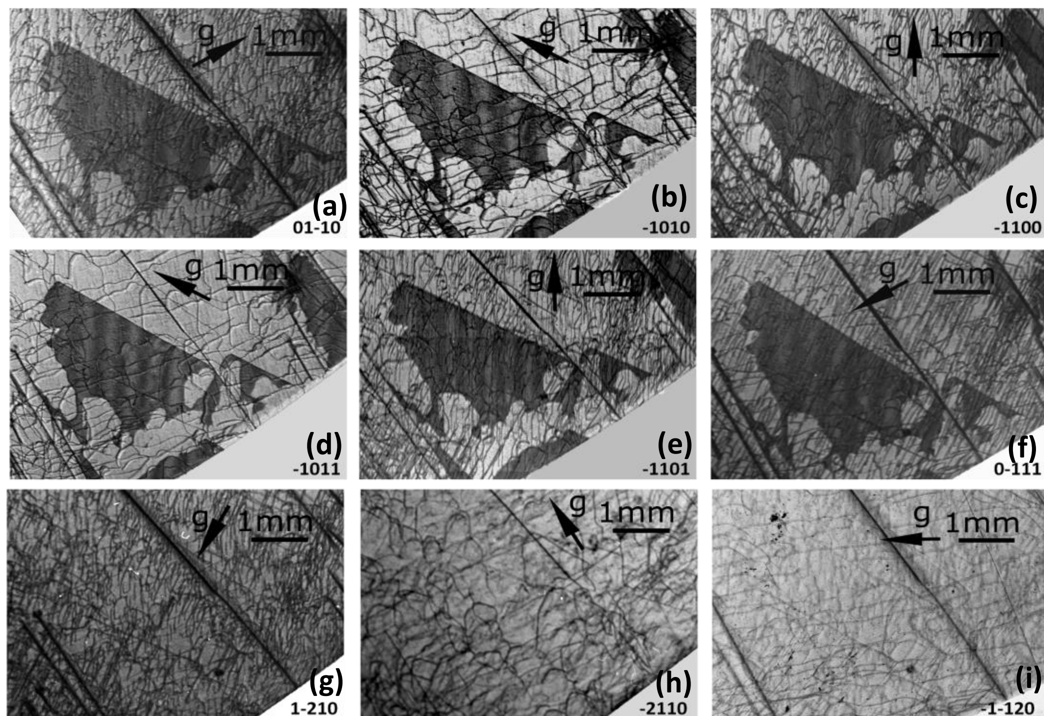


Figure 36 (a)- (i) SWBXT images in transmission geometry of multiple reflections used for determining the Shockley fault vector of 1/3[01-10] recorded from the edge of 76mm n$^+$4H- SiC

wafer with 4^0 offcut angle. Contrast of the faults is visible in all <01-10> and <10-11> type reflections and disappears on <11-20> type reflections. One side of the fault is straight which corresponds to the sessile partial and the glissile partial that glides creating the large stacking faults that are visible. The partial that glides encounters obstacles during the glide which creates that uneven shape on one side.

Figs. 36 (a)- (i) are SWBXT images recorded from a section of a 76mm n+ 4H- SiC crystal showing stacking fault configurations which has one straight edge on side and curved fault region on the other. The stacking fault shows contrast in all the six reflections in the SWBXT images 36 (a)-(f) but shows no contrast on three <11-20> reflections, the extinction contrast analysis shown in table1 from nine different reflections confirms these stacking faults have fault vector 1/3[01-10] which are Shockley fault type.

Table 1. Fault vector determination by g.R contrast analysis for images in figure 36.

g	01-10	-1010	-1100
g·R	2/3	-1/3	1/3
g	-1011	-1101	0-111
g·R	-1/3	1/3	-2/3
g	1-210	-2110	-1-120
g·R	-1	0	-1

For the Shockley faults resulting from deflection of threading dislocations of the type c+a as shown in figure 34 (a) - (c), the two extra half planes associated with a- component happen to be bisected by a spiral c- height step. As shown in the illustration in figure 37 the overgrowth of macrostep causes the deflection of this dislocation onto the basal plane where the partials associated with a- component are separated by the height of the step causing one partial to be above the step riser and another below. During the deflection process the surface termination

lines of the two extra half planes on the terrace become the line directions of two Shockley partials associated with a- component.

Once on the basal plane it becomes possible for the c+a to dissociate into its c and a components, since the latter is potentially glissile on the basal plane. The stress in the crystal depending on the direction causes one of the partials either above or below the step riser to glide faulting the plane, but the trailing partial separated can no longer unfault it causing expansion of one fault resulting in large Shockley faults as shown in figure 37. The c+a dislocation in the schematic which is overgrown by macrostep and direction of stress has resulted in Shockley fault expansion below the step and the partial above the step is locked preventing it from unfaulting the fault created by gliding partial.

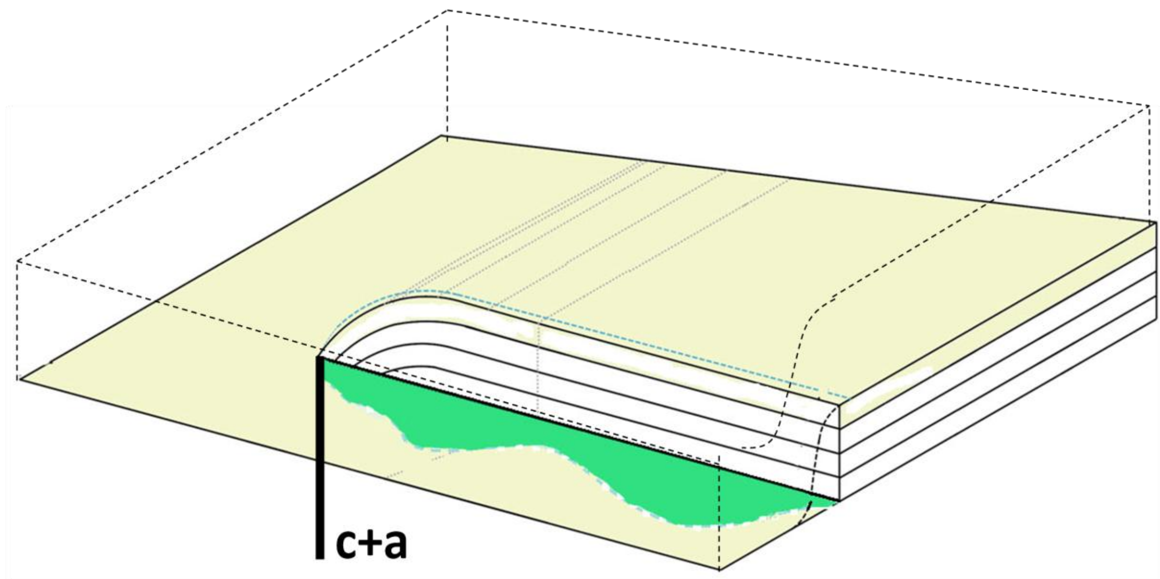


Figure 37 Is a schematic representing the Shockley type fault from a c+a type defect, in which the sessile partial is locked on top of the step riser whereas the partial that glides creating fault is below.

For the above mechanism to happen inside the growing crystal and macrostep overgrowth to result it is important to understand two cases.

Case I:

Under normal cases in SiC due to low stacking fault energy the BPDs tend to exist as two partials of which one is a leading and other a trailing partial. Under stress the leading partial glides creating stacking faults while the trailing partial separated by approximately 20- 30 nm unfaults the plane as shown in figure 38 (a) - (d). In figure (a) the illustration shows a pair of extra half planes and the distortion around them. In figure (b) only two extra half planes are shown and which are deflected onto the basal plane as two partials of which one is a leading partial and the other being a trailing one. Under stress as shown in figure 38 (c) - (d) the leading partial separated from the trailing partial glides creating stacking faults as shown and the trailing partial gliding along with it under similar stress unfaults it. This is explained in figure 39 (a) - (c) by showing the corner sharing tetrahedrons.

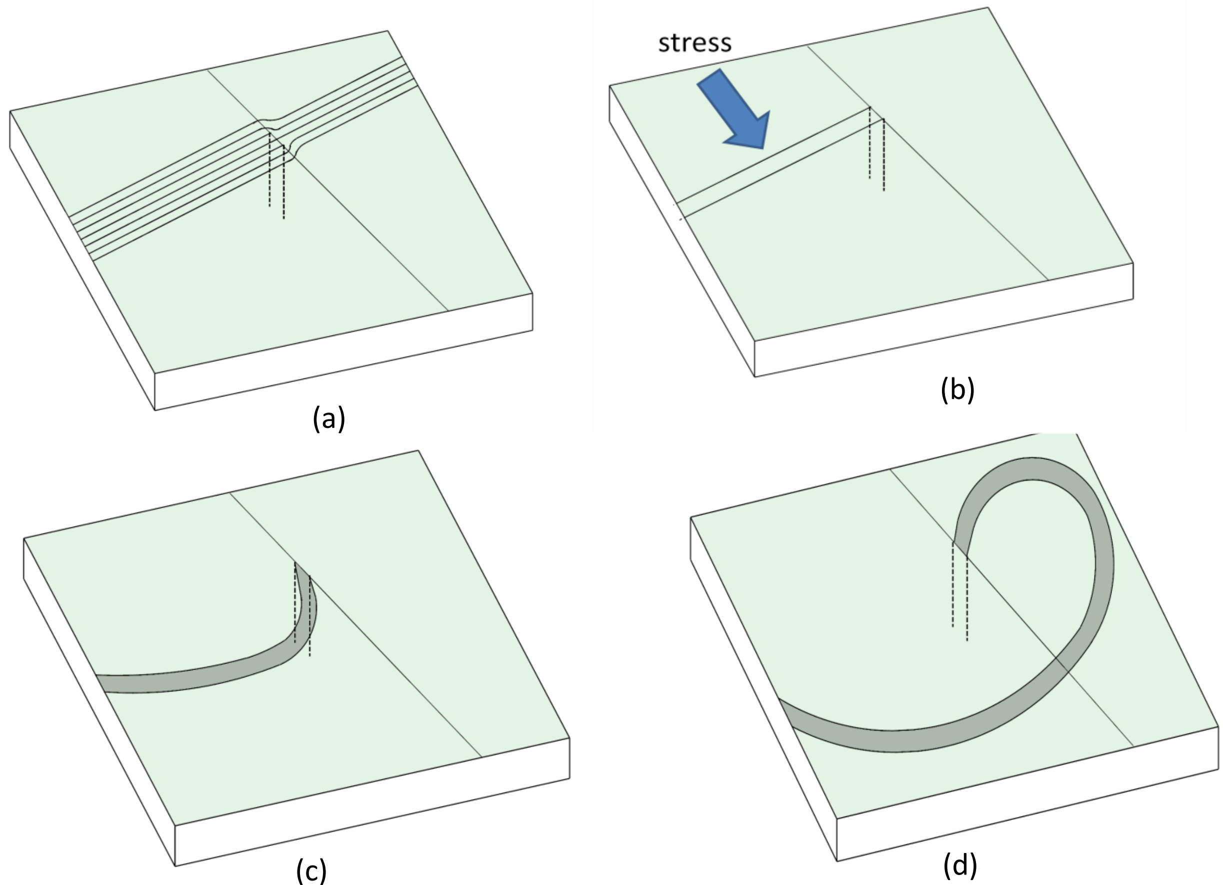
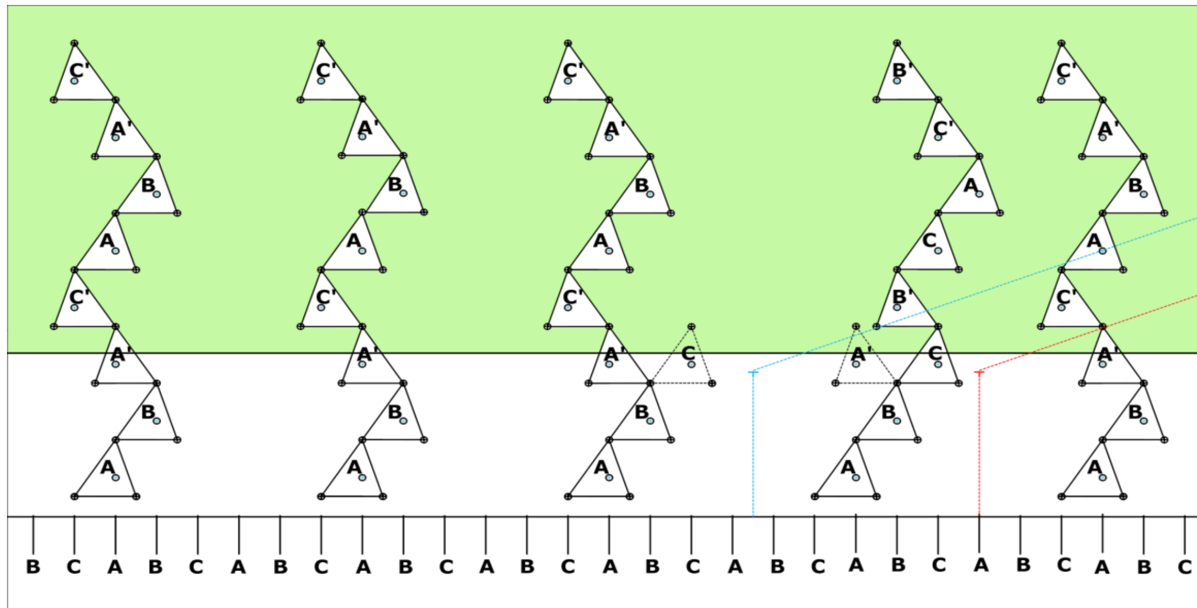


Figure 38 (a)- (d) are a set of illustrations showing the the partials on a atomically flat terrace. Macrostep overgrowth results in two partials on the flat terrace where the leading partial glides creating the stacking fault while the trailing partial unfaults the plane.

Figure 39 (a) - (c) show illustrations of corner sharing tetrahedrons in 4H- SiC where the stacking sequence ABA’C’ repeat every four bilayers. In figure 39 (a) two partials are denoted with the leading colored in red and the trailing partial denoted in blue. Under stress the leading partial in red glides as shown in figure 39 (b) faulting the plane i.e. by converting the A’ tetrahedral to C (untwining) which happens in accord with the stacking rules. The trailing partial gliding along with the leading one under the same stress denoted by blue in figure 39 (c), unfaults the plane by converting the unprimed tetrahedral C back to primed tetrahedral i.e. A’ thereby negating the stacking fault that had resulted by motion of leading partial.

(a)

(b)



(c)

Figure 39 (a)- (c) is the illustrations showing corner sharing tetrahedral explaining the movement of partials on the flat terrace. In (b) the leading partial shown in red faults the plane by converting A' to C whereas the trailing partial represented in blue unfaults the plane by converting C to A'.

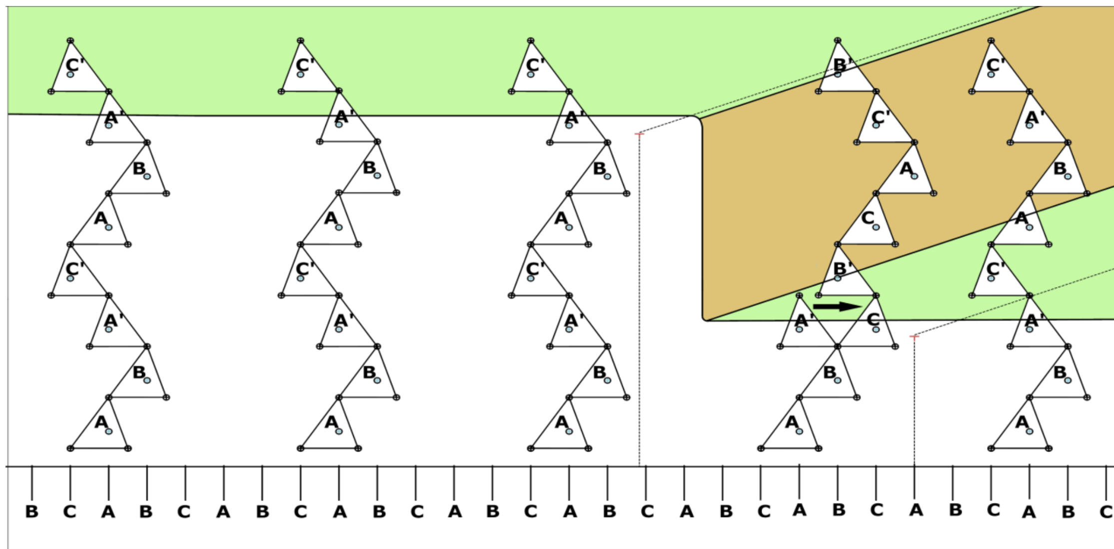
CASE II:

The above mechanism happened on an atomically flat terrace where the partials are on same surface whereas Case II takes into account a surface that is intersected by screw dislocations of varying step heights. As mentioned previously the screw dislocations can be divided into different integral step heights in SiC, in this case let us consider the step height to be four bilayer step height. So the screw dislocations tend to bisect the extra half planes we get the dislocation core having both 'c' and 'a' components. The overgrowth of such a dislocation results in two partials separated by the step height and no longer on the same surface also explained previously.

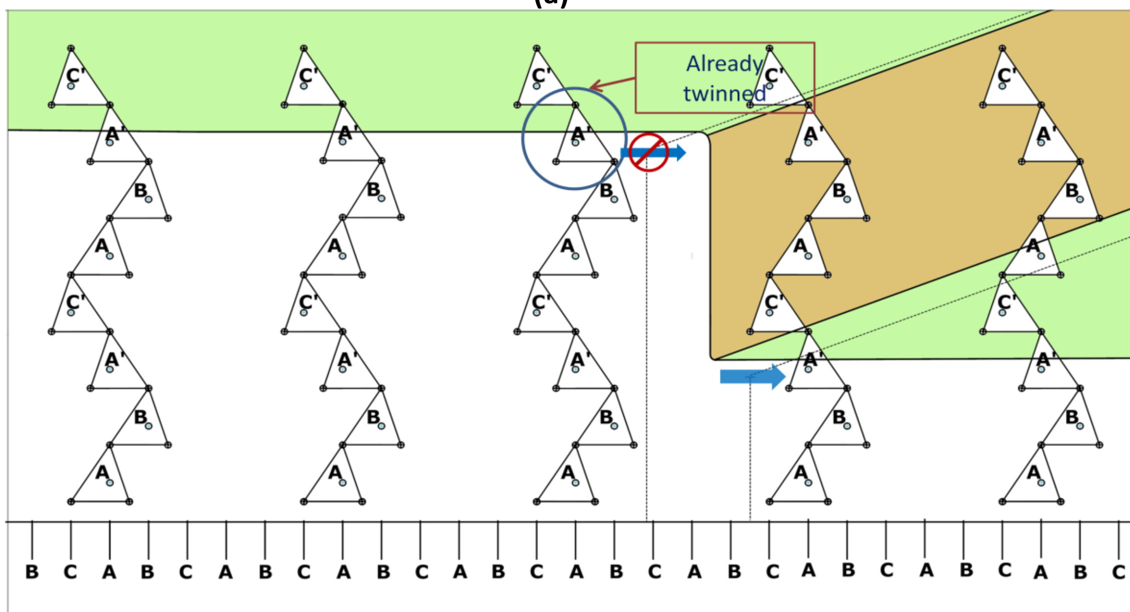
For the overgrowth of a macrostep to be permitted it must be follow the stacking rules in SiC and only than the stacking faults shown in figure 33 can occur during growth from a c+a type defect. Let us now consider another set of illustrations in figure 40 (a) - (c) again using

corner sharing tetrahedrons that explains why only one of the partials glides while the other one becomes sessile depending on direction of stress.

In Figure 40 (a) the direction of stress is towards the leftof the image, in this case the partial that is below the step height glides creating the large faults shown in the SWBXT images in figure 36. The large stacking faults are created because the partial that is above the step height gets locked and is no longer to glide with the leading partial to unfault the plane which is generally the case if the partials were on a flat terrace. In figure 40 (b) the opposite happens with the stress direction is towards the right of the image which allows the partial above the step riser to glide creating the large stacking faults while the one that is below the riser gets locked.



(a)



(b)

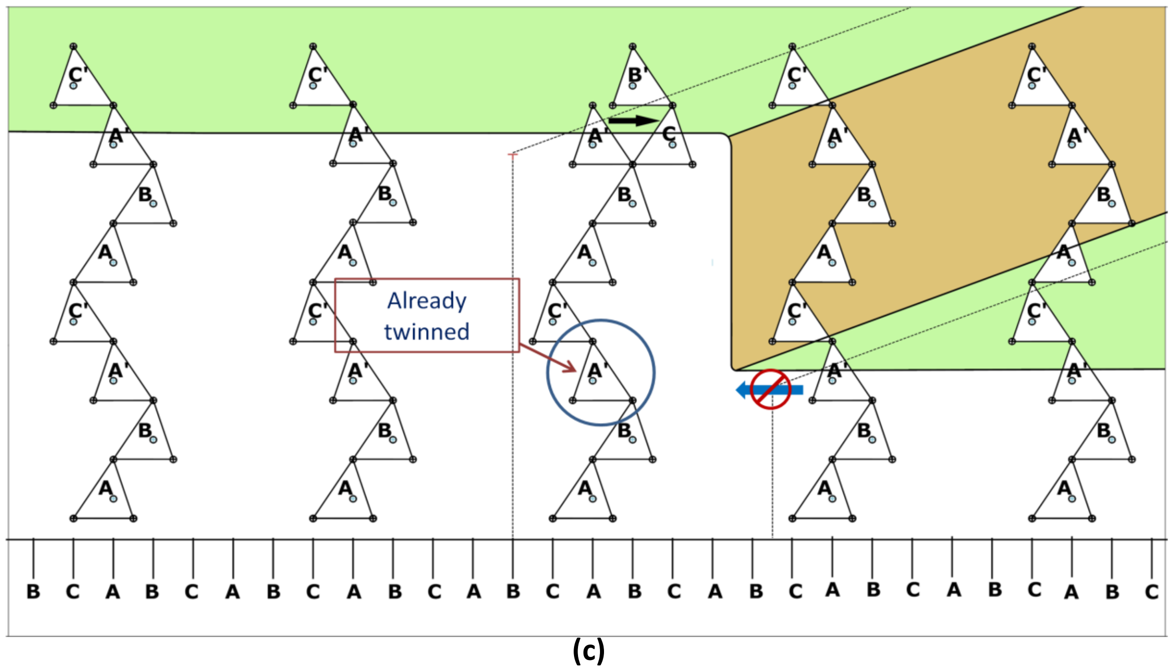


Figure 40 (a) - (c) are set of illustrations again showing corner sharing tetrahedra to explain Case II. The partials are now no longer on the same flat terrace as shown in (a) which are divided by the step riser. The direction of stress in (a) - (b) is towards the left of the image which causes the partial below the step riser to glide whereas the partial on top gets locked which is marked in (b). In illustration (c) the opposite happens with the partial on top of riser glides as stress is towards right of image creating faults, that is converts A' to C as it glides whereas the partial below cannot glide as the tetrahera is already twinned.

3.5. Conclusion

The c+a defects in which the dislocation core have both c and a components have been proven to exist in SiC by studying both the horizontally cut wafers and axial slices cut parallel to the growth direction. The c+a defects during growth get deflected out the crystal boule resulting in defect density reduction, but the deflection causes the partials to be separated by the height of the step riser associated with screw dislocation. Depending on the direction of stress only one of the partials is able to glide creating the large stacking faults. Stacking fault contrast analysis by studying the faults in multiple reflections has resulted in the determination of fault vector to be of the type 1/3[01-10].

4. Simulation of threading c+2a and nc dislocations via X-ray Topography in 4H- SiC

4.1.Outline

Wafers cut horizontally and axial slices cut parallel to the growth direction have both been studied in numerous 4H- SiC boules using mainly SWBXT. The studies have confirmed the existence of both threading $n_1c + n_2a$ and threading nc dislocations in all these samples. A novel technique known as Ray Tracing simulation has been successfully developed to simulate these defects and determine their senses which can provide further insight into their propagation and formation mechanisms during growth. In this work, grazing incidence topography is performed using monochromatic beam for horizontally cut wafers to record pyramidal reflections of 11-28 type and also transmission geometry is used to record multiple reflections in axially cut slices to determine threading c+2a dislocation.

4.2.Introduction

Numerous studies have shown the advantages of using SiC devices for high power applications but the presence of various types of defects have impeded device performance. Extensive work has been done for several decades to lower the defect density by incorporating new growth modifications in PVT and CVD techniques. SWBXT has played a big role in the analysis and in developing mechanisms to explain the formation of these defects during growth which in turn has led to the reduction of yield limiting defects that can replicate from the substrate to epilayer. Zero MP density wafers are commercially available in the market supplied by companies such as Dow Corning, Cree Inc. and II-VI Inc. that has paved the way for SiC devices to be used for many high temperature applications. The presence of various other type of defects in high density such as stacking faults (SFs), triangular defects in epi, BPDs, closed- core threading screw dislocations (TSDs), threading edge dislocations (TEDs) needs closer attention in order to further increase the wafer size and bring down costs.

Recently we reported SXRT studies on axial slices cut from 4H-SiC PVT-grown boules which unambiguously proved the existence of threading dislocations with Burgers vector of c+a. [72]. However, cutting such axial slices while good for research purposes is not economical as it is destructive to the boule. Recently we also reported observations carried out on commercial

offcut (0001) wafers of complex stacking faults with fault vectors such as s+c/2 and s+c/4 which was interpreted as indirect evidence for the existence of threading dislocations with Burgers vector of c+a. The formation mechanism of these faults involved the deflection of threading c+a dislocations onto the basal plane. For those threading c+a dislocations that go through the wafer, interaction with the surface must exist and evidence to reveal the character must exist if suitable characterization technique can be used. Etching is widely used to characterize the defects in SiC crystals, but no evidence to date has been found to support the existence of threading c+a dislocations. This may simply be due to the fact that the stress field associated with the c-component of Burgers vector is much stronger than that of a-component so that the etching associated with the c-component may mask that of the a-component. On the other hand, synchrotron x-ray topography, which has much higher resolution than traditional x-ray topography, is sensitive to the detailed stress field associated with defects. Back reflection and grazing incidence geometries are frequently used to examine threading dislocations and the contrast behavior can be interpreted by comparison with detailed image simulation. Amongst the various simulation techniques, the ray tracing method, which was developed in our group, provides a straightforward way of simulating defect images. This technique has been successfully used to simulate many different kinds of defects in SiC. For example, Chen et al. were able to determine the sense of micropipes and TSDs via grazing topography [32]; Kamata et al [64] used the technique to determine the Burgers vector of six different types of threading edge dislocations (TEDs) from grazing topography; and X. Huang et al. also used the technique to determine the signs of basal plane dislocations [73]. In this paper, ray-tracing simulation of contrast from threading c+2a dislocation in grazing-incidence synchrotron x-ray topograph is carried out and the results are compared with the observed contrast patterns to determine their Burgers vectors. The c+2a threading defect has been confirmed by Transmission topography of axially cut slice parallel to [0001] growth direction. Multiple reflections have been studied to perform the g.b analysis in order to confirm the Burgers vector magnitude of this threading defect.

4.3.Experiment

4H-SiC wafers grown by physical vapor transport technique were used in our study. Grazing-incidence SXRT images of 11-28, -12-18, and 2-1-18 reflections were recorded from Si-faces of

the specimens at an x-ray incident angle of 2°, using Agfa Structurix D3-SC film at a specimen-to-film distance of 25–35 cm at Argonne National Lab. Transmission topography experiments for studying c+2a defects were carried out at Synchrotron facility in Brookhaven National Lab, Beamline X-19C. Simulation and plotting were carried out using commercial software Mathematica.

4.4.Theory

Before going on to the simulation of nc and c+2a defects it is important to discuss the displacement field of individual dislocations in SiC. The displacement field involved with each of these dislocations will be used for the simulation of topograph images.

4.4.1. Displacement field of Threading Screw Dislocations (TSDs)/ Micropipes

As discussed previously the Burgers vector magnitude for both TSDs and MPs varies, their dislocation lines and burgers vector are both approximately parallel to c- axis as shown in figure 41 (a). The displacement field of such dislocations according to fundamental theory has only c- component shown in figure 41 (b).

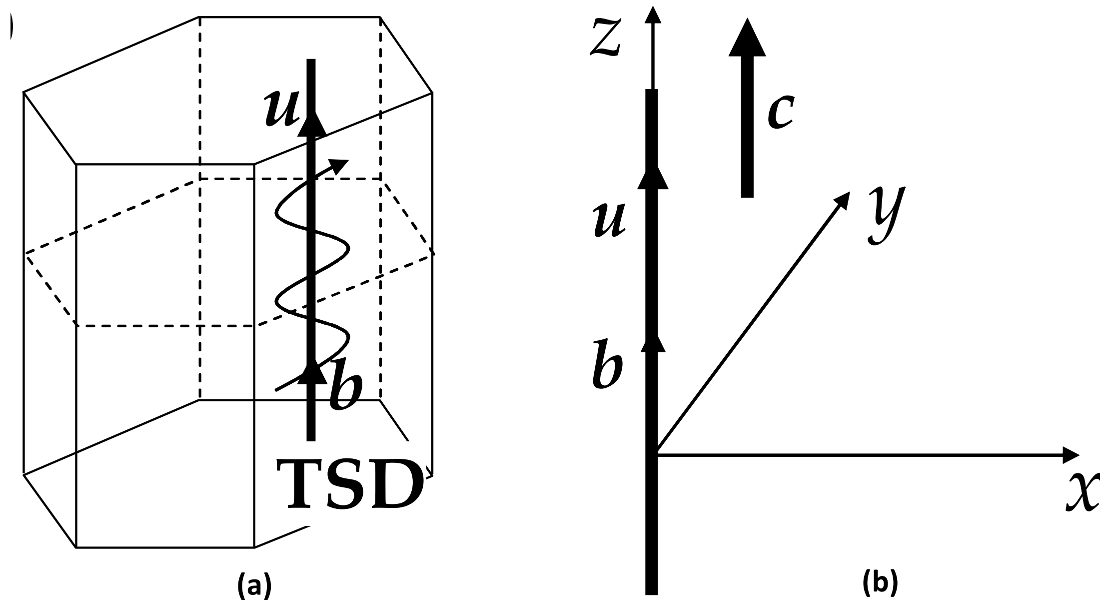


Figure 41 (a) A TSD in SiC. (b) Geometry used in obtaining the displacement field of a TSD or MP [31].

Taking this into account the displacement field of TSD/ MP is given by:

$u_z=(b/2\pi)\arctan(y/x)$

Where u_z is the displacement along z- axis, b is the magnitude of Burgers vector which is also along z- axis as shown in the figure 41.

In order to completely define the displacement field of TSD/ MP it is important to consider a phenomenon known as the surface relaxation effect. In a crystal the TSD/ MP that is close to the surface of material which has strain components perpendicular to the surface has an additional in- plane i.e. c- plane displacement due to surface relaxation and this plays a critical role in the simulation which will be discussed later. According to Eshelby and Stroh the displacement effect of this additional component for a screw dislocation in an infinite plate/ disc with surfaces $z=\pm t$:

$$u_x = u_\theta(x,y,z)\frac{-y}{\sqrt{x^2+y^2}};$$

$$u_y = u_\theta(x,y,z)\frac{x}{\sqrt{x^2+y^2}},$$

Therefore the total displacement field of a TSD/ MP taking this into account is now given by:

$$u_\theta(x,y,z) = -\frac{b}{2\pi}\sum_{n=0}^{\infty}(-1)^n\left\{\frac{x^2+y^2}{(2n+1)t-z+\sqrt{\left[(2n+1)t-z\right]^2+\left(x^2+y^2\right)}}-\frac{x^2+y^2}{(2n+1)t+z+\sqrt{\left[(2n+1)t+z\right]+\left(x^2+y^2\right)}}\right\}$$

4.4.2. Displacement field of Threading Edge Dislocations (TEDs)

To find the displacement field of a TED let us assume one along c- axis, the Burgers vector is not exactly parallel to the x- or y- axis along [11-20] and [-1100] direction but at an angle Θ as shown in figure 42 (a).A new coordinate system is set in such a way that x'- axis is parallel to the Burgers vector direction, y'- axis is pointing toward the extra half plane associated with the a- component as shown in figure 42 (b).

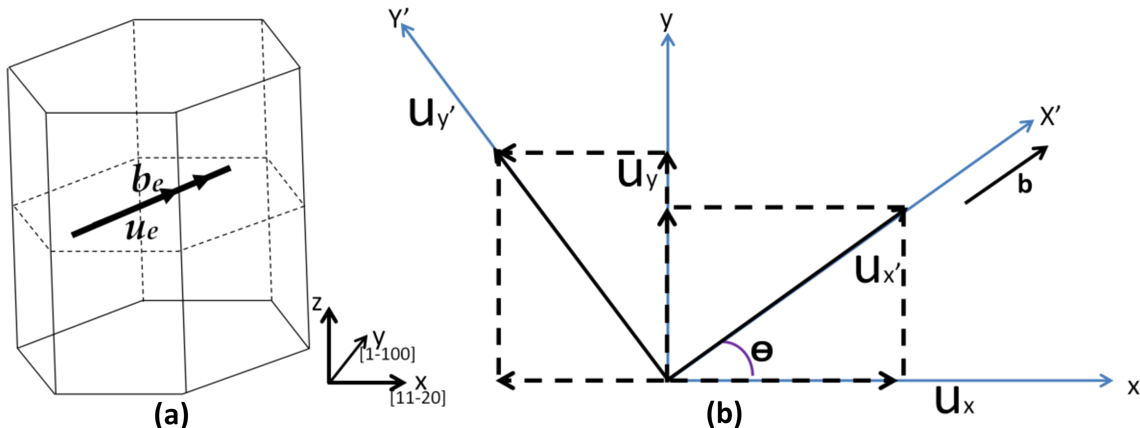


Figure 42 (a) A TED in SiC. (b) Geometry used in obtaining the displacement field of a TED.

The displacement along x' and y' is now given by:

$$u_x' = \frac{b}{2\pi}\left[\tan^{-1}\frac{y'}{x'} + \frac{x'y'}{2(1-\nu)(x'^2+y'^2)}\right]$$

$$u_y' = \frac{b}{2\pi}\left[\frac{1-2\nu}{4(1-\nu)}\ln(x'^2+y'^2) + \frac{x'^2+y'^2}{4(1-\nu)(x'^2+y'^2)}\right]$$

Applying Cartesian coordinate transformation the displacement field along x and y can be written as:

$$u_x = \cos\theta u_x' - \sin\theta u_y'$$

$$u_y = \cos\theta u_y' + \sin\theta u_x'$$

4.4.3. Displacement field of $n_1c + n_2a$ type defect

The displacement field of $\mathbf{n_1c + n_2a}$ can be extracted by combining the displacement fields of individual c and a- type defects as shown in figure 43 (a).

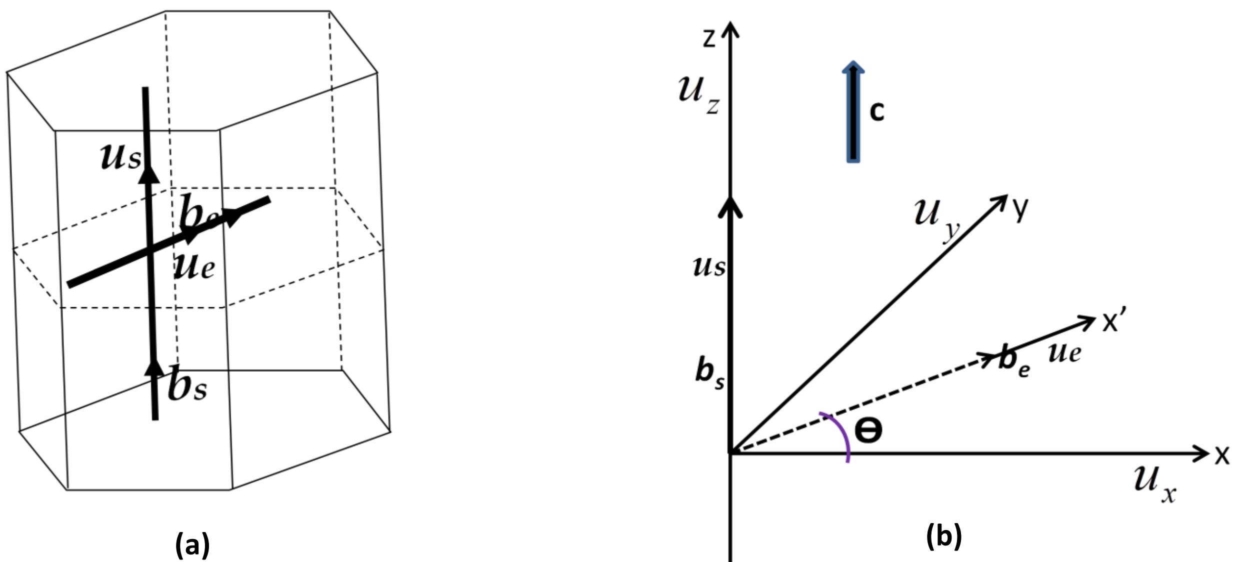


Figure 43 (a) A nc+ma defect in SiC. (b) Geometry used in obtaining the displacement field of a nc+ma defect.

The displacement field for $\mathbf{n_1 c} + \mathbf{n_2 a}$ is given by:

$$u_x = \cos\theta u_x' - \sin\theta u_y' + u_\theta(x,y,z)\frac{-y}{\sqrt{x^2+y^2}}$$

$$u_y = \cos\theta u_y' + \sin\theta u_x' + u_\theta(x,y,z)\frac{x}{\sqrt{x^2+y^2}}$$

$u_z=(b/2\pi)\arctan(y/x)$

Once the displacement field of individual dislocations is determined by setting the right coordinate system, it can be used for the simulation of topograph images by ray tracing technique. As discussed previously there are mainly two types of contrast mechanisms in SiC dislocations which are: Orientation and Extinction contrast analysis. Huang et al [25] have proved by extensive comparison of various topographs that the more dominant of the two in SiC is the orientation contrast; therefore the ray tracing technique is based on this contrast mechanism. The technique has been successfully used to quantitatively and qualitatively interpret the topographic observations of several dislocations including partial dislocations in stacking faults in SiC by all three types of topography geometries.

The schematic used for simulation based on ray- tracing principle is shown in figure 44.The technique basically divides the specimen surface into small squares of constant areas, each of which is independently diffracting beams. There are key parameters such as the plane normal after distortion given by $\boldsymbol{n}(x,y,z)$ due to strain field associated with dislocation and plane normal before distortion $\boldsymbol{n}^0(x,y,z)$which is calculated from each constant square area. The final contrast on the simulated image of the dislocation is calculated by the superimposition or separation of beams diffracted from individual small areas on specimen surface. A modification to this technique can also take into effect not only the diffracted beams from specimen surface but also beneath the surface of crystal allowing photoelectric absorption.

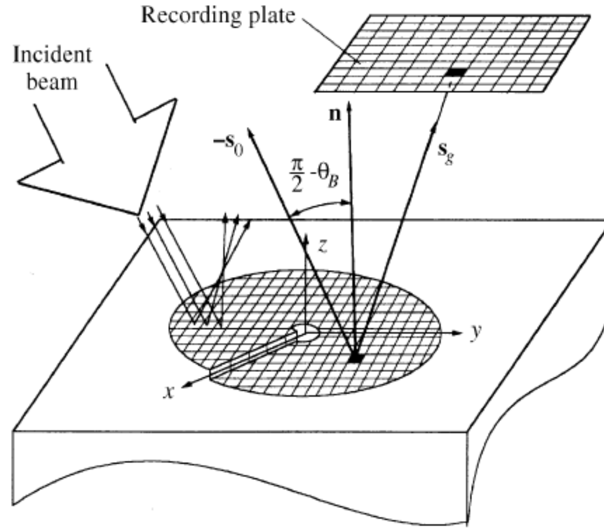


Figure 44 Schematics showing the simulation based on ray-tracing principle. The principle takes into account the orientation contrast mechanism in SiC [25].

The plane normal after distortion in ray tracing technique is calculated by using the equation:

$$\vec{n} = \vec{n}^0 - \nabla[\vec{n}^0 \cdot \vec{u}]$$

This is one of most important equation in the technique where $\boldsymbol{n^0}(x,y,z)$ is the plane normal before distortion and $\boldsymbol{u}(x,y,z)$is the displacement field of the dislocation. Displacement field can be calculated from the type of dislocation involved which will be explained in the next few paragraphs.

Once the plane normal $\boldsymbol{n(x,y,z)}$ after distortion is calculated for the dislocation involved, the diffracted wave vector given by $\boldsymbol{s}$ should be calculated by using another critical equation given by:

$$\vec{s}_0 \times \vec{n} = -\vec{n} \times \vec{s}$$

Here $\boldsymbol{s_0}$ is the wave vector of the incident beam which in this case is assumed to be an ideal plane wave and is fixed. Once the diffracted beam vector is calculated from each constant area, the dislocation observed on the topograph can be simulated by mapping all the beams. The

simulation is carried out using Mathematica, by writing the mathematical code to trace all the individual rays from the specimen surface by selecting an appropriate coordinate system so that the displacement field of each dislocation is calculated. The coordinate system for the simulation of c+2a and nc threading dislocations was set in the following way for the (11-28) type pyramidal reflections:

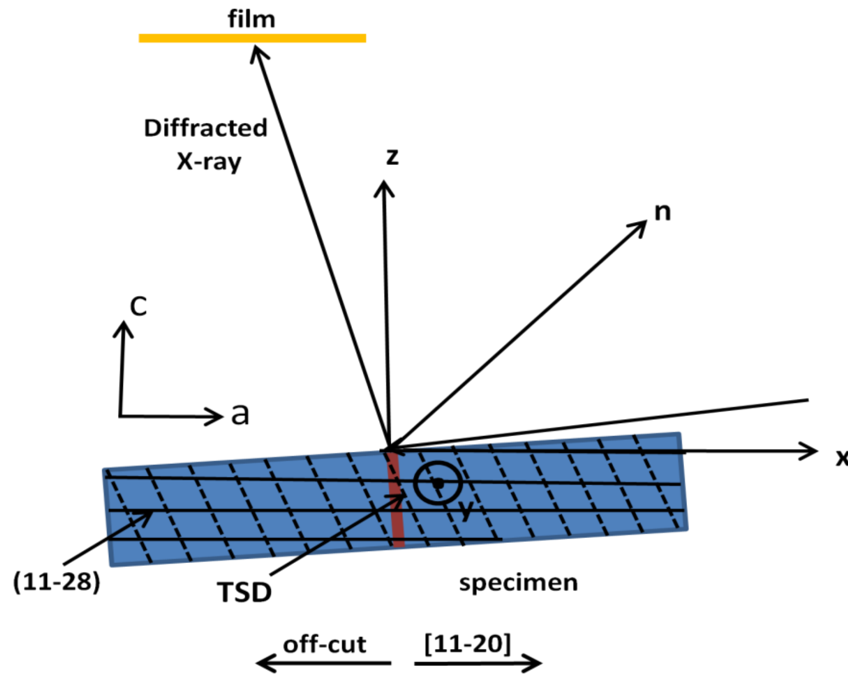


Figure 45 Schematic showing the setting of coordinate system used in simulation of c+2a defect in SiC by grazing XRT of (11-28) reflection.

4.5.Results and Discussions

Elementary extinction analysis (computation of g.b, where g is the active reciprocal lattice vector normal to the reflecting planes and b is the Burgers vector) confirms that the Burgers vector of this dislocation is c+2a, i.e. 1/3[2-423] as shown in table 2. Note the presence of other short segments in figures 46(b)-(d) which are not visible on 43(a). These comprise segments of basal plane and threading edge dislocation with Burgers vector of 1/3<11-20>.

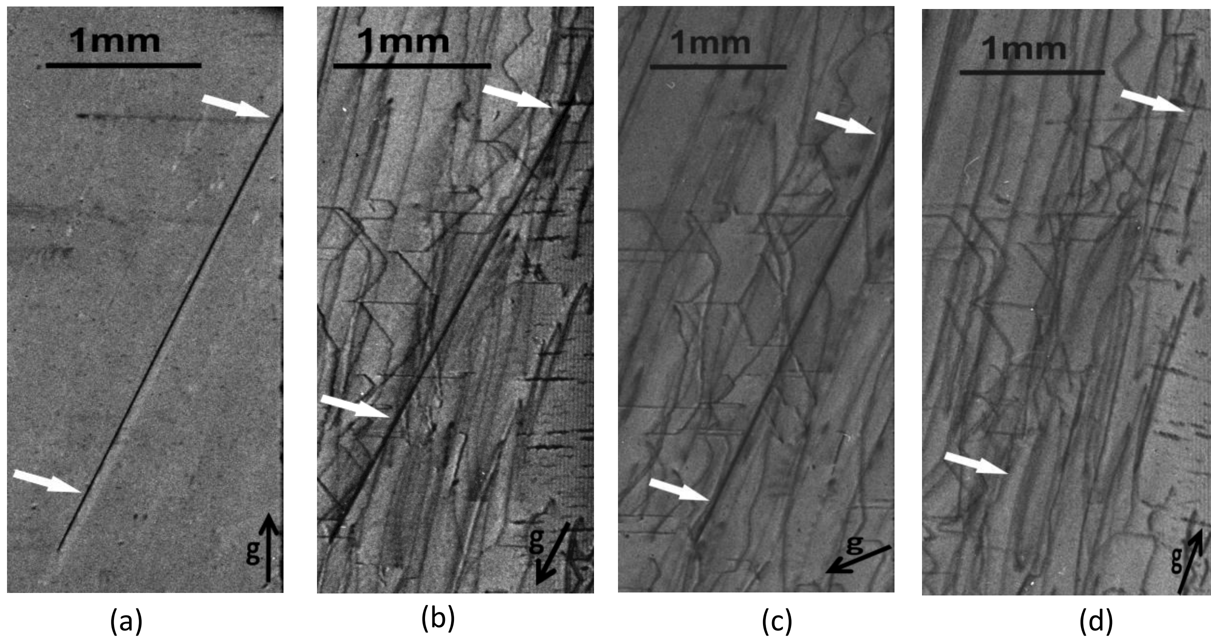


Figure 46 SWBXT images recorded from an axial slice cut parallel to the [0001] growth axis: (a) g=0004; (b) g=1-210; (c) g=0-110; and (d) g=-12-14. In (b) the feature marked in white arrows corresponding to the c+2a defect disappeares.

Table 2. Results of **g.b** analysis for the images shown in Fig. 46.

g.b **b** \ **g**	**0004**	**1-210**	**0-110**	**-12-14**
c+2a: 1/3[2-423]	4	4	2	0

Although one can study axial slices and discern various details of nc + ma type defects on axial slices but it is destructive in nature and time consuming. Therefore it becomes important to also study horizontal wafers to determine the nature of defects like the Burgers vector magnitude and sense of dislocation. Previously our group was able to use Ray- Tracing simulation principle to simulate other type of defects such as TSDs and TEDs. Ray- Tracing principle especially has been able to accurately identify six types of TEDs in SiC and with TSDs other information such as magnitude of Burgers vector has been evaluated accurately. The same principle was used to simulate c+2a defect in this work. Figure 47 (a) shows a topograph taken using monochromatic

beam of [11-28] reflection taken by Grazing geometry. The figure 47 (b) shows a simulated image of c+2a defect and it was possible to correlate that with the topograph shown in (a). The simulation of c+2a was done using Ray- Tracing principle via Mathematica, it took multiple hours to generate the image. The dark feature surrounding the image is due to the surface relaxation effect and that can be observed in the experimental image in the figure 47 (a). One advantage of using this technique is to predict what kind of defect we are looking at in SWBXTs non- destructively and get information for example in case of TSDs whether it is a micropipe or closed- core screw.

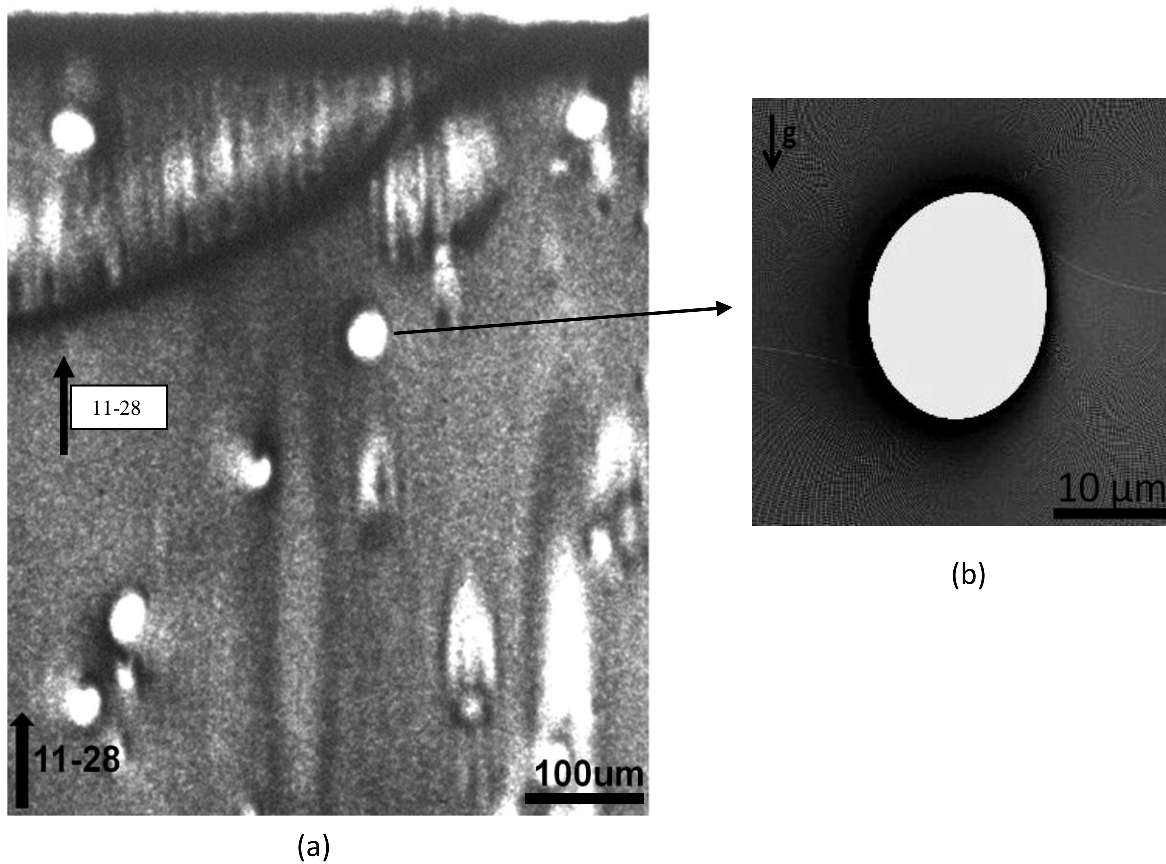


Figure 47 (a) Shows a (11-28) reflection taken by grazing geometry using monochromatic beam. The white spots correspond to the nc and nc+ma type threading defects in SiC. (b) shows a simulated image of c+2a defect correlated with the threading defect in (a) marked by the arrow.

Ray – Tracing principle as mentioned has been successfully utilized to simulate other defects such as the TSDs, TEDs [32] and BPDs [73]. In the case of TSDs shown in figure 48 (a)

- (b) it is possible to reveal both Burgers vector magnitude and sense of dislocations depending on the direction of cant. Ray- tracing principle with respect to TEDs was able to identify six different types which were correlated with the experimental images previously [64]. Figure 48 (a) - (c) shows three images comparing c, -c (*1c TSDs*) and c+2a type defect in 4H- SiC. It becomes difficult sometimes to accurately differentiate c+2a defect with a c- defect or other nc + ma type defect of different Burgers vector magnitude as the direction of cant and surface relaxation effect might make it look similar in nature.

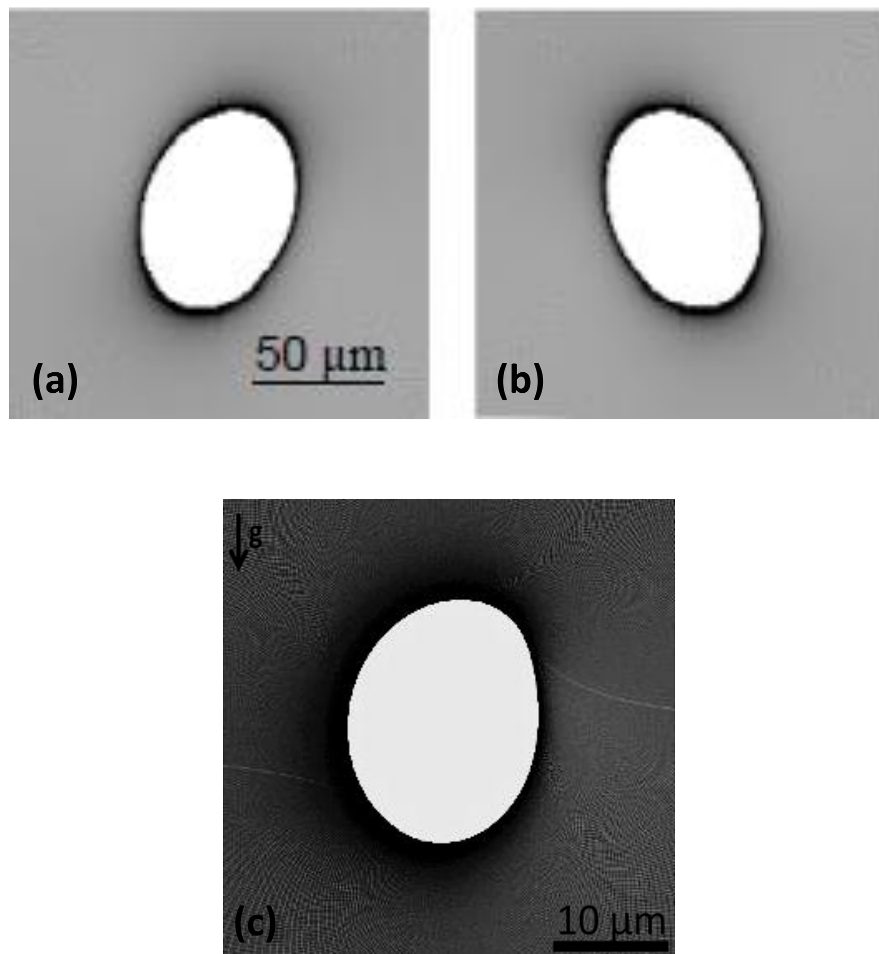


Figure 48 (a) - (c) shows three simulated images from Ray- Tracing principle. (a) - (b) correspond to c and –c screw dislocations respectively [32] and (c) is the simulation of c+2a type dislocation in the same grazing geometry.

4.6.Conclusions

Studies carried out on axial slices cut parallel to growth direction has for the first time been able to actually identify c+2a type defects in SiC. Ray- Tracing simulation based on orientation contrast mechanism has been used to successfully simulate the c+2a type defect which can provide detailed information about the defect. Although the simulated image of c+2a type defect has been correlated with the XRT image in [11-28] reflection but it was identified that sometimes becomes difficult to differentiate it with a c- type defect or other nc+ma type defect as the nature of cant and surface relaxation effect might make it look similar. The studies carried out in this work successfully identify c+2a type defect in SiC and Ray- Tracing simulation of the defect further compound the experimental studies.

5. Observation of Single Ended Frank Read sources in low dislocation density 4H-SiC

5.1. Outline

Right from its inception Silicon Carbide (SiC) has been recognized for its outstanding electrical properties over other conventional semiconductor materials. However, the high defect density in SiC has precluded it from being used on a large scale basis. With extremely low dislocation densities, the new generation wafers provide a unique opportunity to discern details of previously irresolvable basal plane dislocations. Some interesting BPD behaviors in wafers cut from low stress Physical Vapor Transport (PVT) are reported, like the Single Ended Frank Read Sources which are regenerative multiplications of dislocations where an extended line is out of slip plane and is thus sessile acting as a single ended pinning point.

5.2. Introduction

The detrimental effects of dislocations on SiC device performance [18, 19, 62 and 74] have made the lowering of their densities a primary goal of the SiC crystal growth community. SWBXT has played a key role in revealing the detailed configurations of these defects and has been able to shed much light on their origins thereby enabling the development of strategies for their elimination. The identification of TSDs and TEDs as growth defects is notable as is the identification of BPDs as deformation induced defects. The latter has facilitated the development of stress reduction strategies to minimize the driving force for BPD motion behind the growth interface. In recent years, BPD densities typically encountered in wafers cut from PVT grown SiC boules have been of the order of between 10^4 and a few times 10^5 cm^{-2} making it difficult to resolve detailed dislocation behavior. In the crystals studied here, reduction of thermal stress during growth has enabled the lowering of BPD densities by up to three orders of magnitude providing a unique opportunity to discern details of BPD behavior which were previously mostly unresolvable. Here we report detailed SWBXT studies of BPD behavior in wafers cut from such low stress PVT SiC boules.

5.3. Experiment

76mm n^+ 4H- SiC wafers grown by PVT and cut at 4^0 offcut angle towards [11-20] direction were used for the studies. Transmission, Grazing and Back Reflection topography experiments for studying these loop hole configurations behaving as Single- Ended Frank Read source, were carried out at Synchrotron facility in Brookhaven National Lab, Beamline X-19C. AGFA X- ray films were used to record multiple reflections.

5.4. Results and Discussion

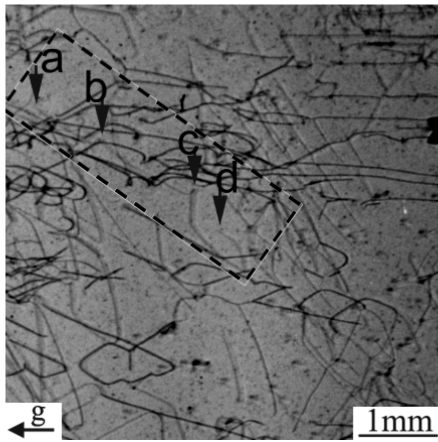
Figs. 49 (a)-(d) shows details from SWBXT images recorded in transmission geometry demonstrating a BPD density of 4.4 x 10^2 cm^{-2} (obtained by measuring the total line length visible in Fig 49 (a) and dividing by the volume sampled which is given by the product of the image field of view and the crystal thickness). In Fig. 49 (a) BPDs (g=-1-120) belonging to the three 1/3<11-20>(0001) slip systems can be observed (note that in all images, BPDs appear as whole dislocations since although they are all most probably dissociated into pairs of Shockley partials, the partial separation (~33nm [38]) is too small to be resolvable in X-ray topography) while in Figure 49 (b)-(d) (g= 1-100, 0-110 and -1010, respectively) dislocations belonging to one of the three slip systems are out of contrast. Note the dislocation configuration labeled **L1** in Figure 49 (b). This dislocation appears to be traveling from top right to bottom left of the image and is pinned at points labeled ***a, b, c*** and ***d***. Here we will focus on pinning points ***a*** and ***d***. At ***a***, there is a TSD close to the surface intersection of the BPD which appears to be responsible for the pinning at that point while no TSD is present at ***d***.

The possibility of a "forest" TED being responsible for the pinning at ***d*** can be ruled out since they are known to be ineffective as BPD pinning points since the dipole trails left in the wake of the advancing BPD simply annihilate allowing the BPD to advance effectively without hindrance [41].On the other hand, while TSDs are quite effective barriers to BPD motion, the spiral configuration of atomic planes surrounding the TSD core ensures that the trailing dipole created comprises dislocations vertically spaced by the magnitude of the TSD Burgers vector. These dipole dislocations experience huge attractive forces (GPa) which can either lead to cross-slip and mutual annihilation if they have screw character or which otherwise lock them in position [75, 76]. For the case of pair of TSDs, the dipoles comprise dislocations on parallel basal planes separated by the Burgers vector of the TSD. These experience huge attractive forces which force either to lock the dipole in place or, in the case of a screw oriented dipole, cross- slip and self- annihilate allowing the dislocations to advance beyond the barrier although pinned by the relatively sessile jog left behind by the annihilation process.

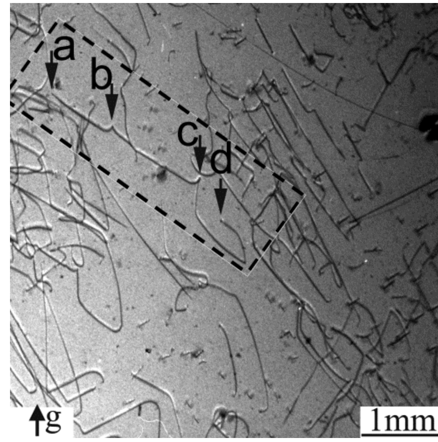
However, if a TSD was for the pinning at ***d*** evidence of a BPD dipole attached to two advancing BPD arms should be visible. Furthermore, there is a segment of BPD that has advanced further towards the offcut direction (towards the right) than ***d*** so that the absence of the

other BPD segment connected to the dipole generated cannot be explained by its escaping through the growth surface. Detailed examination of grazing incidence reflection topographs recorded from both sides of the wafer as well as etch pit patterns from the Si side of the wafer confirms that neither a TSD nor a TED threaded through the wafer from surface to surface at ***d***. Moreover, the BPD appears to terminate at point ***d*** where it must somehow, therefore, emerge on the wafer surface. Since ***d*** is behind the segment of BPD which has advanced furthest towards the offcut direction (down-step direction) this means that the dislocation must leave the slip plane in order to make contact with the wafer surface at this point. A plausible explanation for these observations can be provided by the conversion of the BPD into a TED at ***d*** during growth. Since, slip in SiC is confined to the basal planes; the point at which the BPD is converted into a sessile TED becomes a very effective single ended pinning point for the BPD. As the crystal grows, the BPD continues to glide forming a spiral configuration around the TED pinning point as shown schematically in Fig. 49(e) thus operating as a single-ended Frank-Read source. Similar arguments were used recently to explain the formation of Half Loop Arrays during CVD epilayer growth [76]. Close examination of Fig. 49 (c), where L1 is out of contrast (confirming a Burgers vector of b= 1/3[-2110]) reveals weak contrast associated with the short segment of TED at the pinning point ***d*** since although **g**.**b**=0 for the both the BPD which has long segments of screw character and the TED, **g**.**b**x**l** is non-zero for the TED segment.

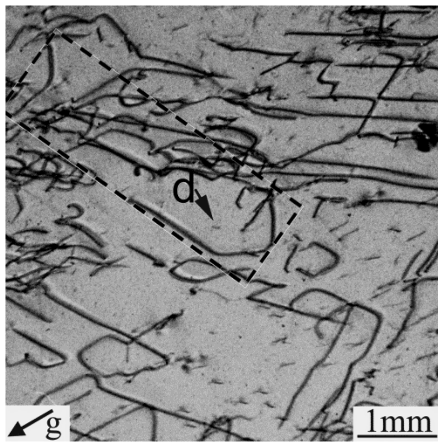
For this mechanism to work the TEDs interconnecting the BPD segments of the dislocation can be considered as jogs. Therefore, during this process of repeated deflection, thermal shear stress on the basal plane (experienced at high temperatures in growth chamber) can cause relatively sessile jogs to act as pinning points for glissile BPD segments, which are initially in screw orientation. When the BPD get converted to sessile TEDs with this happening multiple times, the BPD segments on parallel basal planes must be separated by a distance large enough that their mutual repulsive forces can be overcome. Under stress, the advancing BPD segments will initially draw out a dislocation dipole comprising opposite sign BPD segments. In order for these dislocations to be able to pass beyond this configuration and advance past each other, the force per unit length τb on each segment of the BPD due to applied stress τ need to exceed the maximum value of their mutual attraction force.



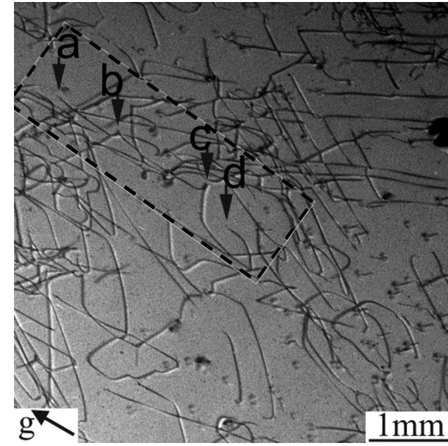
(a)



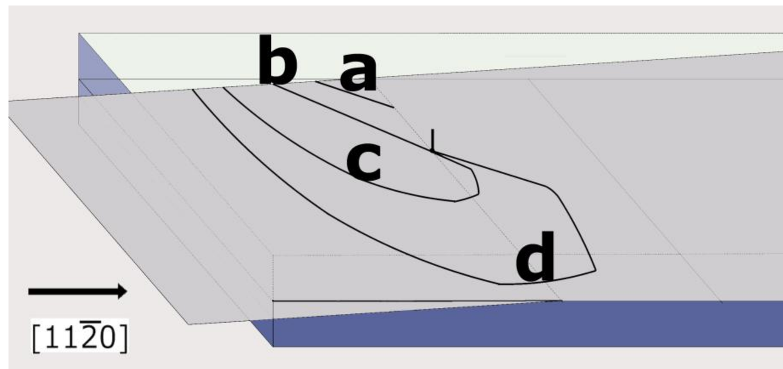
(b)



(c)



(d)



(e)

Figure 49: (a) g=-1-120; (b) g=1-100; (c) g=0-110; (d) g= 10-10; (e) Schematic diagram showing the originally screw oriented BPD being converted into a TED and beginning to act as a single-ended Frank-Read source.

Figure 50 (a) - (d) show images of another dislocation configuration labeled **L2**. This dislocation disappears on the 1-100 reflection showing that it has a Burgers vector of 1/3[11-20]. This dislocation appears to be travelling from bottom to top on the image and has been pinned at five point's ***a-e***. The pinning at ***a*** appears to have occurred close to the wafer surface at a TSD while no TSDs are observed at any of the other pinning points. Again, the loop-hole configurations observed at ***b***, ***c***, ***d*** and ***e*** could not have been formed at either isolated TEDs or TSDs. A plausible explanation for the phenomena leading to the configuration observed in **L2** again involves the conversion of BPD segments into TEDs during growth but also includes the re-conversion of the same TED into a BPD in a process that repeats throughout the growth process. This is shown schematically in Figure 50 (e).

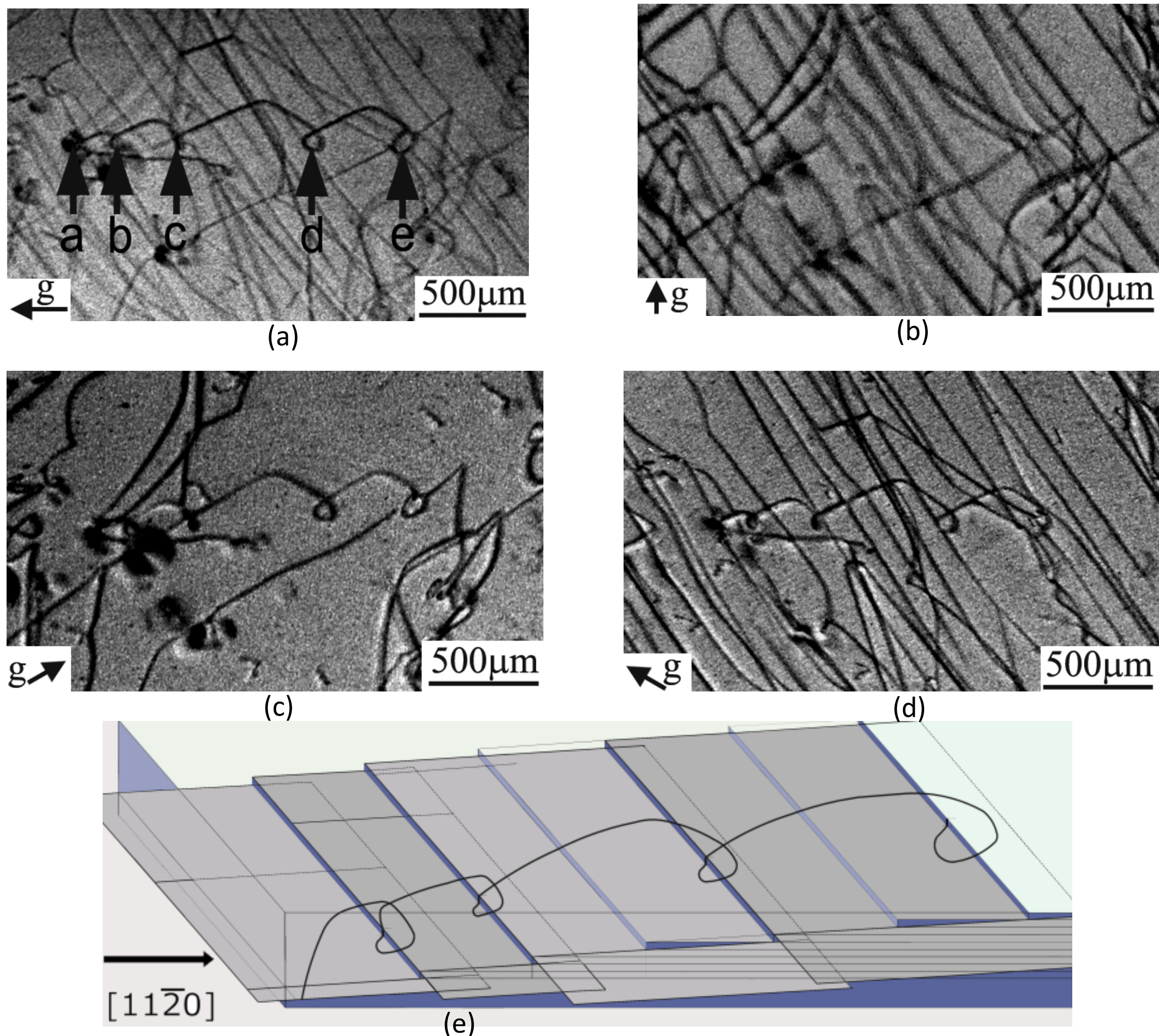


Figure 50: SWBXT images showing dislocation loop-hole configurations: (a) g=-1-120; (b) 1-100 (c) g=01-10; (d) g=10-10; (e) Schematic diagram showing the deflection of the BPD gliding

on basal plane 1 into a TED, continued glide on basal plane 2 followed by deflection onto basal plane 3 through overgrowth by a macrostep and repeating through basal planes 3 and 4.

The initial BPD segment may have had screw orientation but continued glide may cause it to move away from screw orientation at its growth surface intersection rendering it susceptible to conversion into a TED. During further growth, this short TED segment acts as a single-ended pinning point for the BPD which continues to glide under thermal stress. This TED can be re-directed back into the basal plane as a screw oriented BPD through overgrowth by a macrostep traveling from left to right (such macrosteps were observed to be prevalent on the as-grown boule surface). Once back in the basal plane, the screw oriented BPD, being glissile, begins to glide in spiral configuration about its single ended TED pinning point. Again, once the BPD moves away from screw orientation it becomes more susceptible to conversion into a BPD and the whole process repeats as shown schematically in Fig. 50 (e) leading to the type of configuration observed in Figs. 50 (a)-(d).

5.5. Conclusion

Studies are presented of defect configurations and behavior in a new generation of 100mm diameter, 4H-SiC wafers with BPD densities of the order of a few hundred per square centimeter. The low BPD densities have enabled observation of the details of BPD behavior. The conversion of non-screw oriented glissile BPDs into sessile TEDs are observed to provide pinning points for the operation of single-ended Frank-Read sources. In some regions, once converted TEDs are observed to re-convert back into BPDs in a repetitive process which provides multiple BPD pinning points.

6. Correlation between defects and device performance in 4H- SiC wafers

6.1. Outline

SiC is known to be a suitable material as substrates for fabricating high performance and high temperature application devices. The high defects density in SiC in comparison to Si affects the device performance and the properties of SiC to be fully utilized thereby increasing the wafer fabrication costs. In this work patterned wafers fabricated on n^+ 4H- SiC substrates and homoepitaxially grown 4H- SiC epilayer were subjected to failure analysis by SWBXT to correlate as to how defects density affected the device performance. Commonly observed defects affecting the device performance were imaged using SWBXT to create defects density maps of bare 4H- SiC wafers. It was observed that the common device killing defects such as micropipes, triangular defects and stacking faults affected the performance while screw dislocations did not seem to have significant impact on the device breakdown voltage reduction.

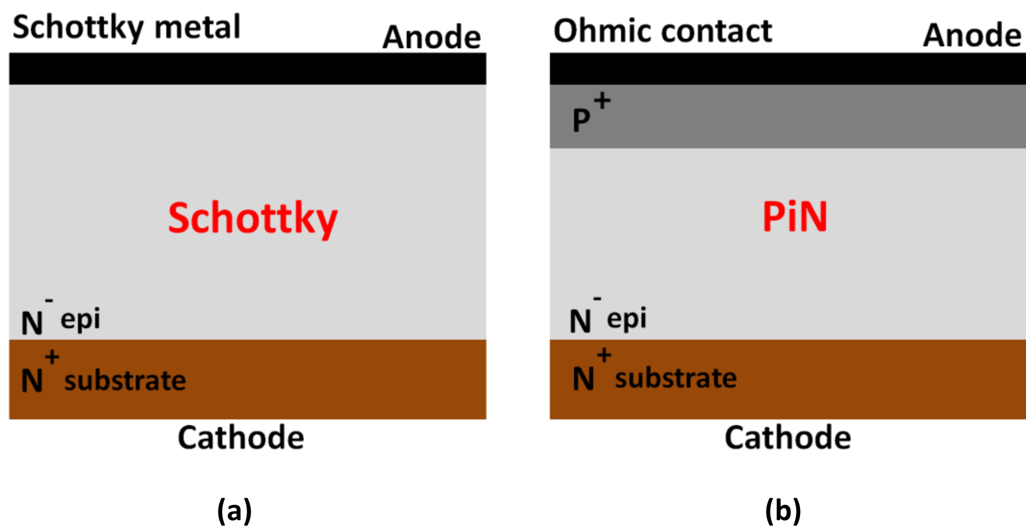
6.2. Introduction

The high temperature applications and semiconductor properties of SiC were realized by William Shockley himself [78] during the time first transistor came into existence. Besides the interesting properties such as high electron mobility, high breakdown field, high thermal conductivity, and good radiation resistance it also has lower lattice mismatch with some of the materials that are used in Light Emitting Diodes [LEDs].

The devices that were fabricated on N^+ 4H- SiC 4^0 off- cut 76 mm wafers were the Junction Barrier Schottky (JBS) rectifiers which had a 107.5 µm thick drift layer epitaxy, doping concentration of 8.8e14/cc and sub- resistivity was 0.021 ohm-cm. In power electronics the key components are switches and rectifiers which cover a wide range of applications, from power transmission to control electronics and power supplies [79]. It has been estimated that the JBS and Schottky rectifiers are likely candidates to replace Si PiN diodes in the 300- 3300V blocking voltage range where Si are not effective. As mentioned before the defects density in SiC affects all these properties and it becomes important to study these defects as to understand how they further impact device performance. It has been studied that the pn junction in SiC has a large forward voltage drop (about 3V) because of the wide bandgap energy. This forward drop becomes significant for low and medium voltage applications, 300- 4500V which causes static

losses in these SiC PiN diodes. On the other hand, by using a Schottky diode as the rectifier where forward voltage drop (1-1.5V) is proportional to the Schottky barrier height may result in excessive reverse leakage current, thus limiting the desired blocking voltage.

A JBS rectifier is a unipolar diode that combines Schottky- like on- state and switching characteristics with PiN- like blocking characteristics. The JBS device was first demonstrated in Si [80, 81] and is a Schottky structure with a p+n junction grid integrated into its drift region. Illustrations of cross sections of Schottky and PiN diode structures in comparison with a JBS structure are shown in Figure 51 (a) - (c). In forward conduction mode the current flows unipolar through the multiple conductive channels under the Schottky contact with a voltage drop determined by the metal semiconductor Schottky barrier height. In reverse blocking mode the p+n junctions become reverse biased and the depletion layers spread into the channel and pinch off the Schottky barrier. After pinch- off a potential barrier is formed which limits the electric field at the Schottky contact while the drift region supports further increase in voltage. The spacing between the P^+ regions should be designed so that pinch- off is reached before the electric field at the Shcottky contact increases to the point where excessive leakage currents occur due to tunneling currents. Lowering of the leakage current without too much increase in on- resistance can be obtained for the JBS if an optimized spacing is used in the P^+ grid design. More than 300 of these rectifier diodes were fabricated on the PVT grown 76 mm wafers with a off- cut angle of 4^0 toward [11-20] and the thickness of the wafer was 300 µm.



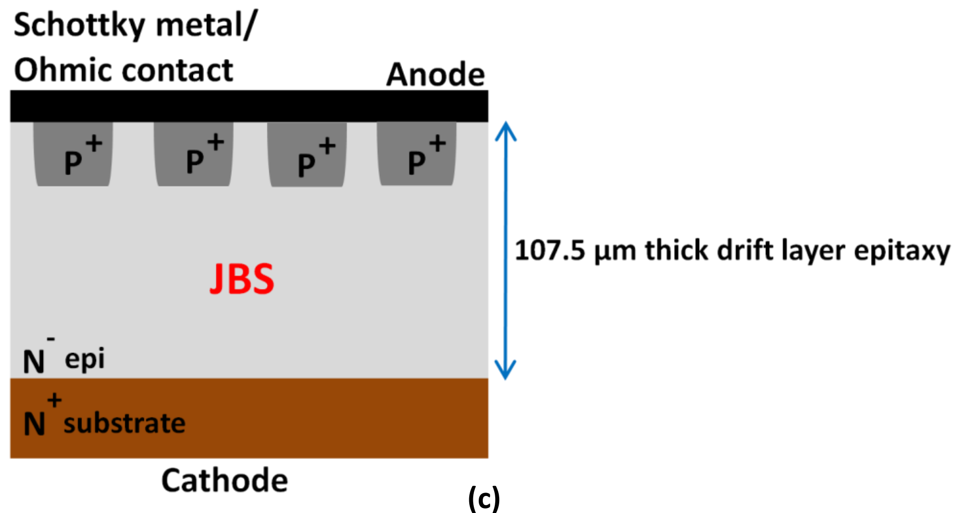


Figure 51 (a) shows a Schottky device, 50 (b) shows a PiN device and (c) shows a JBS rectifier which is a combination of (a) and (b).

The high temperature and high breakdown voltage JBS rectifiers were fabricated on homoepitaxial CVD grown epitaxy using n^+ 4H- SiC PVT grown wafers. The bare wafers were subjected to SWBXT and Nomarski microscope studies to determine the defects density and choose wafers with the least overall defects density for epi growth. The defects in SiC is known to replicate right from the seed to top of the boule and can also replicate into the epi so it becomes important to know the exact density distribution in the wafer selected for fabrication. The extended defects in SiC commonly present are the closed- core screw dislocations (Burgers vector 1c or 2c), hollow- core known as micropipes or giant screw dislocations (Burgers vector larger than 2c), threading edge dislocations (from conversion of basal plane dislocations in the substrate into TEDs in the epi), stacking faults (four type of stacking faults, carrot defects and trapezoidal defects) and triangular defects (3C- inclusions known to exist in triangular shape with the triangle expanding towards the off- cut direction). All these extended defects have been known to affect the performance for instance, the screw and threading edge cause premature breakdown as well as increased leakage current [82]. Triangular defects and micropipes limit the operating voltage in the reverse voltage to a fraction of the breakdown voltage [83]. The BPDs that replicate unconverted into TEDs, to the epi from substrate can serve as recombination centers as the BPDs exist as partials in SiC due to low stacking fault energy. The partials can dissociate leading to the glide of one partial creating stacking faults and this expansion of stacking faults can cause drop in forward voltage with time [47].

The devices fabricated using these wafers were used for high temperature applications with high breakdown voltages. The defects density was calculated in the bare wafers in the beginning and wafers with low density were selected for epilayer growth. It is imperative for SiC wafers to have epi on top of it as direct ion implantation or diffusion of dopants on the substrate wafer, as in the case of Si is not possible in SiC. The diodes fabricated were subjected to failure analysis by using SWBXT for comparative studies, the defects density in the device active areas were calculated and compared with device performance for that particular device selected. For more than 200 high voltage diodes studied it was noted the screw dislocation density in the substrate and epi did not have significant influence on device performance, but the triangular defects and stacking faults caused premature breakdown.

6.3. Experiment

A batch of around 45 n^+ 4H- SiC bare wafers grown by PVT were selected for SWBXT studies. The wafers used had an off- cut angle of 4^0 toward the [11-20] direction and were all 76mm wafers with 300µm thickness. The wafers studied were all from different boules grown by PVT at high temperatures. The bare wafers were first studied under Nomarski Microscope to check for scratches and other polishing damages. For calculation of defect density distribution, the wafers were subjected to SWBXT studies using both Grazing Topography and Transmission geometry.

The wafers with low defect density distribution were selected for fabrication of high voltage diodes for high temperature applications. Before fabrication of devices the wafers selected were etched and had a thin layer of epi grown by CVD. The devices fabricated on this layer were subjected to breakdown voltage measurements; the breakdown voltage is defined as the voltage yielding a current density of $0.1A/cm^2$. After measurements the metallization in the devices were chemically removed to reduce noise in SWBXT images and backside of wafer then chemically- mechanically polished (CMP) to reduce strain. These patterned wafers were than studied at Stony Brook Topography Facility (Beamline X-19C) at National Synchrotron Light Source, BNL. The wafers were again subjected to both grazing and transmission topography to get the defect count after fabrication of devices.

Windows based Laue Program was used in both sets of experiments to choose the right diffraction patterns, determine the SiC polytype and setting the crystal in the right orientation for Topography studies.

6.4. Results and Discussions

The substrate wafers studied showed the commonly observed defects like the closed core screw SSDs, TEDs and BPDs in all the wafers, with few of them containing the device killing micropipes and also stacking faults mentioned previously. After device fabrication the wafers observed showed the epi defects such as triangular defects, stacking faults along with the defects observed in substrates. Figure 52 (a) shows a transmission XRT image taken from the substrate wafer showing contrast from regular defects along with stacking fault at the bottom of image and figure 52 (b) and (c) show XRT images taken by transmission and grazing XRT from the same wafer after device fabrication. One can clearly notice the triangular defects to be present all across the wafer with stacking fault after epi to have expanded into device active area.

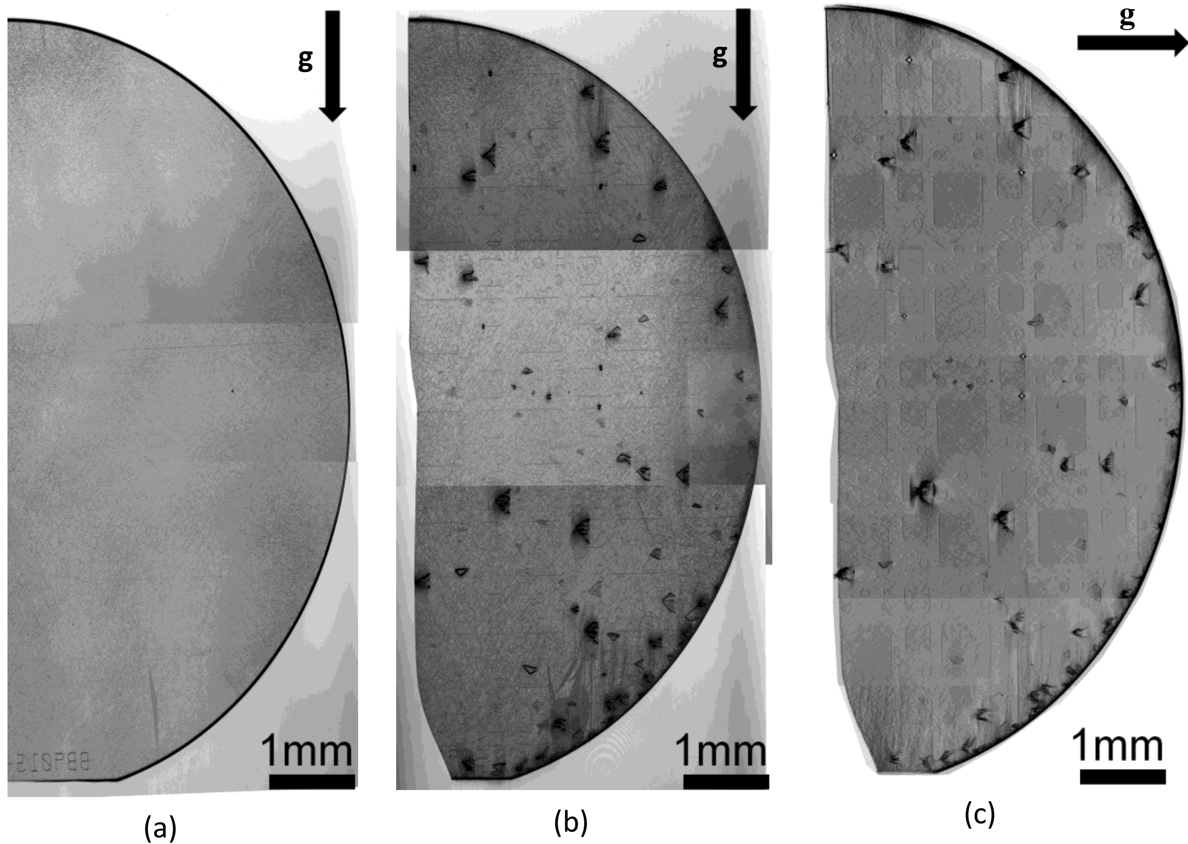
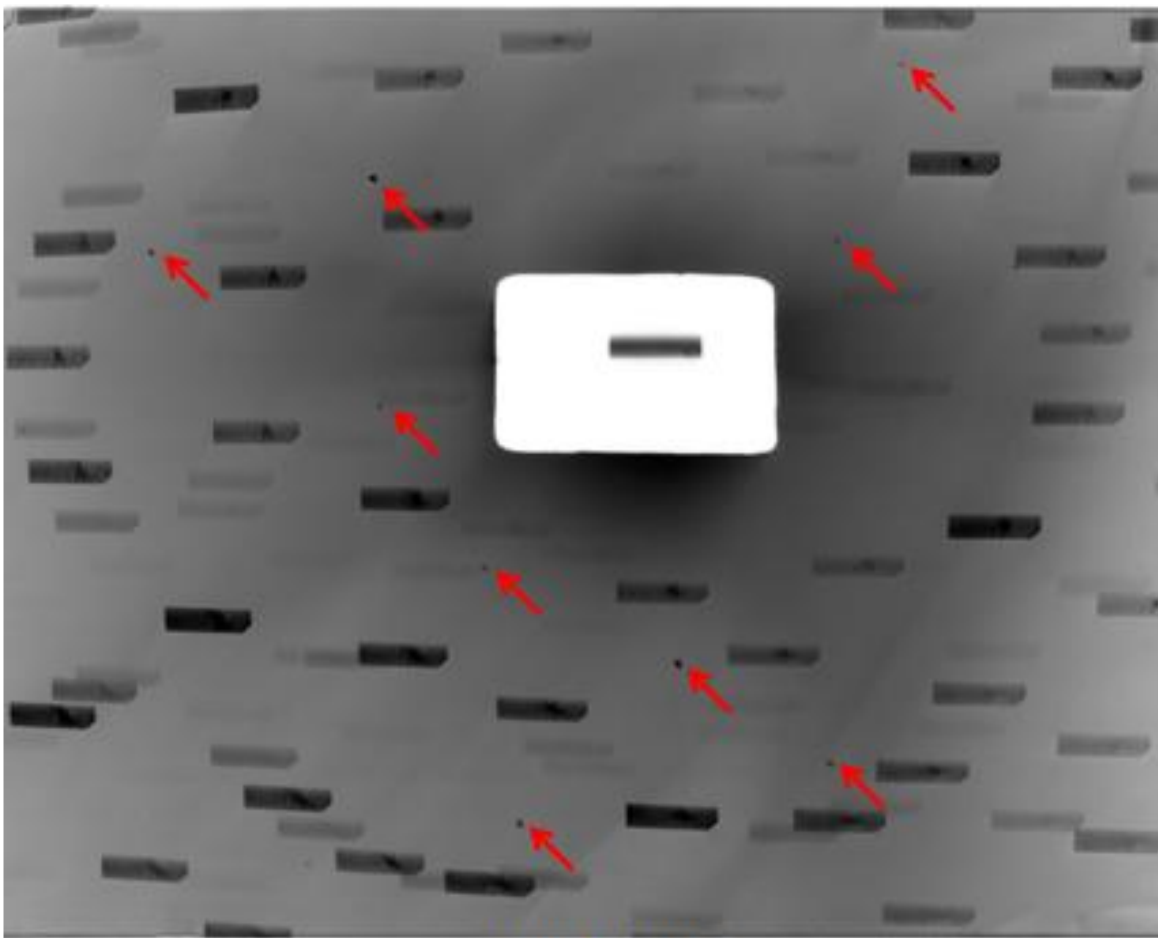


Figure 52 (a)- (c) are SWBXT images recorded from the same area of n^+ 4H- SiC wafer by SWBXT. Image (a) is <10-10> type reflection recorded by Transmission geometry from the substrate wafer, (b) is also a <10-10> type reflection recorded by Transmission geometry after device fabrication and (c) is (11-28) reflection recorded by Grazing geometry after device fabrication.

The triangular defects in the SWBXT images shown above were proven to be 3C-inclusions by correlating the Laue spots on the X-ray film with the simulated pattern using the Laue program as shown in figure 53 (a) - (b). Figure 53 (a) shows a Transmission SWBXT image taken from one of the areas containing the triangular defect, the red arrows marked in the image is the diffraction from triangular defect which is simulated using the software in figure 53 (b) again marked by the arrows. These defects as mentioned previously are detrimental to the devices as it causes premature breakdown if present in the device active area. This is the reason step controlled epitaxy has become hugely accepted method to grow CVD epilayers, but still cannot completely get rid of them in the epi.



(a)

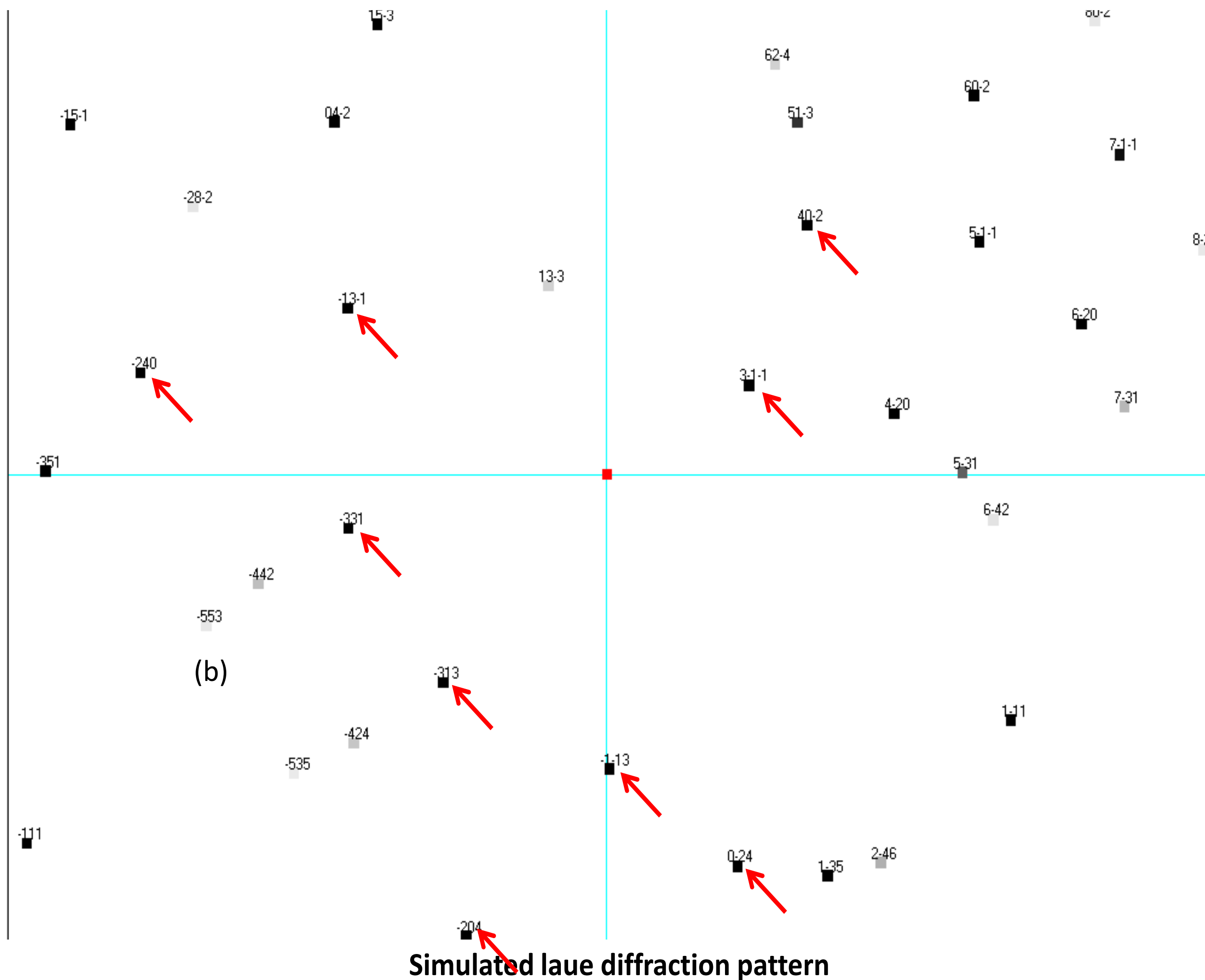


Figure 53 (a) shows a Transmission SWBXT diffraction pattern recorded from an area containing triangular defect which results in a separate diffraction pattern other than the matrix which is 4H- SiC. The pattern of the triangular defect (3C- inclusion) is simulated in (b) using Laue program to confirm the presence of the defect.

Figure 54 (a) shows a Transmission SWBXT image taken in the substrate showing contrast of the stacking fault in [11-20] reflection and the same area imaged after fabrication shows the faults to have expanded in figure 54 (b). After contrast analysis using a set of different reflections as done previously the fault vector in this case revealed to be a combination of Shockley plus a Frank fault. These faults might have further expanded either by recombination enhanced dislocation glide or by the further glide of one leading partial and could be both these phenomena occurring at the same time causing the fault to expand further into device active area.

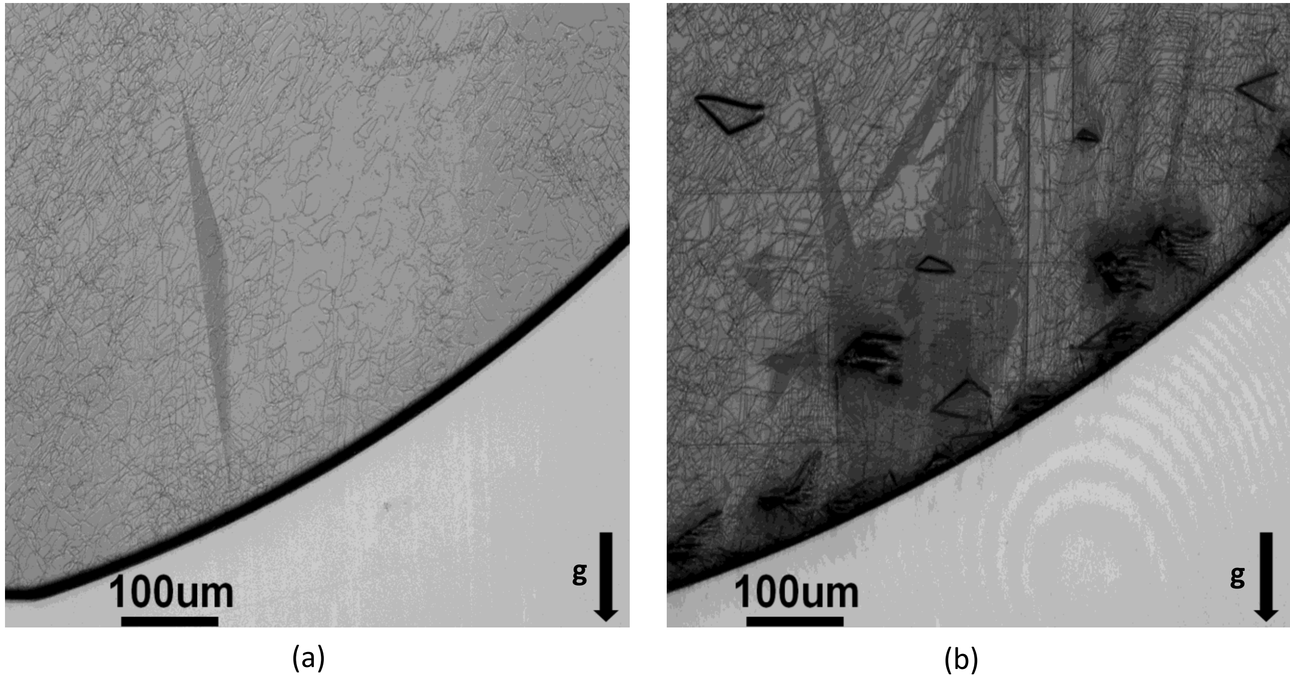


Figure 54 (a) is a Transmission <10-10> type SWBXT image recorded from a region near edge of 4H- SiC substrate wafer showing contrast from stacking fault. The same region in (b) is recorded by Transmission geometry after device fabrication which shows the fault to have expanded into the device active area.

Figure 55 shows a patterned wafer having more than 150 high voltage diodes in different shapes fabricated all over the half wafer without metallization. The areas marked 1-4 in the figure 55 correspond to diodes which had a high breakdown voltage [>1900V] whereas the devices marked 5-8 failed having low breakdown voltage [<100V].

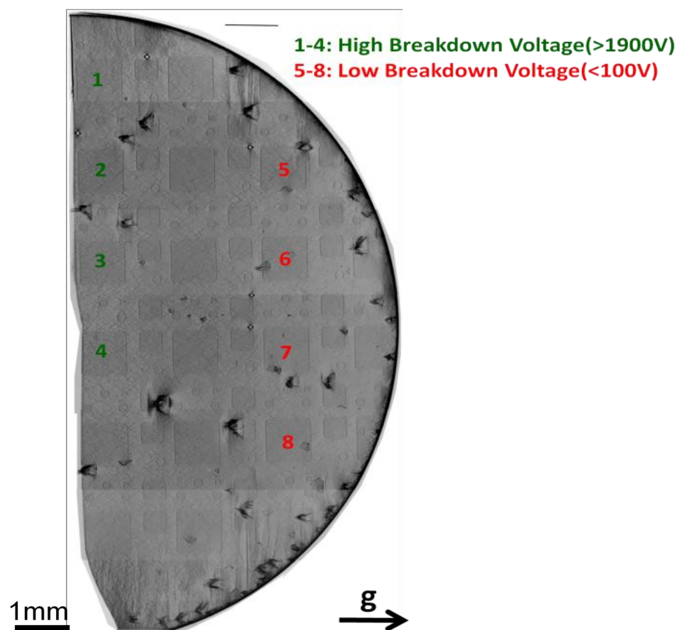


Figure 55 is (11-28) SWBXT image recorded by Grazing geometry after device fabrication. The areas marked 1-4 in green represent the devices that have high breakdown voltage (>1900V) and devices marked 5-8 in red represent devices that failed (<100V).

The devices 1-4 shown in figure 56 (a) - (d) were recorded by Grazing SWBXT geometry which can reveal both the TEDs and TSD density count, the image also shows the defect density count of TSDs in the substrate and after epi. One can clearly notice the density of screws has not changed much after epi growth compared to that in the substrate, while the density is high in devices 3- 4 compared to 1-2 but that has not had a significant impact on the breakdown voltage which still remains >1900V for all the four devices studied.

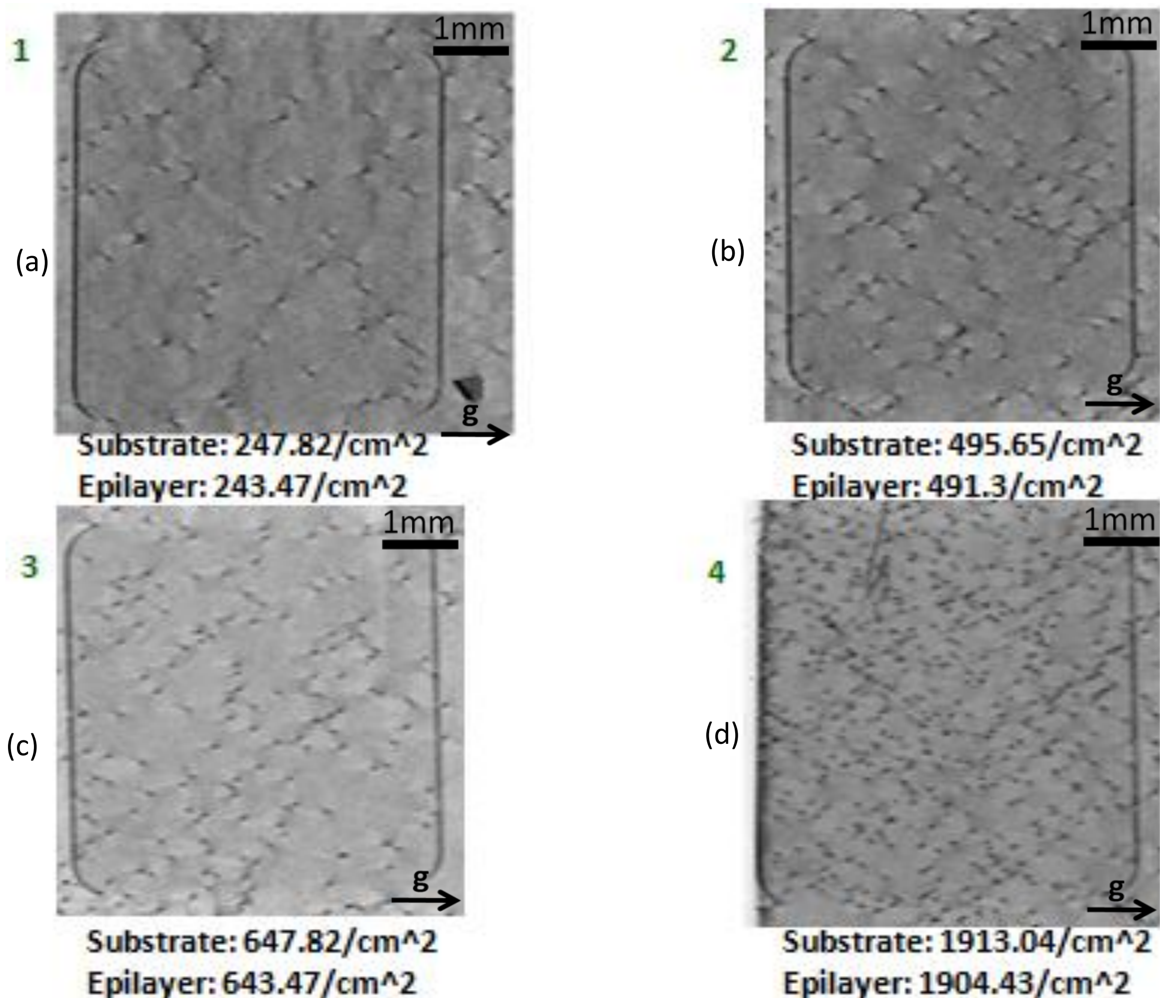


Figure 56 (a) - (d) show four devices that have high breakdown voltage from the region marked 1-4 in figure 49 which have been blown- up. (a)- (d) have screw dislocation density calculated before device fabrication i.e. from substrate and after from epilayer.

Figure 57 (a) - (d) shows devices 5-8 with screw dislocation density in both substrate and after epi which failed, the breakdown voltage for these are as low as 100V. It is interesting to note that the screw dislocation density calculated for these devices are comparable to devices 1-4 with few of them having a greater density count than devices 5-8. This scenario is redundant for almost more than 150 rectifiers fabricated on the wafer which clearly suggest that screw dislocations in these devices has not played a significant role in the reduction of breakdown voltage. In figure 57 (a)- (d) one can clearly notice the triangular defects in the device active areas, insinuating that these defects were responsible for the failure and not the screw dislocations or threading edge dislocations.

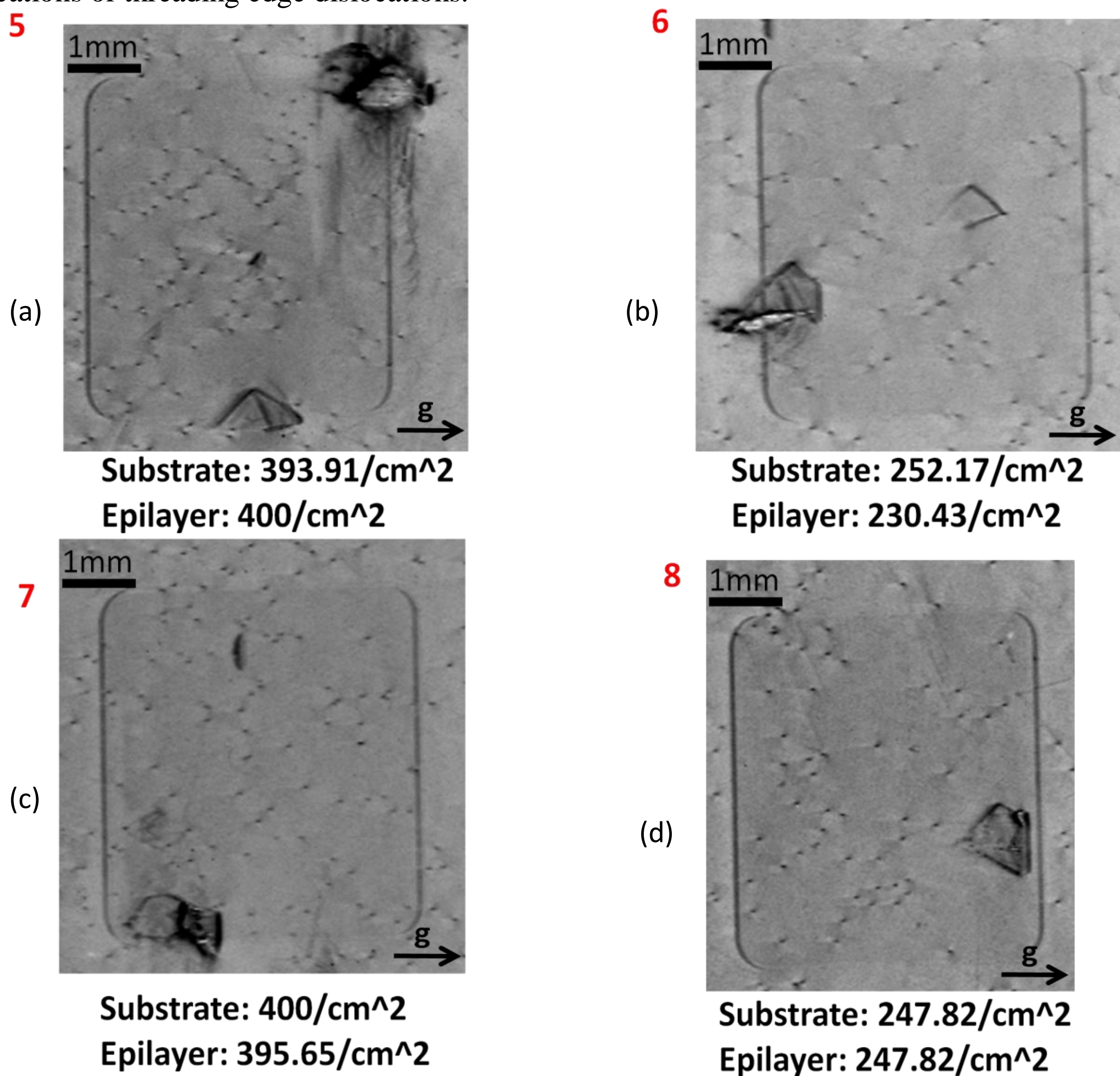


Figure 57 (a) - (d) shows four devices that failed from the region marked 5-8 in figure 49 which have been blown- up. (a)- (d) have screw dislocation density calculated before device fabrication i.e. from substrate and after from epilayer.

6.5. Conclusions

More than 150 devices fabricated on 76mm 4H-SiC substrate were subjected to SWBXT studies using different geometries. The wafer selected for device fabrication was subjected to SWBXT studies for calculation of defect density distribution in the substrate wafer and the same studies were done after fabrication removing metallization. The failure analysis was performed on all these wafers to find out as to how a particular defect has impacted the breakdown voltage. It was revealed that the screw dislocations did not have significant influence on the device performance unlike other defects observed such as triangular defects and stacking faults which clearly affected the performance.

7. Conclusions and Future Work

[1] The c+a defects in which the dislocation core have both c and a components have been proven to exist in SiC by studying both the horizontally cut wafers shown in figure 58 (b) and axial slices cut parallel to the growth direction. The c+a defects during growth get deflected out the crystal boule resulting in defect density reduction as shown in figure 58 (a) - (b), but the deflection causes the partials to be separated by the height of the step riser associated with screw dislocation. Depending on the direction of stress only one of the partials is able to glide creating the large stacking faults as shown in figure 59 (a) - (c). Stacking fault contrast analysis by studying the faults in multiple reflections has resulted in the determination of fault vector to be of the type 1/3[01-10].

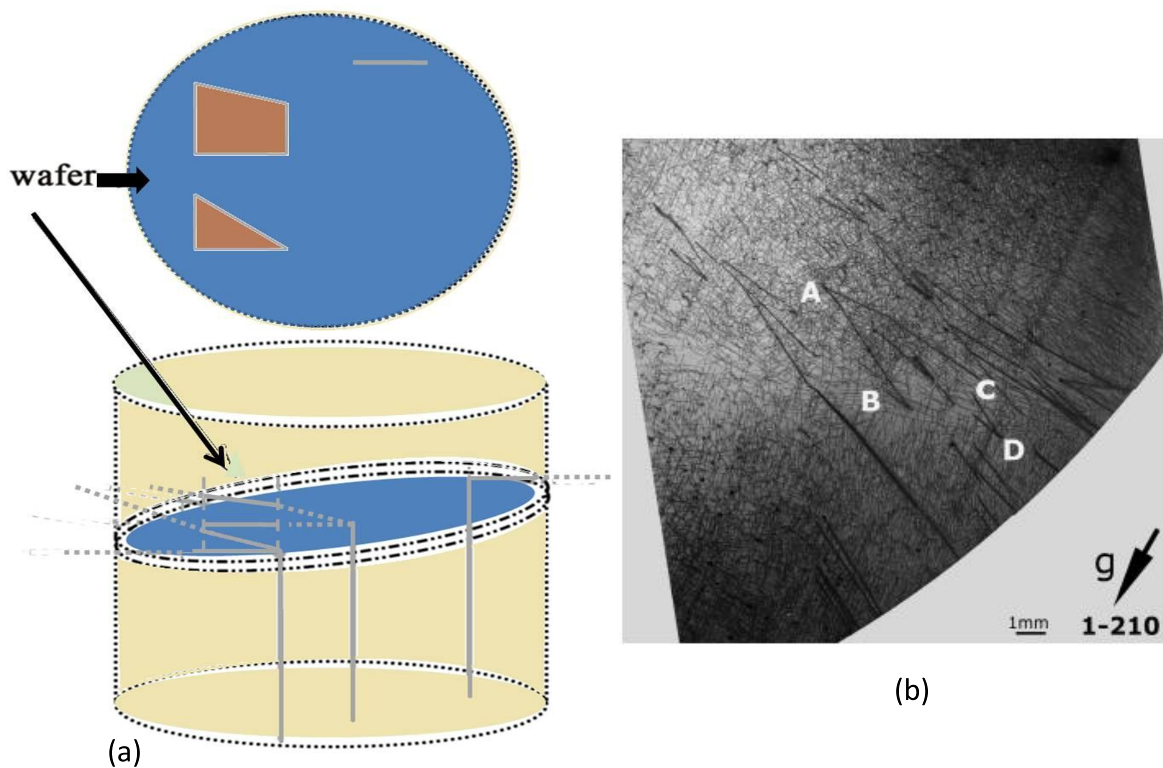


Figure 58 (a) Schematic of deflection of threading dislocations during growth that get deflected out of the crystal boule in the offcut wafer. (b) shows a SWBXT image taken by Transmission geometry from the edge of a wafer showing long dislocations getting deflected out.

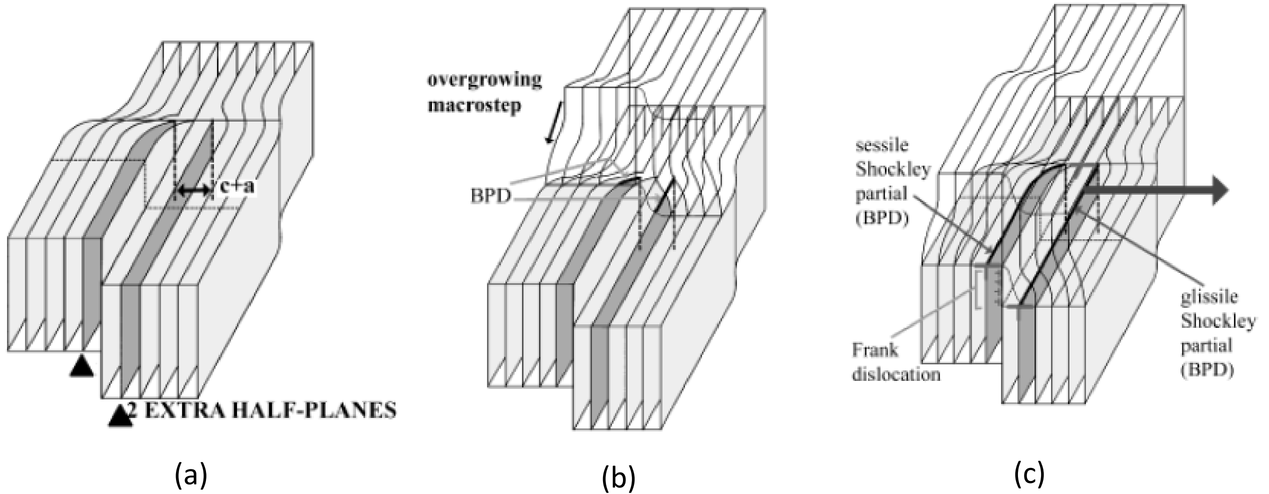


Figure 59 (a)-(c) show c+a defect which is overgrown by a macrostep resulting in two partials that are separated by the step riser.

Figure 60 (a) - (b) shows two SWBXT Transmission images taken from the same area showing the contrast from stacking faults. The contrast behaves differently in different reflections as the wavefields undergo phase shift as they cross the stacking fault.

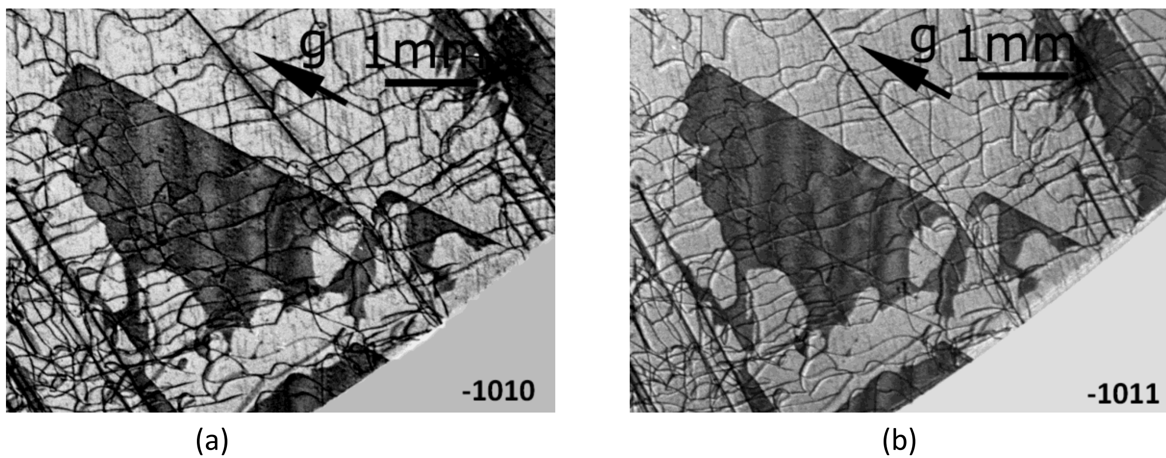


Figure 60 (a) - (b) are SWBXT images taken by Tranmission geometry of (-1010) and (-1011) reflections showing contrast of stacking faults.

[2] Studies carried out on axial slices cut parallel to growth direction has for the first time been able to actually identify c+2a type defects in SiC as shown in figure 61. Ray- Tracing simulation based on orientation contrast mechanism has been used to successfully simulate the c+2a type defect which can provide detailed information about the defect shown in figure 62 (b). Although the simulated image of c+2a type defect has been correlated with the XRT image in [11-28] reflection but it was identified that sometimes it becomes difficult to differentiate it with a c- type defect or other nc+ma type defect as the nature of cant and surface relaxation effect might make it look similar. The studies carried out in this work successfully identify c+2a type defect in SiC and Ray- Tracing simulation of the defect further compound the experimental studies.

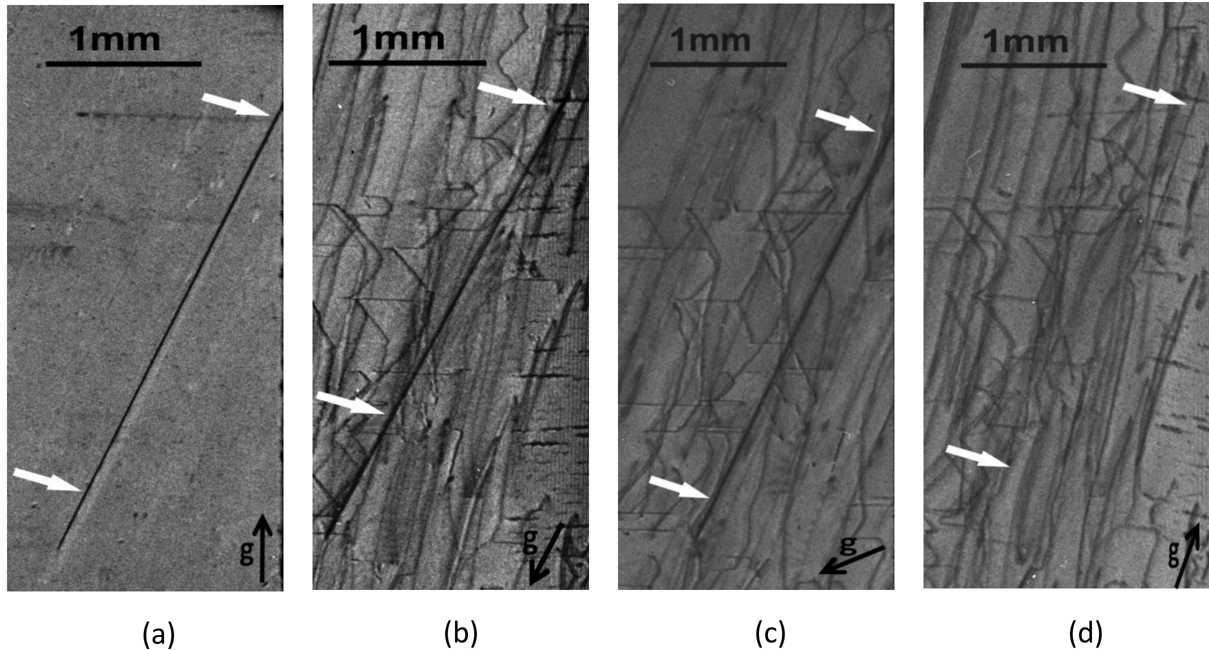


Figure 61 (a) - (d) show four SWBXT images from different reflections taken by Transmission geometry for determination of c+2a type defect.

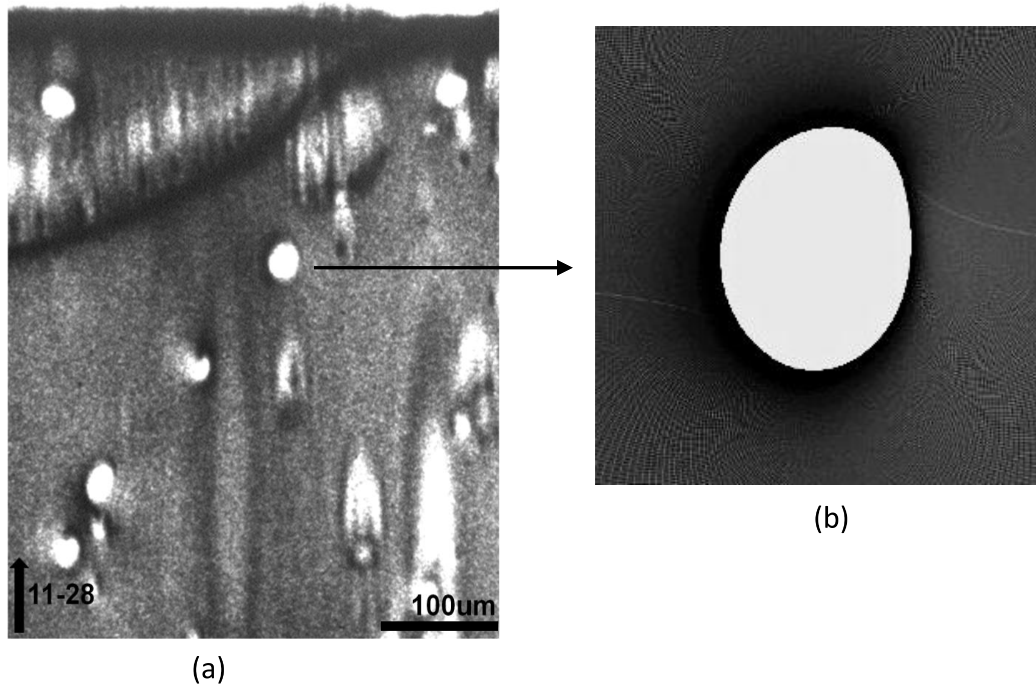


Figure 62 (a) Shows a (11-28) reflection taken by Grazing geometry using monochromatic beam. The white spots correspond to the nc and nc+ma type threading defects in SiC. (b) Shows a simulated image of c+2a defect which matches closely to the threading defect in (a).

[3] Studies are presented of defect configurations and behavior in a new generation of 100mm diameter, 4H-SiC wafers with BPD densities of the order of a few hundred per square centimeter. The low BPD densities have enabled observation of the details of BPD behavior. The conversion of non-screw oriented glissile BPDs into sessile TEDs are observed to provide pinning points for the operation of single-ended Frank-Read sources. In some regions, once converted TEDs are observed to re-convert back into BPDs in a repetitive process which provides multiple BPD pinning points as shown in figure 63 (a) - (d) with illustration of the mechanism in (e).

This phenomena further helps to understand the defect multiplication mechanisms taking place within SiC crystals which can aid in reduction of further defect density. Also gives an understanding as to how the macrostep overgrowth mechanism works in the system resulting in these defect sources.

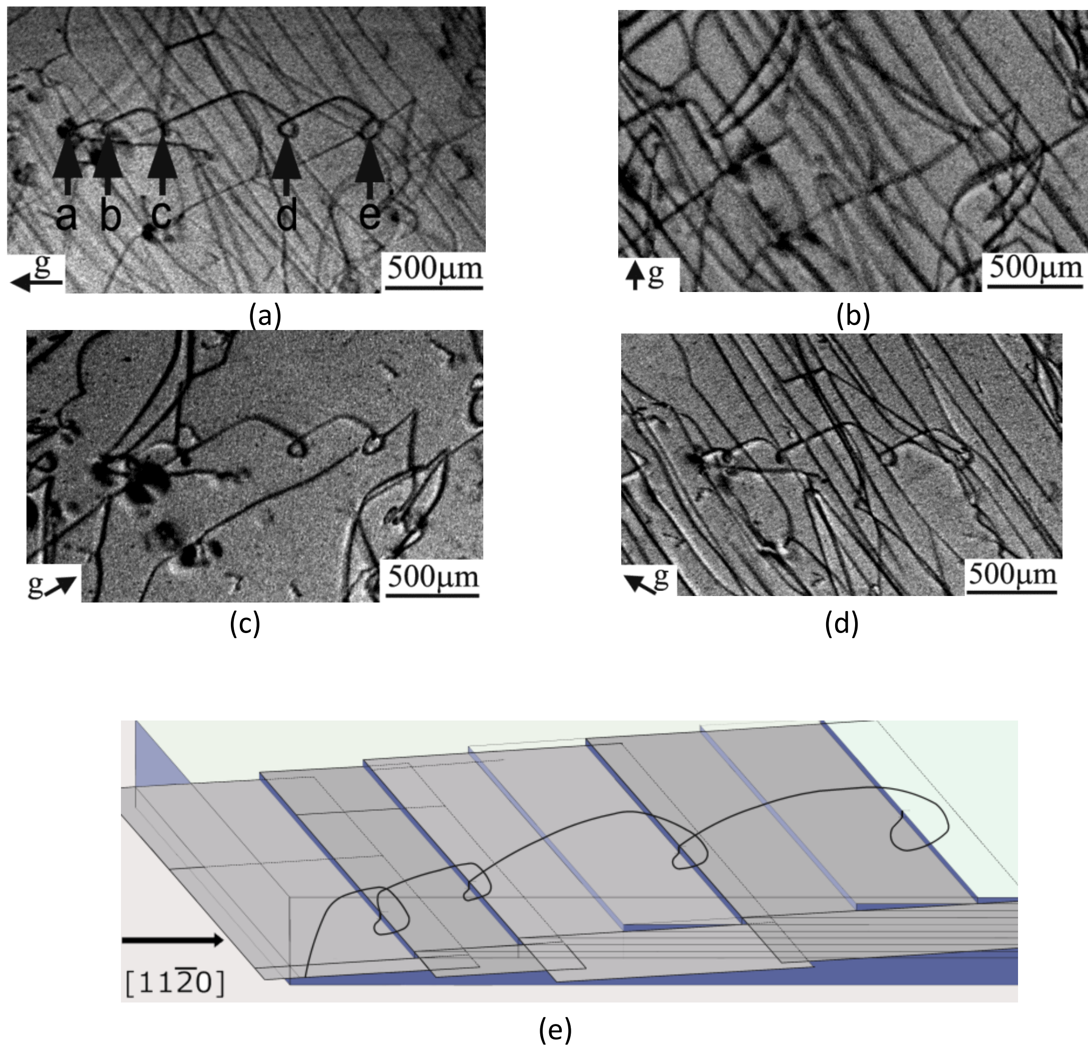


Figure 63 SWBXT images showing dislocation loop-hole configurations: (a) g=-1-120; (b) 1-100 (c) g=01-10; (d) g=10-10; (e) Schematic diagram showing the deflection of the BPD gliding on basal plane 1 into a TED, continued glide on basal plane 2 followed by deflection onto basal plane 3 through overgrowth by a macrostep and repeating through basal planes 3 and 4.

[4] More than 150 devices fabricated on 76mm 4H-SiC substrate were subjected to SWBXT studies using different geometries. The wafer selected for device fabrication was subjected to SWBXT studies for calculation of defect density distribution in the substrate wafer and the same studies were done after fabrication removing metallization. The failure analysis was performed on all these wafers to find out as to how a particular defect has impacted the breakdown voltage of the JBS rectifiers. It was revealed that the screw dislocation density as

calculated in both substrate and epi in devices shown in figure 64 (a)- (d) did not have significant influence on the device performance unlike other defects observed such as triangular defects and stacking faults which clearly affected the performance. This was true for more than 150 devices studied.

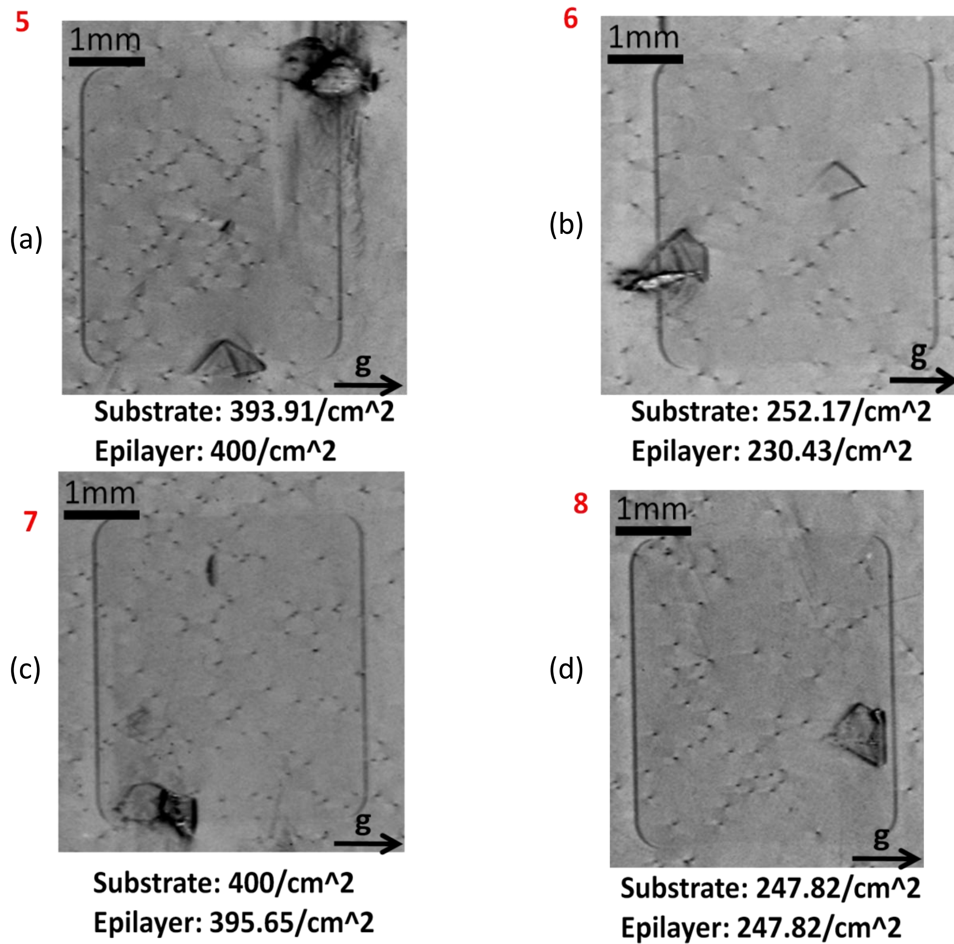


Figure 64 (a) - (d) show four devices marked 5-8 that failed and have low breakdown voltage. The SWBXT images (a) - (d) also show screw dislocation density in both substrate and epilayer.

Future Work

Silicon Carbide with its excellent electrical, mechanical, physical and chemical properties over conventional semiconductor materials has the potential to replace these materials and play a major role especially in energy sector which is receiving lot of attention at this moment. Large scalecommercial use of SiC in energy sector can definitely improve the efficiency and reliability of high power electronics lowering the cost and amount of energy consumption. For this to become a reality the main problem affecting their usage which is high defect density has to continue to receive attention so that new phenomena related to defects might be revealed and defect density especially the crystallographic go down to the level of Si.

The defect densities have gone down in last five years which aided us to study interesting defect features and develop growth models for processing teams in industries. This collaboration of SiC industries with research labs at universities must continue as to further reduce the density of defects. Models can be further developed to understand the stacking fault formation in substrates and epilayers especially the combination of Shockley plus Frank type faults which will definitely shed further light as to how devices are failing. The stacking faults need to be completely eliminated from the wafers for this it is important to study the seed carefully, take into account the offcut angle used and other factors that can affect the defect density. The vacuum furnaces used for PVT and CVD growth of SiC needs to be studied like the shape of furnace, temperature, pressure used and it must be kept free of contaminants which can be also become a big factor affecting the density of defects. Most of the defects studied in this work are in the primary slip system but the defects occurring in prismatic slip system also needs more detailed careful attention as that can reveal interesting phenomena contributing in reduction of density.

One of the ways of reducing the manufacturing costs is to increase the size of wafers and the processes used for current 150mm needs to become more consistent as the density of various defects are not same in wafers studied recently from multiple boules.

References

[1] A.R. Verma and P. Verma, *Polymorphism and Polytypism in Crystals* (Wiley, New York, 1966)

[2] H. Baumhauer, Z. Kristollogra. 50, 33 (1912)

[3] N.W. Jepps and T.F. Page, Prog. Cryst. Growth Charact. 7, 259 (1983).

[4] R.S. Ramsdell, Am. Mineral. 32, 64(1947)

[5] R.C. Glass, D. Henshall, V.F. Tsvetkov, C.H. Carter Jr.*: SiC- seeded crystal growth, MRS bulletin* 22,30-35(1997)

[6] Acheson, A. G. 1892. Engl. Pat. 17911 (The method has been described in W. F. Knippenberg. (1963). Growth phenomena in SiC. Philips Research Reports. 18, 161-274. (Ed, the Research Laboratory of N. V., Eindhoven, Netherlands: Philips gloeilampenfabriken)

[7] A. J. Lely: *Darstellung von Einkristanllen von Siliziumcarbid und Beherrschung von Art und Menge der einggebauten Verunreinigungen, Ber. Dtsch. Keram. Ges*. 32, 229-231(1955)]

[8] Tairov, Y.M. and V.F. Tsvetkov. 1978. *J. Crystal Growth.* 43:209

[9] Tairov Y.M. and V.F. Tsvetkov. 1981. General principles of growing large- size single crystals of various SiC polytypes. *J. Cryst. Growth.* 52:146-150

[10] R.L. Myers, Y. Shishkin, O. Kordina, I. Haselbarth and S.E. Saddow. High epitaxial growth rate of 4H-SiC using Horizontal Hot- wall CVD, Materials Science Forum Vols. 527-529(2006)187-190.

[11] Rong Jun Liu, Chang Rui Zhang, XinGui Zhou and YingBin Cao; J. Crystal Growth 270(2004), 1-2, pp.124-127

[12] Yingbin and Mark S. Gordon; J. Phys. Chem. A 111 (2007) pp. 1462-1474

[13] T. Ohno, H. Yamaguchi, S. Kuroda, K. Kojima, T. Suzuki, K. Arai; J. Crystal Growth 260(2004), 209-216

[14] K. Kojima, H. Okumura, S. Kuroda, K. Arai, A. Ohi, and H. Akinaga; Material Science Forum, 483-485(2005), 93-96

[15] S. E. Saddow and A. K. Agarwal, *Advances in silicon carbide processing and applications*. (Artech House, 2004).

[16] Microelectronics Reliability 46(2006) 713-730

[17] K. Koga, Y. Fujikawa, Y. Ueda and T. Yamaguchi, Springer Proc. Phys. 71, 96 (1992)

[18] P. G. Neudeck and J. A. Powell, IEEE Electron. Device Letters 15, 63 (1994)

[19] P. G. Neudeck, W. Huang and M. Dudley, Solid-State Electronics 42, 2157 (1998)

[20] J . P. Bergman, H. Lendenmann, P. A. Nilsson and P. Skytt, Mater. Sci. Forum 353-356 (2001) 299

[21] R. E. Stahlbush, M. Fatemi, J. B. Fedison, S. D. Arthur, L. B. Rowland and S. Wang, J. Electron. Mater. 31 (2002) 827

[22] W. M. Vetter and M. Dudley, J. Appl. Cryst. 35, 689 (2002)

[23] M. Dudley, X.R. Huang , W. Huang, A. Powell, S. Wang, P. Neudeck, M. Skowronski. The mechanism of micropipe nucleation at inclusions in SiC, Applied Physics letters, Vol. 75, 6, 784-786
[24] E. K. Sanchez, J. Q. Liu, M. D. Graef, M. Skowronski, W. M. Vetter and M. Dudley, J. Appl. Phys. 91, 1143 (2002)
[25] X. R. Huang, M. Dudley, W. M. Vetter, W. Huang, S. Wang and C. H. Carter, Jr. Appl. Phys. Lett. 74 (1999) 353
[26] T. A. Kuhr, E. K. Sanchez, M. Skowronski, W. M. Vetter and M. Dudley, J. Appl. Phys. 89, 4625 (2001)
[27] M. Dudley, S. Wang, W. Huang, C.H. Carter Jr., V.F. Tsvetkov and C. Fazi, J. Phys. D: Appl. Phys. 28(1995) A63
[28] W. Wang, M. Dudley, J. C. H. Carter, V. F. Tsvetskov and C. Fazi, Mat. Res. Soc. Symp. Proc. 375, 281 (1995)
[29] Skwronski student paper- trapezoidal and find the reference there
[30] M. Skowronski, J. Q. Liu, W. M. Vetter, M. Dudley, C. Hallin and H. Lendenmann, J. Appl. Phys. 92, 4699 (2002)
[31] S. Ha, N. T. Nufher, G. S. Rohrer, M. D. Graef and M. Skowronski, J. Eletron. Mater. 29 (2000) L5
[32] Y. Chen, Ph. D. thesis, State University of New York at Stony Brook (2008)
[33] H. Wang, S. Sun, M. Dudley, S. Byrappa, F. Wu, B. Raghothamachar, G. Chung, E.K. Sanchez, S.G. Mueller, D. Hansen and M. Laboda, in Jour. Electronic Mater., Vol. 42, pp. 794- 798 (2013)
[34] Z. Zhang and T. S. Sudarshan, Applied Physics Letters, 87, 151913(2005)
[35] K. Maeda, K. Suzuki, S. Fujita, M. Ichihara and S. Hyodo, Phil. Mag. A 57(1988)573
[36] M. Skowronski, J. Q. Liu, W. M. Vetter, M. Dudley, C. Hallin and H. Lendenmann, J. Appl. Phys. 92, 4699 (2002)
[37] M. Dudley, N. Zhang, S. Byrappa, Y. Zhang, B. Raghothamachar and E.K. Sanchez, Mater. Sci. Forum, 645-648, 295 (2010).
[38] M. Selder, L. Kadinski, F. Durst, T.L. Straubinder, P.L. Wellmann and D. Hofmann: Mater. Sci. Forum Vol. 353-356(2001), p.65
[39] M. Dudley, S. Byrappa, H. Wang, F. Wu, Y. Zhang, B. Raghothamachar, G. Choi, E.K. Sanchez, D. Hansen, R. Drachev and M. Loboda, Mater. Res. Soc. Symp. Proc., 1246-B02-02 (2010).
[40] S. Byrappa, F. Wu, H. Wang, B. Raghothamachar, G. Choi, S. Sun, M. Dudley, E.K. Sanchez, D. Hansen, R. Drachev and M. Laboda, in Mater. Sci. Forum, Vols. 717-720, pp. 347-350 (2012).
[41] S. Ha, M. Skowronski, S. Ha, Jour. Of Appl. Phys., 96, pp. 393-398 (2004).
[42] H. Wang, S. Byrappa, F. Wu, B. Raghothamachar, M. Dudley, E.K. Sanchez, D. Hansen, R. Drachev and M. Laboda, in Mater. Sci. Forum, Vols. 717-720, pp. 327-330 (2012).

[43] H. Lendenmann, F. Dahlquist, N. Johansson, R. Soderholm, P. A. Nilsson, J. P. Bergman, and P. Skytt, *Mater. Sci. Forum*, 353-356, 727 (2001)
[44] A. Galeckas, J. Linnros, and P. Pirouz, *Appl. Phys. Lett.,* 81, 883 (2002)
[45] J. D. Weeks, J. C. Tully, and L. C. Kimerling, *Phys. Rev. B*,12, 3286 (1975)
[46] H. Sumi, *Phys. Rev. B,* 29, 4616 (1984)
[47] Y. Chen, M. Dudley, K. X. Liu, and R. E. Stahlbush, *Appl. Phys. Lett.*, 90, 171930 (2007)
[48] J.J. Sumakeris, J.P. Bergman, M.K. Das, C. Hallin, B.A. Hull, E. Janzen, H. Lendenmann, M.J. O'Loughlin, M.J. Paisley, S. Ha, M. Skowronski, J.W. Palmour, and C.H. Carter, Jr., Mater. Sci. Forum, 141, pp. 527-529 (2006).
[49] H. Song, T. Rana, and T.S. Sudarshan, J. Crys. Growth, 320, 95 (2011).
[50] X. Zhang and H. Tsuchida, in Jour. Of Appl. Phys., 111, 123512 (2012).
[51] B.L. VanMil, R.E. Stahlbush, R.L. Myers- Ward, K-K Lew, C.R. Eddy, Jr., and D.K. Gaskill, J. Vac. Sci. Technol. B 26, 1504 (2008).
[52] H. Matsunami, T. Kimoto: Step Controlled Epitaxial Growth of SiC: High Quality Homoepitaxy, Mater. Sci. Eng. R20, 125-166 (1997)
[53] K. Shibahara, S. Nishino, H. Matsunami, in Appl. Phys. Lett., 50 (26): 1888-1890 (1987).
[54] H. Chen, G. Wang, X. Jia and M. Dudley, Mater. Res. Soc. Symp. Proc. 0911-B05-24 (2006).
[55] David R Black and Gabrielle G. Long, X-ray topography handout, April 2004
[56] A. Authier, in "*Dynamical Theory of X-ray Diffraction*", Oxford University Press, 2001 pp. 46
[57] B.K. Tanner, X-Ray Diffraction Topography, Pergamon press, 1976, pp.1-3
[58] B. Raghothamachar, G. Dhanaraj, J. Bai and M. Dudley, Microscopy Research and Technique, 69:000-000 (2006)
[59] Information and images on TEM from Electron Microscopy Facility at ETH Zurich website.
[60] W. Lang, Reprinted from Zeiss information no. 70, 16th year, pp. 114-120 (1968).
[61] P. Neudeck, W. Huang and M. Dudley, IEEE Trans. Electron. Devices, 46, 478-484; (1999).
[62] H. Chen, B. Raghothamachar, W. Vetter, M. Dudley, Y. Wang, B.J. Skromme, Mater. Res. Soc. Symp. Proc., 911, 0911-B12-03, 169-174, Warrendale, PA, (2006).
[63] M. Dudley, W. Si, S. Wang, C.H. Carter, Jr., R. Glass, and V.F. Tsvetkov: I1 Nuovo Cimento Vol. 19D (1997), p. 153.
[64] I. Kamata, M. Nagano, H. Tsuchida, Y. Chen, and M. Dudley: J. Cryst. Growth Vol. 311 (2009), p. 1416
[65] M. Dudley, Y. Chen and X.R. Huang: Mater. Sci. Forum, Vol. 600-603 (2009), p. 261
[66] M.H. Hong, A.V. Samant, and P. Pirouz, Philos. Mag. A 80, 919 (2000).
[67] P. Pirouz, J.L. Demenet, and M.H. Hong, Philos. Mag. A 81, 1207 (2001).
[68] M. Skowronski and S. Ha, J. Appl. Phys. 99, 011101 (2006).
[69] H. Tsuchida, I. Kamata, and M. Nagano, J. Cryst. Growth, 310, 757 (2008).

[70] A. Authier and Y. Epelboin, Phys. Status Solidi A, 41, K9 (1977).

[71] P. Pirouz and j.W. Yang, Ultramicroscopy, 51, 189- 214 (1993).

[72] M. Dudley, H. Wang, F. Wu, S. Byrappa, B. Raghothamchar, G. Choi, E.K. Sanchez, D. Hansen, R. Drachev, S.G. Mueller and M. Laboda, Mater. Sci. Forum, Vols. 679-680, p. 269- 272 (2011).

[73] X.R. Huang, et al., Appl. Phys. Let., Vol. 91, 231903 (2007)

[74] H. Lendenmann, F. Dahlquist, N. Johansson, R. Soderholm, P. A. Nilsson, J. P. Bergman and P. Skytt, Mater. Sci. Forum 353–356, 727 (2001).

[75] Y. Chen, G. Dhanaraj, W. Vetter, R. Ma and M. Dudley, Materials Science Forum, 556-557, 231-234, (2007)

[76] M. H. Hong, A.V. Samant and P. Pirouz, Philosopical Magazine A, 2000, Vol. 80, No. 4, 919-935

[77] N. Zhang, Y. Chen, Y. Zhang and M. Dudley, Appl. Phys. Lett., 94, 122108, (2009).

[78] W. Shockley, Introductory Remarks, in: Silicon Carbide: A High Temperature Semiconductor, Pergamon, Oxford, 1960.

[79] F. Dahlquist, Karlstad University, Dissertation thesis, 2001.

[80] B.M. Wilamowski, Solid- State Electronics, 26, 491 (1983).

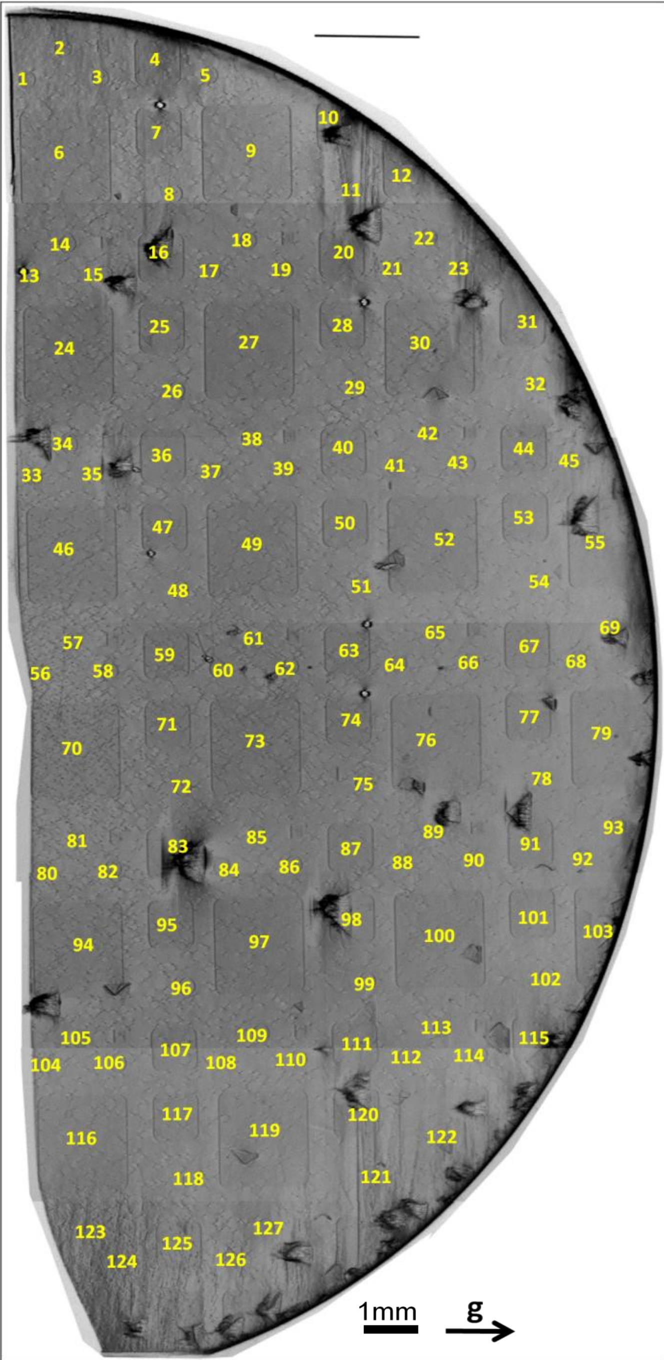
[81] B.J. Baliga, IEEE Elec. Dev. Lett., 5, 194 (1984).

[82] R.A. Berechman, M. Skowronski, S. Soloviev, P. Sandvik, Jour. Of App. Physics, 107, 114504 (2010).

[83] R.A. Berechman, M. Skowronski, and Q. Zhang, Jour. Of App. Physics, 105, 74513 (2009).

Appendix

Appendix I. Correlation of defects with device (JBS rectifiers) performance



SWBXT image by Grazing geometry recorded after device fabrication and devices are marked 1- 127

Table below shows a list of 127 devices. The density of screws was calculated from substrate and after device fabrication which was correlated with the breakdown voltage for each rectifier. Screw dislocation density (SDD/ cm^2) in the table below was calculated in the substrate and also after JBS rectifiers were fabricated.

Device Number	Screws(Substrate)	SDD /cm^2	Screws(Device)	SDD /cm^2	Breakdown Voltage
1	0	0	0	0	>1900
2	2	400	2	400	<100
3	2	400	1	200	>1900
4	not good	Not good	16	266.6667	No device map
5	2	400	1	200	<100
6	57	247.82609	56	243.4783	>1900
7	24	400	21	350	>1900
8	2	400	1	200	>1900
9	72	313.04348	67	291.3043	>1900
10	cut	cut	cut	cut	No device map
11	3	600	3	600	>1900
12	cut	cut	cut	cut	No device map
13	3	600	3	600	>1900
14	0	0	0	0	>1900
15	3	600	2	400	>1900
16	13	216.66667	7	116.6667	<100
17	1	200	2	400	>1900
18	1	200	1	200	>1900
19	2	400	0	0	>1900
20	14	233.33333	14	233.3333	100-1700
21	3	600	3	600	>1900
22	4	800	3	600	>1900
23	3	600	3	600	No device map
24	114	495.65217	113	491.3043	>1900
25	18	300	16	266.6667	>1900
26	3	600	3	600	>1900
27	54	234.78261	54	234.7826	>1900
28	22	366.66667	20	333.3333	>1900
29	2	400	2	400	>1900
30	86	373.91304	92	400	<100
31	6	100	6	100	No device map
32	1	200	1	200	No device map
33	4	800	2	400	>1900
34	3	600	3	600	>1900
35	4	800	3	600	>1900

36	17	283.33333	15	250	>1900
37	1	200	1	200	>1900
38	3	600	2	400	>1900
39	3	600	2	400	>1900
40	31	516.66667	31	516.6667	>1900
41	0	0	0	0	>1900
42	2	400	2	400	>1900
43	2	400	1	200	>1900
44	19	316.66667	16	266.6667	1700-1800
45	3	600	2	400	No device map
46	149	647.82609	148	643.4783	>1900
47	23	383.33333	22	366.6667	>1900
48	3	600	3	600	>1900
49	109	473.91304	109	473.913	>1900
50	16	266.66667	16	266.6667	>1900
51	4	800	4	800	>1900
52	58	252.17391	53	230.4348	<100
53	11	183.33333	11	183.3333	>1900
54	2	400	1	200	>1900
55	40	173.91304	40	173.913	No device map
56	9	1800	9	1800	>1900
57	5	1000	7	1400	>1900
58	8	1600	4	800	<100
59	43	716.66667	39	650	>1900
60	3	600	3	600	>1900
61	4	800	3	600	>1900
62	4	800	7	1400	>1900
63	36	600	36	600	>1900
64	4	800	2	400	>1900
65	2	400	1	200	>1900
66	4	800	4	800	>1900
67	21	350	21	350	>1900
68	1	200	1	200	100-1700
69	0	0	0	0	No device map
70	440	1913.0435	438	1904.348	>1900
71	37	616.66667	34	566.6667	>1900
72	1	200	1	200	>1900
73	148	643.47826	147	639.1304	>1900
74	27	450	26	433.3333	>1900
75	6	1200	6	1200	>1900
76	92	400	91	395.6522	<100
77	14	233.33333	13	216.6667	<100
78	1	200	1	200	>1900

79	40	173.91304	40	173.913	No device map
80	2	400	2	400	>1900
81	8	1600	8	1600	>1900
82	6	1200	6	1200	>1900
83	18	300	10	166.6667	<100
84	3	600	2	400	>1900
85	1	200	1	200	>1900
86	0	0	0	0	>1900
87	24	400	19	316.6667	>1900
88	1	200	1	200	>1900
89	0	0	0	0	>1900
90	3	600	3	600	>1900
91	12	200	6	100	<100
92	1	200	2	400	No device map
93	1	200	1	200	No device map
94	150	652.17391	138	600	<100
95	32	533.33333	28	466.6667	>1900
96	0	0	0	0	>1900
97	71	308.69565	62	269.5652	<100
98	11	183.33333	4	66.66667	<100
99	1	200	1	200	>1900
100	57	247.82609	57	247.8261	<100
101	9	150	9	150	No device map
102	2	400	1	200	No device map
103	cut	cut	cut	cut	No device map
104	4	800	4	800	>1900
105	3	600	2	400	>1900
106	0	0	0	0	>1900
107	20	333.33333	17	283.3333	>1900
108	0	0	0	0	>1900
109	2	400	1	200	>1900
110	2	400	2	400	>1900
111	22	366.66667	20	333.3333	<100
112	1	200	1	200	>1900
113	0	0	0	0	>1900
114	2	400	2	400	No device map
115	11	183.33333	7	116.6667	No device map
116	79	343.47826	66	286.9565	>1900
117	21	350	16	266.6667	>1900
118	4	800	4	800	<100
119	76	330.43478	72	313.0435	<100
120	15	250	9	150	<100
121	4	800	2	400	No device map

122	cut	cut	cut	cut	No device map
123	2	400	2	400	>1900
124	4	800	4	800	>1900
125	24	400	17	283.3333	<100
126	2	400	2	400	No device map
127	1	200	0	0	No device map

Appendix II. Structure factor calculations for 4H- and 6H- SiC

X- Ray Topography takes into account point to point variation of diffracted beam intensity therefore structure factor which determines the diffraction intensity becomes a critical parameter for defects study.

Table. Fractional coordinates of Si and C atoms for *4H*- and *6H*-SiC unit cells

	4H-SiC	**6H-SiC**
Si	(0,0,0), (0,0,1/2), (1/3,2/3,3/4),(2/3,1/3,1/4)	(0,0,0), (0,0,1/2), (1/3,2/3,1/3), (1/3,2/3,2/3), (2/3,1/3,1/6), (2/3,1/3,5/6)
C	(0,0,11/16), (0,0,3/16), (1/3,2/3,15/16), (2/3,1/3,7/16)	(0,0,1/8), (0,0,5/8), (1/3,2/3,11/24), (1/3,2/3,19/24), (2/3,1/3,23/24), (2/3,1/3,7/24)

The structure factors of 4H- and 6H-SiC are given by the following:

4H-SiC:

$$F_{hkl} = \sum_i f_i e^{-i2\pi(hu+kv+lw)}$$

$$= f_c\left(e^{-i2\pi\frac{11}{16}l} + e^{-i2\pi\frac{3}{16}l} + e^{-i2\pi(\frac{1}{3}h+\frac{2}{3}k+\frac{15}{16}l)} + e^{-i2\pi(\frac{2}{3}h+\frac{1}{3}k+\frac{7}{16}l)}\right) + f_{Si}\left(e^{-i2\pi 0} + e^{-i2\pi\frac{1}{2}l} + e^{-i2\pi(\frac{1}{3}h+\frac{2}{3}k+\frac{3}{4}l)} + e^{-i2\pi(\frac{2}{3}h+\frac{1}{3}k+\frac{1}{4}l)}\right)$$

6H-SiC:

$$F_{hkl} = \sum_i f_i e^{-i2\pi(hu+kv+lw)}$$

$$= f_c\left(e^{-i2\pi\frac{1}{8}l} + e^{-i2\pi\frac{5}{8}l} + e^{-i2\pi(\frac{1}{3}h+\frac{2}{3}k+\frac{11}{24}l)} + e^{-i2\pi(\frac{1}{3}h+\frac{2}{3}k+\frac{19}{24}l)} + e^{-i2\pi(\frac{2}{3}h+\frac{1}{3}k+\frac{23}{24}l)} + e^{-i2\pi(\frac{2}{3}h+\frac{1}{3}k+\frac{7}{24}l)}\right)$$
$$+ f_{Si}\left(e^{-i2\pi 0} + e^{-i2\pi\frac{1}{2}l} + e^{-i2\pi(\frac{1}{3}h+\frac{2}{3}k+\frac{1}{3}l)} + e^{-i2\pi(\frac{1}{3}h+\frac{2}{3}k+\frac{2}{3}l)} + e^{-i2\pi(\frac{2}{3}h+\frac{1}{3}k+\frac{1}{6}l)} ++ e^{-i2\pi(\frac{2}{3}h+\frac{1}{3}k+\frac{5}{6}l)}\right).$$