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Investigating the Tolerance of Wirelessly Powered Charge-Recycling Logic to Power-Clock Phase Difference Deviations

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Abstract of the thesis

Investigating the Tolerance of Wirelessly Powered Charge-Recycling Logic to Power-Clock Phase Difference Deviations

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Internet-of-things (IoT) has emerged as an exciting application domain for semiconductor electronics. Recently, a new circuit design framework has been developed where charge-recycling circuits were leveraged to wirelessly power IoT based devices. Most of the existing charge-recycling circuits require multiple AC signals (referred to as power-clock signals) with certain phase difference to operate. The primary objective of this thesis is to investigate the tolerance of wirelessly powered charge-recycling circuits to non-ideal phase differences among power-clock signals. The operation principle of the most common charge-recycling (also referred to as adiabatic) circuits is described. The power consumed by efficient charge recovery logic (ECRL), complementary energy path adiabatic logic (CEPAL) and static CMOS logic are compared. The circuit considered for power comparison is a 16-bit carry select adder (CSA) and results verify that the charge-recycling operation consumes less power as compared to static CMOS logic which is in coherence with the theoretical expectation. In ECRL, each stage receives a power-clock signal that ideally should be 90° ahead of the power-clock signal of the previous stage. The VDD counterpart of static CMOS is the power-clock signal whereas the GND remains the same. In CEPAL, each logic gate employs two power-clock signals

with 180° phase difference. These power-clock signals correspond to the VDD and GND in static CMOS. The 16-bit carry select adder (designed in both ECRL and CEPAL) was used to investigate the effect of non-ideal phase differences on power consumption and accuracy. The tolerance of each charge-recycling logic to phase difference deviation has been quantified. For ECRL logic, a deviation of up to 30° does not affect the power consumption and functionality, irrespective of the power-clock frequency. If the phase difference deviation is higher than 30°, the power consumption significantly increases, but functionality is maintained. However for CEPAL, the tolerable deviation is inversely proportional with the power-clock frequency. For example, for a power-clock frequency of 10 MHz, CEPAL operates correctly until a phase difference deviation of 30° whereas for power-clock frequency of 30 MHz, CEPAL fails if the phase difference deviation is above 10°. Furthermore, unlike ECRL, in CEPAL the non-ideal phase difference affects the functionality rather than the power consumption.

To my dearest parents Banalata Panda and Parameswar Panda...

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Acknowledgements

My journey towards the Masters degree has been a really memorable one with some awesome persons coming into my life. The special mention of course goes to my thesis advisors Professor Emre Salman and Professor Milutin Stanacevic.

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Last but definitely not the least, I am thankful to my parents for their never-ending support and unconditional love towards me. I will do anything and everything to bring a smile on their face and strive all my life to make them proud. Love you and thank you.

Chapter 1

INTRODUCTION

As of 2015, 5.5 billion transistors can be integrated on a commercially available CPU [1]. Following Moore's Law, the total number of transistors on an integrated circuit has almost doubled every two, and most recently three years. With the increasing number of transistors and the Dennard scaling paradigm hitting the utilization wall, the power consumption has become a major concern [2]. Various techniques such as voltage scaling, minimizing interconnect capacitance by compact layout, clock gating, and power gating have been proposed to reduce power consumption in static CMOS circuits [3].

The output signals in static CMOS are obtained by either charging or discharging the output capacitance [4]. During the process of output evaluation, the charge is either drawn from the power source, thereby charging the output node capacitance to obtain logic one or transmitted to the ground, thereby discharging the output node capacitance to obtain a logic zero. This process of charging and discharging the output capacitance is irreversible.

Thermodynamically, a process that does not involve the transfer of heat or matter into or out of a system is called an adiabatic process [5]. In the world of very large scale integration (VLSI), the charge can be considered analogous to matter and hence an adiabatic circuit can be defined as a circuit that does not involve any charge dissipation at the load capacitance [6]. Since there is no charge dissipation, the energy dissipated at the load capacitance is zero. There is however energy dissipation across the on-resistance of the transistors. The zero energy dissipation at the load capacitance is possible only when the charge that has been transferred to the output node capacitance is given back

to the power source rather than being dissipated to ground. This phenomenon can be achieved by employing various circuit topologies referred to as charge-recycling or adiabatic circuits [7]. The charge-recycling circuits operate with a trapezoidal or AC power supply referred to as power-clock signal (PC). There can be single or multiple PCs in a particular logic [8]. In charge-recycling logic with multiple PCs, a certain phase difference should be maintained between the PCs in order to obtain the desired operation.

The operation of charge-recycling circuits, in general, can be divided into four intervals:

1. Evaluation (E): During the *evaluation* interval, the output is evaluated from the stable input signals.
2. Hold (H): During the *hold* interval, the outputs are maintained constant to provide stable inputs to the subsequent stage.
3. Recover (R): Energy is recovered during the *recover* interval.
4. Wait (W): To maintain the symmetry in the signal a *wait* interval is inserted as symmetric signals are easier to generate.

Figure 1.1 represents the various intervals of operation for charge-recycling circuits.

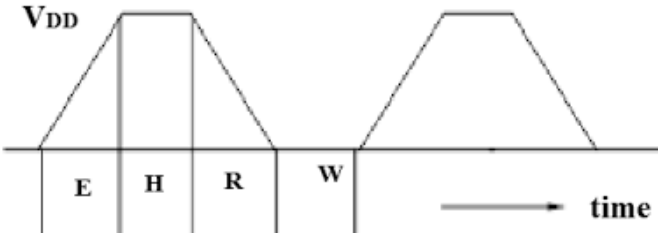

FIGURE 1.1: Various intervals of operation for charge-recycling circuits [9].

Depending on the number of power-clock signals employed in the circuit, the number of intervals can change and two or more of the above intervals can be combined to form one interval for the circuit [10].

1.1 Synergy Between Wireless Power Harvesting and Charge-Recycling Circuit

Charge-recycling circuits have been investigated since 1990s, but have not become a mainstream design method due to the following reasons:

5. The power-clock signals are AC signals and the process of converting the DC signal into multiple AC signals is highly lossy, sacrificing most of the energy saved during operation.

6. The charge-recycling circuits operate at a much lower frequency as compared to the static CMOS circuits.

Since the charge-recycling circuits employ AC signals to operate and the wirelessly harvested power is in the form of an AC signal, a unique synergy exists between charge-

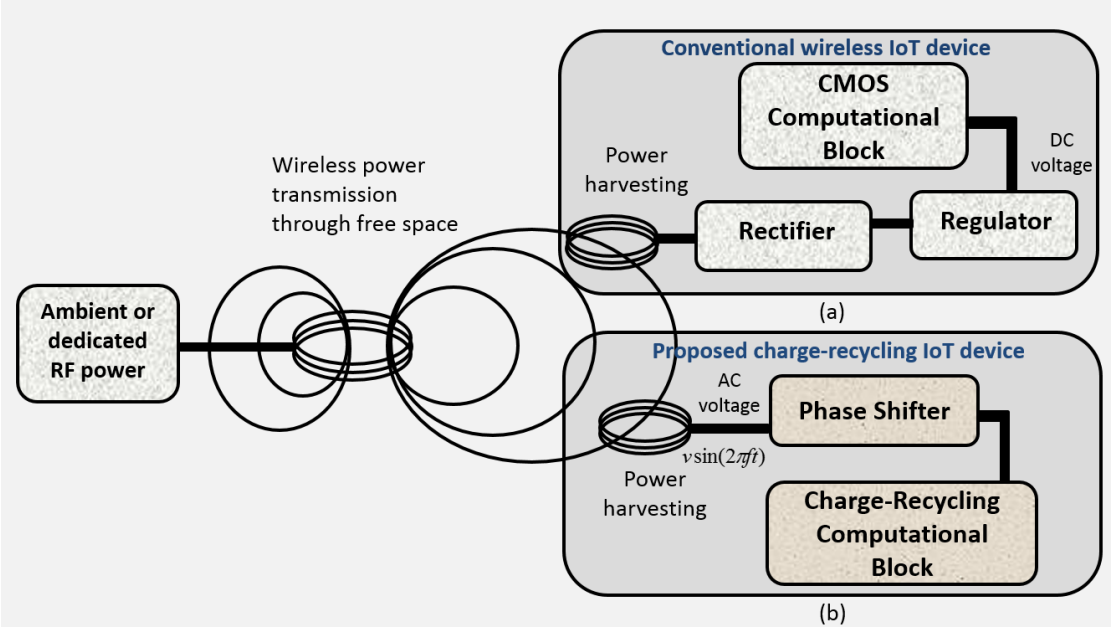

FIGURE 1.2: Conceptual diagram for wireless power harvesting [11].

recycling circuits and wireless power harvesting [11]. Figure 1.2 is a conceptual diagram which shows the conventional and the recently proposed wireless power harvesting technique. The proposed technique eliminates the highly lossy rectifier and regulator. Instead, a phase shifter is used that provides the required power-clock signals with desired phase difference. These multiple AC signals are directly used by the charge-recycling logic.

An issue that needs further investigation is the effect of non-ideality (which can be exhibited by phase shifter) on the power consumption and functionality. This thesis is aimed at investigating this non-ideality in the phase difference and determine the tolerable deviation that does not significantly affect the power consumption and functionality. The primary operating frequency is 13.56 MHz which is one of the RFID operating frequencies.

The thesis is organized as follows. Chapter 2 presents a theoretical comparison of power consumed by static CMOS and charge-recycling circuits, followed by a brief insight into the types and operation of various adiabatic logic families. Chapter 3 focuses on two of the adiabatic logic families and comparison with static CMOS topology in terms of operation and power consumption. Chapter 4 describes the simulation results about the relationship among the power-clock phase difference deviation, power consumption and power-clock frequency for two charge-recycling logic families. Finally, Chapter 5 has the concluding remarks.

Chapter 2

BACKGROUND ON CHARGE-RECYCLING

In this chapter, the power consumed by CMOS and charge-recycling circuits is compared followed by the operation principle of common charge-recycling logic circuits. The power consumption comparison also describes how charge-recycling circuits consume low power at the expense of low operating frequency.

2.1 Power Consumption: A Quantitative Approach

2.1.1 Power Consumption in Static CMOS

First, a static CMOS inverter is observed for power consumption over a period of time t_1 to t_2. Figure 2.1 shows a static CMOS inverter with a load capacitance C at the output. The capacitor is either charged or discharged depending on whether the PMOS or NMOS is on [7]. Amount of charge stored in the capacitor is given as $Q = CV_{dd}$ and the energy consumed from the source is given as

$$E_{V_{dd}} = QV_{dd} = CV_{dd}^2. \tag{2.1}$$

Energy stored at the load capacitor is

$$E_C = \frac{1}{2}CV_{dd}^2. \tag{2.2}$$

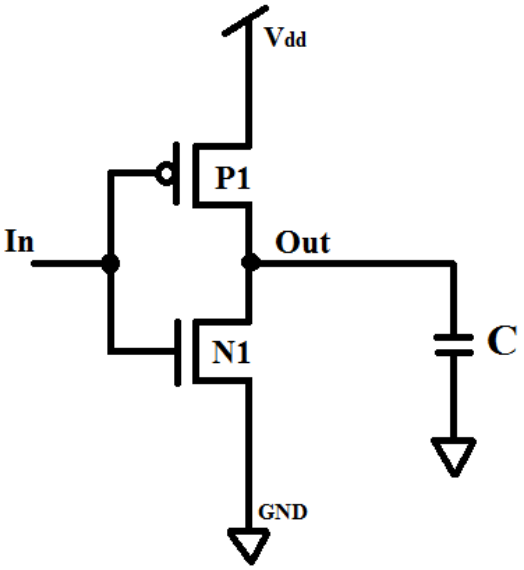

FIGURE 2.1: Static CMOS inverter with load capacitance.

Overall energy dissipated in the PMOS transistor is given as

$$E_{diss} = E_{V_{dd}} - E_C = \frac{1}{2}CV_{dd}^2. \tag{2.3}$$

The energy dissipation of a switching event in static CMOS gate is

$$E_{CMOS} = \alpha\frac{1}{2}CV_{dd}^2, \tag{2.4}$$

where α is the switching probability. Over a period of time from t_1 to t_2, the power consumed is

$$P = \frac{1}{T}E_{CMOS}, \tag{2.5}$$

where T $= t_2 - t_1$.

2.1.2 Power Consumption in Charge-Recycling Circuits

Power consumed by charging a capacitor adiabatically can be calculated by considering the circuit shown in Figure 2.2 [7, 12, 13]. If *in* is initially 1, N1 is on which causes P2 to turn on. Assuming the on-resistance of a transistor is R and power-clock signal ϕ=$v(t)$ goes from 0 to V_{dd} gradually over a time T, a small voltage difference $v_R(t)$ is maintained

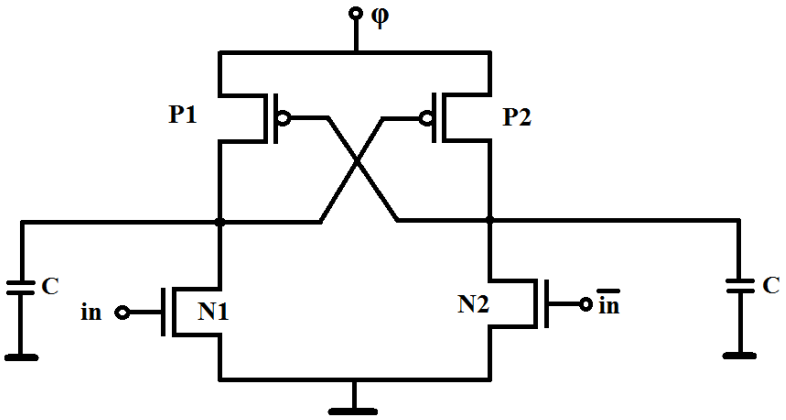

FIGURE 2.2: An example of adiabatic inverter with load capacitance.

across the transistor. Since the voltage build up across the capacitor is gradual, $v_C(t)$ follows power-clock signal, thereby $v_C(t) \approx v(t)$. Hence, the current in the circuit is given as

$$i(t) = C\frac{dv(t)}{d(t)} = C\frac{V_{dd}}{T}. \tag{2.6}$$

Energy consumed while charging the load capacitor is

$$E = \int_0^T p(t)\mathrm{d}t = \int_0^T v(t)i(t)\mathrm{d}t = \int_0^T (v_R(t) + v_C(t))i(t)\mathrm{d}t. \tag{2.7}$$

Over one clock cycle, the integral of $v_C(t)i(t)$ is zero as there is no energy dissipated across the capacitor, attributed to the recovery of the charge. Hence the overall energy consumed because of the on-resistance R of the transistor is given as

$$E = \int_0^T R\frac{C^2{V_{dd}}^2}{T^2}\mathrm{d}t = \frac{RC}{T}C{V_{dd}}^2. \tag{2.8}$$

As one complete cycle consists of charging and recovery, the same amount of energy is dissipated twice across the on-resistance, thereby the total energy dissipation in the charge-recycling logic is

$$E_{AL} = 2\frac{RC}{T}C{V_{dd}}^2. \tag{2.9}$$

Equation (2.9) shows that the total energy is a function of operating frequency. Thus, unlike static CMOS where dynamic energy consumption is independent of frequency, in adiabatic logic, a lower operating frequency reduces the energy dissipation. A minimum transition time T for which the adiabatic circuits are more efficient than static CMOS

is

$$T > \frac{4RC}{\alpha}, \tag{2.10}$$

where α is the switching probability of static CMOS circuit, R is the on-resistance of the transistor in the adiabatic circuit and C is the load capacitance [7].

2.2 Types of Charge-Recycling logic

This section describes the operation of an inverter in several charge-recycling logic families [14–17].

2.2.1 Efficient Charge Recovery Logic (ECRL)

Figure 2.3 shows an ECRL inverter and the power-clock signal ϕ [7, 18, 19]. It is assumed that in is at logic high and $\overline{in}$ is at logic low. When power-clock signal ϕ rises

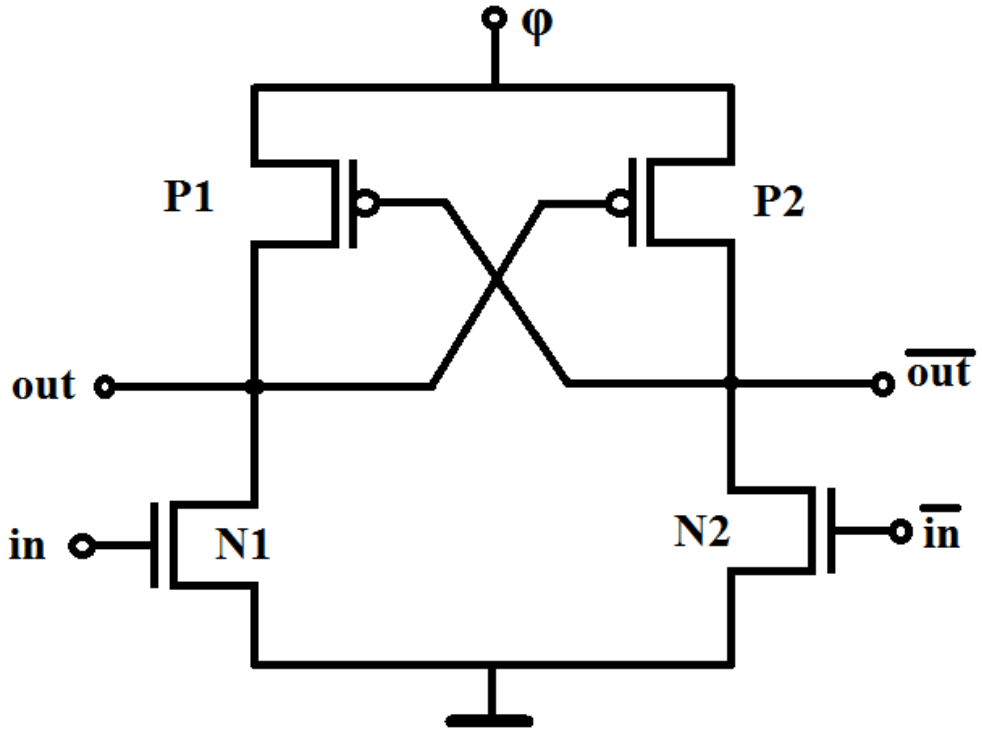

FIGURE 2.3: ECRL inverter.

from 0 to V_{dd}, out is at 0 as N1 is on thereby P2 is on. As ϕ goes above V_{tp}, P2 starts

conducting and $\overline{out}$ follows ϕ. As ϕ reaches V_{dd}, both out and $\overline{out}$ are at valid logic and this state is held until ϕ maintains its state at V_{dd}. Once ϕ starts falling from V_{dd} to 0, the charge stored at load capacitance is transferred back to the power supply but only until P2 turns off (ϕ falls to V_{tp}). Lastly, ϕ is held at 0 for an equal amount of time to maintain symmetry in the power-clock signal. Figure 2.4 shows the input and output waveforms of an ECRL inverter. In case of cascaded gates in ECRL, the power-

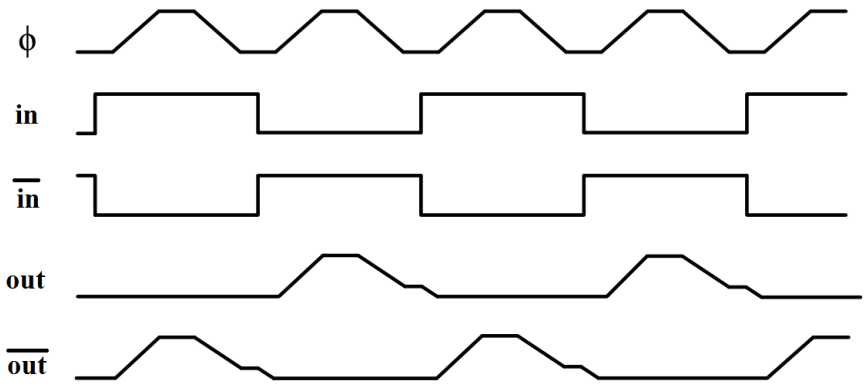

FIGURE 2.4: ECRL inverter input and output signals.

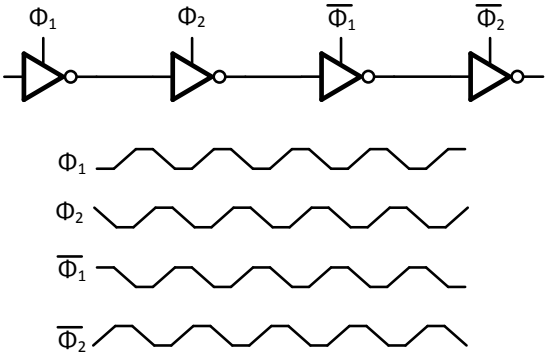

FIGURE 2.5: Cascaded ECRL inverter with power-clock signal for each stage.

clock signals of two consecutive stages have a 90° phase difference. Figure 2.5 shows the power-clock signals for a 4-stage cascaded logic assuming that the power-clock signal is trapezoidal. The detailed operation and relevance of power-clock phase difference are discussed in the next chapter.

2.2.2 Positive Feedback Adiabatic Logic (PFAL)

Figure 2.6 shows a PFAL inverter and the supply power-clock signal ϕ [7, 20]. Initially, when *in* is at 1, N4 is on, thereby $\overline{out}$ follows power-clock signal ϕ which switches N2

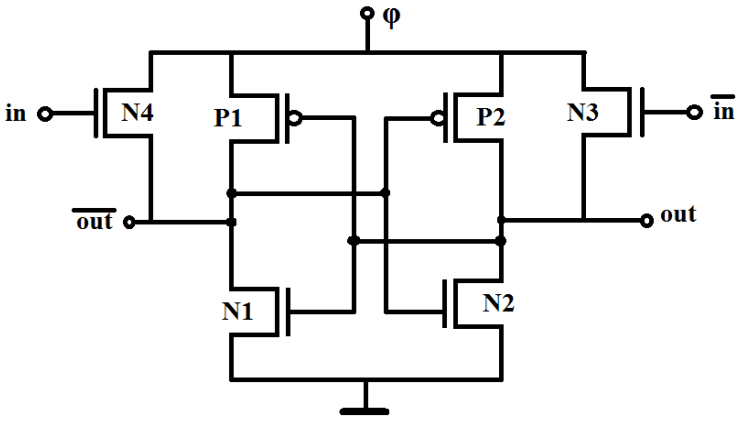

FIGURE 2.6: PFAL inverter.

on. Switching N2 on pulls *out* to 0. *Out* is the input to P1 hence P1 is on, thereby ensuring $\overline{out}$ remains at V_{dd} as long as ϕ is at V_{dd}. Once ϕ starts falling to 0, $\overline{out}$ follows power-clock signal and starts discharging. Since *out* is held at 0, there exists a path for the complete discharge of $\overline{out}$ unlike ECRL inverter. When ϕ is held at 0, $\overline{out}$ follows power-clock signal and *out* is still at 0. *out* starts following power-clock signal only when $\overline{in}$ changes to 1, i.e., *in* switches to 0. Similar to ECRL, PFAL also has a 90° phase difference between consecutive stages of logic.

2.2.3 Clocked Adiabatic Logic (CAL)

Figure 2.7 shows a CAL inverter with a power-clock signal ϕ and auxiliary timing control signal CX [21]. CX controls transistors N4 and N6 which are in series with logic transistors N3 and N5, respectively. When CX is high, logic evaluation is enabled. For $in = 0$, N5 is on because of which $\overline{out}$ is pulled down to logic 0. Since gate of P1 is connected to $\overline{out}$, *out* follows ϕ. If the auxiliary clock becomes 0, the previously stored logic state is maintained at the output irrespective of the inputs. Figure 2.8 shows the waveform response of CAL inverter [21]. All logic stages are supplied with the same power-clock signal and logic evaluation is enabled at every other logic stage by the auxiliary clock. Hence, CAL takes in new input every other power-clock cycle.

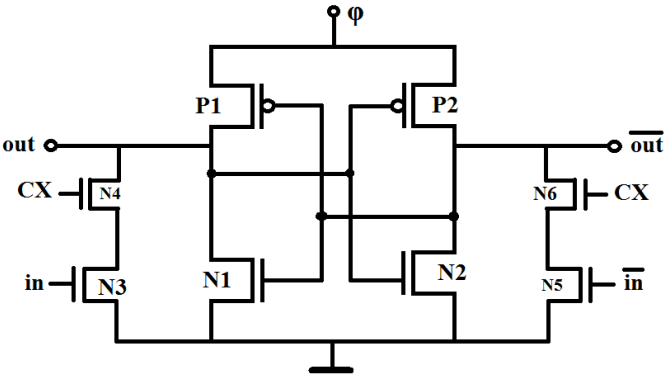

FIGURE 2.7: CAL inverter.

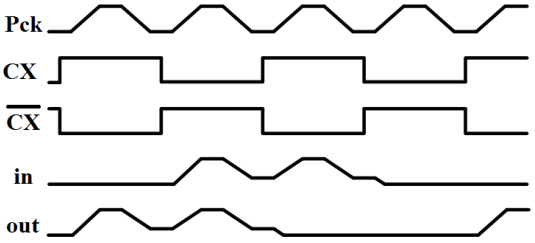

FIGURE 2.8: CAL inverter waveforms.

2.2.4 Complementary Pass Transistor Adiabatic Logic (CPAL)

A CPAL inverter is illustrated in Figure 2.9 [22]. The circuit consists of two main parts:

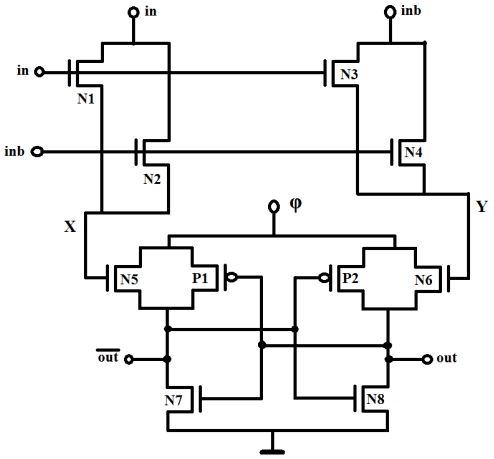

FIGURE 2.9: CPAL inverter.

the logic function and the load driven circuit. The transistors N1 to N4 constitute the

logic circuit employing the complementary pass transistor logic. The load driven circuit comprises of two transmission gates (N5, P1) and (N6, P2). The transistors N7 and N8 act as the clamp transistors with the main purpose of making the undriven output node grounded. The node X follows *in* and Y follows *inb*, hence when *in* is 1, X follows *in* and switches on N5, thereby allowing $\overline{out}$ to follow power-clock signal ϕ. When ϕ rises from 0 to V_{dd}, $\overline{out}$ goes to logic 1 and switches N8 on, thereby pulling *out* to 0. And since *out* is connected to gate of P1, it further enhances the charging process of $\overline{out}$ node. Similar to ECRL, cascaded CPAL requires multiple PCs with 90° phase difference.

2.2.5 Quasi Static Energy Recovery Logic (QSERL)

QSERL has an ideal diode that is connected between the source node of transistors and power line, as shown in Figure 2.10 [10]. The ideal diodes are replaced by diode

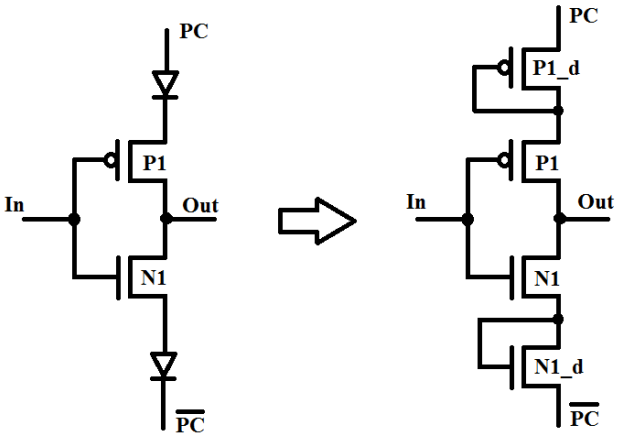

FIGURE 2.10: QSERL inverter with ideal diodes and diode connected transistors.

connected transistors and the power lines have AC power supplies (power-clock signals) which are 180° phase apart. For $In = 0$, the logic PMOS is on and as the PC goes from 0 to Vdd, the PMOS diode becomes forward biased, thereby *Out* follows the power-clock signal PC. For a cascaded QSERL logic, the power lines need to be switched for every other stage, i.e., if stage 1 PMOS diode receives PC, the following stage PMOS diode receives $\overline{PC}$ as the power-clock signal [10]. QSERL has the limitations of interlaced circuit configuration, floating output that are overcome by the complementary energy path adiabatic logic, as described in the following section. [23].

2.2.6 Complementary Energy Path Adiabatic Logic (CEPAL)

CEPAL is an improvement over the QSERL. The circuit configuration for a CEPAL

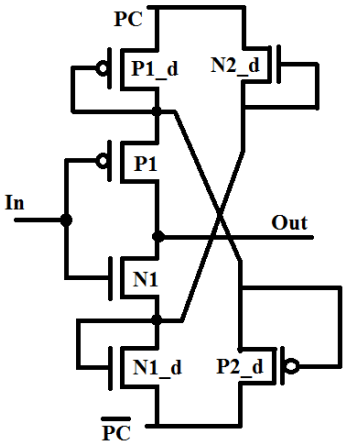

FIGURE 2.11: CEPAL inverter.

inverter is shown in Figure 2.11 [10, 23]. The improvement is achieved by placing an NMOS diode in parallel with the PMOS diode connected to the source of logic PMOS and also a PMOS diode in parallel with the NMOS diode connected to source of logic NMOS. Placement of these parallel complementary diodes provides a path between the source of logic transistors to power-clock signal at all times, unlike in QSERL, thereby eliminating the floating output condition. The cascaded stages have a continuous PC and $\overline{PC}$ without the need of alternating the power-clock signals. The CEPAL topology is discussed in more detail in the following chapter.

In this chapter, the design of an inverter in several charge-recycling logic families has been discussed and it was observed that for the logic families that need multiple power-clock signals for proper operation (cascaded or single stage), a certain phase difference between the power-clock signals needs to be maintained.

The main objective of the thesis is to study the effects of non-ideal phase difference among power-clock signals on the power consumption and functionality. A more complex circuit, 16-bit adder, is designed for this objective, as discussed in the following chapter.

Chapter 3

16-BIT ADDER DESIGN USING CHARGE-RECYCLING LOGIC

This chapter first describes the design and operation of a 16-bit carry select adder (CSA) designed in each logic, followed with a comparative analysis of power consumption. The motivation behind choosing ECRL and CEPAL for this study is:

7. ECRL employs a 90° phase difference between two consecutive stages and has the least number of transistors among the charge-recycling circuit families.

8. CEPAL employs 180° phase difference between the power-clock signals and is an improvement over the QSERL.

Static CMOS has been considered as the reference for the power comparison.

3.1 Circuit Architecture

The design approach for the 16-bit CSA is depicted in Figure 3.1 [24]. The design can be implemented in various approaches depending on the design of the 1-bit full adder. The 1-bit full adder has been implemented in two ways:

9. Propagate/Generate (PG) Logic: According to this logic, the operation can be performed by implementing the following Boolean expressions using the corresponding

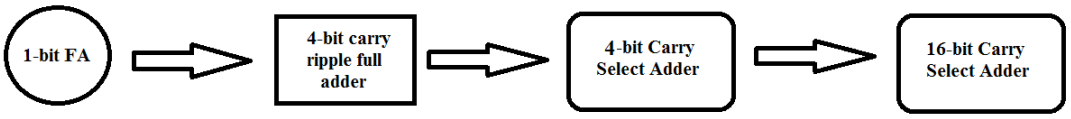

FIGURE 3.1: Hierarchical carry select adder design.

gates:

$$Sum = A \oplus B \oplus C_{in} \tag{3.1}$$

$$Carry = A \bullet B + (A \oplus B) \bullet C_{in}. \tag{3.2}$$

10. 28-transistor mirror adder: This is a single complex gate having 28 transistors to evaluate the sum and carry functions shown by Eqns. (3.1) and (3.2). The schematic for this circuit is shown in Figure 3.3.

The design and simulations are performed using FreePDK45 which is a 45 nm, 1 V process technology from North Carolina State University [25]. Nominal threshold voltage devices are used and simulations are performed using HSPICE.

The hierarchical structure of the 16-bit CSA is the same for all the logic types. There are minor changes in the design approach for ECRL 16-bit CSA which are explained later. Unless mentioned, the approach remains similar to the static CMOS logic.

3.1.1 Static CMOS based 16-bit CSA

3.1.1.1 Design of 1-bit FA

Figures 3.2 and 3.3 show the 1-bit full adder using the propagate/generate logic and 28 transistor mirror logic, respectively.

3.1.1.2 Design of 4-bit Ripple Carry Adder

The 4-bit adder is designed using the carry ripple topology. Figure 3.4 shows the circuit implementation. The 1-bit FA can either be the propagate/generate or mirror adder.

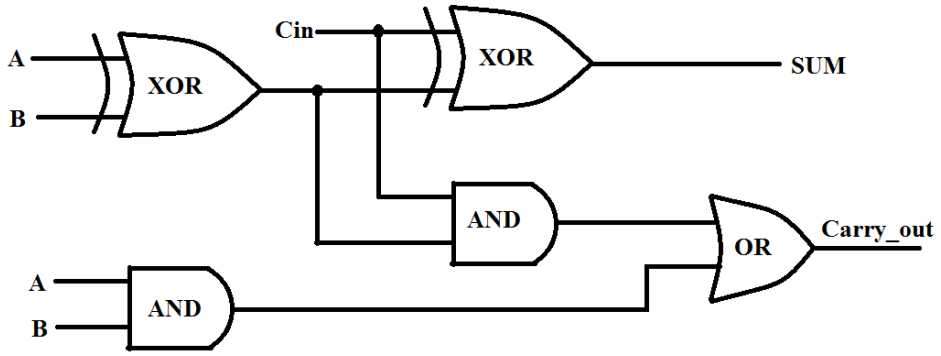

FIGURE 3.2: Propagate/Generate logic for 1-bit full adder.

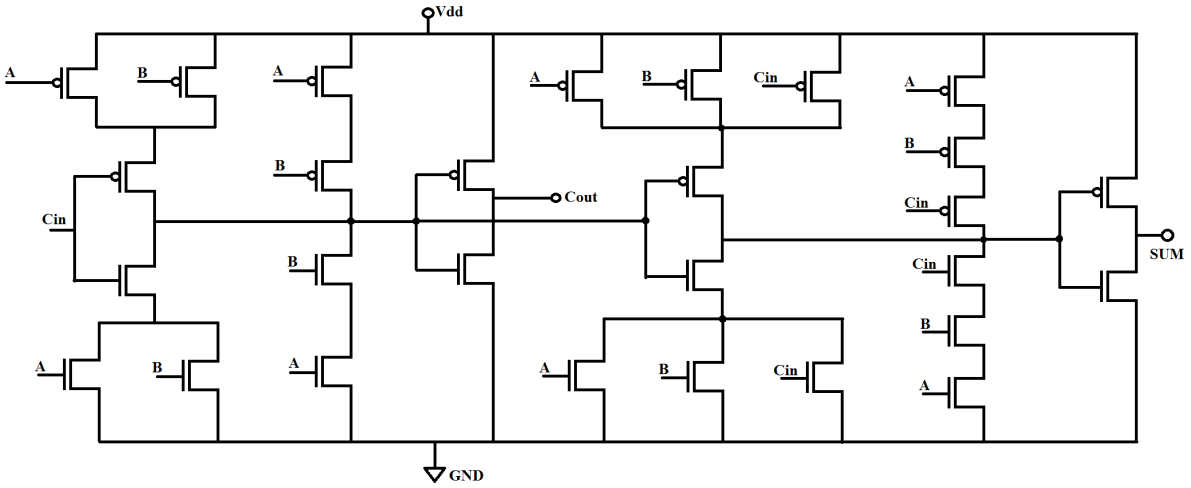

FIGURE 3.3: 28-transistor mirror 1-bit full adder.

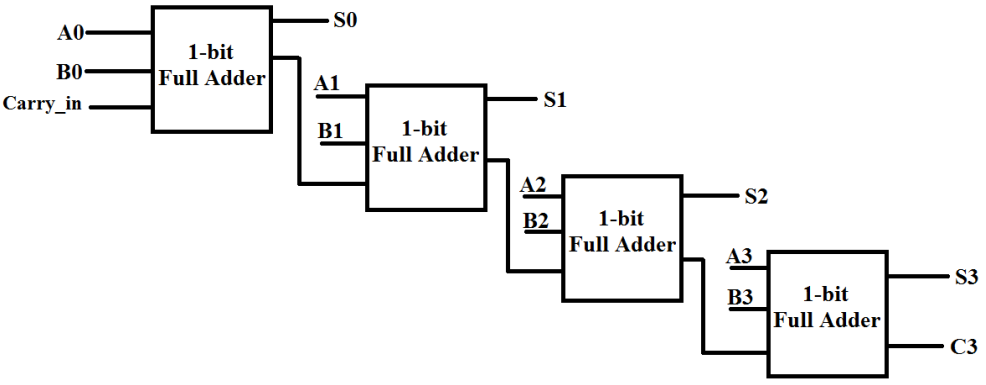

FIGURE 3.4: 4-bit static CMOS carry ripple adder circuit.

3.1.1.3 Design of 16-bit Carry Select Adder

The approach to the design of 16-bit CSA is as follows:

11. Two of the 4-bit carry ripple adders are used in a hierarchy, first one receives `Carry_in` as 1 and the second one receives `Carry_in` as 0. The outputs are provided to multiplexers to select the correct sum and carry values, as shown in

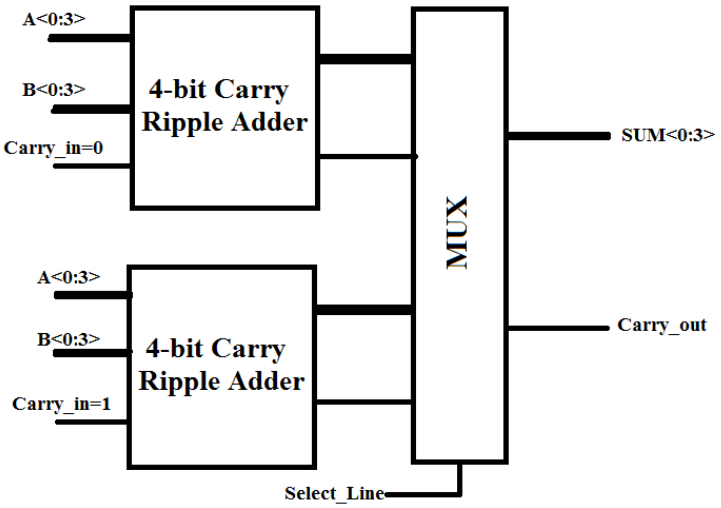

FIGURE 3.5: 4-bit static CMOS carry select adder.

   Figure 3.5. The select line of multiplexer is the actual `Carry_in` that is provided to the adder.

12. Four such 4-bit CSAs are combined to obtain the 16-bit CSA. The select line of the multiplexer is the `Carry_out` from the previous stage. For the first stage, the select line is 0, but in order to maintain the reusability, all four 4-bit CSAs are designed to be identical. Figure 3.6 shows the 16-bit carry select adder.

13. To make the design synchronous, flip-flops are added to the primary inputs and outputs. Thus, the correct outputs are obtained after two active edges with respect to the inputs.

Since the 1-bit FA can be implemented in two ways, there are two designs for the 16-bit CSA, each employing one of the 1-bit FA logic.

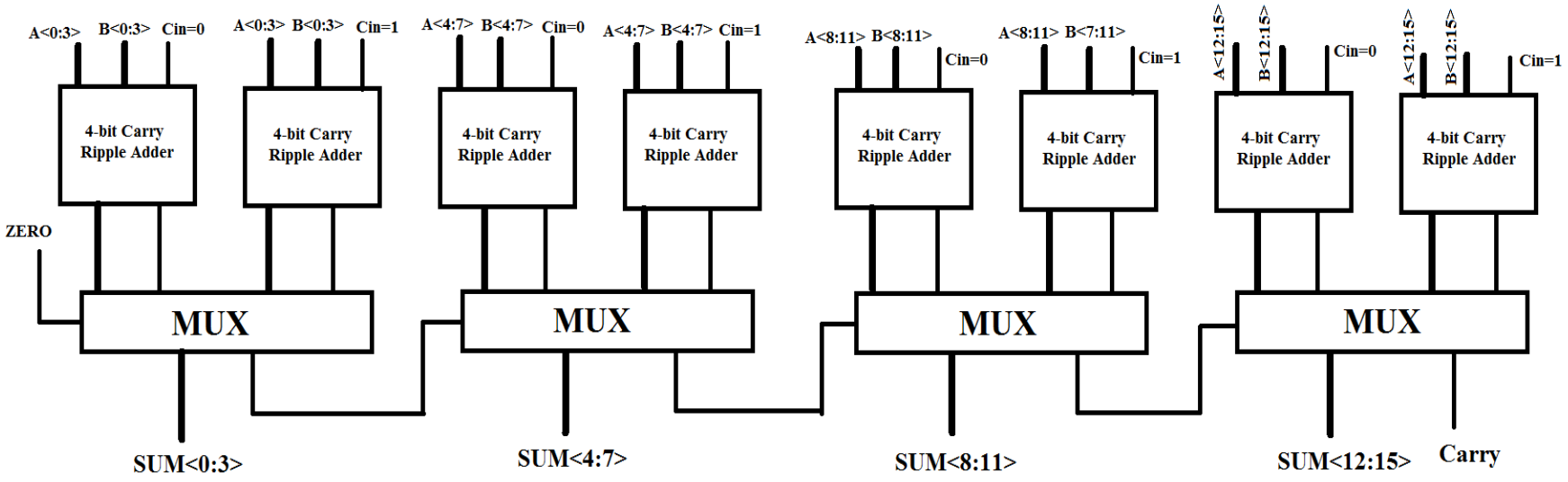

FIGURE 3.6: 16-bit static CMOS carry select adder.

3.1.1.4 Simulation Setup for Evaluating Functionality

To evaluate functionality, the 16-bit CSA is provided with 32 input signals. A load capacitance of 5 fF is connected to each output node. The circuit is then simulated for various combinations of input signals. Also, each hierarchy is checked for correct functionality which re-affirms the correctness of the overall design. The input and corresponding output for the 1-bit full adder are shown in Figure 3.7.

3.1.2 ECRL based 16-bit CSA

The ECRL inverter design can be generalized to understand the design of various other gates. Figure 3.8 shows that the NMOS logic for an inverter can be replaced by the NMOS F_n logic to realize any logic functionality. Since ECRL produces complementary outputs, the NMOS $\overline{F_n}$ logic generates the complement of the desired output. Also, attributing to the self-complementing functionality, ECRL needs to have the input signal and its complement. Designing a circuit in ECRL is different than static CMOS since there are 4 power-clock signals and one particular interval for a stage acts as the subsequent interval for the following stage [18]. In the case where a stage accepts inputs from two different stages, the signals need to be propagated through the same number of logical gates since ECRL is inherently pipelined. This step is necessary to ensure that both signals have the correct phase, as discussed more in detail later. The AND, OR, XOR and 2:1 MUX transistor level design using ECRL are shown in Figures 3.9 to 3.12.

3.1.2.1 Design of 1-bit FA:

14. Propagate/Generate FA: Figure 3.13 shows the design of a 1-bit full adder which implements the propagate/generate logic. The inputs A and B, and their complements, are provided to the AND and XOR gates. These two gates can evaluate at the same time as they are not dependent on any signal/output from any other stage. Hence, these two gates receive the same power-clock signal. The next stage comprises of the XOR and AND gates. The XOR gate produces the sum as the output whereas the output of AND gate is provided to the next stage OR gate which evaluates the carry. The XOR and AND gate of stage 2 are independent.

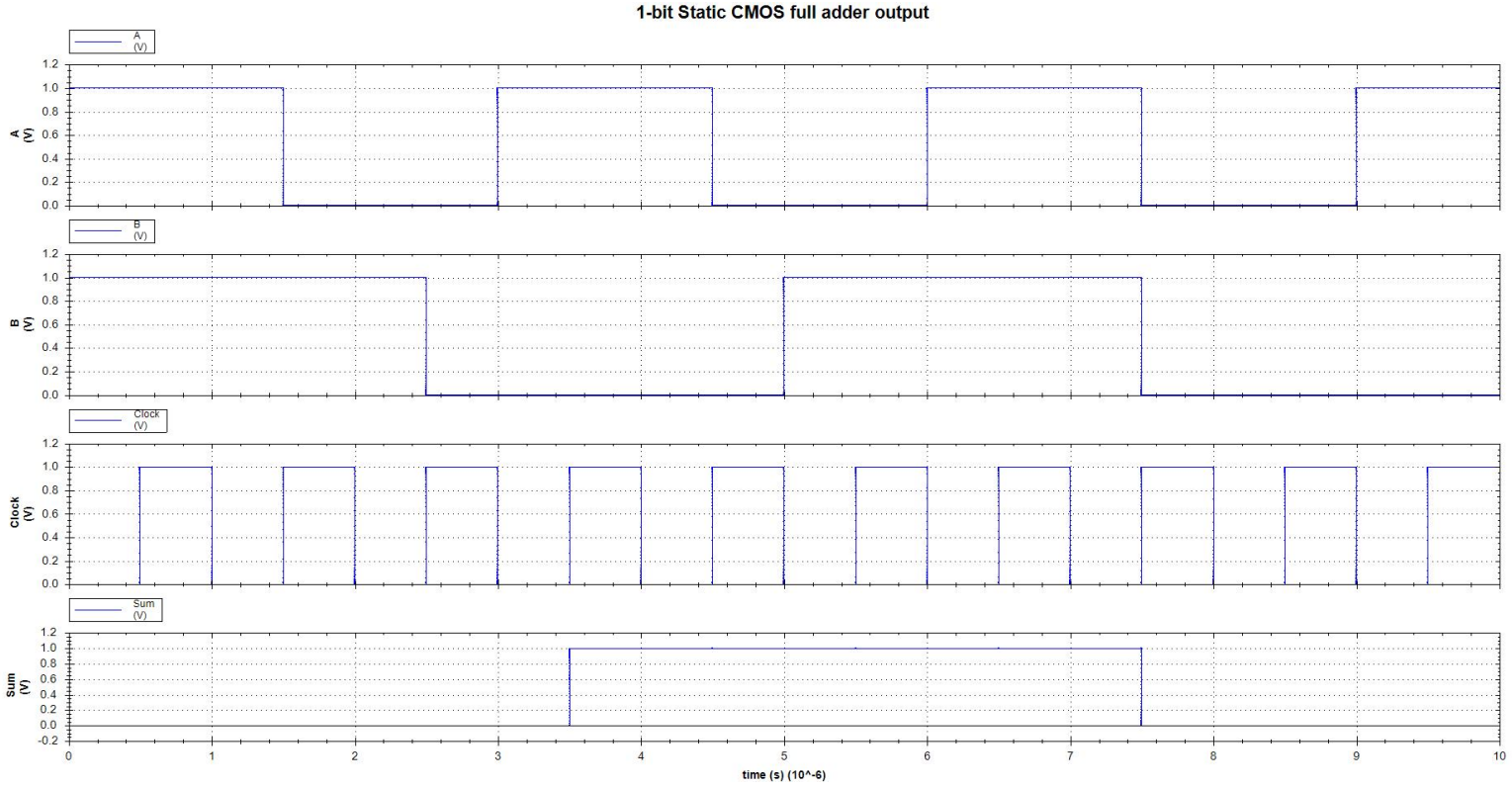

FIGURE 3.7: Static CMOS 1-bit full adder input and output.

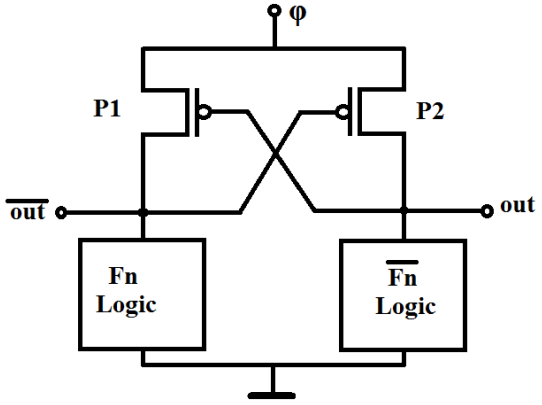

FIGURE 3.8: Generalized ECRL circuit.

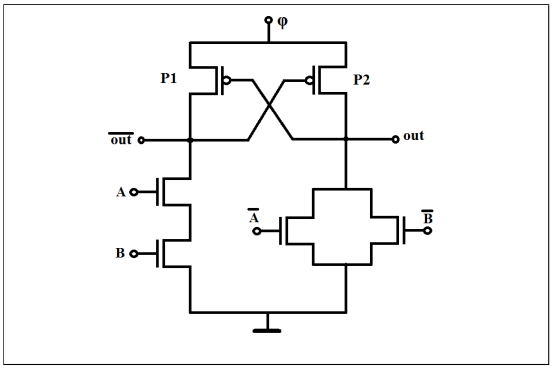

FIGURE 3.9: ECRL AND circuit.

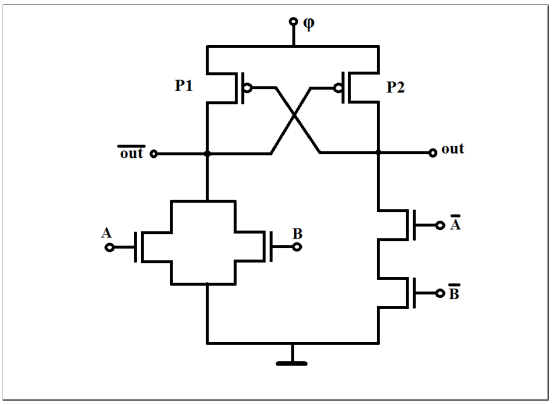

FIGURE 3.10: ECRL OR circuit.

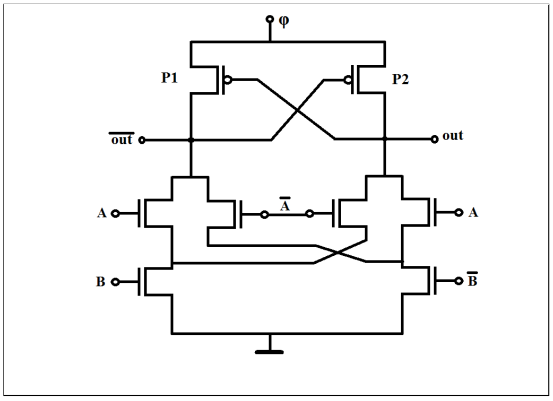

FIGURE 3.11: ECRL XOR circuit.

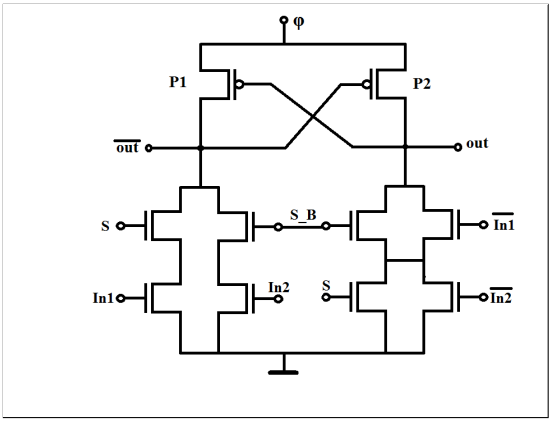

FIGURE 3.12: ECRL 2:1 MUX circuit.

Hence, they receive the same power-clock signal whereas the OR gate that evaluates the carry receives a different power-clock signal as this gate is in a different stage because of the dependency on the output of the AND gate in stage 2. The

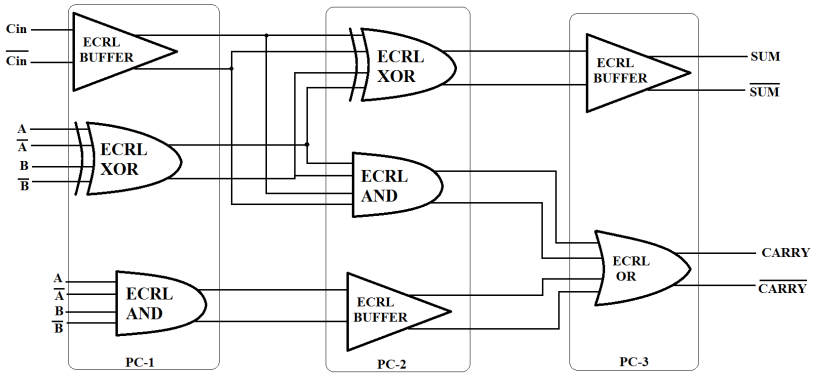

FIGURE 3.13: ECRL 1-bit FA using the propagate/generate logic.

signals/inputs are propagated through buffers until the stage where they are provided as input to other gates. Hence, the adder is divided into three stages and the three power-clock signals have 90° phase difference, as shown in Figure 3.13.

15. 28-transistor mirror FA:

    The 1-bit mirror adder shown in Figure 3.3 can be divided into two stages, as shown in Figure 3.14.

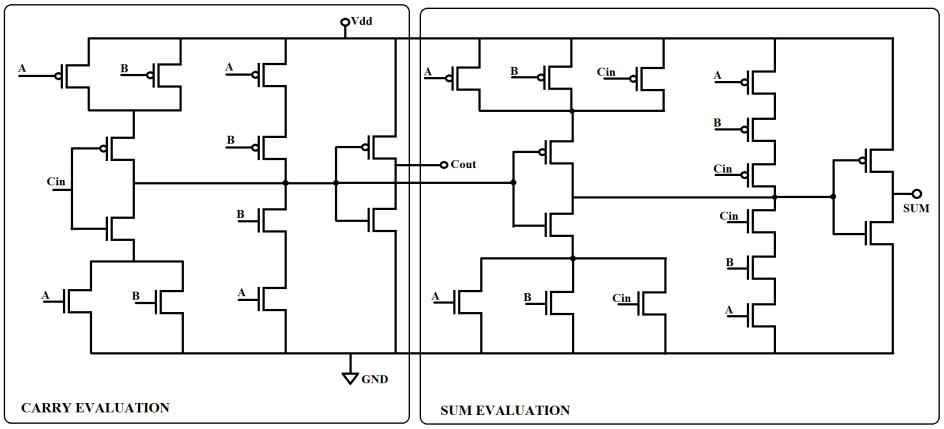

FIGURE 3.14: ECRL 1-bit mirror adder.

(a) Carry Evaluation Stage

(b) Sum Evaluation Stage.

The ECRL circuitry of carry and sum evaluation is shown in Figures 3.15 and 3.16, respectively. As the sum evaluation depends on a signal that is generated during the carry evaluation, there exists a dependency, hence the circuit takes in

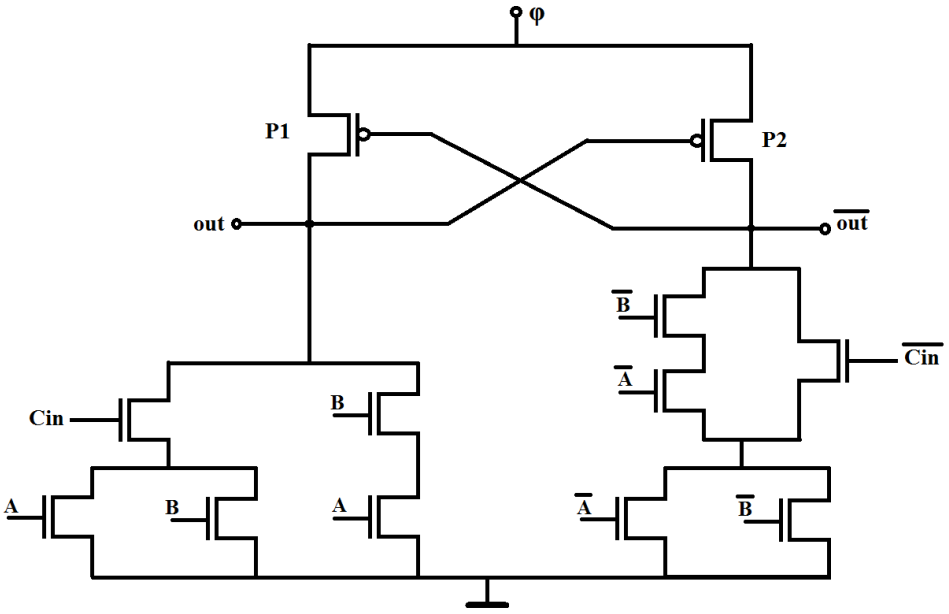

FIGURE 3.15: ECRL circuit for implementation of carry evaluation in mirror adder.

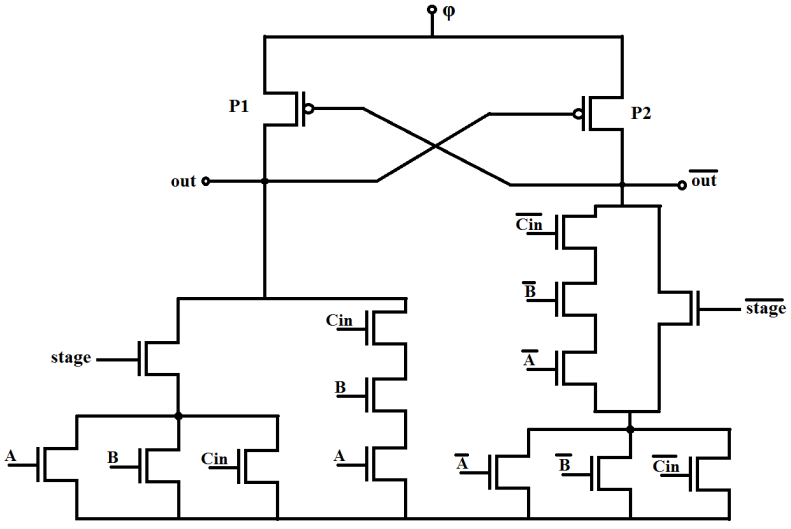

FIGURE 3.16: ECRL circuit for implementation of sum evaluation in mirror adder.

two power-clock signals that are 90° phase apart. The symbolic representation is shown in Figure 3.17.

The inputs and corresponding outputs for the 1-bit adder are shown in Figure 3.18.

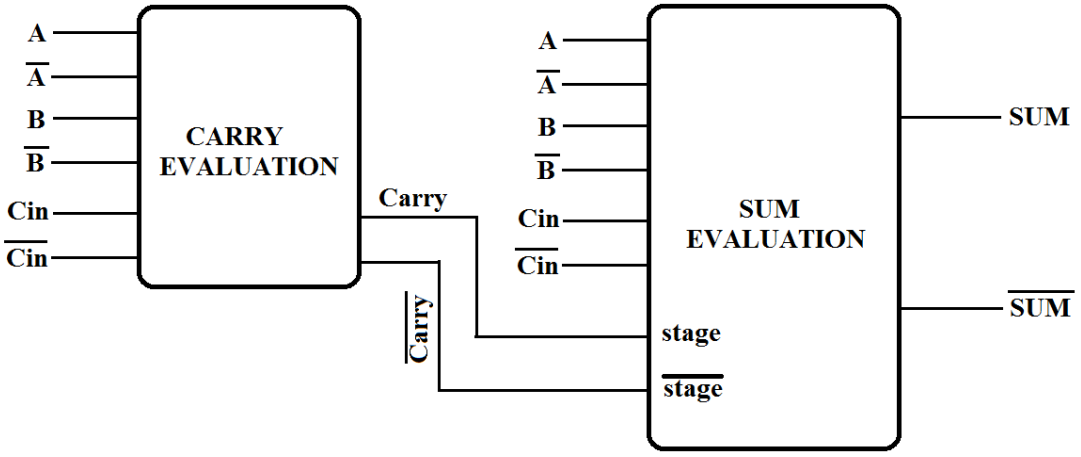

FIGURE 3.17: Symbol for 1-bit ECRL mirror adder.

3.1.2.2 Design of 4-bit Carry Ripple Adder

To design a 4-bit FA, a gate-level representation is adopted (without higher level hierarchy) to provide a better picture and understanding of the power-clock connectivity. The basic computation remains the same as explained in the previous subsection. The signals need to pass through buffers in order to propagate until the stage wherein they are used as inputs for evaluation. The sum value for each pair of bits is also propagated through buffers in order to make the entire circuit synchronous by generating all of the outputs at the end of the same corresponding power-clock signal. Figure 3.19 and Figure 3.20. represent the 4-bit ripple carry adder employing PG logic and mirror adder logic, respectively.

The following observations are noted:

16. The 4-bit adder with mirror FAs requires fewer stages to evaluate the final output.

17. Assuming that gates in one vertical line form one stage and the four power-clock signals are PC1, PC2, PC3, and PC4 then stage 'n' and stage 'n+4' receive the same power-clock signal.

18. The correct outputs are obtained after 'n/4' number of power-clock cycles (where 'n' is the number of stages), as that many number of power-clock cycles is required to evaluate and propagate the output and also maintain the synchronicity of the circuit.

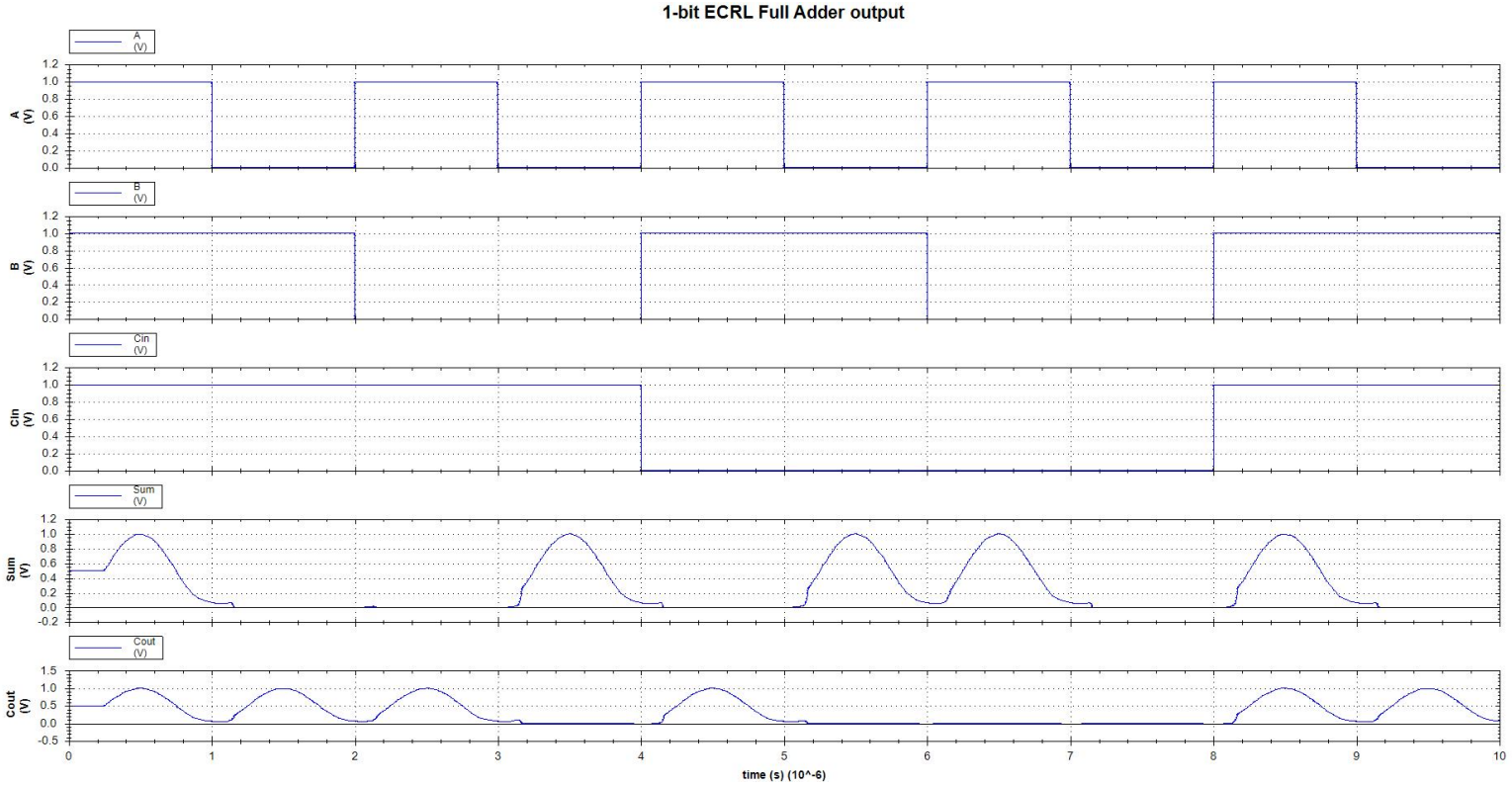

FIGURE 3.18: ECRL 1-bit full adder input and output.

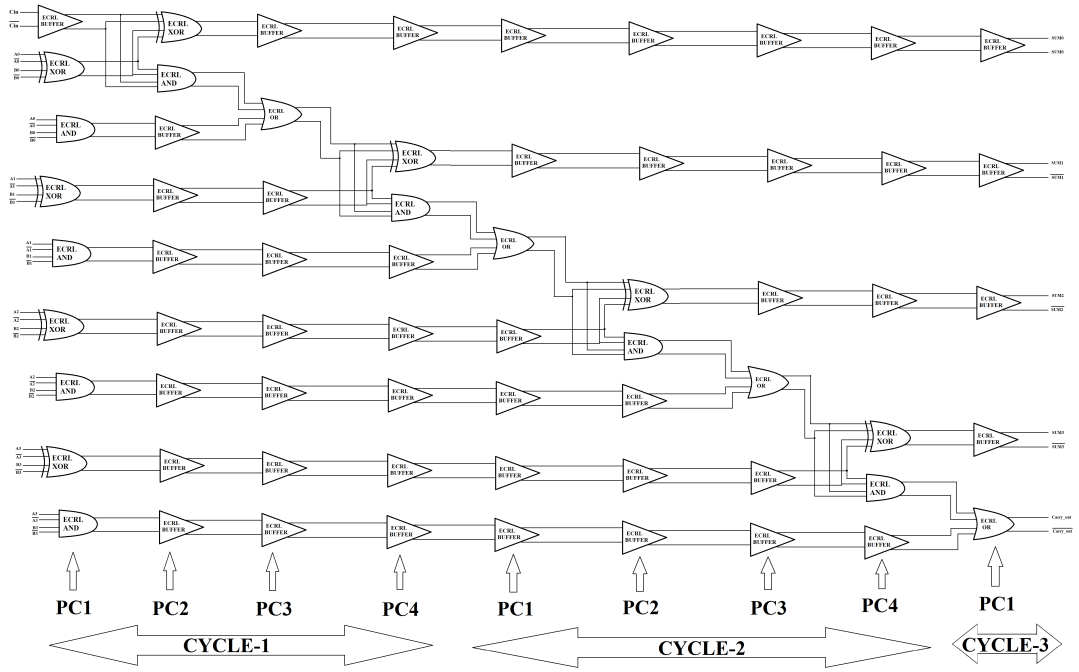

FIGURE 3.19: ECRL 4-bit adder using propagate/generate logic.

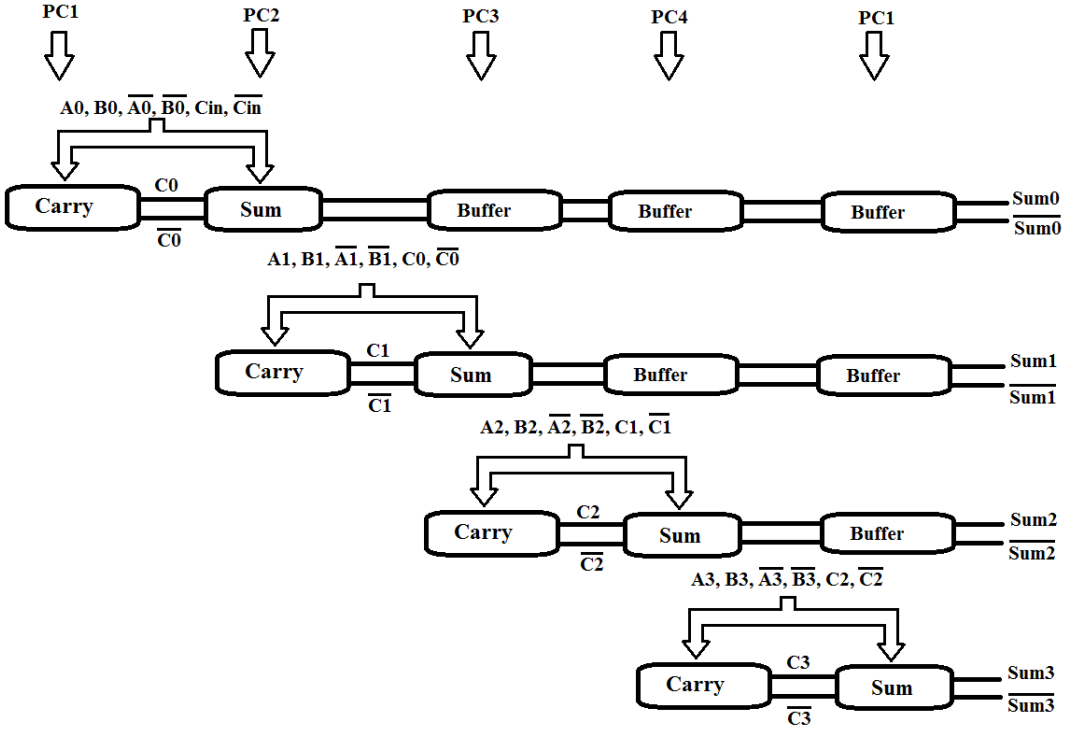

FIGURE 3.20: ECRL 4-bit adder using mirror adder logic. Note that the buffers needed to ensure synchronous operation are not shown.

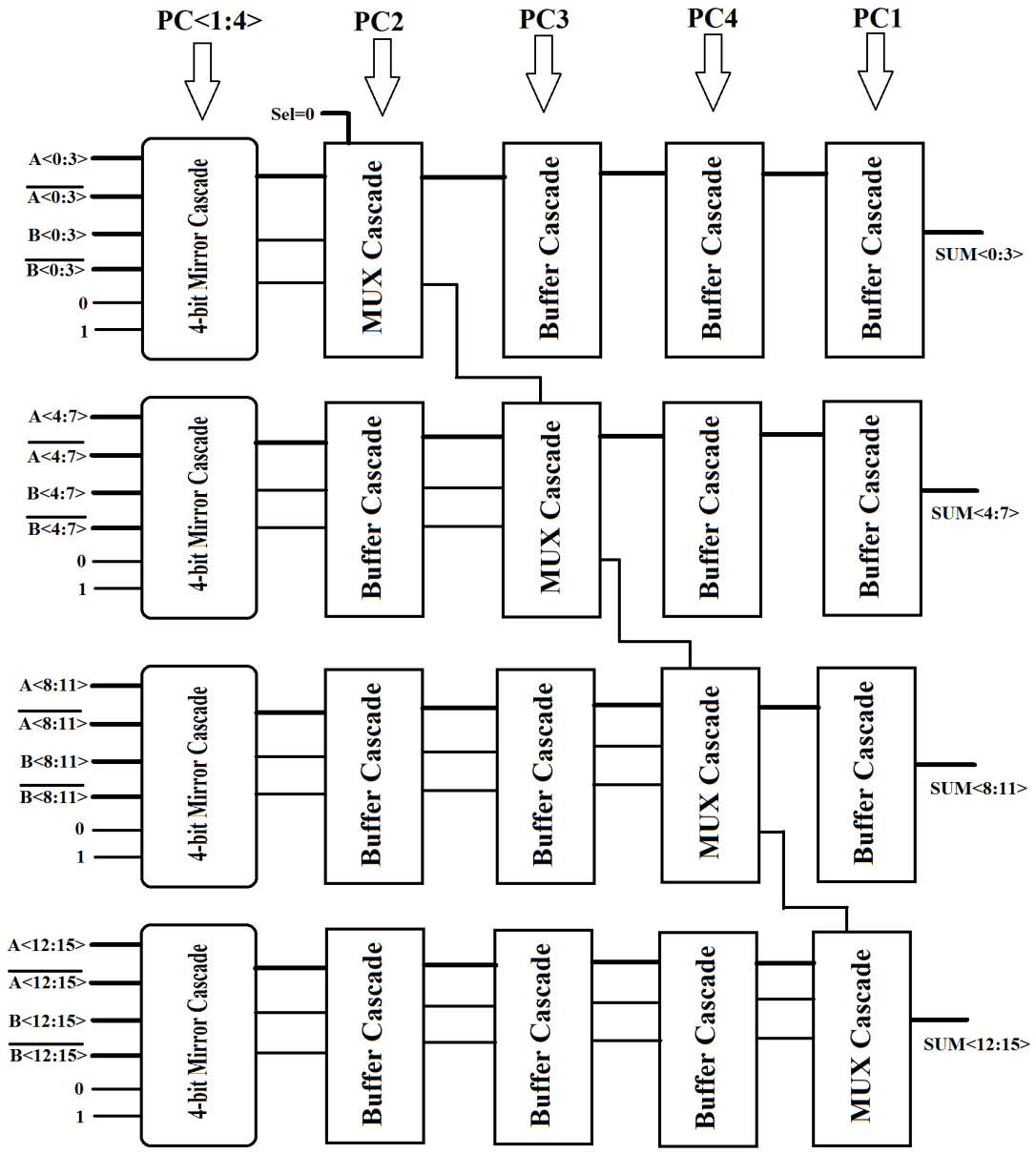

FIGURE 3.21: 16-bit carry select adder with ECRL logic.

19. The synchronicity of the system is maintained without the use of flip-flops because the operation is based on the principle that one stage can evaluate only after the previous stage has finished evaluating and is in the hold interval. Hence, the design is inherently pipelined.

3.1.2.3 Design of 16-bit Carry Select Adder

Figure 3.21 illustrates the design of a 16-bit CSA using four 4-bit adders. The 4-bit adders can either use PG FA or mirror FA. The sum values need to be propagated through buffers until the corresponding multiplexer receives the select signal from the previous 4-bit adder.

Each of the multiplexers shown in Figure 3.21 is a combination of five 2:1 multiplexer (MUX), all receiving the same select signal. The multiplexer outputs are also propagated through a chain of buffers until all the outputs are obtained at the same power-clock signal. Note that depending upon the kind of logic used for 1-bit FA, the number of power-clock cycles for evaluation and output generation varies. The 16-bit CSA with PG FA requires 3.25 power-clock cycles whereas the 16-bit CSA with mirror FA requires 2.25 power-clock cycles.

3.1.3 CEPAL based 16-bit CSA

As mentioned earlier, CEPAL is an improvement over QSERL and both families employ the basic structure of static CMOS [23]. Hence, a general circuit with the CEPAL logic can be designed as shown in Figure 3.22. Unlike static CMOS, there is no ground (GND)

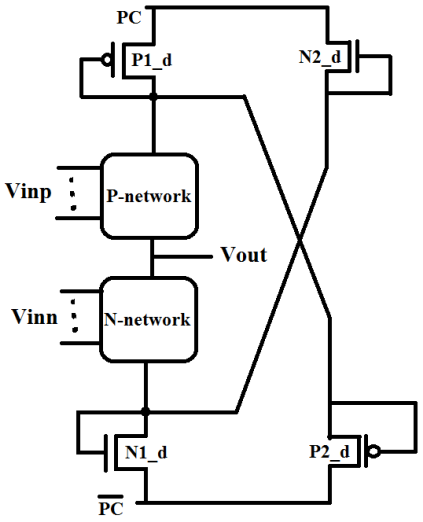

FIGURE 3.22: A generalized representation of CEPAL.

supply to CEPAL logic. Instead, CEPAL has two power-clock signals which are 180° phase apart. Unlike ECRL, cascaded stages, as shown in Figure 3.23, share the same power-clock signals. Note that the PMOS and NMOS bulk nodes cannot be biased with

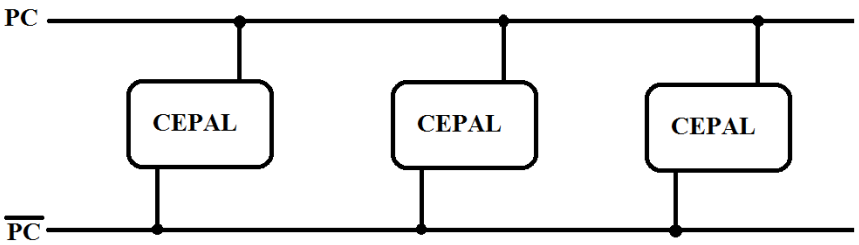

FIGURE 3.23: Cascaded CEPAL topology.

the same voltage as their respective power-clock signals since the PN junctions within the transistors become forward biased and therefore deteriorates the functionality of the circuit.

3.1.3.1 Design of 1-bit FA

The implementation of propagate/generate design and 28 transistor mirror adder design are similar to that of static CMOS except the presence of AC power-clock supply instead of a DC supply voltage. More specifically, VDD in static CMOS is replaced by PC and GND is replaced by $\overline{PC}$, in addition to the diode connected transistors, as shown in Figure 3.22. The input and output waveforms for a 1-bit adder are shown in Figure 3.24. Note that the output signal does not reach VDD and GND due to the diode connected transistors. Thus, output signals in CEPAL have reduced voltage rail.

3.1.3.2 Design of 4-bit Carry Ripple Adder

The 1-bit propagate/generate FA and mirror FA are used as the building block to design two types of 4-bit carry ripple adders, similar to static CMOS. Figures 3.2 and 3.3 are used for reference.

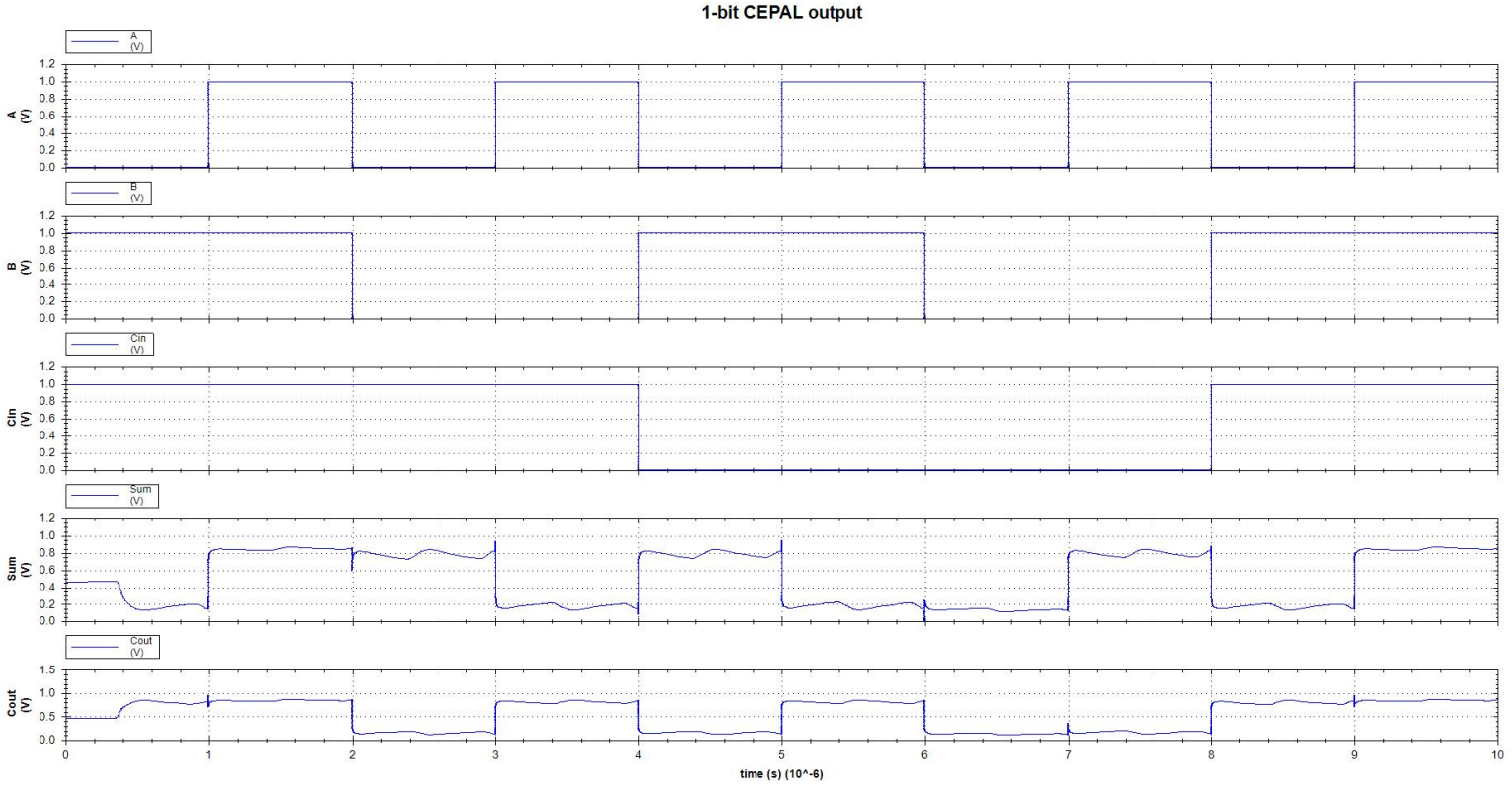

FIGURE 3.24: CEPAL 1-bit full adder input and output signals.

3.1.3.3 Design of 16-bit Carry Select Adder

The same carry select adder architecture is used. There are four 4-bit carry ripple adders. Unlike ECRL and similar to static CMOS, the synchronicity in CEPAL is maintained by using flip-flops at the primary inputs and outputs, thereby obtaining the correct output signals after two active clock edges with respect to the inputs.

3.1.3.4 Simulation Setup for Evaluating Functionality

A load capacitance of 5 fF is connected to each output node. The circuit is supplied with two power-clock signals which are 180° phase apart. For the bulk connections, a DC source for PMOS and a ground supply for NMOS are provided. The external clock frequency (required for the flip-flops) is the same as the power-clock frequency. The circuit is then simulated for various combination of input signals. The 16-bit carry select adder with CEPAL works until 30 MHz, beyond which timing (max delay constraint) violations occur.

3.2 Simulation Setup and Results for Power Consumption

The power consumption over 100 power-clock cycles is obtained for each logic for various frequencies [26]. Theoretically, it is expected that

20. The overall power consumption should increase at higher power-clock frequencies.
21. The power consumption by charge-recycling logic (ECRL and CEPAL) should be much lower as compared to the static CMOS power consumption.

The simulation results for power consumed by 16-bit carry select adder designed in various logic families are listed in Table 3.1 to Table 3.3.

Simulation results confirm the theoretical expectations. Note the following observations:

22. At low frequency of operation (1-5 MHz), the power consumed by charge-recycling circuits is only 3-4 times less than the static CMOS circuits.

Frequency (MHz)	Mirror (μW)	PG (μW)
1	4.28	4.77
5	7.41	8.01
10	11.33	12.07
20	19.18	20.17
50	42.73	44.52
100	81.98	85.03

TABLE 3.1: Power consumed by static CMOS 16-bit CSA.

Frequency (MHz)	Mirror (μW)	PG (μW)
1	0.95	1.4
5	1.05	1.49
10	1.3	1.81
20	1.92	2.56
50	4.27	5.72
100	9.19	12.1

TABLE 3.2: Power consumed by ECRL 16-bit CSA.

Frequency (MHz)	Mirror (μW)	PG (μW)
1	1.37	1.64
5	3.55	4.07
10	5.93	6.79
20	10.39	11.48
50	19.63	21.84
100	24.35	30.18

TABLE 3.3: Power consumed by CEPAL 16-bit CSA.

23. As the power-clock frequency is increased, the overall power consumption increases for each of the circuits, but the rate of increase is much lower for the charge-recycling circuits as compared to the static CMOS.

24. ECRL power consumption is approximately 8-9 times lower than that of static CMOS whereas CEPAL power consumption is almost half to one-forth of the static CMOS power consumption depending on the power-clock frequency. Figure 3.25 and Figure 3.26 show the power comparison as a function of power-clock frequency.

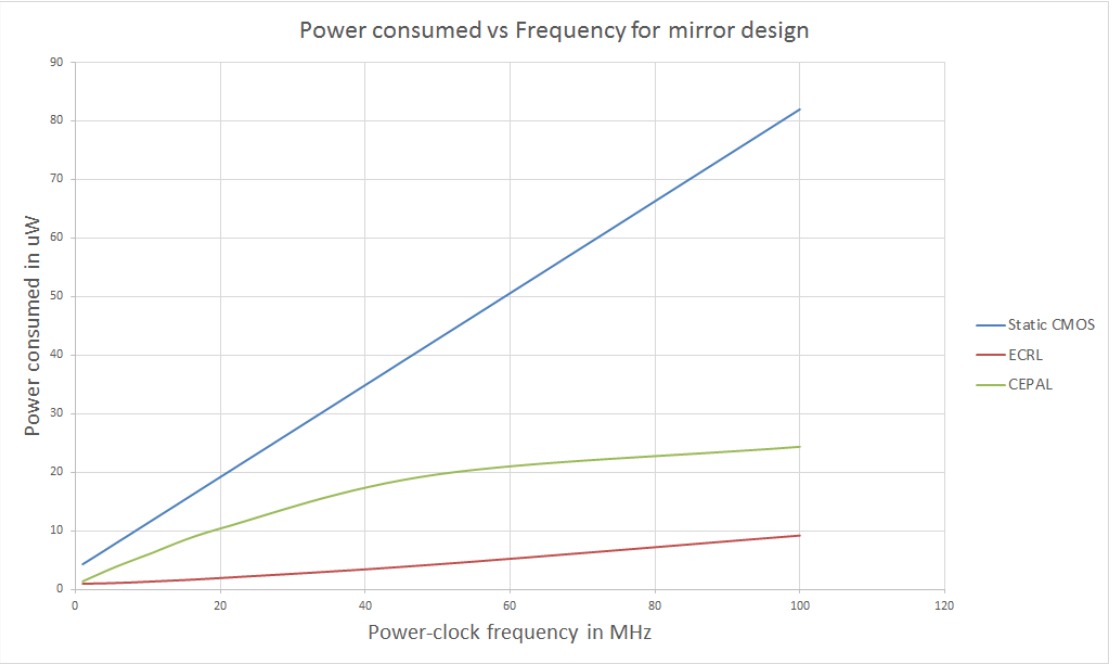

FIGURE 3.25: Power consumed by 16-bit CSA employing 1-bit adder with mirror logic.

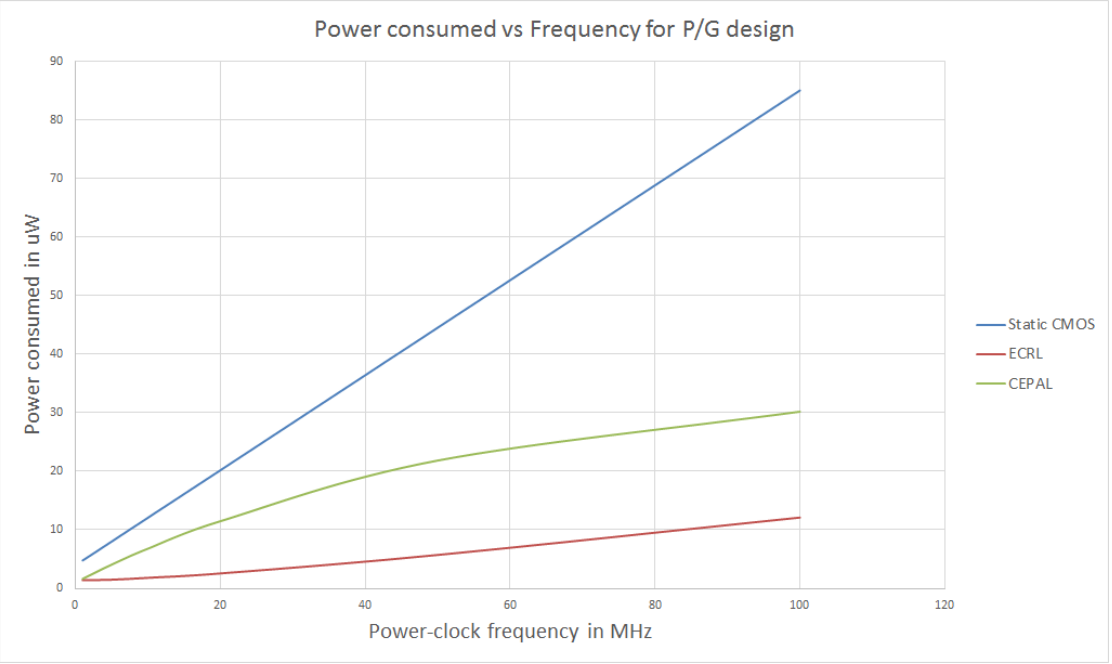

FIGURE 3.26: Power consumed by 16-bit CSA employing 1-bit adder with propagate/-generate logic.

Chapter 4

EFFECTS OF NON-IDEAL POWER-CLOCK PHASE DIFFERENCE ON CIRCUIT CHARACTERISTICS

As mentioned in the previous chapters, the ECRL and CEPAL employ power-clock signals among which a certain phase difference should be maintained. In this chapter, the primary objective is to investigate the effect of non-ideal phase differences on the power consumption and functionality. The operating frequencies considered for this investigation vary from 10 MHz to 100 MHz.

4.1 Simulation Setup

For the simulation setup to analyze power consumption, the same method is used as mentioned in the previous chapter. The steps followed to obtain the power consumption corresponding to various phase differences are as follows:

25. For ECRL, the phase difference of one power-clock signal is varied from 40° to 140° (ideally should be 90°) with respect to the adjacent power-clock signal while maintaining the rest of the power-clock signals at the ideal state. This process is

performed for each of the four power-clock signals. The phase difference is varied in steps of 5° to obtain sufficient accuracy in the results. The outputs and power consumption at the end of each simulation are compared to that of the ideal output and power consumption.

26. For CEPAL, the phase difference of one of the two power-clock signals is varied from 140° to 220° (ideally should be 180°) with respect to the other power-clock signal, ensuring that the second power-clock signal is at ideal state. The same process is performed for the second power-clock signal. The phase difference is varied in steps of 10°. The outputs and power consumption at the end of each simulation are compared to that of the ideal output and power consumption.

4.2 Output and Power Consumption Analysis

4.2.1 ECRL

For ECRL, the outputs remain the same as that of the ideal outputs for the entire range of phase difference for all of the frequencies, i.e., 10 MHz, 13.56 MHz, 50 MHz and 100 MHz whereas there is a noticeable change in the power consumed by the circuit.

Tables 4.1 to 4.4 in the following pages list the power corresponding to each phase difference. These results are also shown in Figures 4.1 to 4.4. According to these results, if the phase difference between two consecutive power-clock signals is 120° or more (rather than the ideal 90°, representing more than 30° phase deviation), the power consumption by the following (next logic gate) power-clock signal exponentially increases. For example, if PC3 and PC4 have a phase difference more than 120°, PC4 consumes more power as compared to a phase difference of 90°. If more than one pair of power-clock signals exhibit non-ideal phase difference, then each pair should be considered separately and the same principle should be followed to analyze the power consumption. The power consumption vs. phase difference plots for power-clock frequency of 10 MHz, 13.56 MHz, 50 MHz and 100 MHz are shown, respectively, in Figures 4.1, 4.2, 4.3 and 4.4. For all of the power-clock frequencies, the behaviour of power consumption remains the same. Also note that the overall power consumption corresponding to each phase increases at higher power-clock frequencies. For example, at 10 MHz and phase difference of 120°

between PC2 and PC3, the power consumption is 1.47μW whereas at 50 MHz, the same phase difference between the same power-clock signals produces a power consumption of 4.35μW.

As the phase difference between two consecutive power-clock signals varies, the output of the first stage shifts in time (since the output follows the power-clock signal in ECRL). When this shifted output is used as the input for the following logic gate (which has ideal power-clock signal), the shift in the output waveform is fixed, thereby ensuring correct operation. However, due to the shift at the output of the first stage, this signal falls under the evaluation interval of the following power-clock signal (where the signal should ideally remain stable). Since the input changes during evaluation interval due to the non-ideal phase difference, the power consumed by the second stage increases.

TABLE 4.1: Power (in μW) consumed by each of the four power-clock signals at 10 MHz while the phase difference between PC1 and PC2 varies from 40° to 140°. The correct phase difference is 90°.

	140	135	130	125	120	115	110	105	100	95	90	85	80	75	70	65	60	55	50	45	40
PC1	0.46	0.45	0.45	0.44	0.44	0.44	0.44	0.43	0.43	0.43	0.43	0.43	0.44	0.44	0.46	0.48	0.53	0.62	0.77	1.00	1.36
PC2	2.12	1.46	1.02	0.73	0.55	0.44	0.39	0.36	0.35	0.34	0.34	0.33	0.33	0.33	0.33	0.33	0.33	0.33	0.33	0.33	0.34
PC3	0.47	0.30	0.28	0.28	0.28	0.28	0.27	0.27	0.27	0.27	0.27	0.27	0.28	0.28	0.28	0.28	0.28	0.28	0.29	0.29	0.29
PC4	0.26	0.26	0.26	0.26	0.25	0.25	0.26	0.26	0.26	0.26	0.26	0.26	0.26	0.26	0.26	0.26	0.26	0.26	0.26	0.26	0.26

TABLE 4.2: Power (in μW) consumed by each of the four power-clock signals at 10 MHz while the phase difference between PC2 and PC3 varies from 40° to 140°. The correct phase difference is 90°.

	140	135	130	125	120	115	110	105	100	95	90	85	80	75	70	65	60	55	50	45	40
PC1	0.44	0.43	0.43	0.43	0.43	0.43	0.43	0.43	0.43	0.43	0.43	0.42	0.43	0.43	0.44	0.43	0.44	0.44	0.44	0.44	0.44
PC2	0.33	0.33	0.33	0.33	0.33	0.33	0.33	0.33	0.33	0.33	0.34	0.34	0.35	0.36	0.39	0.45	0.56	0.75	1.06	1.54	2.29
PC3	1.90	1.28	0.87	0.61	0.45	0.36	0.31	0.29	0.28	0.27	0.27	0.27	0.27	0.27	0.27	0.27	0.27	0.27	0.27	0.28	0.30
PC4	0.38	0.28	0.26	0.26	0.26	0.26	0.26	0.25	0.25	0.25	0.26	0.26	0.26	0.26	0.26	0.26	0.26	0.26	0.27	0.27	0.27

TABLE 4.3: Power (in μW) consumed by each of the four power-clock signals at 10 MHz while the phase difference between PC3 and PC4 varies from 40° to 140°. The correct phase difference is 90°.

	140	135	130	125	120	115	110	105	100	95	90	85	80	75	70	65	60	55	50	45	40
PC1	0.54	0.42	0.44	0.44	0.43	0.43	0.43	0.43	0.43	0.43	0.43	0.43	0.44	0.44	0.44	0.44	0.44	0.44	0.44	0.44	0.45
PC2	0.34	0.34	0.34	0.34	0.34	0.34	0.34	0.34	0.34	0.34	0.34	0.34	0.34	0.34	0.34	0.34	0.34	0.34	0.34	0.34	0.35
PC3	0.29	0.28	0.28	0.28	0.28	0.28	0.28	0.27	0.27	0.27	0.27	0.27	0.28	0.29	0.31	0.36	0.45	0.62	0.88	1.30	1.95
PC4	1.55	1.04	0.72	0.51	0.39	0.32	0.28	0.27	0.26	0.26	0.26	0.25	0.25	0.25	0.25	0.26	0.26	0.26	0.26	0.26	0.28

TABLE 4.4: Power (in μW) consumed by each of the four power-clock signals at 10 MHz while the phase difference between PC4 and PC1 varies from 40° to 140°. The correct phase difference is 90°.

	140	135	130	125	120	115	110	105	100	95	90	85	80	75	70	65	60	55	50	45	40
PC1	1.32	0.97	0.75	0.61	0.53	0.48	0.46	0.45	0.44	0.43	0.43	0.43	0.43	0.43	0.43	0.43	0.43	0.43	0.43	0.44	0.46
PC2	0.43	0.35	0.34	0.34	0.34	0.34	0.34	0.33	0.33	0.34	0.34	0.34	0.34	0.34	0.34	0.34	0.34	0.34	0.34	0.34	0.34
PC3	0.28	0.28	0.28	0.28	0.28	0.28	0.27	0.27	0.27	0.27	0.27	0.27	0.27	0.27	0.27	0.28	0.28	0.28	0.28	0.28	0.28
PC4	0.26	0.26	0.26	0.26	0.26	0.26	0.26	0.26	0.26	0.26	0.26	0.26	0.26	0.27	0.28	0.32	0.39	0.52	0.73	1.06	1.58

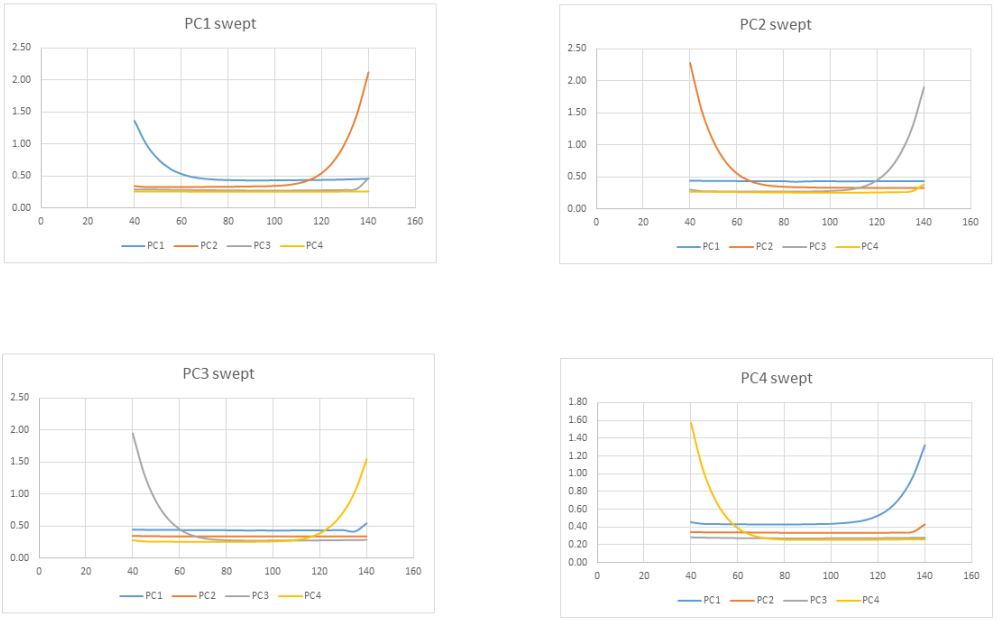

FIGURE 4.1: Phase difference (in °) vs. power consumed (in μW) by each power-clock signal for power-clock frequency 10 MHz.

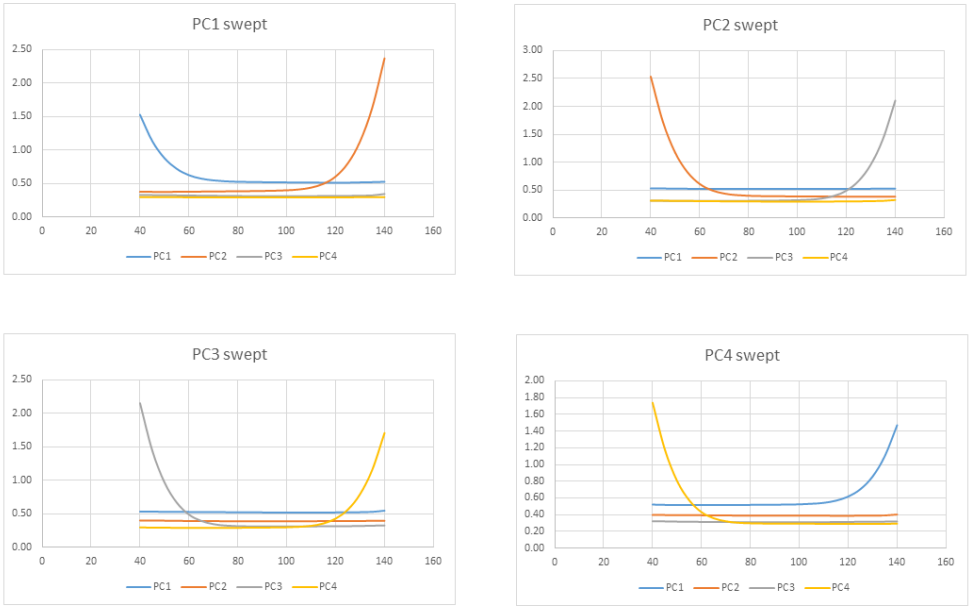

FIGURE 4.2: Phase difference (in °) vs. power consumed (in μW) by each power-clock signal for power-clock frequency 13.56 MHz.

TABLE 4.5: Power (in μW) consumed by each of the four power-clock signals at 13.56 MHz while the phase difference between PC1 and PC2 varies from 40° to 140°. The correct phase difference is 90°.

	140	135	130	125	120	115	110	105	100	95	90	85	80	75	70	65	60	55	50	45	40
PC1	0.53	0.52	0.52	0.51	0.51	0.51	0.52	0.52	0.52	0.52	0.52	0.52	0.53	0.53	0.55	0.57	0.63	0.72	0.88	1.14	1.53
PC2	2.37	1.64	1.13	0.80	0.60	0.50	0.44	0.41	0.40	0.39	0.39	0.39	0.39	0.38	0.38	0.38	0.38	0.38	0.37	0.38	0.38
PC3	0.34	0.32	0.32	0.32	0.31	0.31	0.31	0.31	0.31	0.31	0.31	0.31	0.31	0.31	0.32	0.32	0.32	0.32	0.33	0.33	0.33
PC4	0.30	0.30	0.30	0.29	0.29	0.29	0.29	0.29	0.29	0.29	0.29	0.29	0.29	0.29	0.29	0.29	0.29	0.30	0.30	0.30	0.30

TABLE 4.6: Power (in μW) consumed by each of the four power-clock signals at 13.56 MHz while the phase difference between PC2 and PC3 varies from 40° to 140°. The correct phase difference is 90°.

	140	135	130	125	120	115	110	105	100	95	90	85	80	75	70	65	60	55	50	45	40
PC1	0.52	0.52	0.52	0.52	0.52	0.52	0.52	0.52	0.52	0.52	0.52	0.52	0.52	0.52	0.52	0.52	0.52	0.52	0.52	0.53	0.53
PC2	0.38	0.38	0.38	0.38	0.38	0.38	0.38	0.39	0.39	0.39	0.39	0.39	0.40	0.41	0.44	0.50	0.61	0.82	1.17	1.72	2.54
PC3	2.10	1.42	0.96	0.66	0.49	0.40	0.35	0.33	0.32	0.31	0.31	0.31	0.31	0.31	0.31	0.31	0.31	0.31	0.31	0.31	0.31
PC4	0.32	0.31	0.30	0.30	0.30	0.29	0.29	0.29	0.29	0.29	0.29	0.29	0.30	0.30	0.30	0.30	0.30	0.30	0.31	0.31	0.31

TABLE 4.7: Power (in μW) consumed by each of the four power-clock signals at 13.56 MHz while the phase difference between PC3 and PC4 varies from 40° to 140°. The correct phase difference is 90°.

	140	135	130	125	120	115	110	105	100	95	90	85	80	75	70	65	60	55	50	45	40
PC1	0.55	0.53	0.52	0.52	0.52	0.52	0.52	0.52	0.52	0.52	0.52	0.52	0.52	0.52	0.53	0.53	0.53	0.53	0.53	0.53	0.53
PC2	0.39	0.39	0.39	0.39	0.39	0.39	0.39	0.39	0.39	0.39	0.39	0.39	0.39	0.39	0.39	0.39	0.39	0.39	0.40	0.40	0.40
PC3	0.33	0.32	0.32	0.32	0.31	0.31	0.31	0.31	0.31	0.31	0.31	0.31	0.31	0.32	0.35	0.39	0.49	0.67	0.97	1.45	2.16
PC4	1.71	1.16	0.79	0.56	0.43	0.36	0.32	0.31	0.30	0.30	0.29	0.29	0.29	0.29	0.29	0.29	0.29	0.29	0.29	0.29	0.30

TABLE 4.8: Power (in μW) consumed by each of the four power-clock signals at 13.56 MHz while the phase difference between PC4 and PC1 varies from 40° to 140°. The correct phase difference is 90°.

	140	135	130	125	120	115	110	105	100	95	90	85	80	75	70	65	60	55	50	45	40
PC1	1.47	1.10	0.86	0.71	0.62	0.57	0.54	0.53	0.52	0.52	0.52	0.52	0.52	0.52	0.52	0.52	0.52	0.52	0.52	0.52	0.52
PC2	0.40	0.39	0.39	0.39	0.39	0.39	0.39	0.39	0.39	0.39	0.39	0.39	0.39	0.39	0.39	0.39	0.39	0.39	0.40	0.40	0.40
PC3	0.32	0.32	0.32	0.32	0.31	0.31	0.31	0.31	0.31	0.31	0.31	0.31	0.31	0.31	0.31	0.31	0.31	0.32	0.32	0.32	0.32
PC4	0.29	0.29	0.29	0.29	0.29	0.29	0.29	0.29	0.29	0.29	0.29	0.30	0.30	0.30	0.32	0.36	0.43	0.57	0.81	1.18	1.74

TABLE 4.9: Power (in μW) consumed by each of the four power-clock signals at 50 MHz while the phase difference between PC1 and PC2 varies from 40° to 140°. The correct phase difference is 90°.

	140	135	130	125	120	115	110	105	100	95	90	85	80	75	70	65	60	55	50	45	40
PC1	1.44	1.43	1.41	1.41	1.40	1.41	1.41	1.42	1.42	1.43	1.43	1.44	1.44	1.46	1.46	1.49	1.54	1.64	1.81	2.12	2.63
PC2	3.50	2.43	1.78	1.39	1.20	1.11	1.07	1.04	1.04	1.03	1.02	1.02	1.01	1.00	0.99	0.98	0.97	0.97	0.96	0.96	0.96
PC3	0.94	0.94	0.93	0.93	0.93	0.93	0.93	0.92	0.92	0.92	0.93	0.93	0.93	0.94	0.94	0.94	0.95	0.96	0.96	0.96	0.96
PC4	0.90	0.90	0.89	0.89	0.89	0.89	0.89	0.89	0.89	0.89	0.89	0.89	0.89	0.89	0.90	0.90	0.90	0.90	0.90	0.90	0.91

TABLE 4.10: Power (in μW) consumed by each of the four power-clock signals at 50 MHz while the phase difference between PC2 and PC3 varies from 40° to 140°. The correct phase difference is 90°.

	140	135	130	125	120	115	110	105	100	95	90	85	80	75	70	65	60	55	50	45	40
PC1	1.44	1.44	1.44	1.43	1.43	1.44	1.44	1.43	1.43	1.43	1.43	1.43	1.43	1.44	1.44	1.44	1.44	1.45	1.45	1.46	1.47
PC2	0.92	0.94	0.95	0.96	0.97	0.98	0.99	0.99	1.01	1.02	1.02	1.03	1.04	1.06	1.08	1.12	1.22	1.44	1.86	2.61	3.79
PC3	3.11	2.12	1.54	1.21	1.06	0.99	0.96	0.94	0.94	0.93	0.93	0.92	0.91	0.90	0.89	0.88	0.87	0.87	0.87	0.86	0.86
PC4	0.91	0.90	0.90	0.89	0.89	0.89	0.89	0.88	0.88	0.89	0.89	0.89	0.90	0.90	0.91	0.91	0.91	0.92	0.92	0.92	0.92

TABLE 4.11: Power (in μW) consumed by each of the four power-clock signals at 50 MHz while the phase difference between PC3 and PC4 varies from 40° to 140°. The correct phase difference is 90°.

	140	135	130	125	120	115	110	105	100	95	90	85	80	75	70	65	60	55	50	45	40
PC1	1.45	1.44	1.43	1.42	1.42	1.41	1.42	1.42	1.43	1.43	1.43	1.43	1.44	1.44	1.44	1.45	1.45	1.45	1.45	1.44	1.44
PC2	1.03	1.03	1.03	1.02	1.02	1.02	1.02	1.02	1.02	1.02	1.02	1.03	1.03	1.03	1.03	1.04	1.04	1.04	1.04	1.06	1.06
PC3	0.88	0.88	0.89	0.89	0.90	0.90	0.91	0.91	0.92	0.93	0.93	0.93	0.93	0.94	0.96	0.99	1.07	1.23	1.56	2.18	3.19
PC4	2.57	1.79	1.35	1.10	0.98	0.93	0.91	0.90	0.90	0.90	0.89	0.88	0.87	0.87	0.86	0.86	0.85	0.84	0.84	0.84	0.84

TABLE 4.12: Power (in μW) consumed by each of the four power-clock signals at 50 MHz while the phase difference between PC4 and PC1 varies from 40° to 140°. The correct phase difference is 90°.

	140	135	130	125	120	115	110	105	100	95	90	85	80	75	70	65	60	55	50	45	40
PC1	2.50	2.02	1.75	1.59	1.52	1.48	1.47	1.46	1.44	1.44	1.43	1.42	1.41	1.40	1.39	1.38	1.37	1.36	1.35	1.34	1.34
PC2	1.03	1.03	1.03	1.02	1.02	1.02	1.02	1.02	1.02	1.02	1.02	1.03	1.03	1.03	1.03	1.03	1.03	1.04	1.04	1.04	1.04
PC3	0.94	0.94	0.94	0.93	0.93	0.93	0.93	0.92	0.92	0.92	0.93	0.93	0.93	0.93	0.94	0.94	0.94	0.94	0.96	0.96	0.96
PC4	0.83	0.83	0.85	0.86	0.87	0.87	0.87	0.88	0.89	0.89	0.89	0.89	0.89	0.89	0.91	0.93	0.98	1.11	1.36	1.84	2.63

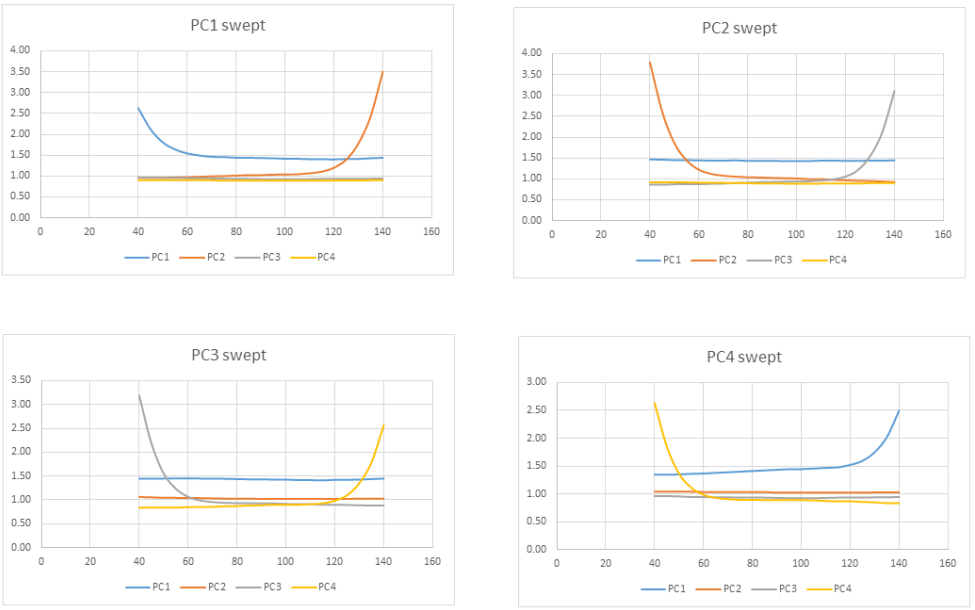

FIGURE 4.3: Phase difference (in °) vs. power consumed (in μW) by each power-clock signal for power-clock frequency 50 MHz.

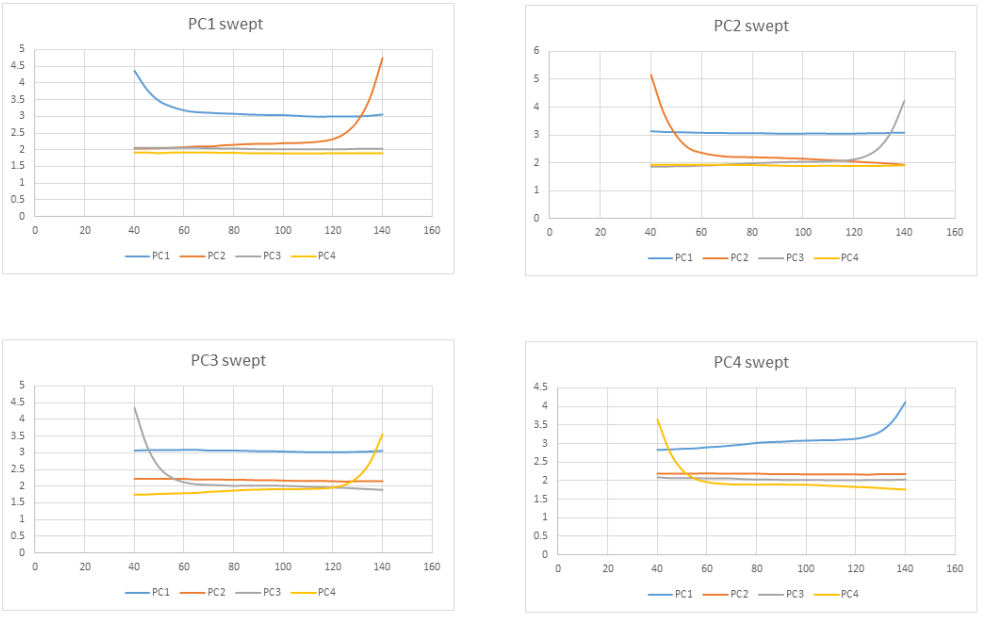

FIGURE 4.4: Phase difference (in °) vs. power consumed (in μW) by each power-clock signal for power-clock frequency 100 MHz.

TABLE 4.13: Power (in μW) consumed by each of the four power-clock signals at 100 MHz while the phase difference between PC1 and PC2 varies from 40° to 140°. The correct phase difference is 90°.

	140	135	130	125	120	115	110	105	100	95	90	85	80	75	70	65	60	55	50	45	40
PC1	3.06	3.02	3	3	3	2.99	3	3.02	3.04	3.04	3.05	3.06	3.08	3.09	3.11	3.13	3.18	3.29	3.46	3.81	4.37
PC2	4.75	3.56	2.87	2.5	2.32	2.25	2.22	2.2	2.2	2.18	2.18	2.17	2.15	2.13	2.1	2.1	2.08	2.06	2.05	2.04	2.04
PC3	2.03	2.03	2.03	2.02	2.02	2.02	2.02	2.02	2.02	2.02	2.02	2.03	2.04	2.04	2.05	2.06	2.06	2.06	2.06	2.06	2.06
PC4	1.9	1.9	1.9	1.9	1.9	1.89	1.89	1.89	1.89	1.9	1.9	1.9	1.91	1.91	1.92	1.92	1.92	1.92	1.9	1.92	1.92

TABLE 4.14: Power (in μW) consumed by each of the four power-clock signals at 100 MHz while the phase difference between PC2 and PC3 varies from 40° to 140°. The correct phase difference is 90°.

	140	135	130	125	120	115	110	105	100	95	90	85	80	75	70	65	60	55	50	45	40
PC1	3.08	3.08	3.06	3.06	3.05	3.05	3.05	3.06	3.05	3.05	3.05	3.06	3.07	3.06	3.07	3.07	3.08	3.09	3.1	3.11	3.14
PC2	1.93	1.97	2	2.02	2.05	2.08	2.1	2.12	2.15	2.16	2.18	2.19	2.2	2.21	2.22	2.27	2.36	2.52	2.98	3.8	5.16
PC3	4.23	3.15	2.54	2.25	2.12	2.07	2.06	2.04	2.04	2.03	2.02	2	1.99	1.96	1.94	1.91	1.9	1.88	1.88	1.86	1.86
PC4	1.91	1.9	1.89	1.89	1.89	1.89	1.9	1.89	1.89	1.89	1.9	1.91	1.92	1.92	1.93	1.93	1.93	1.93	1.93	1.93	1.93

TABLE 4.15: Power (in μW) consumed by each of the four power-clock signals at 100 MHz while the phase difference between PC3 and PC4 varies from 40° to 140°. The correct phase difference is 90°.

	140	135	130	125	120	115	110	105	100	95	90	85	80	75	70	65	60	55	50	45	40
PC1	3.06	3.04	3.03	3.02	3.02	3.02	3.02	3.03	3.04	3.05	3.05	3.06	3.07	3.07	3.07	3.09	3.09	3.08	3.08	3.08	3.07
PC2	2.15	2.15	2.15	2.14	2.15	2.16	2.16	2.16	2.17	2.18	2.18	2.19	2.19	2.2	2.2	2.2	2.22	2.22	2.22	2.22	2.22
PC3	1.89	1.91	1.93	1.95	1.96	1.97	1.98	2	2.01	2.02	2.02	2.02	2.01	2.03	2.04	2.06	2.12	2.26	2.56	3.21	4.35
PC4	3.56	2.72	2.27	2.05	1.96	1.93	1.92	1.91	1.91	1.91	1.9	1.89	1.87	1.85	1.83	1.8	1.79	1.78	1.77	1.75	1.75

TABLE 4.16: Power (in μW) consumed by each of the four power-clock signals at 100 MHz while the phase difference between PC4 and PC1 varies from 40° to 140°. The correct phase difference is 90°.

	140	135	130	125	120	115	110	105	100	95	90	85	80	75	70	65	60	55	50	45	40
PC1	4.12	3.62	3.33	3.2	3.13	3.11	3.09	3.09	3.08	3.07	3.05	3.04	3.02	2.98	2.95	2.92	2.9	2.87	2.86	2.84	2.83
PC2	2.18	2.18	2.18	2.16	2.17	2.17	2.17	2.17	2.17	2.18	2.18	2.18	2.19	2.19	2.19	2.19	2.2	2.19	2.19	2.19	2.19
PC3	2.03	2.02	2.02	2.02	2.01	2.01	2.01	2.02	2.02	2.02	2.02	2.03	2.03	2.04	2.06	2.06	2.06	2.07	2.07	2.07	2.09
PC4	1.76	1.78	1.8	1.82	1.83	1.85	1.86	1.88	1.89	1.89	1.9	1.9	1.89	1.9	1.9	1.92	1.96	2.06	2.29	2.78	3.65

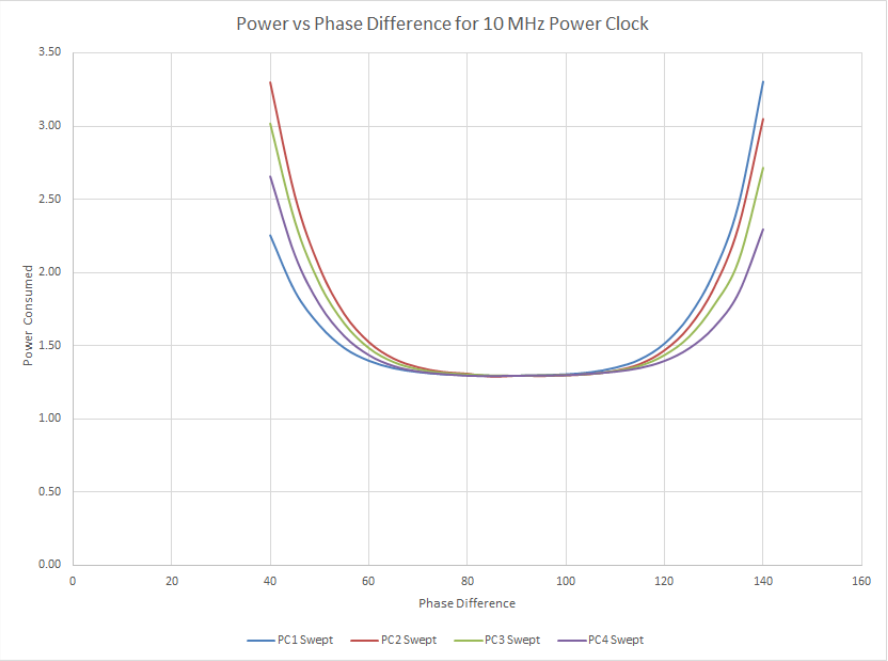

FIGURE 4.5: Overall power consumption in μW (summation of the power consumed by each power-clock signal) vs. phase difference (in °) for 10 MHz power-clock frequency when only the phase difference of one power-clock signal varies (with respect to the following power-clock signal).

FIGURE 4.6: Overall power consumption in μW (summation of the power consumed by each power-clock signal) vs. phase difference (in °) for 13.56 MHz power-clock frequency when only the phase difference of one power-clock signal varies (with respect to the following power-clock signal).

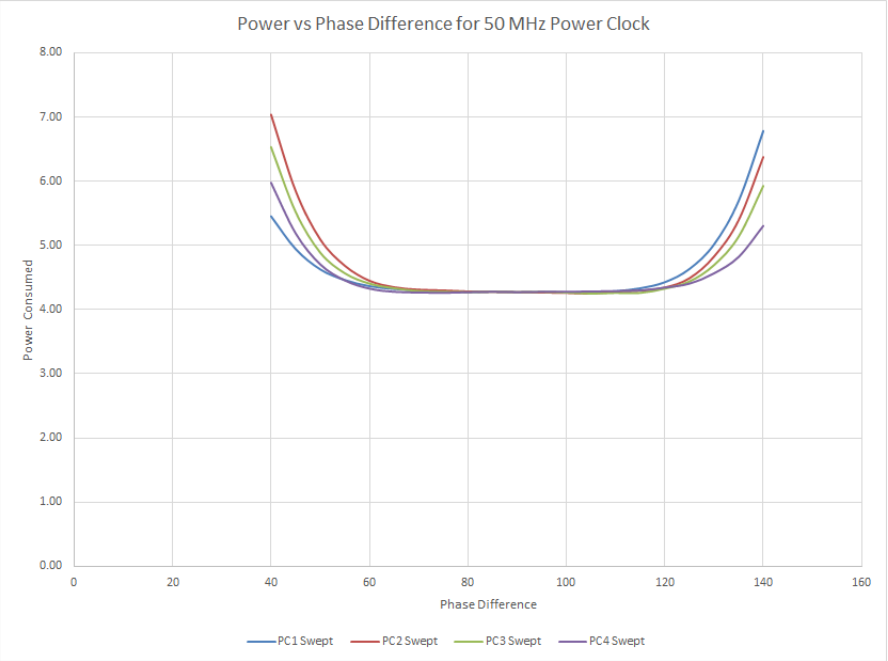

FIGURE 4.7: Overall power consumption in μW (summation of the power consumed by each power-clock signal) vs. phase difference (in °) for 50 MHz power-clock frequency when only the phase difference of one power-clock signal varies (with respect to the following power-clock signal).

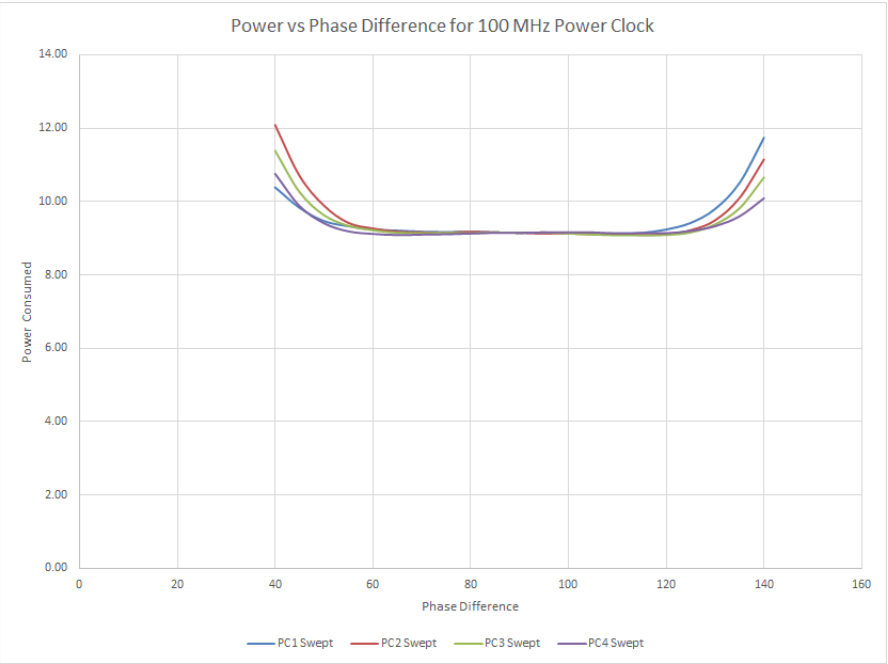

FIGURE 4.8: Overall power consumption in μW (summation of the power consumed by each power-clock signal) vs. phase difference (in °) for 100 MHz power-clock frequency when only the phase difference of one power-clock signal varies (with respect to the following power-clock signal).

4.2.2 CEPAL

Similar to the approach followed for ECRL, the phase difference between PC and $\overline{PC}$ is varied separately by maintaining the other power-clock signal at the ideal state. This analysis is performed for power-clock frequencies of 10 MHz, 13.56 MHz and 30 MHz. The external clock frequency (required for the flip-flops since CEPAL is not inherently pipelined, unlike ECRL) is the same as the power-clock signal. The consumed power, corresponding phase difference and the functionality are listed in Table 4.17 to Table 4.19. According to these tables, the tolerance to non-ideal phase differences decreases with higher power-clock frequencies. For the power-clock frequency of 10 MHz, correct functionality is achieved for a phase difference range of 150° to 210°. Thus, tolerance is 30° on both directions (of 180°). Similarly, for 13.56 MHz the tolerable phase difference range is 150° to 210°. Since the two frequencies are close to each other, the tolerance is the same. However, for a 30 MHz power-clock frequency, the tolerance is 10°, as listed in Table 4.19.

The dependence of power consumption on phase difference is significantly different on CEPAL since this logic does not rely on different intervals (unlike ECRL that has four intervals of hold, evaluation, wait, and recover). It is observed that the power consumption is the highest under ideal condition and slightly reduces as the phase difference changes. Figures 4.9 to 4.11 show the power consumption vs. phase difference for different frequencies.

Phase difference (in °)	Power consumed when PC varied (in μW)	Functionality	Power consumed when $\overline{PC}$ varied (in μW)	Functionality
220	5.48	Failed	5.3	Failed
210	5.89	Correct	5.61	Correct
200	5.96	Correct	5.86	Correct
190	6.02	Correct	6.03	Correct
180	6.06	Ideal	6.06	Ideal
170	6.02	Correct	5.99	Correct
160	5.89	Correct	5.92	Correct
150	5.69	Correct	5.70	Correct
140	5.41	Failed	5.40	Correct

TABLE 4.17: Power consumed (in μW) by CEPAL 16-bit CSA for various phase differences (in °) operating at 10 MHz power-clock frequency.

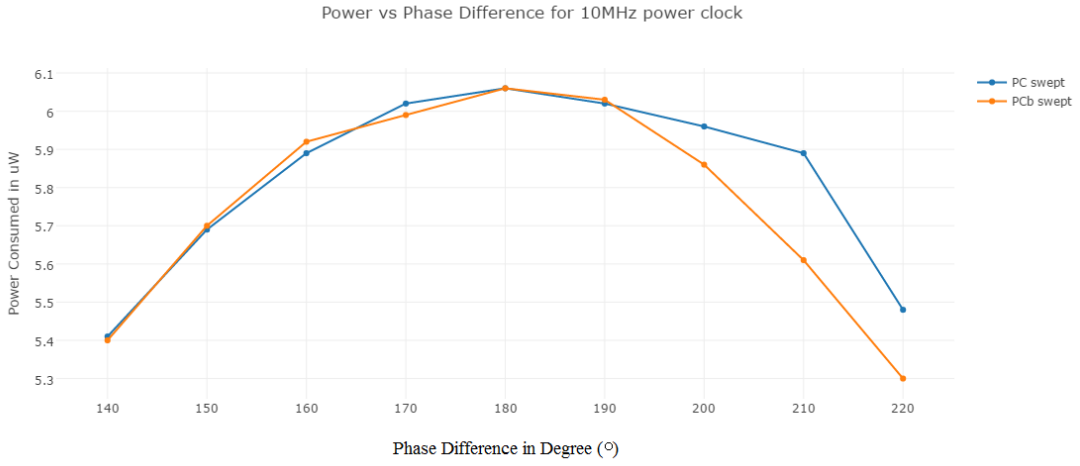

FIGURE 4.9: Power consumed vs. phase difference for CEPAL operating at 10 MHz power-clock frequency.

Phase difference (in °)	Power consumed when PC varied (in μW)	Functionality	Power consumed when $\overline{PC}$ varied (in μW)	Functionality
220	6.8	Failed	6.68	Failed
210	7.34	Correct	7.27	Correct
200	7.51	Correct	7.48	Correct
190	7.61	Correct	7.62	Correct
180	7.67	Ideal	7.67	Ideal
170	7.59	Correct	7.59	Correct
160	7.5	Correct	7.48	Correct
150	7.34	Correct	7.30	Correct
140	6.77	Failed	6.82	Correct

TABLE 4.18: Power consumed (in μW) by CEPAL 16-bit CSA for various phase differences (in °) operating at 13.56 MHz power-clock frequency.

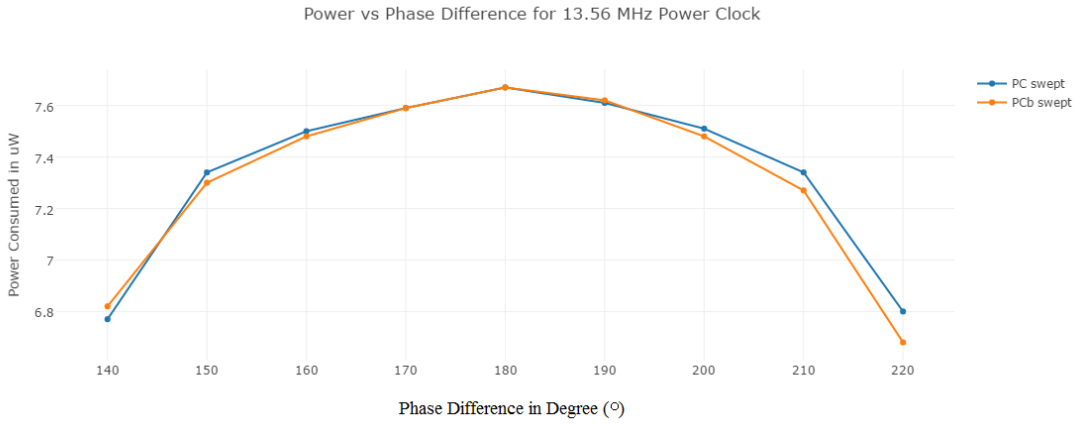

FIGURE 4.10: Power consumed vs. phase difference for CEPAL operating at 13.56 MHz power-clock frequency.

Phase difference (in °)	Power consumed when PC varied (in μW)	Functionality	Power consumed when $\overline{PC}$ varied (in μW)	Functionality
200	13.34	Failed	-	-
190	13.94	Correct	13.92	Failed
180	14.24	Ideal	14.24	Ideal
170	13.99	Failed	13.91	Correct
160	-	-	13.35	Failed

TABLE 4.19: Power consumed (in μW) by CEPAL 16-bit CSA for various phase differences (in °) operating at 30 MHz power-clock frequency.

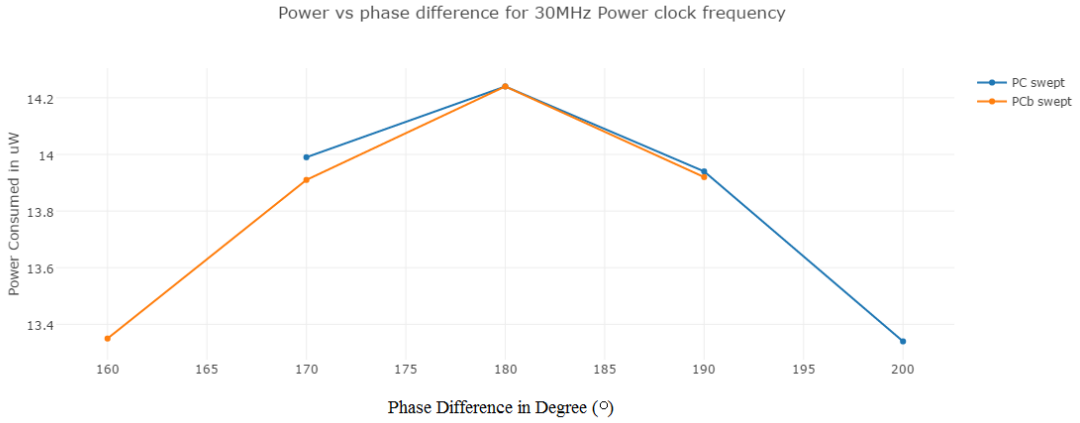

FIGURE 4.11: Power consumed vs. phase difference for CEPAL operating at 30 MHz power-clock frequency.

Chapter 5

CONCLUSION

The primary objective of this thesis is to evaluate the tolerance of two charge-recycling logic families (ECRL and CEPAL) to non-ideal phase differences in power-clock signals. Recently, a unique synergy between wireless power harvesting and charge-recycling logic has been demonstrated. Specifically, harvested wireless energy in the form of AC signal (known as the power-clock signal) is directly used to power charge-recycling logic, thereby eliminating the costly (both in terms of power and area) rectification and regulation stages.

Since most of the charge-recycling logic families require multiple phases to operate, it is important to understand how these circuits behave under non-ideal phase differences. Understanding this behavior is important particularly for wirelessly powered charge-recycling logic since deviations in the ideal phase differences are expected.

Initially, the power consumed by the ECRL, CEPAL, and static CMOS 16-bit carry select adder is investigated. The power comparison between the three logic approaches is studied, as listed in Table 3.1 to Table 3.3. Figure 3.25 and Figure 3.26 show that the ECRL consumes the least power among the three logic families, which verifies the theoretical results.

The effect of non-ideal phase difference on power consumption and functionality is then studied by varying the phase difference among the power-clock signals for the 16-bit CSA. To summarize:

27. For ECRL, the 16-bit CSA is able to tolerate a non-ideality of 30° in the phase difference without affecting the power consumption and functionality. If the deviation is more than 30°, the power consumed by the circuit increases exponentially, however the functionality remains unaffected. Furthermore, the increase in power consumption is higher at higher power-clock frequencies.

28. Alternatively, for CEPAL, the 16-bit CSA fails to correctly operate when the phase difference varies by 40° at 13.56 MHz and by only 10° at 30 MHz. Thus, unlike ECRL, functionality strongly depends upon the phase difference. The power consumption, however, is a weak function of phase difference in CEPAL.

Charge-recycling circuits can provide new and highly exciting opportunities for wireless power harvesting, particularly for IoT based devices. This thesis provides helpful information on the tolerance of this logic to non-ideal phase differences.

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Appendix A: Schematic Figures

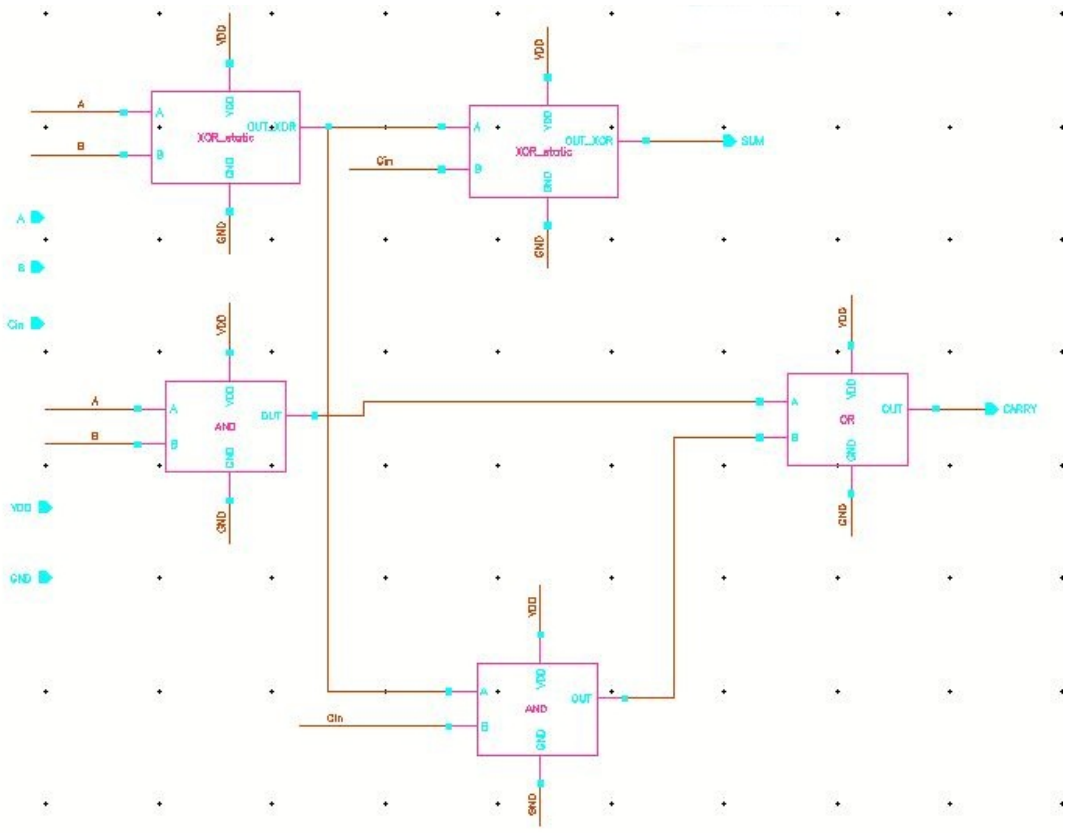

FIGURE E.1: Static CMOS 1-bit full adder employing propagate/generate logic

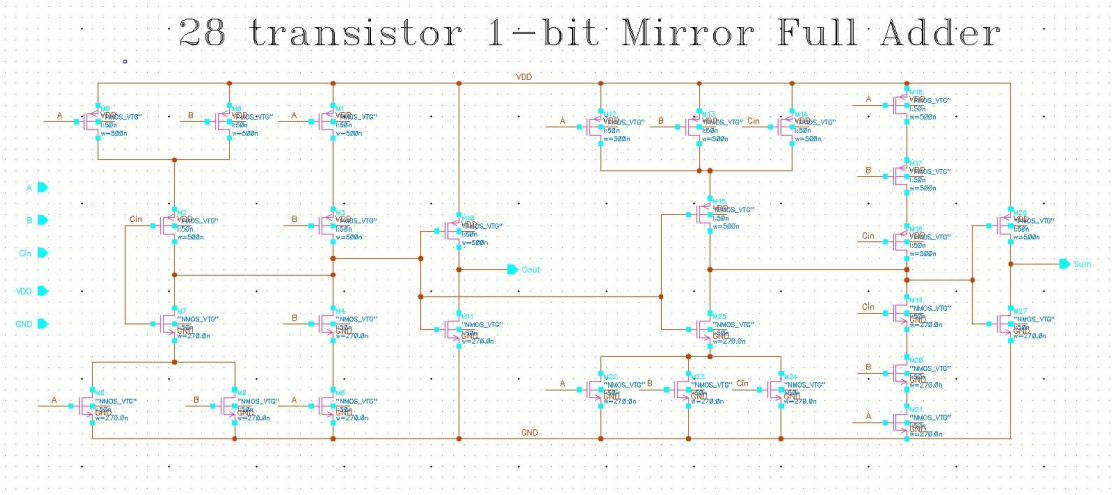

FIGURE E.2: Static CMOS 1-bit full adder employing 28-transistor mirror logic

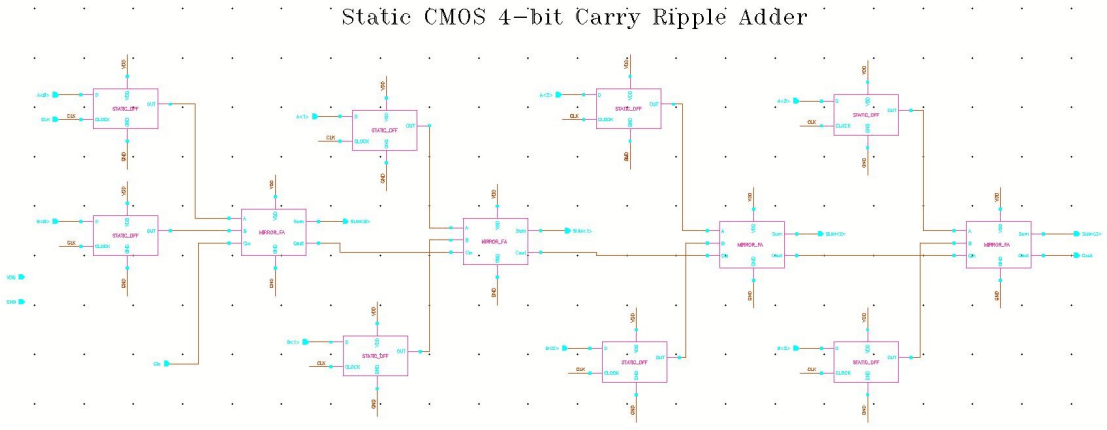

FIGURE E.3: Static CMOS 4-bit carry ripple full adder

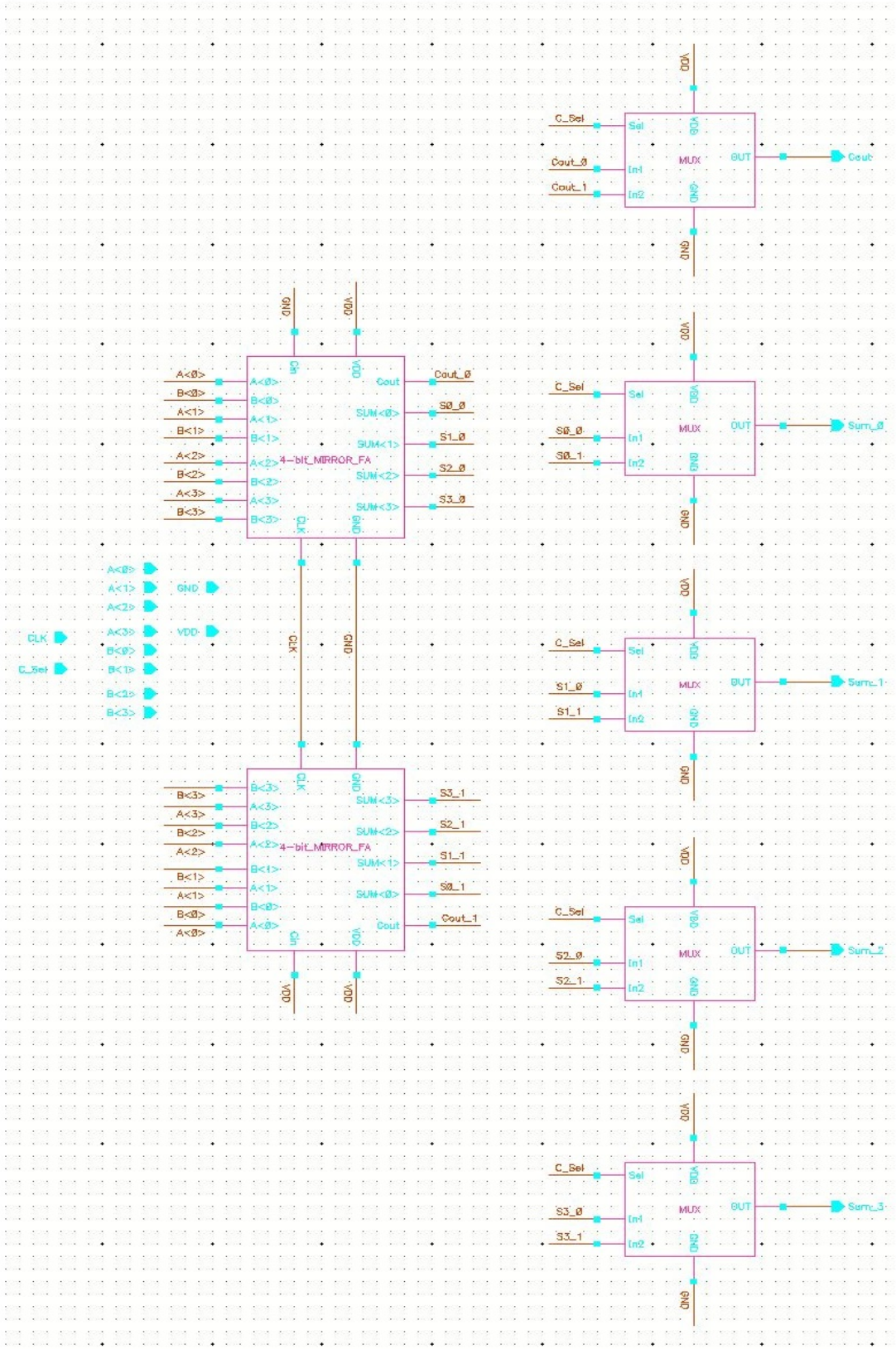

FIGURE E.4: Static CMOS 4-bit carry select full adder

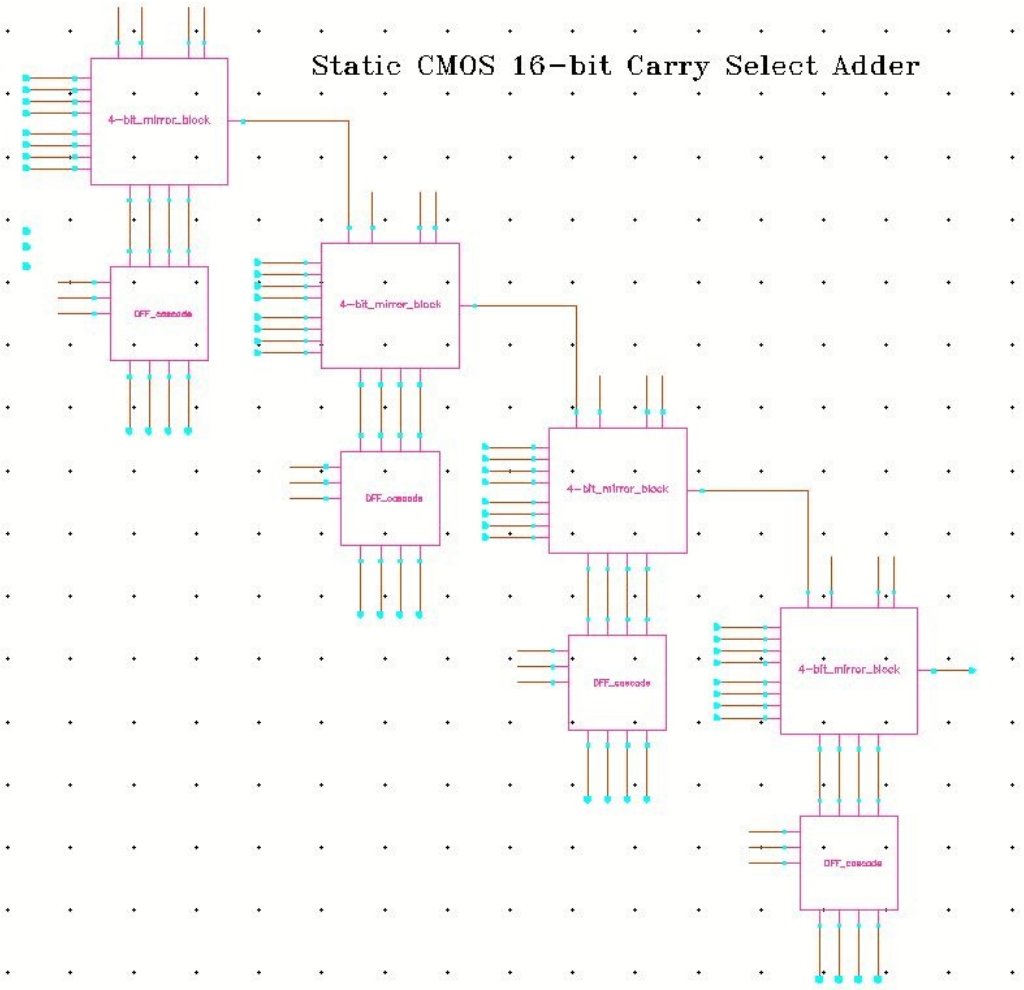

FIGURE E.5: Static CMOS 16-bit carry select adder

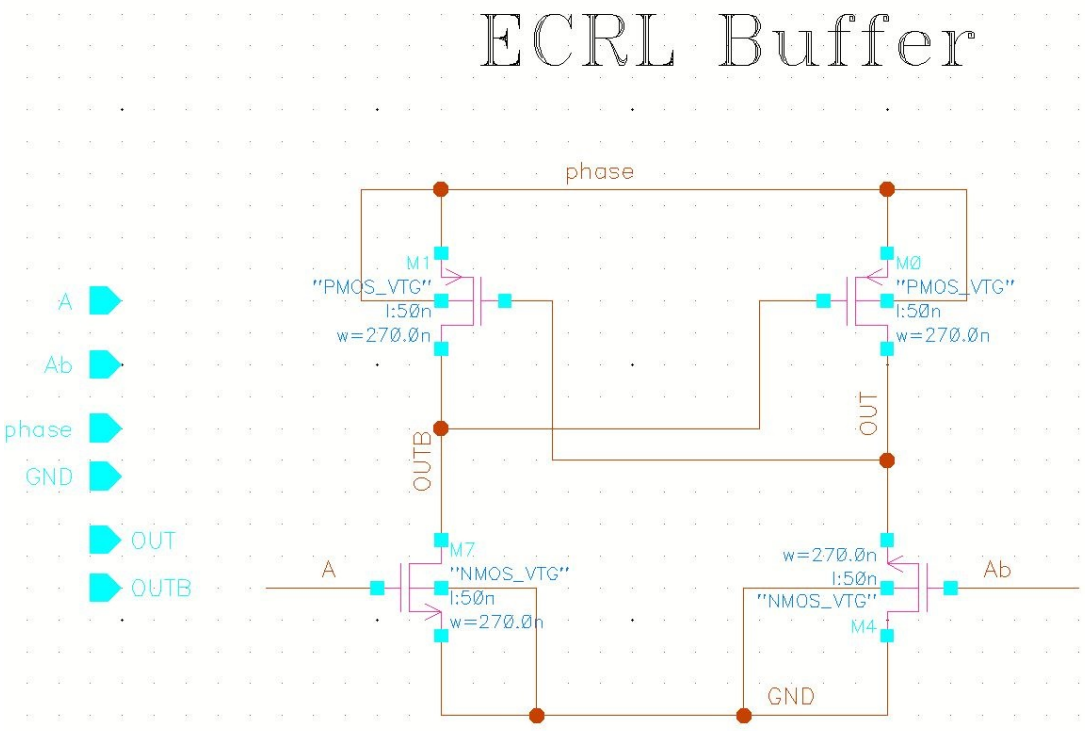

FIGURE E.6: ECRL buffer circuit

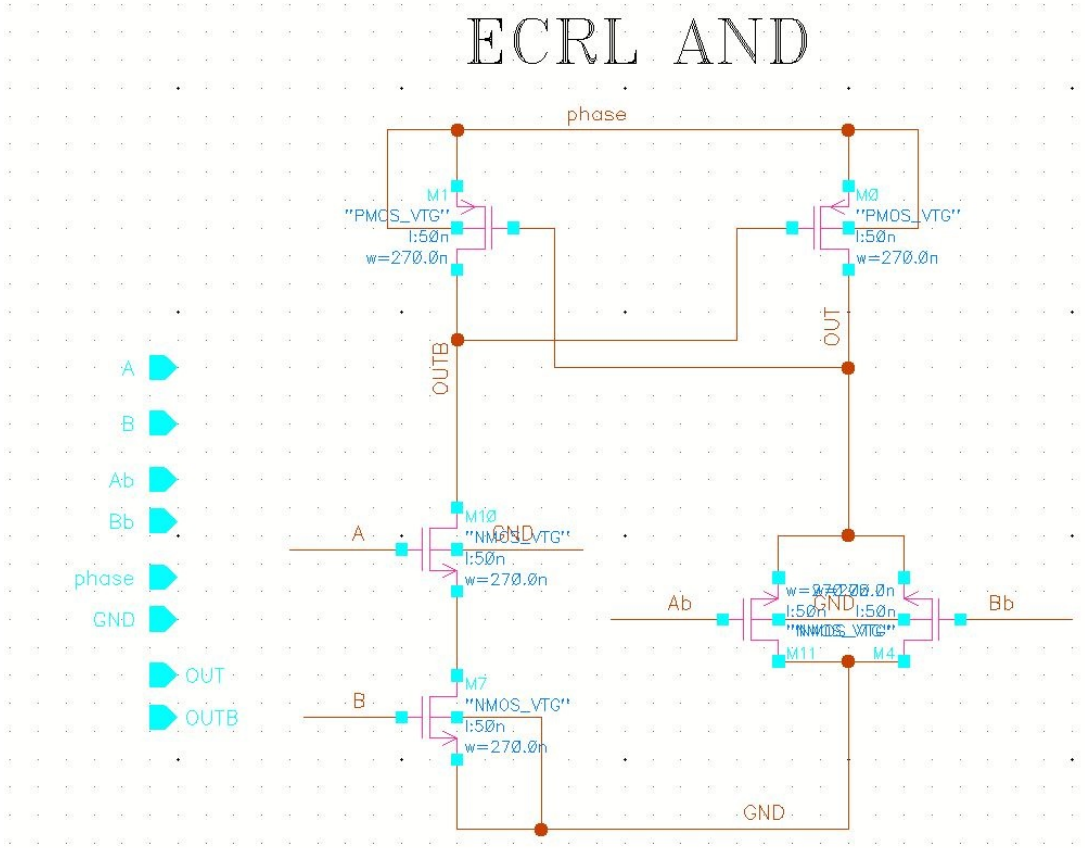

FIGURE E.7: ECRL AND circuit

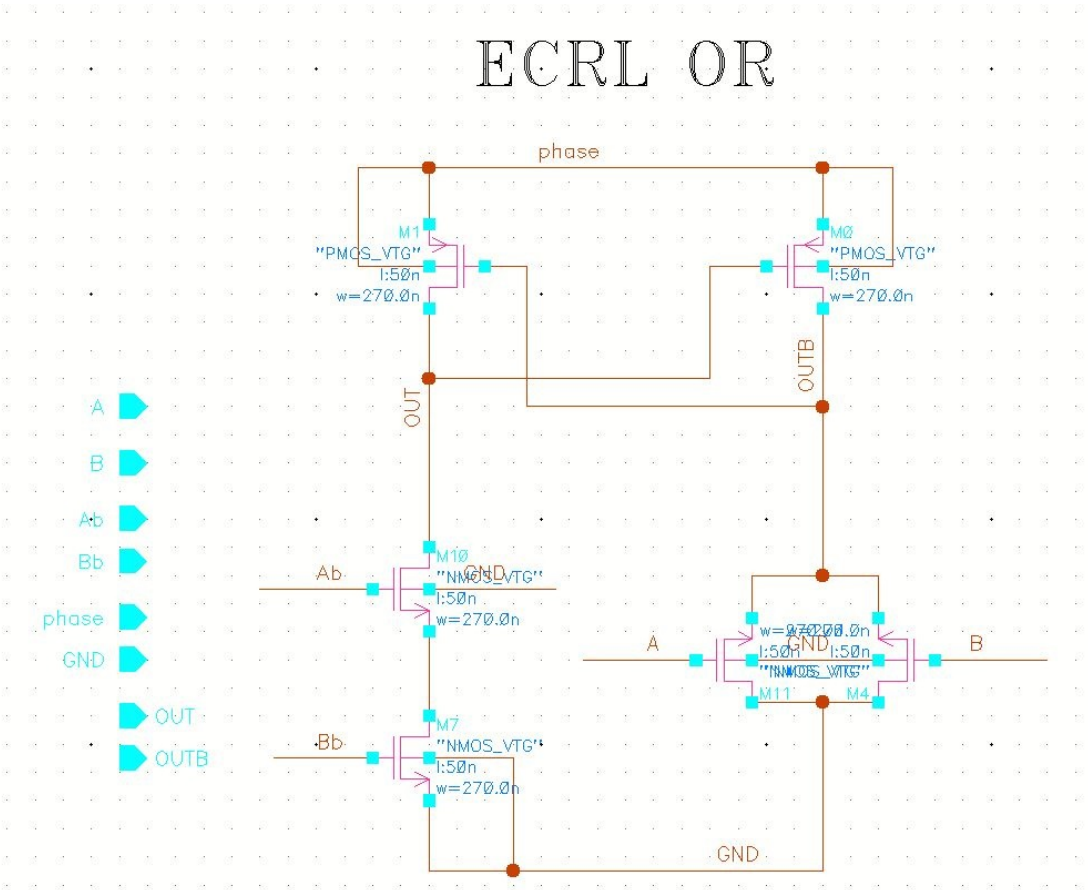

Figure E.8: ECRL OR circuit

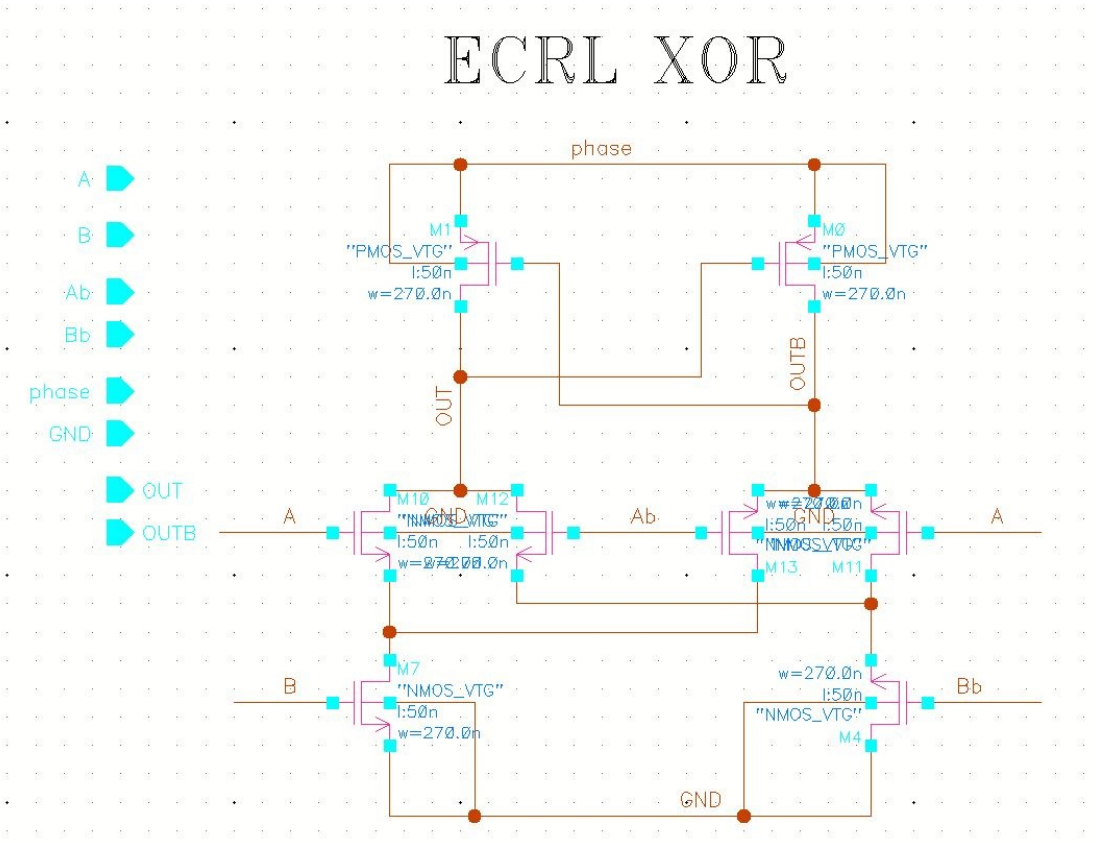

Figure E.9: ECRL XOR circuit

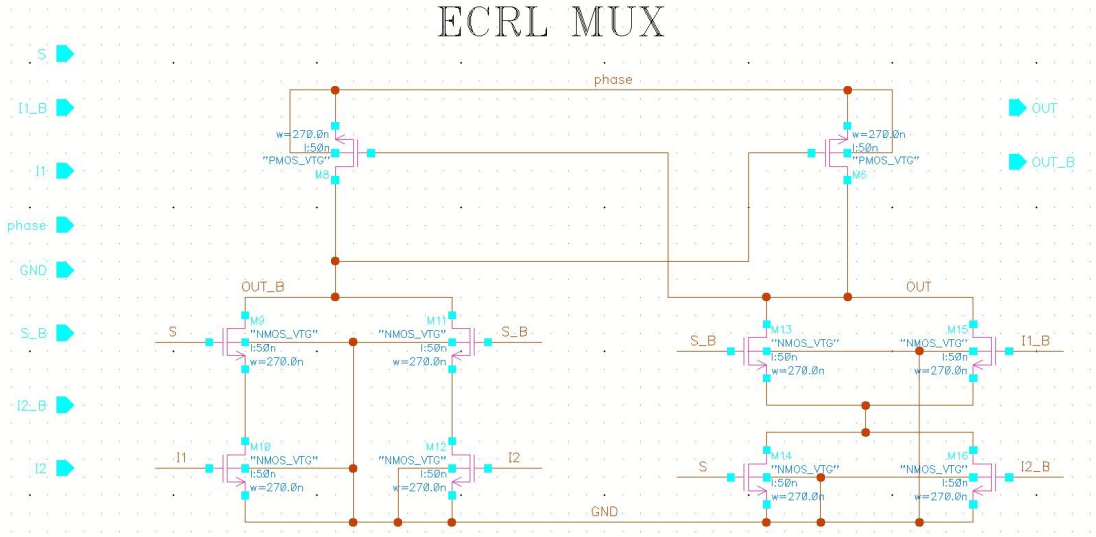

Figure E.10: ECRL mulitplexer circuit

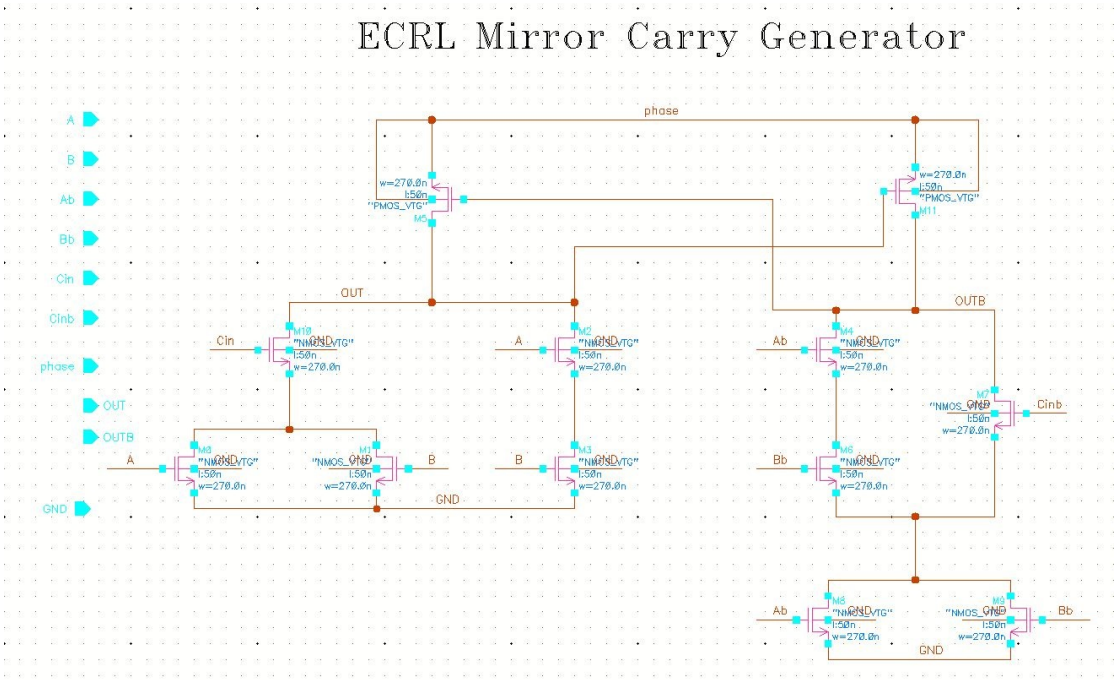

FIGURE E.11: ECRL carry generator circuit of 28-transistor mirror adder

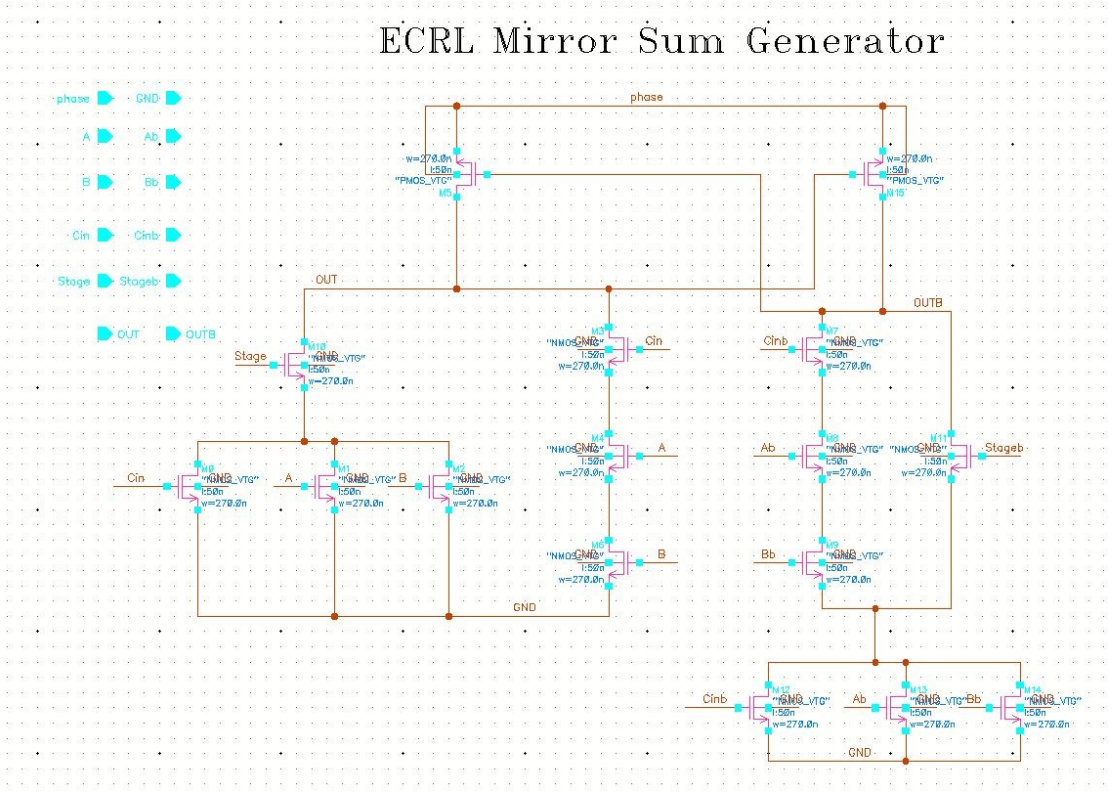

FIGURE E.12: ECRL mum generator circuit of 28-transistor mirror adder

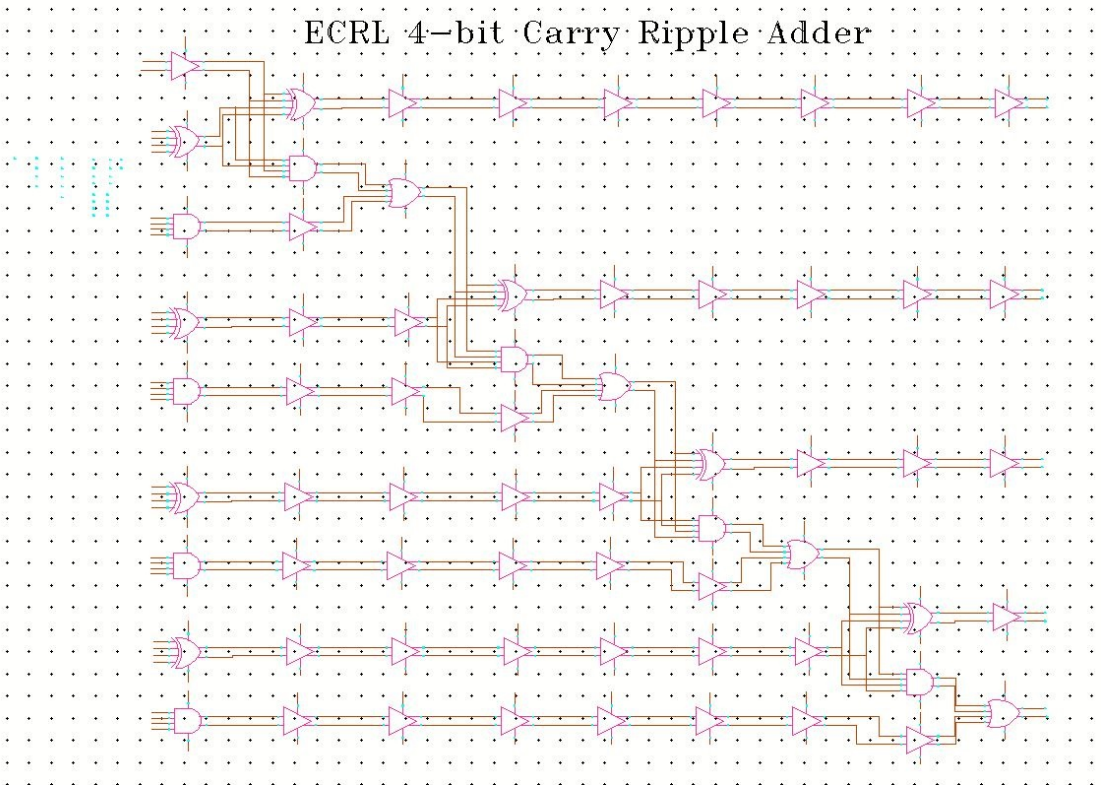

FIGURE E.13: ECRL 4-bit carry ripple adder employing propagate generate logic

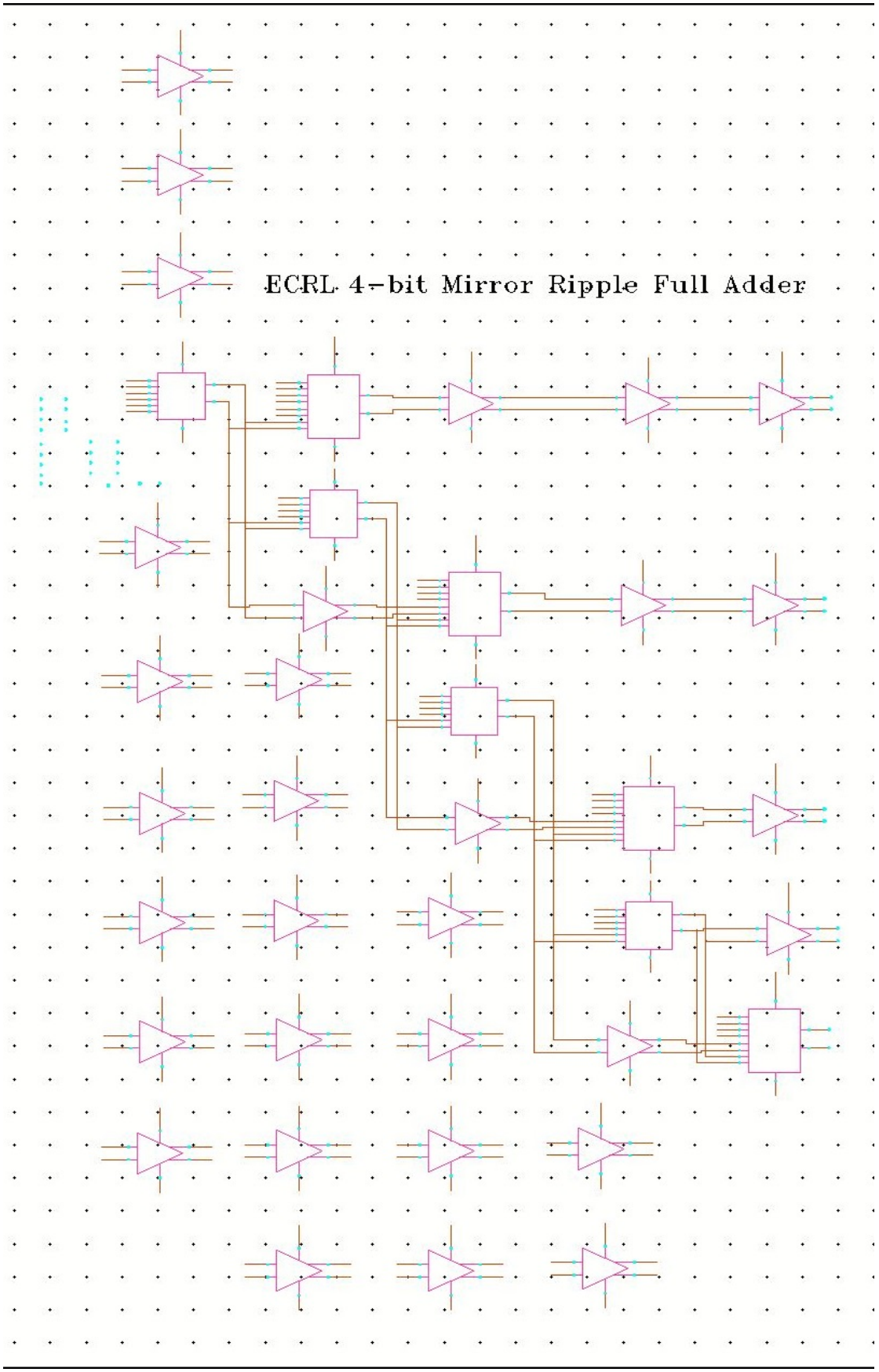

FIGURE E.14: ECRL 4-bit carry ripple adder employing mirror adder logic

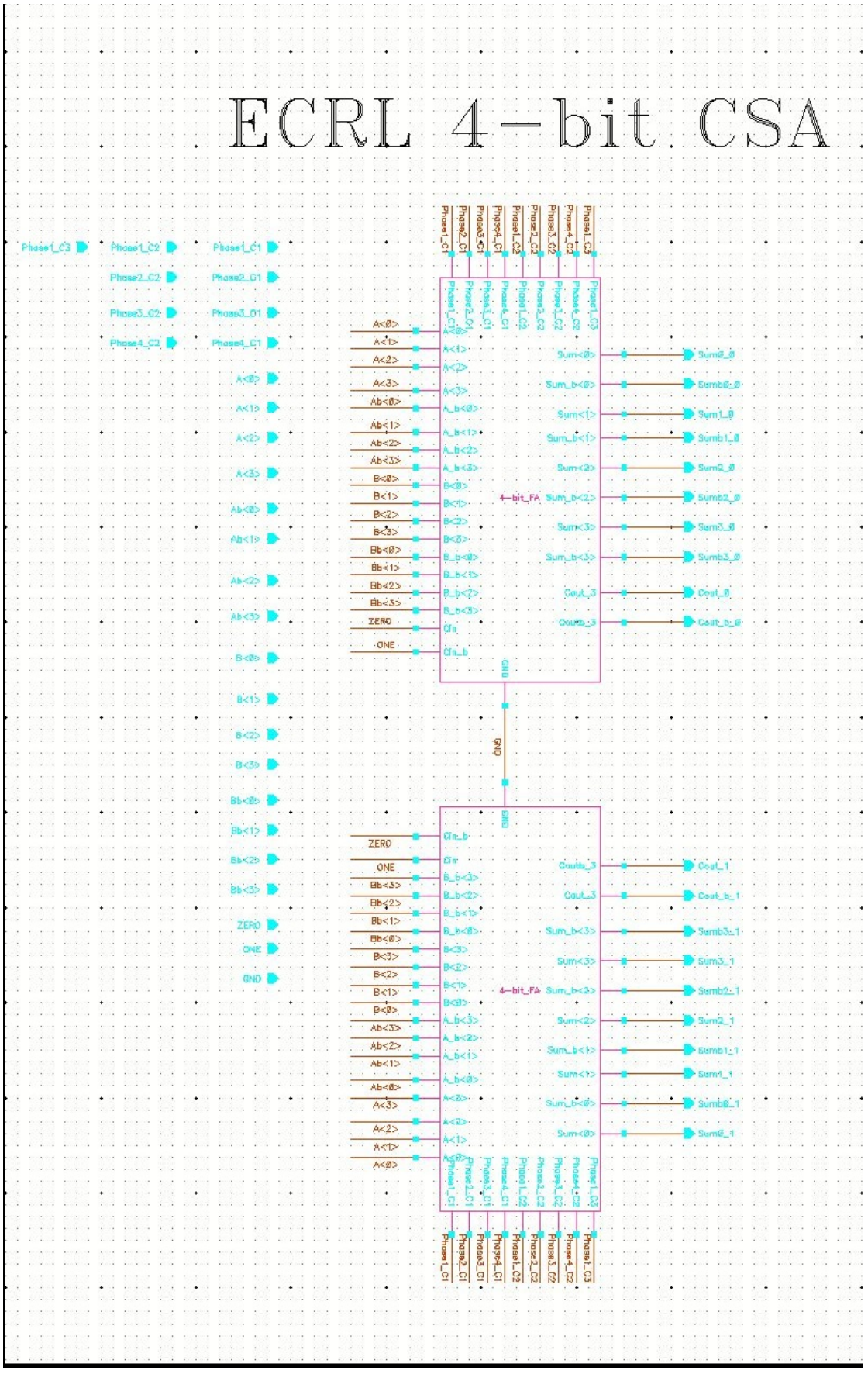

FIGURE E.15: ECRL 4-bit carry select adder

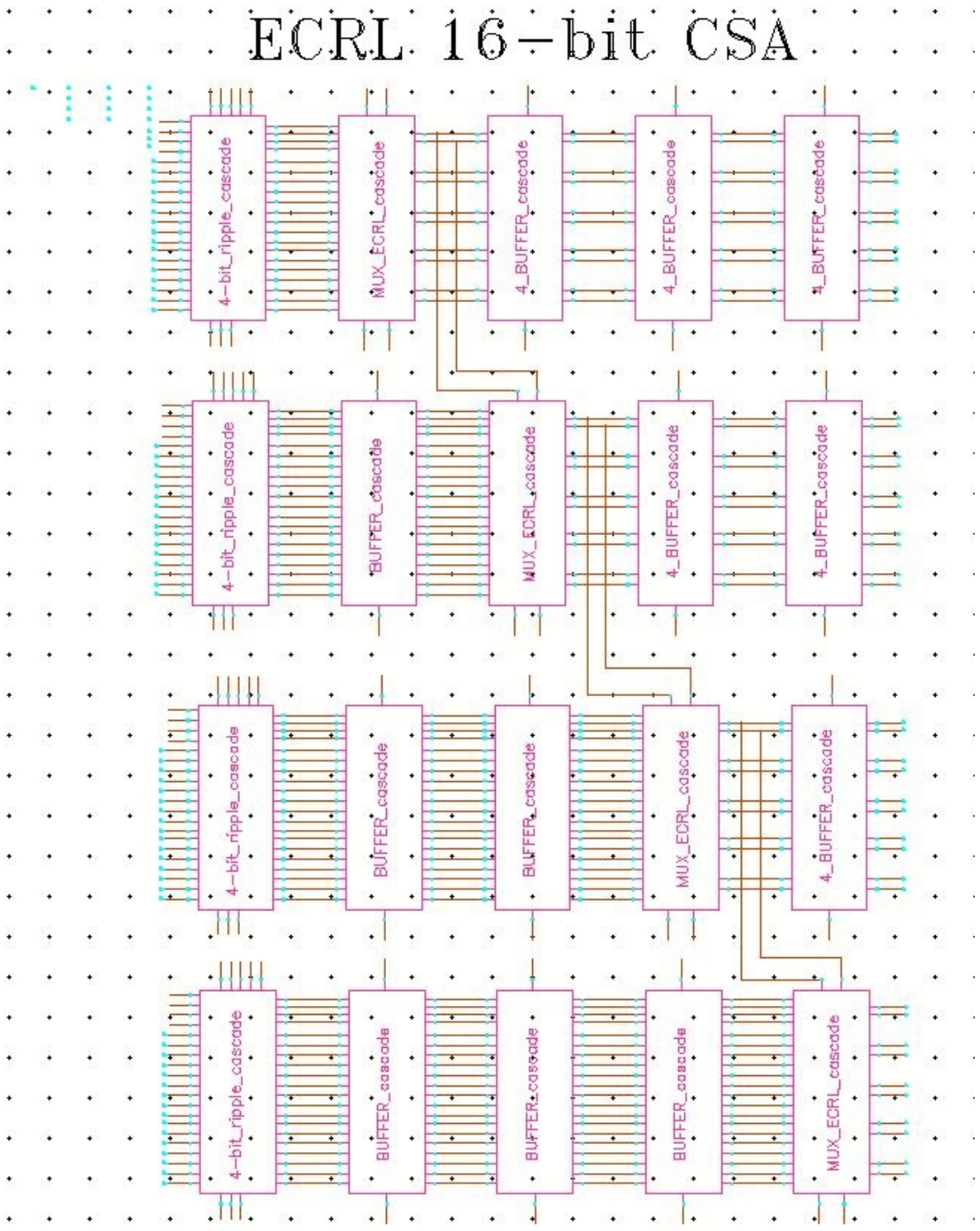

FIGURE E.16: ECRL 16-bit carry select adder

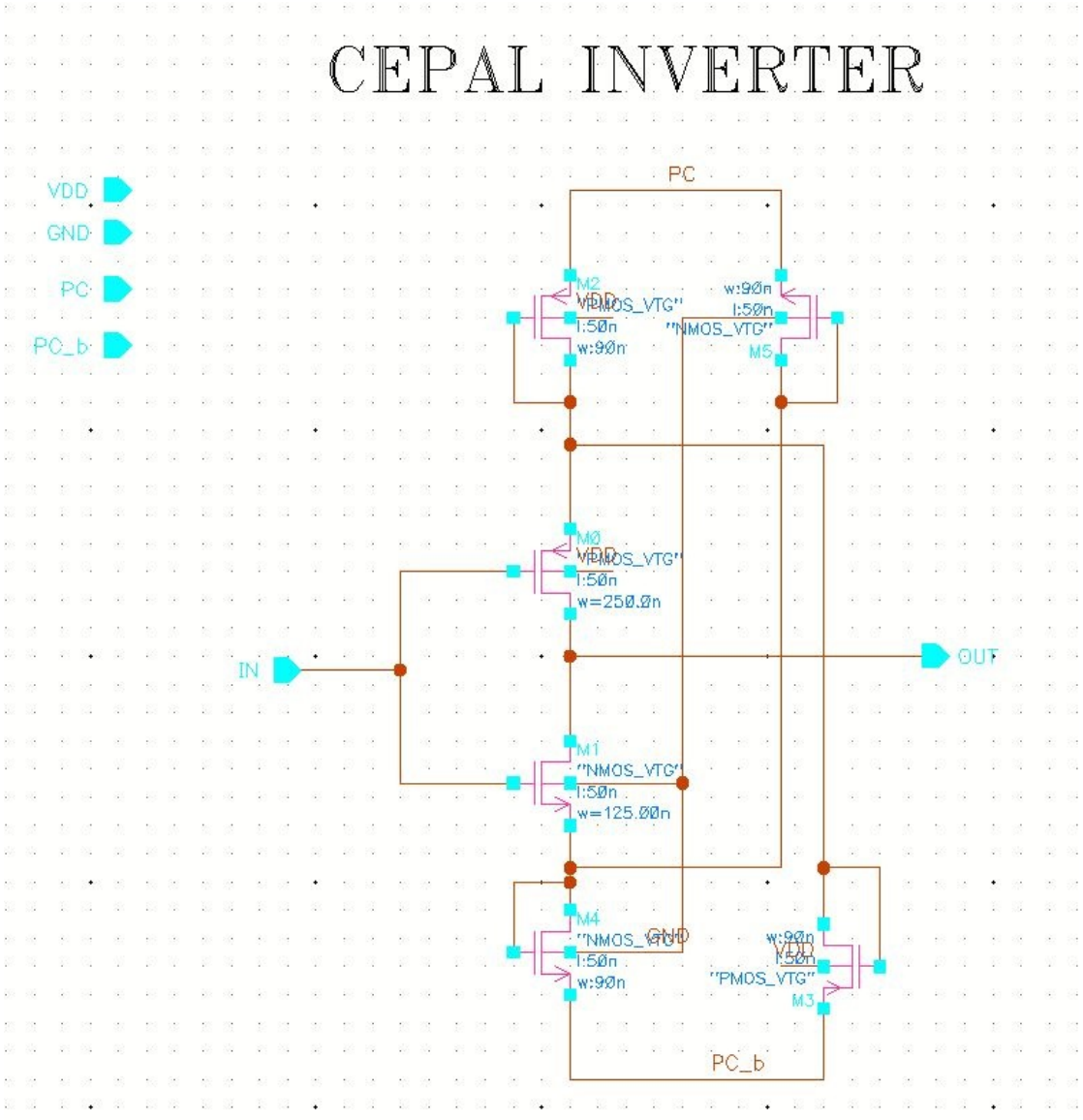

FIGURE E.17: CEPAL inverter circuit

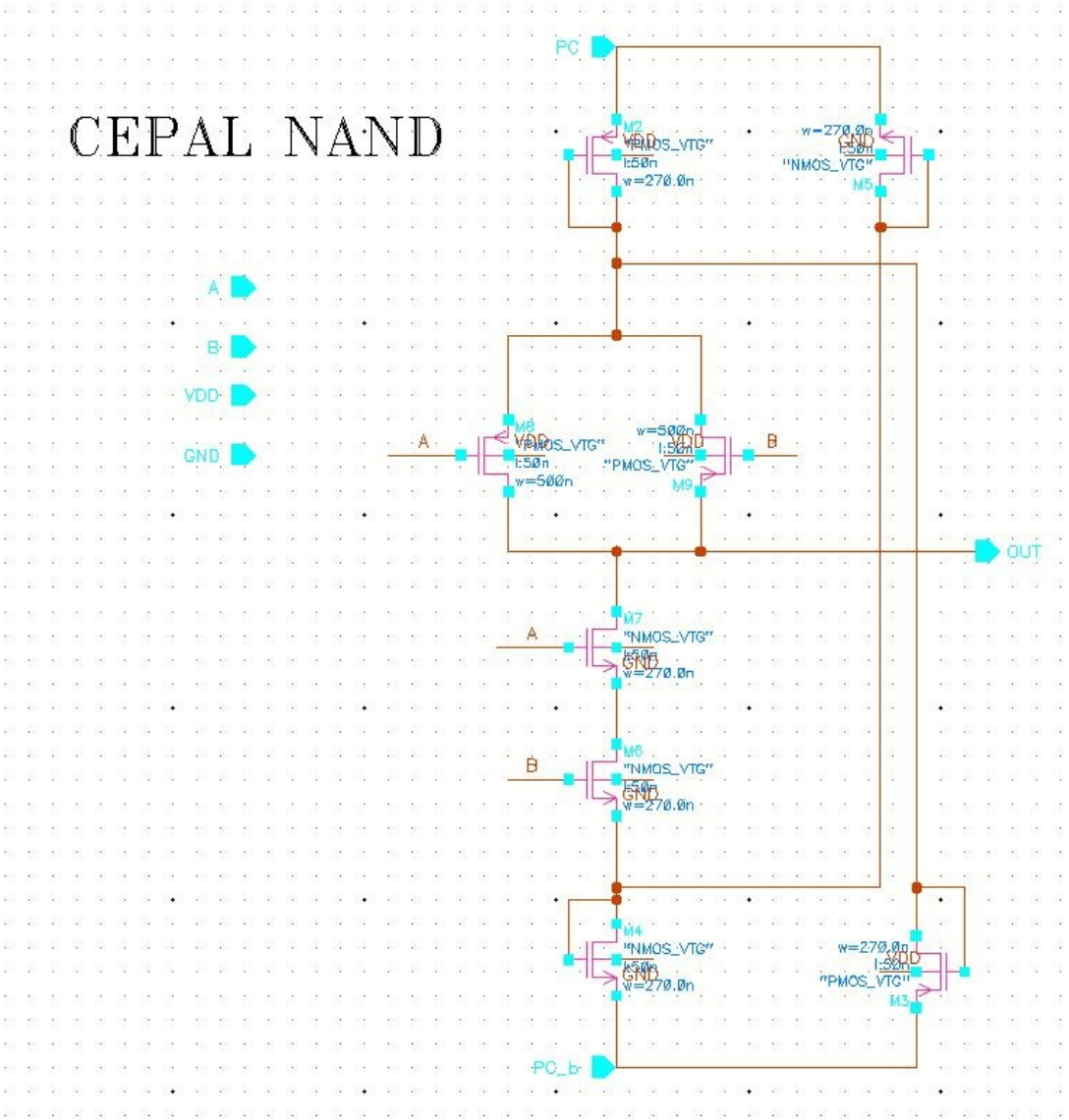

Figure E.18: CEPAL NAND circuit

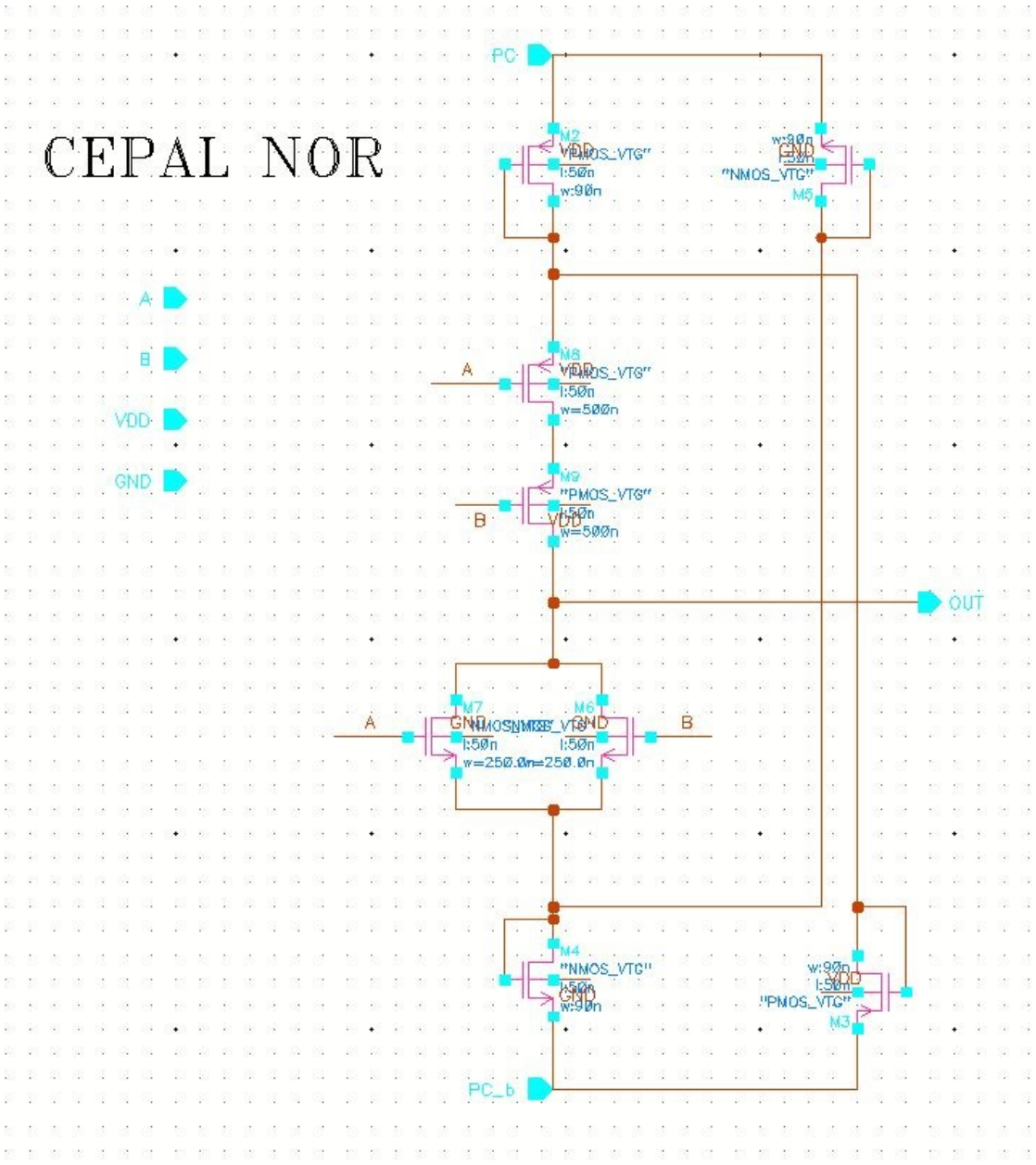

FIGURE E.19: CEPAL NOR circuit

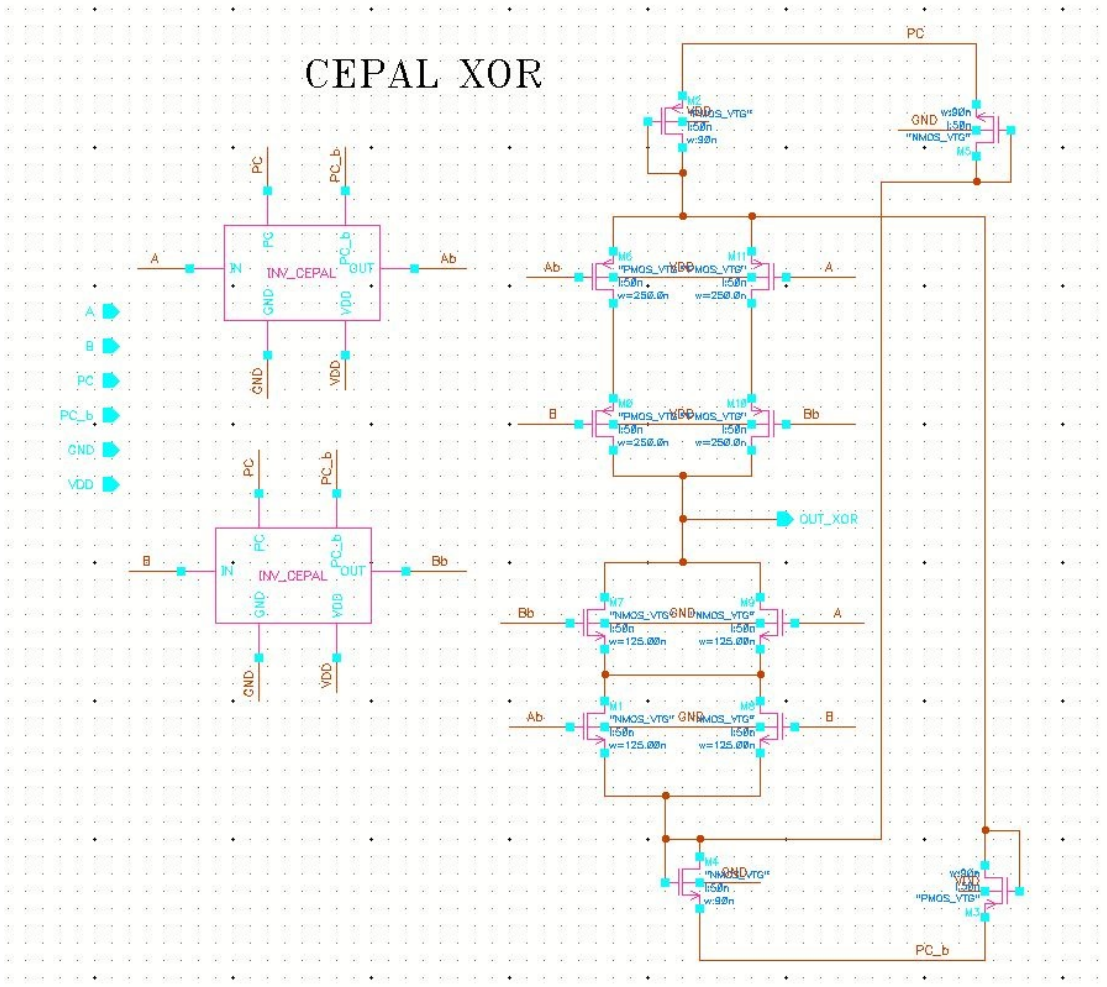

Figure E.20: CEPAL XOR circuit

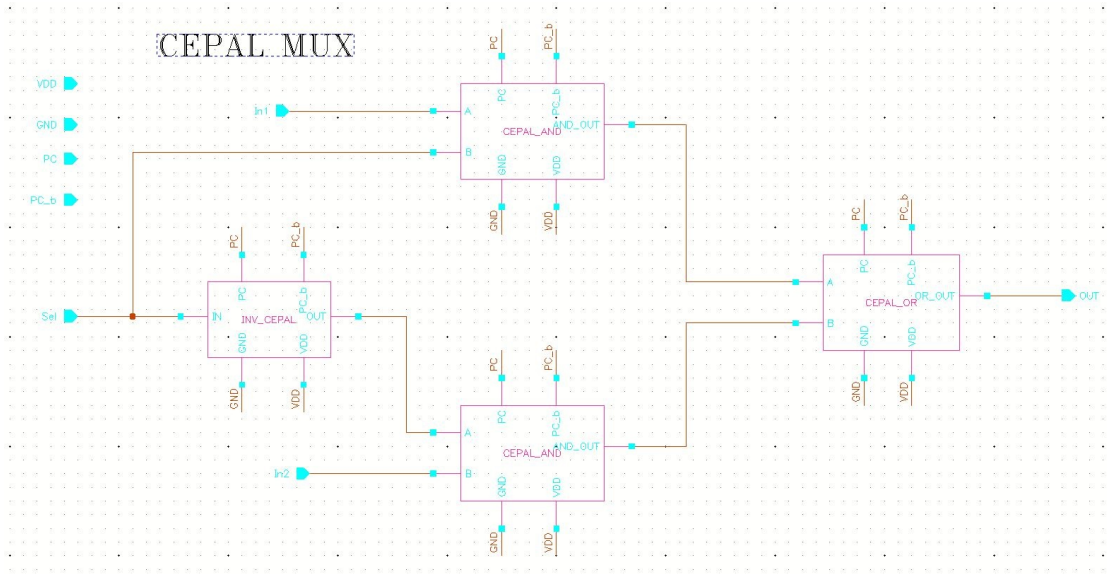

Figure E.21: CEPAL multiplexer circuit

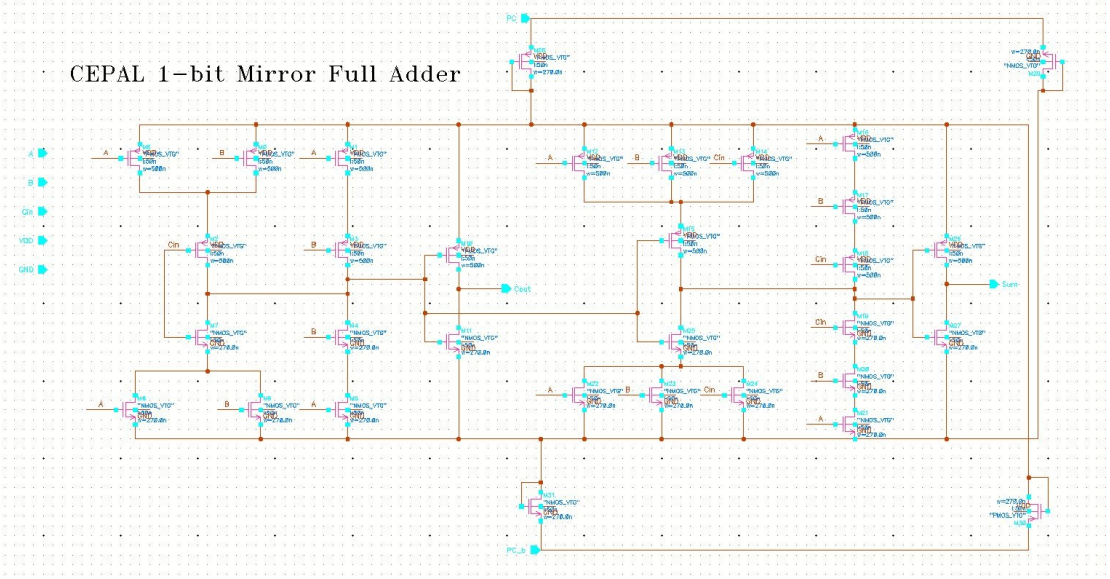

FIGURE E.22: CEPAL 1-bit full adder employing 28-transistor mirror logic