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Systematic Modeling and Characterization of Analog Circuits using Symbolic and Data Mining Techniques

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Abstract of the Dissertation

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Analog circuit design activities mainly depend on designers' expertise and their ability to produce new designs by combining basic devices, subcircuits, and ideas from similar solutions as the source for innovation. There are very few systematic methods that can characterize similarities and differences between analog circuits while maintaining the correlation between design variables, performance, and trade-offs. Moreover, many computer-aided design tools are focused only on routine tasks, like transistor sizing and layout design.

This dissertation presents novel techniques to automatically characterize the analog design space based on feature uniqueness and variety and to perform systematic circuit comparisons using symbolic models. Initially, we

evaluate, for different analog circuit families, design science metrics aimed at capturing feature uniqueness and variety. The studies are useful in producing an overall characterization of analog circuit features. The insight obtained can help in enhancing the circuit design process and developing new automated synthesis techniques that can explore solution space regions that are likely to include novel design features.

A symbolic technique is proposed to automatically create ordered feature clustering schemes that express the main structural similarities and differences among analog circuits. Four separation scores, based on entropy, item characteristics, category characteristics, and Bayesian classifiers are investigated for large sets of state-of-the-art amplifier circuits. The generated representations offer understanding about the uniqueness and importance of specific design features and can be used in topology refinement and automated synthesis. For detailed analysis, an automated mechanism for systematically producing comparison data between two analog circuits is developed. The similar and distinguishing performance characteristics of circuits with respect to gain, bandwidth, common-mode gain, noise, and sensitivity are captured. The technique utilizes matching of both topologies and symbolic expressions of the compared circuits to find the nodes with similar behavior. The impact on performance of the unmatched nodes is used to express the differentiating characteristics of the circuits. The produced comparison data is important for getting insight into unique benefits and limitations of a circuit, selecting fitting circuit topologies for system design, and optimizing circuit topologies. Systematic comparison is the basic operator of a prototype framework for modeling the analog circuit design feature variety. The proposed concept structure model expresses symbolically the design features as well as their advantages and limitations at different levels of abstraction and includes systematic mechanisms that can create new conceptual solutions. Case study examples illustrate application of the proposed methods in a reasoning-based analog circuit synthesis technique. The procedures incorporate cause-effect understanding of the performance limitations generated by circuit structures and precisely addresses them by finding alternatives that relax performance trade-offs.

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Chapter 1

Introduction

Analog circuit design is considered to be by and large an art [6–8]. This is arguably due to the circuit design activity being a less structured process that is not fully formalized as an algorithmic sequence of steps. Designers often rely on similarities with previous designs (experience), on analogies with solutions in other engineering domains, and even on inspiration drawn from biology and anatomy [9]. However, the main vehicle in creating novel circuit solutions is still a designer's talent to combine the defining features of basic devices and building blocks (e.g., sub-circuits) into new design solutions. While the characteristics of the actual building blocks are well understood, the innovating process of creatively combining them is not.

In spite of significant progress on methods and software tools for synthesis and verification of analog circuits, the design process continuous to be relatively slow, expensive, and error-prone. The productivity gap is 100x to 1000x as compared to what is needed to design next-generation electronic systems [10]. Tools can efficiently address tedious but conceptually-well understood, routine activities, like transistor sizing and constructing layouts [6,7, 11–13]. However, computer-aided design (CAD) tools for analog circuit topology synthesis are continuously challenged to keep pace with state-of-the-art design and to *invent* new topologies that closely resemble the kind of circuits that an expert would produce [8,14]. Knowledge-based expert systems [15–18]

for synthesis using static libraries of design rules have been developed to tackle a given family of circuits. For example, the interactive design tool [15] uses knowledge specific to the schematic, general circuit theory, and related to the circuit family. In [19], specification requirements and design knowledge are used to reason out an optimized circuit topology and device dimensions. The topology selection algorithm in [20] uses fuzzy rules based on specification requirements. A decision tree is utilized to select circuit topologies in [17] from a library of existing, characterized circuits. The topology generation procedure in [21] uses designer expertise by operating on a library of basic building blocks. The technique creates combinations of library structures which are filtered through an extensive set of rules that are aimed at producing only designer-trusted circuits. The set of rules includes constraints that relate to correct electrical connectivity of blocks, structure symmetry, and device biasing conditions. Domain knowledge and designer expertise have also been increasingly added to evolutionary analog circuit topology synthesis techniques to improve the quality of the produced solutions. Early methods did not include constraints to guide the search and created *unusual* solutions which were not accepted as *trustworthy* by the design community [14]. To overcome such aspects, more recent tools include various forms of design experience in the synthesis flow. For example, the technique for synthesizing analog-to-digital converter architectures from [22] successively refines the population of designs through a set of designer-specified topology transformations (e.g., increase number of comparators). Heuristic evaluations are used to suggest only relevant transformations which are expected to offer the most improvement in design performance. The tool from [23] synthesizes single-stage and two-stage amplifiers by executing the evolutionary search on a hierarchical library of designer-specified structures. Generated topologies are *trustworthy by construction* as designer knowledge is encoded in the organization of the building blocks which ensures correct connectivity of well-known sub-circuits in the produced designs.

Challenges arise for new design problems that introduce new requirements and extending the available knowledge base needs substantial design

effort. There are usually no closed-form descriptions or specific design rules available unless a significantly large number of conceptually-similar designs are solved first manually. The solving process involves reasoning and decision making in an effort to address open-ended issues and create the missing domain knowledge. Particularly, circuit topology design and refinement requires significant conceptual design for finding new principles of signal processing and control. New ways of connecting structurally the devices, novel rules for constraining the device operation, and new sub-structures might emerge during the process used by designers to reason out the solution.

An intriguing new approach is to automatically identify design knowledge and design strategies that are contained within a collection of existing designs. *Understanding* the features of previous designs is essential in using the explored design space to find consistent design decisions. This includes identifying strategies to efficiently combine different structures and to constrain design parameters such that trade-offs are relaxed. Systematically devising such design plans which can be used in similar contexts constitutes a powerful concept. Analog circuit CAD industry has recently shown great interest in such techniques that leverage insight extracted from existing designs to create constraints for synthesis tools to improve the chances of generating feasible, high quality designs. For example, a practical application involves creating design plans from high quality analog layouts developed by expert designers such that the same design style can later also be applied to other applications. Similar concepts have been explored in evolutionary algorithms literature. The use of run transferable libraries [24] was shown to help scaling and enable more efficient problem solving through geometric programming (GP) techniques by transferring learned domain knowledge to subsequent runs. An example of such an approach is the analog topology synthesis technique which adds novelty in [23]. The method creates new basic structures through GP mutation of well-known circuit features [23] when performance is insufficient and adds these novel elements to the existing amplifier library for future reuse. We believe that, on the long run, devising systematic design plans and models to express expanding and evolving circuit design knowledge will lead to superior

CAD tools and extend the grasp of current analog synthesis techniques to a wider range of problems, including new systematic techniques for enhancing the basic building block libraries [21, 23] and new design improvement strategies [22].

This dissertation lays out the foundations of analog circuit design plan generation methods by presenting novel techniques to systematically characterize the analog circuit design space in terms of common and distinct structures utilized in a collection of designs and their impact on circuit performance. A preliminary study on measuring innovation in circuit design using metrics from design science illustrates the importance of accurately describing the uniqueness and variety of design features. Based on the insight gained from this study, two main systematic methods are proposed for constructing analog circuit design space descriptions:

- Creating ordered node feature clustering representations (ONCR) for large sets of analog circuits based on topology matching,
- Generation of systematic comparison data between analog circuits to capture the performance implications of the distinguishing features.

Given a set of circuits C_1, C_2, ... C_n, the first technique aims to build a symbolic description (model) that presents the main similarities and differences between circuits with respect to their structural features. A good description scheme must easily distinguish the circuits, e.g., there should be a minimum number of criteria that separate a circuit from the other circuits in the set with respect to their topological features. Using a structural symbolic circuit model [25], the method performs topological matching to identify a set of possible separation criteria. These include groups of circuit nodes with similar symbolic expressions of poles and couplings to other circuit nodes. The identified groups (criteria) are then aggregated in the ordered node feature clustering representation. High level clusters present high similarity among nodal features while lower levels illustrate dissimilar features. We evaluated four separation scores to automatically produce the ordered representation: entropy, item characteristics, category characteristics, and Bayesian classifiers [26]. The

generated representations offer understanding about the uniqueness and importance of specific design features and can be used in topology refinement and automated synthesis.

Systematic comparison for analog circuits extends the concepts of topological matching and aims to identify all related design variables, characterizing the impact of similar and distinguishing variables on circuit behavior and performance attributes. Two circuit nodes (from different circuits) have similar electrical behavior, if there are conditions under which the transfer function (TFs) between the nodes and inputs can be matched, such that the two TFs represent the same mathematical expressions. Examples of such conditions include requirements that certain device parameters are equal (matching), some device values are much larger (smaller) than others, certain device parameters can be neglected, and so on. Characterizing the performance differences of two circuits must capture how topological and behavioral changes modify performance attributes with respect to trade-offs, availability of free (orthogonal) variables to control specific performance attributes, achievable performance values, and difficulty in finding the parameter values that set desired performance. The proposed circuit comparison procedure is performed in four steps. First, topological matching relates the structural features of the two circuits. It identifies sets of nodes with similar poles and connectivity to other nodes. Second, symbolic matching describes the electrical behavior of the circuit nodes using the topologically matched nodes as a reference. It computes transfer functions H_{comm} and H_{diff} expressing the similarities and differences in the electrical behavior of the circuit nodes. The third step, constraint generation, creates constraints defining how functions H_{comm} and H_{diff} impact performance, such as the resulting DC gain, bandwidth, noise, and common mode rejection ratio (CMRR). Finally, performance characterization describes the capability of a design to meet the generated constraints, and thus achieve certain performance and trade-off values with respect to the identified differences between the compared circuits. The presented method focuses on AC performance, based on the structural circuit macromodeling technique from [25].

The proposed techniques are used to introduce a prototype framework for modeling the analog circuit design feature variety through concept structures that expresses domain knowledge for analog circuits implementing the same functionality. The proposed model is important to characterize the novel and similar features in a circuit, the conditions under which existing design features can be reused in new circuits, and the exploration of new conceptual designs. Four symbolic operators are used in modeling: circuit concept comparison, circuit concept instantiation-abstraction, circuit concept combination, and design feature induction. The first two operators are used to construct the concept structure for a set of known solutions, while the later two provide the mechanism to extend the knowledge representation to find novel solutions. Circuit comparison relates behavior and performance of concepts. Instantiation-abstraction organizes the features at various levels by replacing signals or blocks in a design through clusters of signals or blocks with the same behavior. The concept combination operator produces a new circuit concept for an application by mixing the features of two existing circuits such that resulting performance is improved. The generic concept induction operator uses the existing information on design feature variety from all concepts in the structure to create novel concepts that have not yet been explored, such as different connection patterns among signal nodes that can relax trade-offs.

The main techniques in analog circuit topology synthesis tackle the problem using optimization [27], evolutionary algorithms [23], or template-based synthesis [28]. The methods introduced in this dissertation create the foundation for an alternative approach to analog circuit synthesis based on reasoning. Characterizing the variety of common and distinct circuit structures through ONCRs and correlating symbolically the distinguishing design variables to performance trade-offs creates the premise for cause-effect *understanding* and *reasoning* the solution. This approach closely resembles an expert designer's style of analog circuit topology refinement and selection. The proposed set of techniques can also be employed to complement library-based numerical search methods [21, 23]. They offer the support to systematically update the library with novel, designer-trusted structures obtained either from

current publications or through combinations of existing building blocks, hence increasing the diversity of topologies explored by these tools.

This dissertation is organized as follows. In Chapter 2, a set of metrics from general design science are applied in the context of analog circuit design. The study is aimed at getting a better understanding of the features that define the uniqueness and variety of a design. The methodology illustrates differences and similarities between circuits at various conceptual levels, such as principles of operation, and is applied to multiple design sets that include current mirror, transconductor, and amplifier circuits. In Chapter 3, an automated technique is presented to extract the common and distinct analog circuit nodal features. An ordered node clustering representation is built for describing the design space for a population of analog circuits. Chapter 4 extends the techniques and proposes a systematic method to compare analog circuits in terms of both electrical behavior and performance trade-offs. The method generates comparison data which captures the symbolic performance constrains, limitations, and advantages specific to dissimilar features of the analyzed circuits. Chapter 5 introduces the prototype framework for modeling the analog circuit design feature variety. The structure expresses symbolically the design features at different levels of abstraction and includes systematic mechanisms that can create new solutions. Case study examples of analog circuit topology synthesis procedures using cause-effect reasoning enabled through the proposed techniques are given in Chapter 6. Conclusions are presented in Chapter 7.

Chapter 2

A Study on Measuring the Uniqueness and Variety of Analog Circuit Design Features

Analog circuit design activity is a less formalized process, in which the main source for innovation is the designer's ability to produce new designs by combining basic devices, sub-circuits, and ideas from similar solutions. There are few systematic methods that can fuse and transform the useful features of the existing designs into new solutions. Developing new design techniques that can combine the existing design features requires metrics that describe the uniqueness and variety of the features. The study presented in this chapter evaluates for analog circuits two such general-purpose metrics proposed in [1, 2]. Three case studies are discussed on using the metrics to characterize the design features of current mirrors, transconductors, and operational amplifiers. The two metrics and the presented study is useful in producing an overall characterization of analog circuit features. This can help in enhancing the circuit design process and developing new automated synthesis tools that can explore more solution space regions that are likely to include novel design features.

2.1 Introduction

An intriguing approach towards developing a theory on creative circuit design is to formalize a computational model that captures the process of feature combination and transformation in circuit design. This model would be based on the main cognitive steps of design innovation, such as expanding and contracting the active conceptual space, imposing a new context on a solution, similarities, and deconceptualization [29–31]. As in other engineering domains, like mechanical engineering design [1,2], the core of the model would include a set of metrics that can accurately express the uniqueness and variety of the design features of the circuits implementing various specifications.

There is currently few work on metrics that describe the uniqueness and variety of design features. Research in design science has recently proposed new metrics used mainly in mechanical engineering [1]. The metrics characterize both the frequency and variety of the features of an individual design as well as a set of designs. Enhancements to the original metrics have been subsequently proposed to increase the scope of the metrics [2]. Alternatively, the new features of a design also depend to a significant degree on the characteristics of the design flow. Many engineering systems are designed through multiple iterations that involve parameter optimization and technological changes [32]. Concepts of creative design have been explored in evolutionary algorithms literature [33, 34] to illustrate that Genetic Programing (GP) techniques can rediscover (from scratch) well-known structures, invent patentable circuit topologies, and include mechanisms similar to those involved in human innovation. Design science research focuses on the human innovation process in an effort to determine the conditions that help generation of solutions with novel yet useful features [32, 35], predict the potential success of a new design feature [36], and characterize ideation effectiveness through objective measures [1, 2].

While such design feature-related metrics are general purpose, there have been no known attempts to study the effectiveness of the metrics in describing the uniqueness and variety of the features of various analog circuit designs. Analog circuits have important differences compared to the engineer-

ing designs discussed in the literature, e.g., they are built from tightly coupled building blocks, there are strong correlations between the overall performance of the design and the parameters of the building blocks, and design reuse is an important design strategy.

This chapter presents a study of the uniqueness and variety of the design features present in popular analog circuits, like transconductors and operational amplifiers, by adapting and applying the related metrics developed by the design science community [1, 2]. The characterized features refer to topological structures for implementing physical principles (i.e. saturation, triode or sub-threshold), working principles (e.g., voltage or current biasing), and embodiment principles (like differential or pseudo-differential). The metrics were applied to a set of circuits that was selected from the recent circuit design literature. In contrast to [1] and [2], the metrics were also computed to study the evolution of their values over time. This is important to understand the robustness of the metrics, e.g., their capability to detect early the most novel and unique design features, and to understand the points in time when new design features are more likely to occur. Instead of being applied to the entire set, the metrics were computed for subsets of circuits, in the chronological sequence of their publication. Such clusters include the circuits published at short intervals in time. The analysis also studied the evolution of the metric values depending on the fabrication process of the circuits. The design features of a set of automatically generated circuits has also been analyzed in an attempt to understand the capability of automated synthesis methods, like Genetic Algorithms, to produce novel, yet efficient designs.

Characterizing the uniqueness and variety of circuit design features can improve the design process by pointing out the main benefits of the features, and the capability to their reuse for other problems. The design set variety can indicate the fraction of the design space that has been explored, and can suggest "directions" along which new design features might be located. The two metrics can act as diversification strategies in situations for which traditional solutions are not sufficient. It is also expected that, on the long run, the metrics can help in better understanding the circuit design process,

developing more systematic circuit design methods, better ways of educating young designers, and lead to superior CAD tools.

The chapter has the following structure. Section 2.2 describes the metrics used in evaluating the uniqueness and variety of design features. Section 2.3 presents the analysis performed for three types of analog circuits, current mirrors, transconductors and operational amplifiers.

2.2 Metrics for Design Feature Characterization

This section presents the adaptation for analog circuit design of two metrics proposed in the literature [1, 2] to measure the uniqueness (frequency of occurrence) of the features of a design, and the variety of the features of a design set.

2.2.1 Design Feature Uniqueness

Shah, Smith and Vargas-Hernandez suggest that the novelty of a design (not only circuit design) can be characterized by the frequency of its features appearing in other designs too [1]. They propose a metric, called design novelty measure, defined as follows:

$$MU_i = \sum_{j=1}^{n} (f_j \times S_j) \tag{2.1}$$

where n is the number of features of the design, f_j is the weight of feature j, and S_j is the novelty index of feature j. The novelty index of an individual feature is given by:

$$S_j = \frac{T_j - C_j}{T_j} \times R \tag{2.2}$$

where T_j is the total number of designs from the investigated set having feature j present, and C_j is the number of designs from the set using the same feature's implementation as the currently evaluated design. The term R normalizes the

index value to the desired range $[0, R]$. For example, if the metric is to score circuits on a scale $[0, 10]$, the normalizing factor is $R = 10$. If the scores are reported as percents, the value is $R = 100$.

This approach to ranking the uniqueness of a design is similar to metrics used to quantify the scientific research impact. For example, the h-index [37] correlates citation counts with the number of publications to provide an estimate of both productivity and impact of an author. Similar techniques are also used in Google's PageRank algorithm [38]. The method counts the number of links to a webpage in correlation with the rank of the webpages where these links appear to estimate importance.

In this work, we applied equations (2.1) and (2.2) to characterize the topological diversity of analog circuits. This allows ranking an individual circuit based on the uniqueness of its design features, as compared to the features of a set of known solutions for the given design problem. In our work, the design feature uniqueness metric is evaluated using equations (2.1) and (2.2) to compute the frequency of occurrence of all topological structures that implement different features, such as the design's physical principles (i.e. saturation, triode, sub-threshold), working principles (e.g., voltage and current biasing), and embodiment principles (like differential and pseudo-differential). Unique features have high scores while common features have low scores.

Example: Let's assume that in the set of twelve circuits with all having a bias feature, four circuits utilize current bias, and eight circuits implement voltage bias. For the normalizing factor $R = 10$, this results in the following uniqueness indexes for the specific biasing features:

$$S_{bias=current} = \frac{12 - 4}{12} \times 10 = 6.66$$
$$S_{bias=voltage} = \frac{12 - 8}{12} \times 10 = 3.33$$

The more often used voltage bias feature has a lower score as compared to current biasing, thus the related circuits have higher topological uniqueness scores according to equation (2.1).

For circuit design, the weights f_j in expression (2.1) describe the significance of the features with respect to the design specification and the hardness of certain requirements. Features in the processing and control paths of a circuit are individually scored, providing greater freedom in selecting possible solution priorities. The processing path represents the structures implementing the main circuit functionality (e.g., the amplification functionality of an amplifier circuit) and the control path describes the structures that enable the operation and adjust the characteristics of the processing path (i.e. the compensation and biasing circuitry of an amplifier circuit). For example, designers may opt to search for less-used control structures while utilizing conventional implementations for the processing path of a circuit by properly adjusting the respective weights in equation (2.1).

Example: Let's consider the design of a moderate gain amplifier but with a high linearity of the gain. The gain factor is determined by the features of the circuit's processing path, and the gain linearity is mainly set by the features of the control path. The design challenge is to identify the control structure that can achieve the linearity requirement rather than to search for processing path features that satisfy the less stringent gain requirement. This can be addressed by properly adjusting the weights f_j in expression (2.1). For example, for two amplifier circuits, $A1$ and $A2$, let's assume the following indexes S_j (with normalizing factor $R = 10$):

$$\begin{aligned} S_{processing(A1)} &= 9 \\ S_{processing(A2)} &= 1 \\ S_{control(A1)} &= 2 \\ S_{control(A2)} &= 8 \end{aligned}$$

The values show that implementation $A1$ uses a unique feature for processing and a common feature for control. Circuit $A2$ has a common feature for the processing path but a rare control path implementation.

Using equal weights f_j in (2.1) yields:

$$MU_{A1} = \frac{1}{2} \times 9 + \frac{1}{2} \times 2 = 5.5$$
$$MU_{A2} = \frac{1}{2} \times 1 + \frac{1}{2} \times 8 = 4.5$$

Even though exploring novel control structures is likely to offer greater benefit for the given problem, for equal weights ($f_j = 1/2$), the overall score of circuit $A1$ is higher due to the unique topological features of its processing path. By adjusting the weights to $f_{processing} = 1/3$ and $f_{control} = 2/3$ to reflect the higher significance of the control path in achieving the harder requirement, the two scores become:

$$MU_{A1} = \frac{1}{3} \times 9 + \frac{2}{3} \times 2 = 4.33$$
$$MU_{A2} = \frac{1}{3} \times 1 + \frac{2}{3} \times 8 = 5.66$$

which suggests that circuit $A2$ offers new topological structures (in the control path) that are more likely to address the linearity requirement of the specification.

2.2.2 Design Set Variety

The variety metric proposed in [1] ranks a set of designs (not necessarily circuit designs) based on the diversity of the features that the designs implement. The variety metric is computed using a hierarchical representation called genealogy tree [1]. The hierarchy in Figure 2.1 results if the tree representation in [1] is adapted for MOS transistor circuits. It has four levels: (i) physical principles level (e.g., saturation, triode, and sub-threshold), (ii) working principles level (e.g., current bias and voltage bias), (iii) embodiment level (e.g., differential, pseudo-differential and single-ended), and (iv) details level (e.g., transistor sizing). Each node indicates the number of designs (of the set) that share the specific feature. Separate hierarchical representations are formulated for the processing and control paths of the circuits to express the variety of

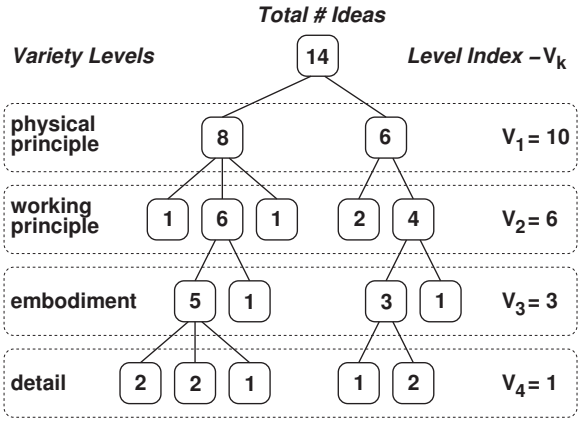

Figure 2.1: Genealogy tree for variety metric used in [1]

the topological features of the two paths.

Based on the genealogy tree representation, the variety metric of a design set is defined as follows [1]:

$$MV_i = \sum_{j=1}^{m} (f_j \times \frac{\sum_{k=1}^{n} (V_k \times b_k)}{MAX_V}) \times R \tag{2.3}$$

where n is the number of levels in the genealogy tree, and b_k indicates the number of branches at level k. m is the total number of features, and f_j is the feature's weight in the overall variety score. Similar to expression (2.1), the weights are selected depending on the significance of the feature in meeting the design requirements. The constant R normalizes the variety score to a desired range.

Parameter MAX_V is the set's maximum achievable variety [1]. This value is the variety score of a hypothetical design set formed of the same number of solutions as the examined set, but in which each circuit implements different features at each level of the representation. Hence, MAX_V is an upper bound of the design space expressed by the analyzed set of designs. MAX_V value can be determined as follows [1]:

$$MAX_V = N \times \sum_{k=1}^{n} V_k \tag{2.4}$$

where N is the total number of circuits of the current set.

The term V_k, called variety index, is a weight associated to each level of the genealogy tree to estimate the total number of detailed implementations (described as leafs in the genealogy tree) that can be produced starting from a node of that level. Figure 2.2(a) indicates the fixed V_k values used in [1]. Note that design differences at higher levels have a greater contribution to the design set's variety score as they can potentially originate more detailed implementations. Also, two circuits are rated as being very different, if they differ mainly according to features at the higher levels, e.g., operation principles. The transistor's region of operation can be considered as the main differentiating attribute as it decides the transistor equations guiding the design process. At lower levels, variations, such as differential or single-ended solutions, have less impact as often the same circuit topology can be realized in either configuration. Furthermore, the differences between variety index values at consecutive levels is progressively smaller as we proceed from physical principles to details.

Two important limitations of the tree representation in [1] refer to the fixed number of levels in the genealogy tree, and the general, thus potentially ambiguous, definition of the levels. Different design problems may require a more precise definition of the levels. Also, more than four levels are possible. To address the limitations, a new approach has been proposed in [2]. It considers genealogy trees with variable number of levels, depending on the design problem. This is important since it offers greater design flexibility by allowing to score higher design features that are more important for a problem. As explained in [2], a representation supporting a variable depth variety can be produced by assigning a binary-weighted variety index at each level in the hierarchy (V_k in equation (2.3)). For example, in Figure 2.2(b), each node of the genealogy tree can have maximum two children, hence $V_k = 2^{n-k}$.

To better address circuit design, a simple modification is to adopt a graph description instead of the tree representation. Through analysis of the two genealogy trees for different analog circuits, we noticed that the tree representations in [1] and [2] do not allow circuits with different physical principles

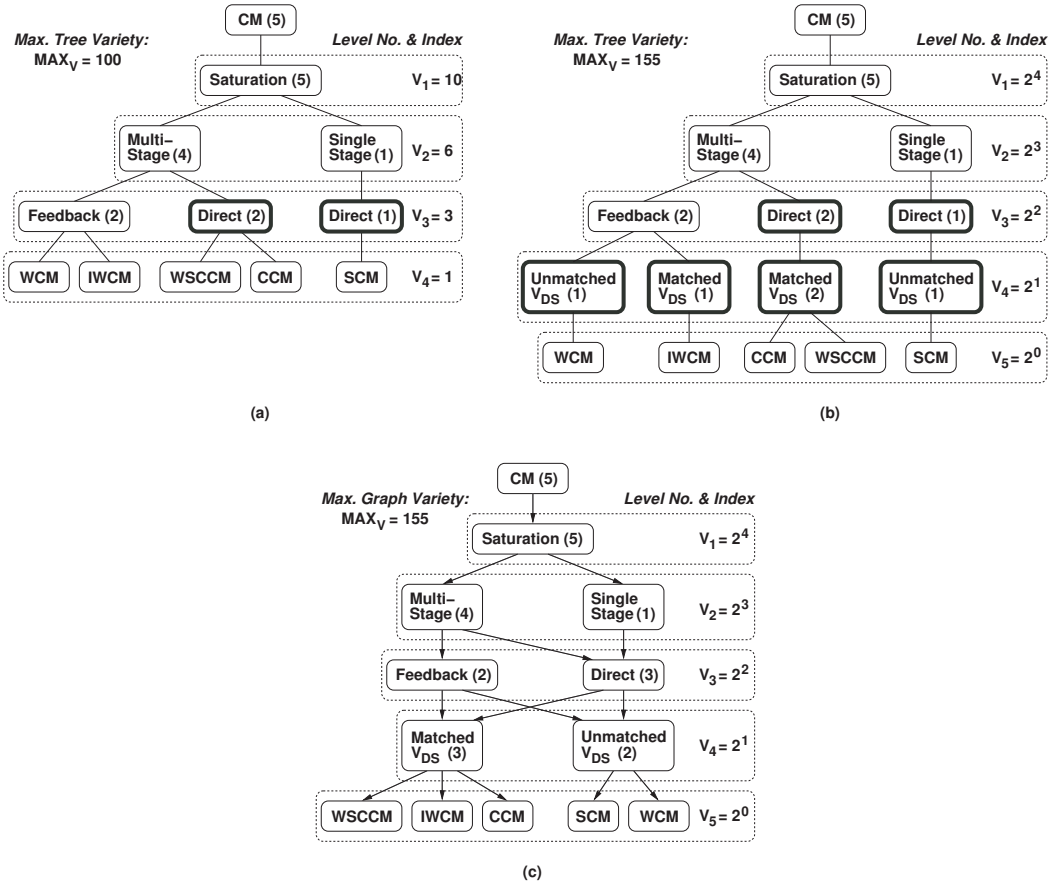

Figure 2.2: Variety representations for a 5 current mirror circuit set: (a) genealogy tree with fixed number of levels [1]; (b) genealogy tree with variable number of levels and binary weighted level indexes [2]; and (c) directed graph with variable number of levels and binary weighted level indexes (highlights show the nodes replicated on different tree branches)

to share the same working principles, or any other lower level features. From a description point of view, having shared features across different principles requires duplicating the same nodes on different branches of the tree. This complicates the structure, and distorts the variety metric in equation (2.3) as the same features are duplicated in the genealogy tree.

A representation similar to the directed variety graph is used in [23] to organize a hierarchical building block library for single-stage and two-stage amplifiers. Starting from the highest level in the hierarchy (differential am-

plifier), amplifier building blocks are presented (e.g., input stage), followed by further subdivision into smaller blocks (e.g., differential pair and load) with alternative options (e.g., folded cascode or simple cascode). Implementation details are progressively added until devices are reached (e.g., resistor, NMOS). The hierarchical library captures the embodiment and implementation details of a design.

The variety representations studied here extend the concepts to include additional semantic levels. For example, design variety can be characterized with respect to physical principles such as designs using transistors operating in saturation, triode, or subthreshold. Different principles of operation can also be captured, for instance current mode (current feedback) or traditional voltage amplifiers. This is important since scaling and changes in fabrication technologies impose tighter constraints on analog circuits (e.g., shrinking voltage headroom) and force designers to explore alternate circuit design principles to meet performance. An example is the unique body-biasing strategy used in [39] for low power applications. The organization of the amplifiers in [23] falls in the class of circuits operating in saturation (as physical principle) and being voltage amplifiers (as operation principle) and mainly captures the details of the structures employed in this subset of designs. This perspective on detailed structures is also apparent from the precise calculation of the total number of possible topologies which can be instantiated through the hierarchical library of building blocks [23]. This is equivalent to the variety score of the lowest level in our representation which consists of the circuit netlists. In addition, the metric analyzed in this work also considers, with progressively increasing weights (V_k), the importance of conceptual principles which differentiate analog circuits. The mechanism allows a more comprehensive characterization of the variety of features present in collection of designs.

The design variety representation offers the flexibility of characterizing different analog circuit features. This aspect correlates well with common designer practices. For example, designers will often defer the biasing circuitry design to later stages of the design process and first focus on the main analog circuit functionality. The analysis in the following section uses this concept to

construct different variety representations for processing features (main functionality) and control features (biasing and other structures that support main functionality) for complex circuits like transconductors and amplifiers.

In our work, we used the same variety metric formula for the graph representation as for the two tree representations with the modification that parameter b_k in equation (2.3) is now the number of incident edges at level k. Also, $V_k = 2^{n-k}$.

Example: Figure 2.2 exemplifies the three descriptions for a set of five current mirror circuits: (1) simple current mirror (SCM), (2) cascode current mirror (CCM), (3) wide swing cascode current mirror (WSCCM), (4) Wilson current mirror (WCM), and (5) improved Wilson current mirror (IWCM) [40]. For each node, the number of circuits using that particular feature is shown in brackets.

Figure 2.2(a) shows the representation from [1] for the circuit set. The number of levels is fixed to four, and due to the tree representation, nodes are duplicated at level three to fully capture the set. Duplicated nodes are highlighted. Physical principles are the operation region of the transistors, working principles are the number of stages, embodiment is determined by the specific signal path implementation, and finally the detail level describes the five individual solutions. Figure 2.2(b) depicts the tree representation from [2]. It shows that more levels can be introduced in the tree (V_{DS} consideration), and each level's weight is binary weighted. However, this representation does not address node duplication. Figure 2.2(c) shows the proposed directed graph description for the set of current mirrors. Similar to the other two descriptions, the concept of levels is preserved through the use of directed edges. A variable number of levels with binary weighted variety indexes supports adaptation to specific design requirements. Within the graph, features from different nodes at higher levels can share features at a lower level without node duplication, thus simplifying the description. For example, each signal path from level three can implement each feature of level four without node duplication.

Example: For the current mirrors in Figure 2.2(c) and a normalization factor $R = 10$, the set's variety metric can be computed as in equation (2.3):

$$MV = 10 \times \frac{1 \times 2^4 + 2 \times 2^3 + 3 \times 2^2 + 4 \times 2^1 + 5 \times 2^0}{5 \times (2^4 + 2^3 + 2^2 + 2^1 + 2^0)} =$$

$$= 3.68$$

The variety metric can offer insight about the potential solution space, and how much of this space is covered by a set of designs. The number of edges and nodes in the variety graph characterize the number of considered design alternatives. Higher variety scores for equation (2.3) result when more distinct circuit features are considered for a fixed number of designs in the set, hence the tree (graph) is more ramified. The set's maximum achievable variety, MAX_V, can be interpreted as a bound of the size of the solution space, since it considers the extreme case when no circuit features are shared at any level of the variety graph. The solution space increases with the number of levels in the variety graph and with the weights V_k describing the alternative features available for level k.

The genealogy trees and variety graphs in this chapter are manually constructed by the designer. However, problem-specific genealogy trees could be automatically produced using techniques inspired by classification methods based on decision tree induction [26]. The methods construct hierarchical classifiers by selecting short sequences of features (attributes) that offer the least randomness in the classification scheme. The attributes of the higher hierarchical levels are those that partition a design set into separate subsets, so that most designs are placed into the right categories. Hence, the selection scheme can serve to identify the defining features of designs. Specific priority functions, such as entropy gain [26], can be utilized for selection. The features at the higher levels of the genealogy tree have higher entropy gain because there are fewer alternatives as compared to the lower levels, and the solutions are grouped into few, distinct subsets (e.g., principles level has three alternatives, saturation, linear, and sub-threshold). At low levels, design set diversification

increases to a point where each individual solution forms its own category (e.g., the individual sizing of each circuit design). This has the smallest entropy.

2.3 Design Feature Characterization for Analog Circuits

This section presents the results for applying the two metrics, design feature uniqueness and variety metrics, to state-of-the-art circuits found in the related literature. To study their versatility, the metrics have been used for three different circuit design problems: design of (1) current mirrors, (2) transconductors, and (3) operational amplifiers.

2.3.1 Current Mirrors

Current mirrors are basic building blocks in many analog circuit design solutions. Ideally, they produce an exact copy of the input current at the output, while supporting wide output voltage swings. A large output impedance is also required in many applications. Five representative current mirror circuit topologies were used for the analysis: (1) simple current mirror (SCM), (2) cascode current mirror (CCM), (3) wide swing cascode current mirror (WSCCM), (4) Wilson current mirror (WCM), and (5) improved Wilson current mirror (IWCM) [40].

Before applying the two metrics, we selected the following features based on which the metric values were computed for current mirrors: (1) single or multi (cascode) stage output, (2) direct or feedback-based operation, and (3) precision enhancement through matching of V_{DS} voltage between the input and output stages.

The experiments determined the uniqueness of the circuit design features. The results are shown in Table 2.1, in decreasing order of the scores. The computation was performed using equation (2.2), and with a normalizing factor of 10. The most common feature in the design set is multi-stage implementation, while single-stage implementation is the rarest. Next, each

Table 2.1: Individual feature uniqueness scores for current mirrors

Circuit Attribute	**Attribute Uniqueness**
Single stage	8
Feedback	6
Unmatched V_{DS}	6
Direct	4
Matched V_{DS}	4
Multi-stage	2

Table 2.2: Design uniqueness scores for current mirrors

Current Mirror	**Uniqueness Score**	**Rank**
SCM	6.00	I
WCM	4.66	II
IWCM	4.00	III
CCM	3.33	IV
WSCCM	3.33	IV

topology's uniqueness score was computed using equation (2.1) with the same weight ($f_j = 1/3$) for each feature class. The results are presented in Table 2.2.

The score rates the SCM topology as having the most unique features among the features of the investigated design set. While most topologies employ multiple stages (4 out of 5) and match V_{DS} (3 out of 5) in an effort to improve performance, the SCM circuit does not use these features. Hence, it has the highest uniqueness score. In contrast, more advanced circuits (e.g., WSCCM and IWCM) score lower on their uniqueness since they use the most common features in the design set. Thus, they are lagging behind the simpler implementations, i.e. WCM. However, an SCM circuit may have reduced applicability in real-life applications because of its lower precision and output impedance. This suggests that the design feature uniqueness metric must be considered together with circuit performance, especially in the final design stages when the focus is set on solution usefulness.

Another observation is that the feature-oriented metric does not consider the specific time instance when the circuits where actually discovered. At the time of its discovery, WCM circuit was probably the first current mirror with feedback. At that moment, this feature's uniqueness index would have been $S_j = \frac{N-1}{N} \times 10$, where N is the number of members in the design set, showing that the index value is high even when few solutions are considered. For $N = 3$, the index is 6.66. This suggests that any design feature-related metric should refer to the particular time at which a circuit was introduced, and not only to the cumulative comparison of the circuit within the set of similar designs. The WCM's popularity indicates its utility, thus the high impact of this design. Furthermore, WCM enabled the emergence of more improved circuits, like IWCM. This suggests that future extensions of the feature-related metrics must also express the potential of a new design feature to originate future modifications.

The variety metric rating of the design set (equation (2.3)) requires building the variety graph for the set of current mirrors. For simplicity, the same set of attributes were considered as for computing the feature uniqueness metric. However, note that the representation supports definitions of graph levels, which can be different from those for the feature uniqueness. This offers flexibility in focusing the circuit feature-related scores on different aspects, hence supporting broader design space explorations and analysis. The current mirror set variety graph is shown in Figure 2.2(c). The level order is decided by the designer based on the circuit aspects desired to have a higher influence in the overall variety metric. The variety score, given by equations (2.3) and (2.4), is equal to 3.68. The small value compared to MAX_V suggests that, potentially, solutions with other attributes might exist in the solution space, and these solutions have not been considered yet. However, a small variety in conjunction with poor performance indicates that the explored solutions are poor, and thus not considered for implementation. With respect to the impact of the level order on the variety score, note that the variety score remains unchanged if the number of nodes per level and the number of a node's children are the same for the different levels. For example, there is

only a minor change in the variety score (from 3.68 to 3.8), if the level capturing the number of stages (level 3 in Figure 2.2) is swapped with the level considering V_{DS} (level 1). Besides, some levels tend to have a fixed position because of the nature of their related features. For example, features like V_{DS} matching refer to individual or small groups of devices, hence relate more to details, while features like feedback structure impact larger groups, thus are more *global*. In the hierarchy, the more global features are placed at higher levels than the features of the individual devices (as shown in Figure 2.2(c)). If the levels differ significantly in terms of their number of nodes and their children, then multiple variety scores can be computed for different orderings of the hierarchy levels.

2.3.2 Transconductor Circuits

The design feature uniqueness and variety metrics were then calculated to rate more complex analog circuits, such as transconductors. A design set of 14 transconductor circuits was selected from the related literature [40–47]. First, the circuits' processing and control path attributes on which the rating is performed were determined. The considered control path features are: (1) current control or voltage control, and (2) direct or feedback control. The processing path considered: (1) transistor saturation or triode operation, (2) single-ended or differential implementations, and (3) single or multi-stage designs. While some of these concepts may not be encountered together within the same application's scope, the feature break-down is used to better illustrate the proposed framework.

Table 2.3 presents the design feature uniqueness scores as computed by equation (2.2). The most common feature of the set is differential processing, while single ended processing is the rarest implementation. Each circuit's uniqueness score was then calculated based on these attributes using equation (2.1), where control and processing paths are uniformly weighted ($f_j = 1/2$). In addition, each of the three processing class attributes were weighted by 1/3 and the selected normalizing factor was 10 to keep the overall score within the range $[0, 10]$. This is required since the processing features

Table 2.3: Individual feature uniqueness scores for transconductors

Circuit Attribute	**Attribute Uniqueness**
Single-ended proc.	8.60
Multi-stage proc.	7.85
Const. voltage ctrl.	7.85
Const. current ctrl.	7.15
Linear proc.	7.15
Feedback current ctrl.	5.00
Saturation proc.	2.85
Single stage proc.	2.15
Differential proc.	1.40

Table 2.4: Design uniqueness scores for linear transconductors

Transconductor Circuit	**Uniqueness Score**	**Rank**
Inverter-based [40] (TR8)	6.19	I
Cross-coupled diff. pairs [41, 43] (TR5)	5.59	II
Bias-offset cross-coupled pairs [40] (TR10)	5.59	II
Tunable triode-based [47] (TR14)	5.58	III
Triode-based diff. pair [40] (TR11)	5.35	IV
Voltage bias src. coupled pair [43] (TR3)	4.99	V
Diff. pair w/ floating voltage src. [40] (TR9)	4.99	V
Simple diff. pair (TR1)	4.64	VI
Cross-coupled src. degen. pairs [45] (TR7)	4.51	VII
Flipped voltage follower-based [44] (TR12)	4.28	VIII
Tunable diff. pair triode-based [46] (TR13)	4.28	VIII
Source degenerated diff. pair (TR2)	3.56	IX
Adaptive bias diff. pair [41, 43] (TR4)	3.56	IX
Adaptive bias w/ src. degen. pair [42] (TR6)	3.56	IX

are grouped into independent classes, and circuits can simultaneously have attributes of different types. The resulting scores are shown in Table 2.4.

The design feature uniqueness metric expresses the same tendency as for current mirrors: it assigns high scores to circuits which use the least com-

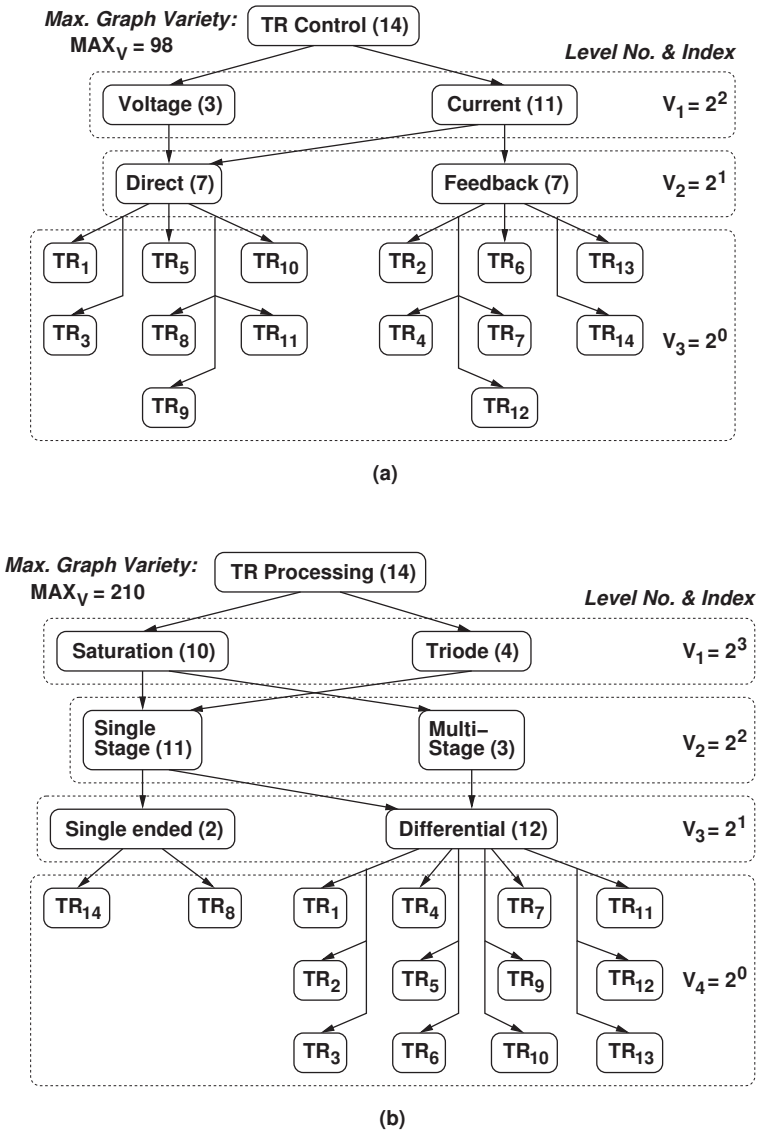

Figure 2.3: Variety graphs for a 14 linear transconductor circuit set: (a) control path variety and (b) processing path variety

mon features of the evaluated design set. As seen from Table 2.4, the circuit detailed in [40], and based on an inverter, has the highest score, suggesting that it includes the most unique features. This circuit uses constant voltage for control (3 out of 14 solutions use this feature), has transistors operating in saturation (10 out of 14), is single ended (2 out of 14), and is a single stage

design (11 out of 14). It is interesting to analyze the rating of an elegant, high-performance solution proposed in [42] (adaptive bias with MOS source degeneration). In terms of the feature uniqueness metric, this design has the lowest ranking of the design set. While the design feature uniqueness metric truly emphasizes unique designs, it is necessary that the metric be considered together with performance attributes in order to correctly assess the impact of different designs.

The control and processing paths' variety graphs are presented in Figures 2.3(a) and 2.3(b), respectively. The number of circuits using the attribute at each node is shown in brackets. The labels TR_i of the leafs show how the individual circuits in Table 2.4 offer the features of the variety graphs. Using equation (2.3), the control path's variety score is 2.86, and the processing path's value is 2.28. This result is counter intuitive based only on Figures 2.3(a) and 2.3(b). The processing variety representation has more nodes and levels, and thus more directed edges in the graph than the control path representation. However, the additional level forces an increase of MAX_V (equation (2.4)), which dominates the variety metric's value. While the control path's maximum variety is equal to 98, for processing, this value is more than double due to the fourth level which introduces only three new edges into the graph.

The average overall variety is 2.57. The variety score of the transconductor set is less than in the case of the current mirrors due to the increase in the number of members from 5 to 14. This yields an increase in the maximum achievable variety while the number of levels and nodes in the variety graph remains relatively constant, except the last detail level, where all solutions are instantiated. The results indicate that the transconductor set is not highly diverse, and the design exploration could be extended towards identifying solutions with other attributes. The result also suggests that the feature characterization scores metrics should not be applied across different sets and circuit types.

2.3.3 Amplifier Circuits

The considered set of amplifier circuits includes single ended, differential, and fully-differential implementations using different frequency compensation and common mode feedback (CMFB) techniques. Both current and voltage mode operation with or without feedforward configurations were selected in the set. Also included are a subset of automatically generated amplifier circuits by means of CAD analog circuit synthesis tool [8]. The broader design space utilized in this study allows for a more comprehensive evaluation of the analyzed metrics.

The evolutionary technique in [8] is based on the unconstrained topology synthesis method from [14]. Without using a library of predefined blocks, the synthesis framework improves the quality of solutions by introducing design knowledge to constrain the Geometric Programming (GP) search. Current flow analysis is employed to correct the population of evolved designs. The technique checks behavior violation and removes or reconnects *faulty* devices. Compared to the original unconstrained solution [14], the correction mechanism checks for correct region of operation of devices and correct direction of branch currents through connected devices. Isolated and floating current branches are identified and eliminated since these structures offer no performance benefits. To further improve the quality of the synthesized solutions, the GP search can be started from a good, designer-given embryonic circuit (i.e., Miller amplifier).

The design feature uniqueness and variety scores are computed for the implementations of the processing and control paths. The considered processing attributes are: (1) voltage or current processing, and (2) the number of amplification stages used for processing (1, 2, 3, or 4 stages). The control path attributes are: (1) frequency compensated or not, (2) employing CMFB or not, (3) implementing feedforward mechanisms (for bypass at high frequency) or simple forward signal propagation, and (4) using body terminal control. The evaluated features were selected to remain consistent with the transconductor attributes analyzed in the previous example.

Table 2.5: Individual feature uniqueness scores for amplifier circuits

Circuit Attribute	**Attribute Uniqueness**
Body biasing ctrl.	9.74
Four amp. stages proc.	9.49
Bypass Feedforward ctrl.	9.23
Current proc.	8.46
Single amp. stage proc.	7.69
CMFB ctrl.	7.44
Three amp. stages proc.	6.67
Two amp. stages proc.	6.15
Compensated ctrl.	5.90
Non-compensated ctrl.	4.10
Non-CMFB ctrl.	2.56
Voltage proc.	1.54
Normal forward path ctrl.	0.77
Non-body biasing ctrl.	0.26

The uniqueness scores of the analyzed features were computed for the 39 circuit set [3–5, 8, 39, 48–71] using equation (2.2). The results are given in Table 2.5. Body biasing is the most unique feature since a single amplifier from the set uses it (AMP29 [39]). The most common feature is a conventional body terminal connection that is used by all other solutions. Using equation (2.1), Table 2.6 shows the design uniqueness scores and the uniqueness ranking for each individual amplifier circuit. Similarly to transconductors, the processing and control features contributed evenly to the circuit's overall score ($f_j = 1/2$). Within each group, the separate attributes were equally weighted, 1/2 for processing and 1/4 for control features. The normalizing factor was 10 in all cases.

The design feature uniqueness metric presents the expected behavior, and correctly singles out the solutions that use the least common features when compared to the rest of the evaluated design set. The highest score is that of a current mode, two stage implementation with compensation and CMFB.

Table 2.6: Design uniqueness scores for amplifier circuits

Amplifier Circuit	**Uniqueness Score**	**Rank**
Solution from [59] (AMP12)	5.83	I
Solution from [63] (AMP18)	5.00	II
Solution *a* from [5] (AMP27)	5.00	II
Solution from [51] (AMP4)	4.90	III
Solution from [39] (AMP29)	4.90	III
Solution from [65] (AMP20)	4.84	IV
Solution from [56] (AMP9)	4.62	V
Solution from [60] (AMP13)	4.62	V
Solution from [4] (AMP15)	4.29	VI
Solution from [70] (AMP25)	4.29	VI
Automated sol'n 6 [8] (AMP35)	3.94	VII
Solution from [55] (AMP8)	3.88	VIII
Solution from [57] (AMP10)	3.88	VIII
Solution from [67] (AMP22)	3.88	VIII
Solution from [66] (AMP21)	3.72	IX
Automated sol'n 8 [8] (AMP37)	3.72	IX
Solution from [52] (AMP5)	3.62	X
Solution from [50] (AMP3)	3.49	XI
Solution from [61] (AMP16)	3.49	XI
Solution from [64] (AMP19)	3.27	XII
Solution from [69] (AMP24)	3.27	XII
Solution from [71] (AMP26)	3.27	XII
Solution *b* from [5] (AMP28)	3.27	XII
Solution from [48] (AMP1)	3.24	XIII
Automated sol'n 5 [8] (AMP34)	3.24	XIII
Solution from [3] (AMP14)	3.10	XIV
Solution from [62] (AMP17)	3.10	XIV
Solution from [68] (AMP23)	3.10	XIV
Automated sol'n 9 [8] (AMP38)	3.10	XIV
Automated sol'n 10 [8] (AMP39)	3.10	XIV
Solution from [49] (AMP2)	3.01	XV
Automated sol'n 1 [8] (AMP30)	3.01	XV
Automated sol'n 2 [8] (AMP31)	3.01	XV
Automated sol'n 3 [8] (AMP32)	3.01	XV
Automated sol'n 4 [8] (AMP33)	3.01	XV
Automated sol'n 7 [8] (AMP36)	3.01	XV
Solution from [58] (AMP11)	2.88	XVI
Solution from [54] (AMP7)	2.88	XVI
Solution from [53] (AMP6)	2.88	XVI

Amplifier 12 [59] has the highest score as it uses the following features: current mode (6 out 39 solution use this feature), two stage processing (15 out of 39) with compensation (16 out of 39), CMFB (10 out of 39), and no feedforward control (36 out of 39), and conventional body connections (38 out of 39). In comparison, solution 15 [4] has a lower score as it uses voltage mode (33 out of 39) through three stage processing (13 out of 39) with compensation (15 out of 39), no CMFB (29 out of 39), feedforward control (3 out of 39), and conventional body connections (38 out of 39). The rare feedforward mechanism present in AMP15 [4], and the body bias in AMP29 [39] greatly increases these solutions' scores. However, the use of more common features for the other design aspects prevents these two designs from having the highest uniqueness scores. Amplifier 11 [58] has a much lower score as it uses more common features: voltage mode (33 out of 39) through two stage processing (15 out of 39) with no compensation (23 out of 39), CMFB (10 out of 39), and no feedforward control (36 out of 39).

The circuits generated by the automated synthesis tool [8] are all ranked in the second half of the set, with the exception of designs AMP35 and AMP37, which have average uniqueness scores. These relatively unique designs employ four amplifications stages, which human designers do not view as *elegant* solutions due to the difficulty and complexity of finding a compensation strategy. For the other automated solutions, 7 out 10 amplifiers rank XIV or XV (XVI being the lowest rank of the set). The produced circuits include only voltage amplifiers, with three stages (6 out of 10), four stages (2 out of 10), and two stages (2 out of 10), with compensation (6 out of 10), and without compensation (4 out of 10). These are among the most popular features of the analyzed circuit set. Note that none uses the feedforward or the body terminal biasing mechanisms.

This analysis suggests that the automated analog synthesis approach used in [8] has difficulties in producing circuits with novel yet useful topological design features. While the produced designs do incorporate some unique and performance-satisfying features, these features are rarely used by designers, thus limiting their usefulness. Among possible reasons is the difficulty to

gain insight on their behavior. This suggests that the capability of reusing a novel feature should be also part of the cost functions used in synthesis. Another interesting corollary is that the correction technique in [8] does not necessarily produce novel solutions but instead encourages specialization of a given pattern. For example, no current mode amplifiers were reported because the set of genetic rules is more likely to evolve only voltage amplifiers out of the initial embryonic circuits. Adjusting only the fitness function cannot address the problem as there is no guarantee that the evolutionary synthesis process actually can produce such design features. Instead, the operators and embryonic circuits should be selected to enhance their potential of creating novel and useful topological structures, thus allowing a more comprehensive design space exploration.

The approach used in [23] trades-off novelty for *trustworthiness* of the synthesized solutions. The GP search is executed on a hierarchical library of well-known, designer trusted building blocks to create topologies which can be readily accepted by designers. With respect to the features considered in this study (Figure 2.4), all designs explored through the original amplifier library in [23] add only leaf nodes to the variety representations (lowest levels). For example, all topologies lie on the voltage→1 stage or voltage→2 stage processing paths. An extension of the method applies small structural novelty by mutating library elements when performance is insufficient [23]. The amount of novelty introduced is minimized using a metric that tracks the frequency of usage of the new structures in a similar manner to the uniqueness metric calculation method described in this Chapter. When relatively complex design transformations are need (e.g., synthesizing current feedback or three-stage amplifiers from a library of only voltage two-stage amplifiers), the basic library needs to be extended to include the adequate designer-specified structures and ensure that useful, trusted designs are also synthesized for these topologies.

The control and processing paths' variety graphs are presented in Figures 2.4(a) and 2.4(b), respectively. The number of circuits using the attribute at each node is shown in brackets. The labels AMP_i of the leafs show how the

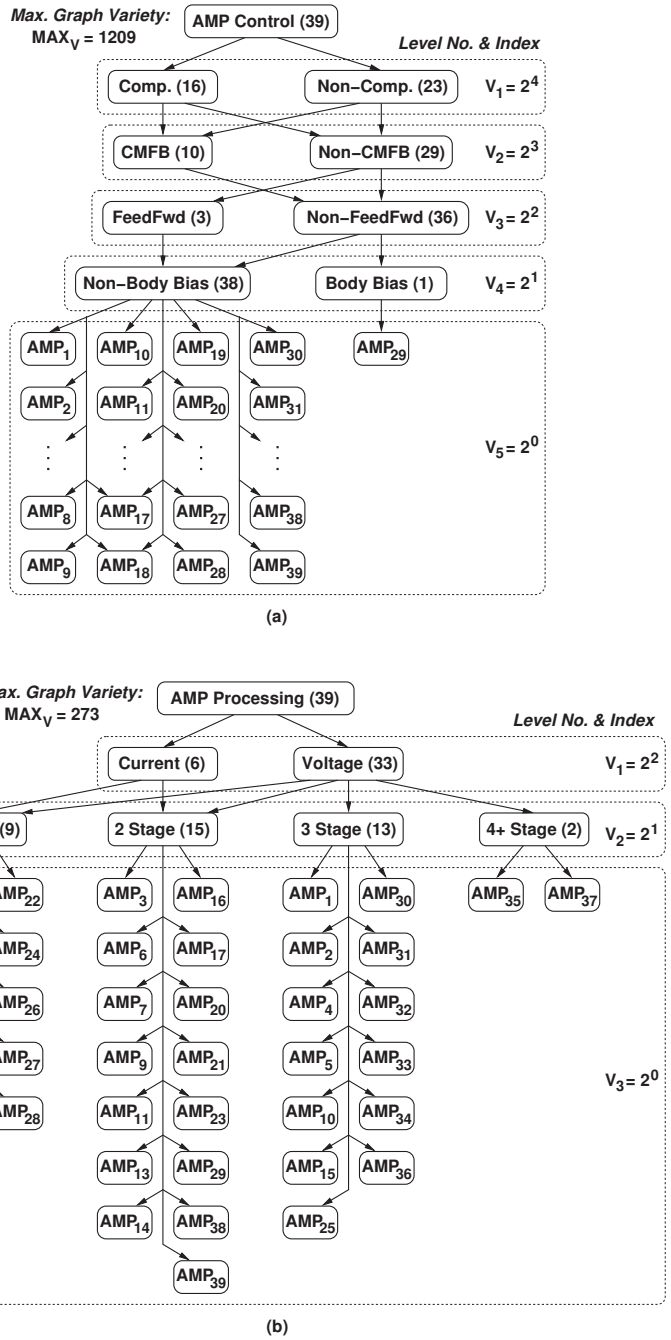

Figure 2.4: Variety graphs for a 39 amplifier circuit set: (a) control path variety; and (b) processing path variety

39 individual circuits in Table 2.6 offer the features of the variety graphs.

The control and processing paths' maximum achievable variety and the design set's variety metric, respectively, were determined using equations (2.3) and (2.4), similarly to the procedure described for transconductors. The entries in Table 2.5 were utilized as graph nodes in the shown level order with their respective variety index values V_k. The processing variety is equal to 2.16 and the control path's value is 1.01 for a normalizing factor of 10. The processing paths' variety is higher than the control paths variety due to the number of levels, nodes, and edges in their respective representations. The processing paths' representation has three levels while the control paths has five. This results in the ratio $\frac{MAX_V(Processing)}{MAX_V(Control)} = 0.23$, and, as previously mentioned, the maximum achievable variety greatly influences a set's variety.

Uniformly weighting in the two values gives the overall variety score of 1.57 for the amplifier circuit set. The relatively low value indicates that only a small fraction of the design space is considered, and more nodes would be needed in the processing and control variety graphs (nodes with more distinct features). Having more solutions in the set increases the maximum achievable variety score, while having only a limited number of nodes (features) in the graph reduces the maximum number of edges present, and thus, the set's variety score. This suggests that the proposed metrics are beneficial in identifying the extent to which the solution space was searched. The metric can be used to guide the design process by expanding the design space, and potentially discovering solution with unique features.

Variety Graph Paths Correlation with Reported Performance

The 29 amplifiers were analyzed to find the correlation between performance and design features (the automatically generated circuits were not considered). The analysis compared the circuits on the same paths in the processing and control variety graphs in Figure 2.4 as the circuits on the same path have the same kind of design features.

The most common path in the processing feature's variety graph is:

$$P_c = \textit{voltage} \rightarrow \textit{2 stage}$$

Ten circuits share this path. The circuits have five different control paths:

$$C_1 = \textit{Comp} \rightarrow \textit{Non-CMFB} \rightarrow \textit{Non-FeedFwd} \rightarrow \textit{Non-BodyBias}$$
$$C_2 = \textit{Comp} \rightarrow \textit{CMFB} \rightarrow \textit{Non-FeedFwd} \rightarrow \textit{BodyBias}$$
$$C_3 = \textit{Non-Comp} \rightarrow \textit{CMFB} \rightarrow \textit{Non-FeedFwd} \rightarrow \textit{Non-BodyBias}$$
$$C_4 = \textit{Non-Comp} \rightarrow \textit{Non-CMFB} \rightarrow \textit{Non-FeedFwd} \rightarrow \textit{Non-BodyBias}$$
$$C_5 = \textit{Comp} \rightarrow \textit{CMFB} \rightarrow \textit{Non-FeedFwd} \rightarrow \textit{Non-BodyBias}$$

The least used processing path is:

$$P_r = \textit{current} \rightarrow \textit{2 stage}$$

Three circuits use the path, and the circuits have two different paths in the control variety graph:

$$C_1 = \textit{Non-Comp} \rightarrow \textit{Non-CMFB} \rightarrow \textit{Non-FeedFwd} \rightarrow \textit{Non-BodyBias}$$
$$C_2 = \textit{Comp} \rightarrow \textit{Non-CMFB} \rightarrow \textit{Non-FeedFwd} \rightarrow \textit{Non-BodyBias}$$

Tables 2.7 and 2.8 summarize the reported performance for the circuits with the most and least common processing feature sets. The rows correspond to the different control feature sets used for the same processing features. The performance of different circuit implementations that share the same control path features is separated in the tables by semicolons. Some performance values are not reported in the papers (marked NR).

The comparison suggests that, for the considered set, the designs with more common features in the processing path (path P_c) offer better performance than those with rare features (path P_r). Micro-power, high gain, and mega-Hertz bandwidth requirements are met by designs of both processing

Table 2.7: Performance of amplifier circuits with common processing features (path P_c)

Control Path	**Supply [V]**	**Gain [dB]**	**BW-3dB [Hz]**	**Power [μW]**
C_1	2.5; 2; 1	20; 45; 42	NR; 62k; 32k	152; 60; 95
C_2	0.5	62	10k	75
C_3	1.8; 1.5	43; 45	32M; 300	6.5m; 3
C_4	1; 1.5; 2.5	28; 14; 17	50M; 20k; 10G	120; NR; 60m
C_5	1.2	NR	NR	NR

Table 2.8: Performance of amplifier circuits with rare processing features (path P_r)

Control Path	**Supply [V]**	**Gain [dB]**	**BW-3dB [Hz]**	**Power [μW]**
C_1	1.8; 3	20; 52	15k; 15k	35; 21
C_2	1.8	15	18M	NR

paths. The implementations on the common path P_c support lower supply voltages. The rarely used processing path P_r does not include any RF amplifiers, while the processing path P_c includes more high-frequency designs. The circuits sharing the same control path present higher average gain and bandwidth for common processing features (path P_c) than for rare processing features (path P_r). However, the less-used design features offer performance benefits customized for certain applications. For example, current-mode processing has the advantage of a relatively constant bandwidth for different gain values. The more commonly-used voltage implementations do not give this advantage. Thus, current-mode amplifiers are well suited for applications where constant bandwidth across a greater gain range is traded-off for the other performance values.

The better performance of circuits with common features might also suggest that, over time, designers have gained more insight on how to exploit

the benefits of these design features. For example, let's consider three circuits that share the same design features, where AMP17 [62] was the earliest solution, followed by AMP14 [3], and then AMP23 [68]. Their performance improved over time, e.g., the supply voltage dropped from 2.5V to 1V while the gain increased from 20 to 42 dB. Similar, trends in performance improvements can be seen also for the circuits with more unique design feature. For example, AMP9 [56] uses a 1.8V supply voltage to achieve a gain of 20dB and bandwidth of 15kHz, while dissipating 35μW. The more recent circuit, AMP13 [60], uses a 3V supply, but achieves more than double the gain (52dB) with the same bandwidth, and a reduced power consumption of only 21μW.

2.3.4 Evolution of the Metrics over Time

The experiments also studied the evolution over time of the unique design features embedded in amplifier circuits. First, the analysis chronologically ordered the designs, and clustered them into six groups, so that designs published about the same time are in the same cluster, and there is a uniform distribution of the total number of designs into groups: (c1) 2001-2005: [4, 5, 39, 62]; (c2) 2006: [3, 50, 59, 65, 68]); (c3) 2008: [48, 51, 55, 63]; (c4) 2009 I: [52, 58, 64, 66]; (c5) 2009 II: [49, 56, 57, 60, 67]; (c6) 2009 III: [53, 54, 61, 69–71]. The metrics were computed recursively for the six clusters: first the metric for cluster 1 (c1) was evaluated, then for both clusters 1 and 2 (c1$\cup$c2), and so on. The last step analyzed all clusters together. We feel that this way of analyzing the circuits emulates closely the process in which the actual circuit designs were developed. The analysis did not consider the automatically generated circuits.

Figure 2.5 presents the design's uniqueness score evolution for five designs from the total 29 designs. The solutions have been introduced into different time-related clusters, and have various uniqueness scores: solutions with high score, i.e. circuits 29 [39] and 12 [59], average score, e.g., circuits 13 [60] and 1 [48], and low score, like design 11 [58]. While some variations in the individual circuit feature uniqueness metric values are noted over time, detailed analysis shows the metric's robustness. The metric identifies

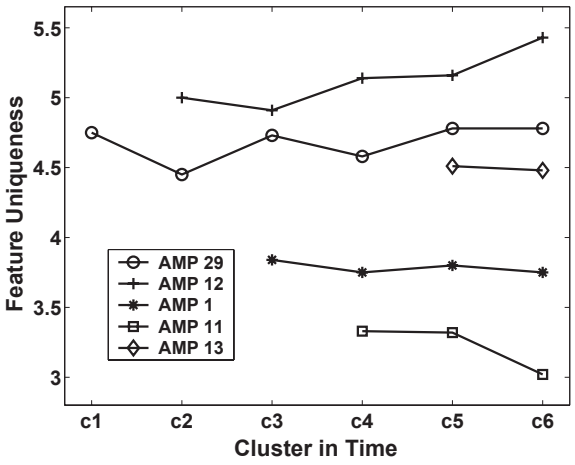

Figure 2.5: Evolution of amplifier circuits feature uniqueness over time

the novel features immediately when they are introduced into the design set. Even if there are value variations across cumulative time clusters, the relative set ranking is preserved. The final results for the clusters are comparable with the results shown in Table 2.6, where the same amplifier circuits are ranked as having the highest feature uniqueness score.

The robustness of the metric is explained by the fact that new design features are rarely introduced, and there is a relatively constant ratio between rare and common features over time. For example, let's consider a feature which is used by 5 out of 30 designs. Its uniqueness index is $\frac{30-5}{30} = 8.33$. Let's consider that at a later point in time two more circuits use the feature, and eight new circuits use a more common feature instead. The new uniqueness index is $\frac{40-7}{40} = 8.25$. The common feature's index changes from 1.66 to 1.75. As long as the features are not equally likely, the relative ranking of the indexes remains unchanged. This is a likely situation considering the reuse of already popular features.

When considering the uniqueness of each cluster over time, the cluster with the highest score is cluster 1 (c1) with the average score of 4.20. The cluster with the lowest value is cluster 6 (c6) with the average uniqueness score of 2.57. The high average score of c1 is explained by the circuit implementations, which all employ a high number of different features. The circuits

in c6 share many features. Nonetheless, the design feature uniqueness metric still manages to identify one design solution with many unique features, and which is included in the low scoring group (solution 25 [70]). However, the comparison of the individual cluster uniqueness with the uniqueness of the set is inconsistent. Taken separately, clusters may not include all the features present in the set of 29 circuits.

Figure 2.5 indicates that the uniqueness scores for the same circuits change over time. Circuit 12 [59] experiences a slight increase in score over time, circuits 1 [48] and 13 [60] have relative constant score, and circuit 11 [58] shows a decrease in score. The change is determined solely by the features that each new cluster brings to the circuit set. Circuit 11's low score is due to its use of the most common features, and circuits 12's high score is given by the use of rare features. Circuit 1 and 13 are characterized by a mix of both types of features. When new clusters are added to the circuit set, the distribution of common and rare features changes. If the new circuits use common features (e.g., because the features are effective), this increases the uniqueness index values for rare attributes and decreases those of the common features. Thus, highly popular design features show a decreasing trend of their uniqueness score (e.g., AMP11), while rare features have an increasing trend (i.e. AMP12).

The variety metric was also computed on the clusters built for the amplifier set. The overall set's variety scores range from 6.75 to 1.77 for cluster 1 (c1), and the cumulative clusters 1-6 ($\cup c_i, i = 1, 6$), respectively. If only detail level entries are added to the variety representation of each cluster, there is a consistent decrease across the intermediate groups: in equation (2.3), the term $\sum_{k=1}^{n}(V_k \times b_k)$ becomes $K_1 + N \times V_n$, where K_1 denotes the constant variety of higher levels. Only the last detail level's contribution ($V_n = 2^0 = 1$) changes with the number of solutions, N. For the set's maximum achievable variety (MAX_V) in equation (2.4), the term $\sum_{k=1}^{n} V_k$ equals a constant K_2. The overall variety becomes dominated by the number N of circuits in the set. For increasing set sizes, the variety drops constantly $(\frac{K_1+N}{N \times K_2})_{(N \to \infty)} \to \frac{1}{K_2}$.

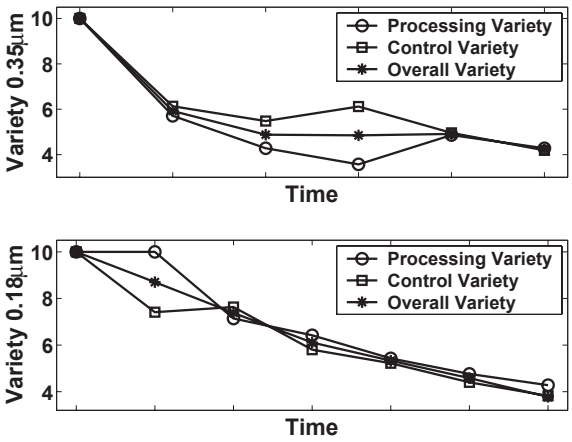

Figure 2.6: Evolution of variety scores for amplifier circuits in $0.35\mu m$ and $0.18\mu m$ process (the scores were computed using seven and six circuits, respectively)

A higher variety is achieved for the initial clusters since all features and the corresponding variety graph's branches are instantiated, while the number of solutions in the set is still small. After clusters 1 and 2 (c1∪c2) are analyzed, the variety graphs for both processing and control do not evolve, since the added solutions bring few or no new features. However, the set's maximum achievable variety increases with the number of members causing the decrease in variety scores for the remaining clusters. This observation suggests that analog circuit design is mostly based on a set of reusable concepts (e.g., library circuits), which designers employ repeatedly. Thus, solutions differ mainly in terms of the lower level details and performance characteristics of the specific application.

We have also investigated the evolution of the variety metric depending on the process used for the circuits. The 29 amplifier circuits are implemented in five different CMOS technologies, with most circuits using $0.35\mu m$ and $0.18\mu m$ process. There are seven circuits for $0.35\mu m$ process, and six for $0.18\mu m$. Figure 2.6 shows the plots for the variety of the control and processing paths, and the overall variety score. The normalizing factor was 10. Due to the smaller number of circuits in each group, each time instance adds only one design to the set.

The overall variety scores decrease over time for both processes. This is due to the growing number of members in each group (hence, increasing the maximum achievable variety) while there are relatively few new features added to the respective variety graphs. The circuits in $0.18\mu m$ process exhibit a relatively constant slope decrease, while the circuits in $0.35\mu m$ process show an accentuated decrease in the initial phases followed by a slow decrease for later steps. For $0.35\mu m$ process, the initial drop in variety is because the new design solutions incorporate only one new feature in the control paths and no new feature in the processing paths. Then, new features are suggested for the processing paths, and its variety score increases. Later, the variety of the control paths increases due some new features being added. For $0.18\mu m$ process, both processing and control path variety scores decrease over time at similar rates. The only exception is the second time instance when the processing path maintains the variety value of 10, since the newly added design includes different features at all levels compared the first solution. In contrast, most features of the control path remain the same. The analysis suggests that new design features have been proposed for $0.35\mu m$ process over a longer period than for $0.18\mu m$ process. This is because designs in $0.18\mu m$ process tend to reuse previous features, and there are less new features being proposed.

2.4 Summary

This chapter investigated the uniqueness and variety of the design features of popular analog circuits by using the set of metrics proposed in the design science literature [1,2]. The considered circuits include current mirrors, transconductors, and operational amplifiers. The features refer to topological structures for implementing physical principles (i.e. saturation, triode or subthreshold), working principles (e.g., voltage or current biasing), and embodiment principles (like differential or pseudo-differential). The metrics were also calculated to observe the evolution of the metric scores over time and their dependence on the fabrication process. The metrics were computed for subsets of circuits in the chronological sequence of their publication. The new

features present in automatically generated circuits has been also analyzed.

The analysis indicates that the studied metrics are capable of characterizing the uniqueness and variety of the design features of analog circuits, especially if the metrics are calculated considering the pool of designs that existed when a circuit was published. Popular design features show a decreasing trend in their scores, which starts at a high value but then decreases over time as more on more new design incorporate that feature. In contrast, design features that are not adopted will maintain a high uniqueness score, indicating that they are rarely used in future solutions. This suggests that studying the evolution of the metric values over time offers more reliable insight on the utility of a design feature as it considers not only its uniqueness but also its usefulness for future designs. Moreover, the uniqueness score must be always considered in conjunction with performance to avoid a high ranking of designs that employ novel features but offer poor performance, thus are rarely used. The analysis of a set of synthesized circuits produced through a constrained evolutionary method [8] indicates that the technique is challenged to automatically produce designs with unique yet useful features. The generated circuits tend to have few novel features. This suggests that devising innovation-related design rules for automated synthesis is an interesting area to explore. Moreover, the uniqueness and variety scores of a design set can give insight on the covered solution space, thus can serve to diversify the search towards unexplored areas.

Chapter 3

Analog Circuit Design Space Description based on Topological Matching and Ordered Clustering of Nodal Features

The study presented in Chapter 2 illustrates the importance of accurately describing the uniqueness and variety of design features. This chapter presents a systematic technique to automatically create symbolic ordered feature clustering schemes that express the main similarities and differences between analog circuits. Four separation scores, based on entropy, item characteristics, category characteristics, and Bayesian classifiers were studied to produce clustering schemes that offer insight about the uniqueness and importance of specific design features in setting AC performance as well as the limiting factors of the designs. The experiments consider a large set of state-of-the-art amplifier circuits. The chapter offers a discussion on further using the insight obtained from circuit feature clustering for topology synthesis and refinement methods.

3.1 Introduction

Macromodels are important tools in describing the main features of analog circuits, including (i) mathematical dependencies between output, nodal and input signals and device parameters, and (ii) expressions of performance attributes depending on design variables. The first type of macromodels are usually called structural models, and the latter kind are denoted as black box models. Circuit macromodels have been utilized for many purposes, including fast performance evaluation [27], insight gain into circuit behavior and performance [72], design verification [19], and circuit and system synthesis, including design parameter sizing [13, 73, 74] and circuit topology selection and generation [27, 28, 72].

There are few modeling methods that characterize a population of circuits to indicate the similarities and differences in their topological and behavioral features as well as their impact on performance. However, descriptions of circuit populations can offer a comprehensive presentation of the design space covered by the design set, the flexibility of design features when used under various constraints, and the uniqueness of features in tackling specific requirements. Such insight results by comparing circuits to find common and unique design features, e.g., the similar and distinct symbolic terms of pole and zero expressions. The comparison helps understanding the performance advantages and limitations of a circuit topology compared to another, the performance impact of circuit nodes and their structural connections to other nodes, the conditions under which alternative circuits offer similar performance, and the design aspects that boost or limit the performance of a circuit compared to alternatives. The obtained insight is useful to synthesize topologies, or refine existing circuits to incorporate useful features from other designs or to identify common characteristics that can be reused for broad sets of performance requirements.

This chapter presents an automated symbolic technique for creating models, called ordered node cluster representation (ONCR), that express the main similarities and differences between a set of analog circuits with common functionality. The insights obtained from the representations are the similar

and dissimilar circuit features, including the related topological structures and their symbolic expressions. The modeling method includes three main steps: (i) identifying the possible separation criteria, (ii) analyzing the criteria with respect to their potential of grouping the circuits, and (iii) building ONCRs such that the separation of dissimilar circuits is maximized. In addition, two initial steps that create the symbolic circuit descriptions used for analysis. The chapter studies four separation scores: entropy, item characteristics, category characteristics, and Bayesian classifiers. This chapter offers a comprehensive study for two sets of state-of-the-art amplifier circuits: one using 10 circuits and the other having 50 circuits. A detailed discussion of the application of ONCRs for topology synthesis and refinement methods is also offered.

The chapter has the following structure. Section 3.2 defines the tackled problem. Section 3.3 describes the proposed algorithm for generating ONCRs. Section 3.4 presents experimental results and a discussion of the applications of ONCRs.

3.2 Building a Representation to Capture the Similarities and Differences Between Analog Circuits

Given a set of circuits C_1, C_2, ... C_n, the problem requirement is to build a symbolic description (model) that presents the main similarities and differences between circuits (in a population of circuits) with respect to their structural features and influence on performance. A good description scheme must easily distinguish the circuits, e.g., there should be a minimum number of criteria that separate a circuit from the other circuits in the set with respect to their topological features and performance attributes.

Figure 3.1 illustrates the theoretical formulation of the problem. Three circuits C_i are shown in the figure. Each circuit is described by the set of its nodes $V_{i,k}$. This captures the circuit structure, which is important to understand how similarities and differences correlate to the circuit topologies.

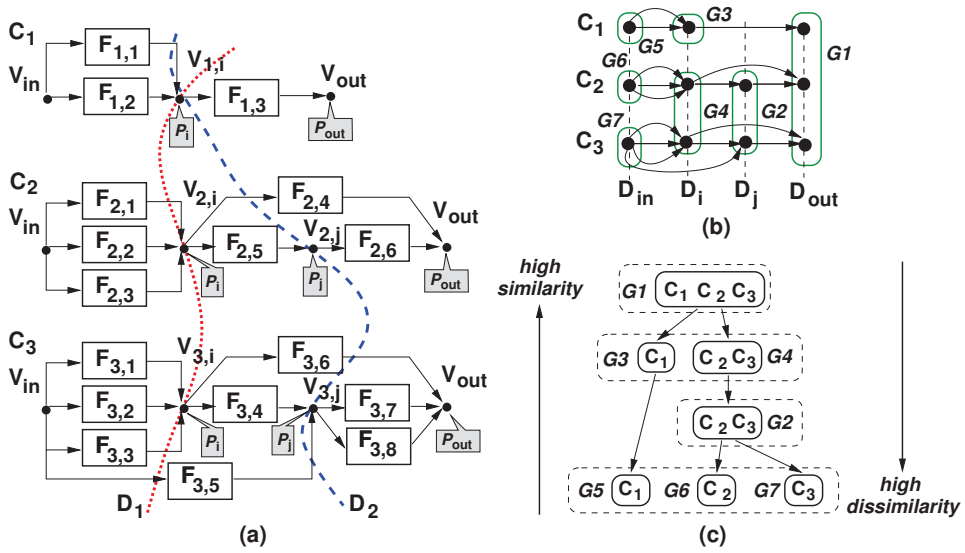

Figure 3.1: Theoretical description of circuit feature clustering problem

Nodes are characterized by functions P_k to express the node poles and $F_{k,p}$ to describe the coupling between nodes. The symbolic functions are related to AC performance, like pole positions and separation, and magnitude and phase response. Expressions P_k and $F_{(k,p)}$ are continuous functions in the s-domain. Functions $F_{(k,p)}$ describe the AC domain coupling between nodes and correspond to the arc labels in Figure 3.1(a). Functions $P_k = R_k/(1 + sR_kC_k)$ characterize the poles at each circuit node, where R_k and C_k are the symbolic expressions for the resistive and capacitive components, respectively.

Producing a feature clustering scheme for the set of circuits C_i must (i) identify the nature of criteria used in finding similarities and differences between the circuits and (ii) find the topological features that realize the similarities and differences. As shown in Figure 3.1(c), the two objectives create a scheme in which the ordered levels correspond to the identified criteria and the node groups (G_i) at each level represent clusters of nodes with similar features. In addition, a reliable separation metric must be available to produce clusters that characterize the amount of dissimilarity between circuits.

There are always more criteria sets possible to distinguish circuits. For example in Figure 3.1(a), the characteristics of the nodes $V_{1,i}$, $V_{2,i}$ and $V_{3,i}$ along curve D_1 can be used for distinguishing the circuits. Alternatively, nodes $V_{1,i}$, $V_{2,j}$ and $V_{3,j}$ along curve D_2 could be used for clustering. The two curves lead to finding different common features for the circuits, e.g. similar symbolic expressions for their poles and coupling. In the first case, node $V_{1,i}$ in circuit C_1 forms a different cluster as it has different coupling to its subsequent node. Note that all possible criteria sets (corresponding to a curve D_k) define the space for clustering. Figure 3.1(b) illustrates all circuit nodes with similar features identified for the curves D_k. The similar nodes are circled together and form a group G_i of similar features, with respect to their pole and coupling to other nodes expressions.

The representation in Figure 3.1(c) aggregates the feature similarity and dissimilarity information for all nodes in the three circuits. This representation is called ordered node cluster representation (ONCR). ONCRs are directed graphs, similar to concept variety from Chapter 2. The upper levels of ONCRs correspond to curves D_k with high similarity of the corresponding node features. The low levels represent nodes with dissimilar features. For example, the output nodes of the three circuits have similar features as their pole expressions are matched. The input nodes are dissimilar as their coupling is different. If a circuit has nodes at different levels of the scheme, then the levels and corresponding groups are joined by a directed edge to indicate the ordered nature of the representation with respect to feature similarity.

The common and dissimilar node features presented in the representation are related to the relevant performance attributes $Perf_i$. For example, for AC domain, the shared node features represent the common symbolic expressions of the poles at the nodes, and the analyzed performance $Perf_i$ defines the position of the common pole on the magnitude and phase response of the circuit.

Example: The impact of a node depends on the nodal poles and coupling to all other nodes in the circuit, e.g., all functions $F_{(k,p)}$ through which the node is connected to the rest of the circuit. For example, the impact of

node $V_{1,i}$ of circuit C_1 in Figure 3.1(a) is characterized by functions P_i (pole expression) and $F_{1,3}$, the coupling to node V_{out}, and functions $F_{1,1}$ and $F_{1,2}$, the coupling from node V_{in}. The AC performance impact of the node includes the dependency of the circuit's magnitude and phase responses on functions P_i, $F_{1,3}$, $F_{1,1}$ and $F_{1,2}$.

The quality of an ONCR depends on the relevance of the common and distinguishing criteria, including their impact on performance and insight on circuit design, e.g., uniqueness of a criterion in controlling a certain performance attribute and brevity of the related expression [26]. Good distinguishing criteria have short mathematical expressions (which makes them easy to understand), and are unique and important with respect to setting performance attributes.

The problem of constructing ONCRs for a set of circuits was formulated as a circuit node clustering problem. In spite of the smaller size of this problem as compared to typical data mining applications [26], there is a high likelihood of finding clusters of nodes with similar features since topological features (e.g., circuit sub-structures) are often reused in design. New transistor sub-structures are rarely invented as seen from the study discussed in Chapter 2. Hence, it is useful to understand which topological features have been reused in various circuits because it allows to understand the characteristics of the applications in which these features can be included and exploited.

3.3 Analog Circuit Feature Clustering Algorithm

Algorithm 3.1 presents the proposed method to construct the ONCR for a set of circuits. Step (1) constructs the specific circuit representation and Step (2) produces the set of separation curves D_i, which define implicitly the alternative circuit node features that can be used to describe the similarities and differences between nodes. Then, in Step (3), the curves are ordered to reflect any ordering specific to the circuits. For example, the design features describing the signal flow between circuit nodes must be preserved to reflect

Algorithm 3.1 Automated ordered node clustering scheme (ONCR) generation

(1) ***Produce*** the circuit representation
for the considered performance;
(2) ***Produce*** the set of possible classification curves D_i;
(3) ***If*** an ordering criterion exists for curves ***then***
order curves D_i;
(4) ***For all*** curves D_i (following their order)
compute the separation cost for clusters of D_i;
(5) ***For all*** curves D_i in increasing order of their separation cost
build ONCR level by adding nodes for clusters of curve D_i;

that flow, e.g., curve D_i is before curve D_j, if all nodes of D_i have outward edges to the nodes of curve D_j. Step (4) computes the separation (called separation cost) between the groups of nodes of each curve D_i. The curves are selected in increasing separation cost order to produce the next level of the clustering scheme in Step (5). Each entry of the new level represents clusters of similar nodes. The procedure continues with generating the next ordered clustering level based on the remaining curves D_i and the separation criteria used in the scheme.

Next, we describe the circuit representation used for clustering features, followed by algorithm details, the separation criteria used, and a case study.

3.3.1 UBBB Macromodel Structural Circuit Description

The circuit features used in clustering are identified from a structural model of analog circuits, called Uncoupled Building-Block Behavioral model (UBBB) [25]. The models express the symbolic dependency between the circuit topology and the AC behavior of the circuits, including poles at circuit nodes and node coupling. Using the circuit topologies would make clustering more difficult as the dependency is not explicitly represented. This subsection offers a summary of UBBB models, a more detailed description is

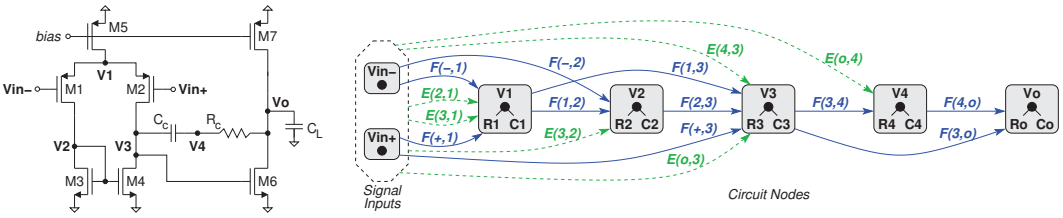

Figure 3.2: Schematic and uncoupled building-block behavioral (UBBB) model graph for a simple two-stage amplifier

in [25]. Note that constructing the UBBB models for circuits corresponds to Step (1) of the procedure in Algorithm 3.1.

UBBB models are directed signal-flow graphs, for which vertices correspond to circuit nodes and their associated pole, and edges capture the signal coupling between nodes. The resistive and capacitive components of poles, and the node coupling (expressed as edge weights) are symbolic expressions of the small-signal parameters present in the circuit at the respective nodes. Figure 3.2 shows a compensated two-stage amplifier and its corresponding UBBB model. All circuit nodes V_i are represented in the model with their resistive (R_i) and capacitive (C_i) components forming the symbolic pole expression P_i of node i. The coupling between two nodes is of two kinds: direct influences between the nodes (denoted as symbolic expressions $F(i,j)$) and decoupled, equivalent influences between signal inputs and other circuit nodes (described as symbolic expressions $E(k,j)$).

The voltage at node V_j is expressed in the s-domain as follows:

$$V_j = \frac{R_j}{1 + sR_jC_j} \times \Big(\sum_{\forall i \in N, i \neq j} F(i,j)V_i + \sum_{k \neq j} E(k,j) \Big). \tag{3.1}$$

Terms R_j and C_j define the pole at node V_j. They are combinations of the transconductance and capacitance parameters of the devices connected at the node.

The direct influence of circuit node i on node j is described in the s-domain by the following expression:

$$F(i,j) = sC_m^{(i,j)} \pm G_m^{(i,j)} \tag{3.2}$$

where $C_m^{(i,j)}$ are the junction capacitances and $G_m^{(i,j)}$ are the terminal transconductance of MOS devices connected to nodes i and j.

Decoupled, equivalent influences result by replacing the cross-coupling (cycles) in the initial coupled model with equivalent influences between AC input signal nodes and other subsequent circuit nodes [25, 75]. In the s-domain, the decoupled, equivalent influences are of the following form:

$$E(k,j) = (sC_m^{(k,j)} \pm G_m^{(k,j)})V_{k,eq}. \tag{3.3}$$

where k is the circuit node where the original cross-coupled dependence originated and j is the influenced node. $C_m^{(k,j)}$ are the junction capacitances and $G_m^{(k,j)}$ are the terminal transconductance of the devices connected to nodes k and j.

Example: The simple example in Figure 3.3(a) illustrates how decoupled, equivalent influences are introduced into the model. Node V_1 (gate) and node V_2 (drain) of the MOS device are cross-coupled, such that V_1 influences V_2 through the edge with expression $sC_{gd} - g_{mg}$ and V_2 influences V_1 through expression sC_{gd}. The coupling between V_2 and V_1 is replaced by an equivalent edge from the *AC Equiv.* node since it is not a valid signal path [75] (drain-to-gate). The expression of this new edge is $E(2,1) = sC_{gd} \times V_{2,eq}$. Similarly, the edge from V_3 to V_2 (invalid drain-to-source) is replaced by equivalent edge $E(3,2) = g_{md} \times V_{3,eq}$ from the *AC Equiv.* node. In general, for a given circuit, the *AC Equiv.* node is characterized by the set of all such decoupled, equivalent influences.

$V_{k,eq}$ in equation (3.3) represents the equivalent voltage of node k when its influence on node j is moved to the input as detailed in [25]. The general

form of an equivalent voltage for p signal inputs is as follows:

$$V_{k,eq} = \sum_{v=1}^{p} \frac{a_{k,n}s^n + ... + a_{k,2}s^2 + a_{k,1}s + a_{k,0}}{b_{k,n}s^n + ... + b_{k,2}s^2 + b_{k,1}s + b_{k,0}} V_{in,v}. \tag{3.4}$$

The symbolic coefficients in equation (3.4) can be found through an iterative process up to the desired degree [25]. They are expressed as follows:

$$a_{k,i}(b_{k,i}) = \sum_{t}(\pm) \prod_{k_i,k_j} [G_m^{(k_i,k_j)}]^{\alpha_k} \prod_{l_i,l_j} [C_m^{(l_i,l_j)}]^{\beta_l}. \tag{3.5}$$

$G_m^{(k_i,k_j)}$ is the transconductance between nodes V_{k_i} and V_{k_j}, and $C_m^{(l_i,l_j)}$ is the transcapacitance between nodes V_{l_i} and V_{l_j}, with $\alpha_k, \beta_l \in \{0,1\}$ and $\sum_{k=1}^{K} \alpha_k = Nr - i$, $\sum_{l=1}^{L} \beta_l = i$. K and L are the total number of $G_m^{(k_i,k_j)}$ and $C_m^{(l_i,l_j)}$ in the model. Nr is the number of circuit nodes.

Example: The output voltage V_o of the model of the circuit in Figure 3.2 is:

$$V_o = \frac{R_o}{1 + sR_oC_o} \times (F(3,o)V_3 + F(4,o)V_4)$$

The pole components of the output node are:

$$R_o = 1/(g_{md6} + g_{md7} + 1/R_c)$$
$$C_o = C_{gd6} + C_{db6} + C_{gd7} + C_{db7} + C_L,$$

The influences of nodes V_3 and V_4 on V_o are as follows:

$$F(3,o) = sC_{gd6} - g_{mg6}$$
$$F(4,o) = 1/R_c$$

The output node of the simple two-stage amplifier is not coupled to the input signal by any decoupled, equivalent influence $E(o,i)$, since it is the last node in the decoupling sequence.

The decoupled, equivalent influence $E(2,1)$ between circuit nodes V_2 and V_1 in Figure 3.2 is equal to:

$$E(2,1) = g_{md1} \times V_{2,eq}$$

If, for brevity, only degree 1 is considered in expression (3.4) then the decoupled, equivalent voltage $V_{2,eq}$ is computed in the form:

$$V_{2,eq} = \left(\frac{s\ C_{db6}\ g_{md4}\ g_{md5}\ g_{mg1} + \cdots}{s\ C_{gd1}\ g_{md2}\ g_{md7}\ g_{ms2} + \cdots} \right) V_{in-} + \\ + (\cdots) V_{in+}$$

3.3.2 Topological Node Matching and Clustering Algorithm Details

Topological node matching (Step (2) in Algorithm 3.1) identifies the circuit nodes that have similar AC behavior due to their poles and coupling to their subsequent circuit blocks. The matching step considers the nodes' pole resistive and capacitive components and the coupling expressions of their outgoing edges. Signal input nodes are also included in the pool of nodes explored for matching, such that the set of circuits is fully characterized.

Node matching finds groups of maximum size formed out of circuit nodes that have equivalent AC behavior within an acceptable error ϵ. The nodes in other groups differ by a matching error greater than ϵ.

Definition (symbolic sets): Every node V_j of a UBBB signal-flow graph is described as the pair $[P_j, E_j]$, where P_j and E_j are symbolic sets. Set P_j is the reunion of symbolic expressions PR_j and PC_j representing the resistive and capacitive components of the node's pole. Set E_j is the reunion of symbolic expressions containing the $C_m^{(j,k)}$ and $G_m^{(j,k)}$ components of each edge originating at node V_j and ending at node V_k.

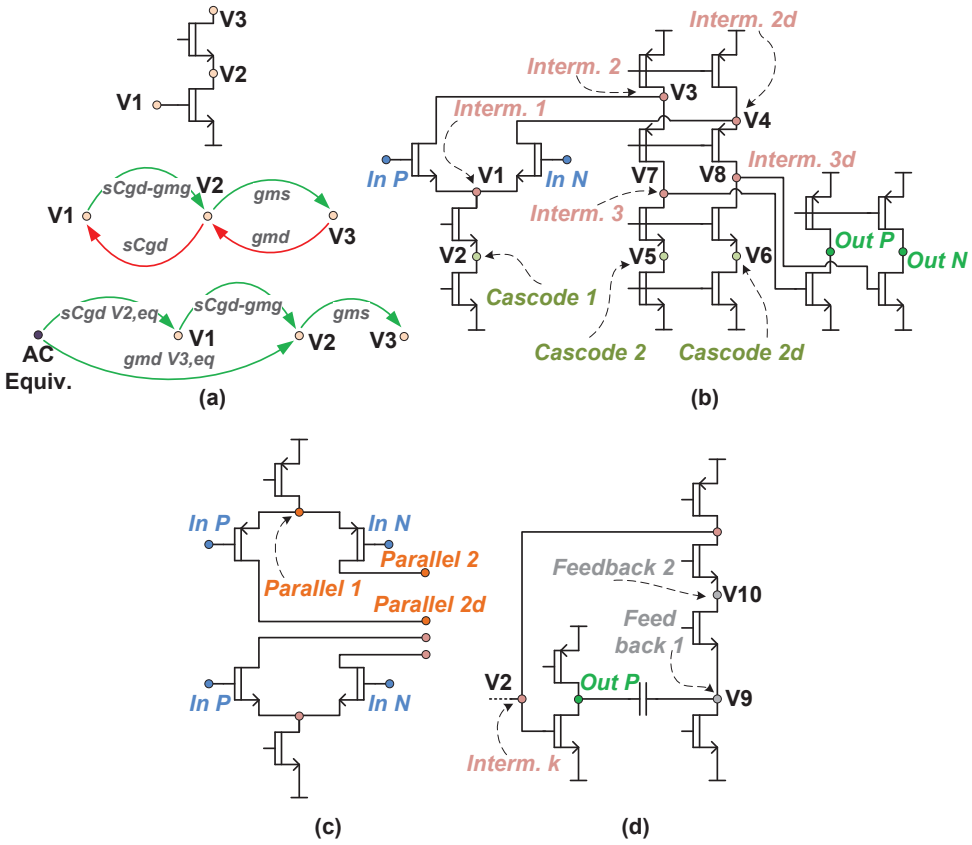

Figure 3.3: Circuit node cluster examples: (a) equivalent, decoupled influence, (b) intermediate order and cascode clusters, (c) parallel structure clusters, (d) feedback loop clusters

Example: The symbolic expressions of node V_1 in Figure 3.2 are as follows:

$$\begin{aligned} V_1 &= [P_1, E_1], \text{ with} \\ P_1 &= PR_1 \cup PC_1 \\ PR_1 &= \{g_{md5} + g_{ms1} + g_{ms2}\} \\ PC_1 &= \{C_{gd5} + C_{db5} + C_{gs1} + C_{sb1} + C_{gs2} + C_{sb2}\} \\ E_1 &= \{F(1,2)\} \cup \{F(1,3)\} = \{+g_{ms1}\} \cup \{+g_{ms2}\} \end{aligned}$$

Definition (matching error): Given two symbolic sets S_1 and S_2, the matching error between symbolic expressions $s_1 \in S_1$ and $s_2 \in S_2$ is function $ers : S_1 \times S_2 \to \mathbb{N}$, such that $ers(s_1, s_2) = n$ and n is the number of symbolic terms that occur in s_1 or s_2 but not in both.

Two circuit nodes, $V_1 = [P_1, E_1]$ and $V_2 = [P_2, E_2]$, are matched within error ϵ if there are correspondences between all the resistive and capacitive components of sets P_1 and P_2 and sets E_1 and E_2, respectively, such that the total number of unmatched symbolic terms is less than error ϵ.

The matching procedure identifies the maximum sets of matched nodes, or equivalently, the maximal partitions of matched nodes for the given set of circuits. It was realized as an optimization method based on two-stage Simulated Annealing. The algorithm takes as input a set of designs represented by their UBBB models and generates the groups of matched nodes. The minimized cost function is as follows:

$$Cost_{matching} = \alpha \times N + \beta \times \epsilon_{tot} \tag{3.6}$$

where α and β are weights associated with the two terms. The first term, N, represents the total number of matched groups in the current solution. The second term, ϵ_{tot}, is the cumulative symbolic error across all node groups produced.

At every iteration, the matching algorithm generates a possible partition of the nodes and computes the matching cost. Error ϵ_{tot} is computed by

examining the symbolic expressions for each pair of nodes, from each partition group, and accumulating the individual errors. The following error components are considered between node pairs:

- Pole expressions:
  - number of unmatched type-C terms
  - number of unmatched type-R terms
- Edge expressions:
  - difference in number of edges for the two nodes
  - number of unmatched type-C terms between edges
  - number of unmatched type-R terms between edges

Type-C symbolic terms refer to capacitive components (e.g., C_{gs}) and type-R terms include transconductance or resistance components (e.g., g_{mg}) in either pole or edge expressions for the analyzed pair of nodes.

Example: Let's consider a pair of nodes V_1 and V_2 and their expressions for edges in sets E_i (excluding poles, for simplicity):

$$(V_1)\ E_1 = \{+sC_{gs}, +sC_{gd}, -g_{mg}, +g_{ms}\}$$
$$(V_2)\ E_2 = \{+sC_{gd}, -g_{ms}, -g_{mg}\}$$

The two nodes have only one edge, hence the error due to different edge count is zero. The symbolic error of type-C terms is equal to 1, since a $+C_{gs}$ term is not present in the expression of V_2. For type-R terms, the symbolic error is equal to 2. Note that $+g_{ms}$ from V_1 is not matched by $-g_{ms}$ from V_2. Both terms express the same transconductance, but the different signs indicate that different structures at the nodes introduce these distinct terms, hence their matching is not appropriate. The errors are of 1 and 2 for type-C and type-R expressions, respectively. The error is minimal since no other matching is possible. Summing all error components gives the node pair's total error equal to 3.

Step (3) in Algorithm 3.1 employs the signal path tracing algorithm [75] to order the groups of nodes based on the signal flow through the circuit. The ordering is inherent to UBBB models as cross-coupled dependencies between nodes are eliminated through decoupling [25]. Then, using the decoupling sequence of each circuit in the analyzed set, the algorithm produces clusters of matched node groups, such that node groups contain nodes with the same position in the signal flow. Hence, this step traces the similarities between circuits with respect to the position of a node in the signal path. For example, groups consisting of input nodes are placed in the *AC Inputs Cluster*. Groups holding circuit output nodes are considered as *Output Cluster*. Groups of nodes that are placed between input and output are clustered as *Intermediate$_i$ Clusters*, where i denotes the position.

Example: Figure 3.3(b) illustrates the ordering of nodes into intermediate clusters. A separate cluster is formed for the positive and negative inputs. By tracing the signal path from the circuit inputs, the first nodes reached are V_1, V_3, and V_4 through gate-to-source and gate-to-drain influences. However, node V_1 comes first in the signal path and is assigned to the *Intermediate 1* cluster because it also influences nodes V_3 and V_4 through valid source-to-drain edges. Node V_3 is then placed in the *Intermediate 2* cluster. The next node reached by the signal path from V_3 is V_7 and it is assigned to the *Intermediate 3* cluster. The process continues until the output is reached. Note that due to the differential nature of the circuit, node V_4 is also a second node in the signal path, but it is placed into a different cluster, *Intermediate 2d*, to avoid matching of groups of nodes from different differential signal paths. Similarly, node V_8 (following V_4) is then placed in the *Intermediate 3d* cluster. A special situation occurs for cascoded biasing/load structures. They include circuit nodes which cannot be reached following the signal path tracing algorithm [75]. For example, nodes V_2, V_5, and V_6 in Figure 3.3(b) are such nodes. These nodes can be reached only through drain-to-source influences which are decoupled and assigned to *AC Equiv*. Such nodes are placed in *Cascode* clusters and their ordering is decided based on the relative position where they appear in the circuit after the intermediate nodes are determined.

Two special cases occur for the following topological structures. Figure 3.3(c) presents complementary circuit structures. In order to distinguish such features, nodes are placed into clusters labeled as *Parallel* with their ordering set in the same way as for *Intermediate* nodes. Second, Figure 3.3(d) shows a circuit with feedback. Nodes along the feedback path are placed into clusters denoted as *Feedback* according to the following steps. First, the sequence of intermediate nodes is identified (V_2) until the output ($Out\ P$) is reached. Then, node V_9 is reached through the capacitor. Next, node V_{10} is reached from V_9. Finally, node V_2 is reached again from V_{10} through the source-to-drain path. However, as node V_2 (intermediate) was already visited, the signal path tracing creates the cycle $V_2 \rightarrow Out\ P \rightarrow V_9 \rightarrow V_{10} \rightarrow V_2$, illustrating the feedback. The sequence enforces that the order of node V_9 follows that of the output for any valid signal path, hence, actually breaking the cycle at the first node following the output. The corresponding edges are decoupled and assigned to *AC Equiv*. Circuit node V_9 is placed in the *Feedback 1* cluster and the feedback loop is ordered in the same manner as intermediate nodes with node V_{10} being placed in the *Feedback 2* cluster. In general, the ordering continues along the loop until the intermediate node is reached. Differential feedbacks are treated using the same clustering technique as previously discussed.

3.3.3 Separation Criteria for Clustering

For Step (4) of Algorithm 3.1, we investigated four separation criteria to order the matched clusters.

The first considered separation criteria was entropy. Entropy is used to describe similarities and differences between circuits, and is popular for classification in data mining [26]. We define a cluster's information content as follows:

$$S_0(Cl_k) = -\sum_{i=1}^{N} p_i \log_N p_i \tag{3.7}$$

N is the total number of circuits with nodes in cluster Cl_k, and p_i is the probability that a circuit in cluster Cl_k is associated with a group of matched

nodes. For each group G_j of matched nodes in cluster Cl_k, the probability is expressed as $|G_j|/|Cl_k|$. This entropy measure characterizes the distribution of nodes within the cluster's groups of nodes, as well as the distribution of groups within the cluster. It equals zero when all circuit nodes form a single group of similar features. This implies perfect matching, when a single group of nodes forms one cluster. The metric is maximum when each circuit node forms its own group. It indicates zero matching, or that the individual nodes are dissimilar from each other and form their own groups within the cluster.

The second analyzed separation criteria is based on item characteristics and is presented in [76]. This measure maximizes the inference potential of attributes. The score of a matched cluster Cl_k is expressed as:

$$S_1(Cl_k) = \frac{p_k N_k}{(1-p_k) + p_k N} \prod_i \left(\frac{N_{k,i}}{Card_k} \right) \tag{3.8}$$

where p_k is the probability of selecting a node and a group from cluster Cl_k, when there are N total groups in the matching solution and N_k groups of nodes in cluster Cl_k. $Card_k$ is the total number of nodes in the cluster, and $N_{k,i}$ is the number of nodes in group G_i of cluster Cl_k.

The third way of computing the separation criteria uses category characteristics to rank their utility [76]. The score of a matched cluster Cl_k is expressed as follows:

$$S_2(Cl_k) = p(Cl_k) \left(\sum_i p(G_i|Cl_k) - p(G_i) \right)^2 \tag{3.9}$$

where

$$\begin{aligned} p(Cl_k) &= \frac{1}{N_c} \\ p(G_i|Cl_k) &= \frac{1}{N_k} \cdot \frac{N_{k,i}}{N_n} \\ p(G_i) &= \frac{Card_k}{N_n} \cdot \frac{N_k}{N} \end{aligned}$$

$p(Cl_k)$ is the cluster probability and is related to the total number of clusters in

the matching solution N_c. Similarly to equation (3.8), N_k is the total number of groups in cluster Cl_k, and $N_{k,i}$ is the number of circuit nodes in group G_i of cluster Cl_k. $Card_k$ is the number of nodes in the cluster, N_n is the total number of nodes in the matching solution, and N is the total number of groups in the solution.

The fourth separation criteria is based on Bayesian classifiers [26]. The score of a matched cluster Cl_k is expressed as:

$$S_3(Cl_k) = p(Cl_k|G_i) = \frac{p(G_i|Cl_k)p(Cl_k)}{p(G_i)} \tag{3.10}$$

where

$$\begin{aligned} p(Cl_k) &= \frac{1}{N_c} \\ p(G_i|Cl_k) &= \frac{\prod_i N_{k,i}}{(Card_k)^{N_k}} \\ p(G_i) &= \frac{Card_k}{N_n} \cdot \frac{N_k}{N} \end{aligned}$$

where all terms have the same meaning as for equations (3.8) and (3.9).

In Step (5) of Algorithm 3.1, the ordered feature representation scheme is built using the selected metric score of matched clusters. The first levels in the representation have the lowest scores, while lower levels have increasing metric scores. In this way, the ordered scheme would first traverse design features that are common to many circuits in the analyzed set. The final levels of the representation illustrate distinct implementation aspects that are specific to individual designs and cannot be matched by other designs to within the accepted symbolic errors.

3.3.4 A Simple ONCR Example

We now consider a set of five two-stage operational amplifiers (OpAmp) to automatically generate the ordered clustering scheme for AC behavior. Figure 3.4 illustrates the structure of the OpAmps, each having a different current mirror circuit load: simple (C_1), Wilson (C_2), improved Wilson (C_3), cascode

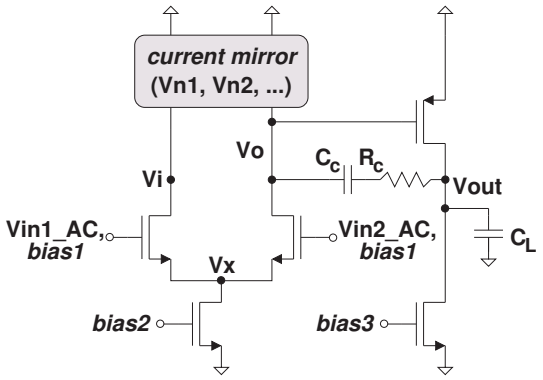

Figure 3.4: Topologies of the considered two-stage OpAmp set

(C_4), and wide swing cascode (C_5) [77].

The produced ordered node clustering structure (ONCR) is shown in Figure 3.5. The structure was determined using entropy as the separation score between clusters. The structure indicates that the topological features of the nodes V_x, V_o, and V_{out} are the same for the five circuits. All nodes of the same level form a single group within the cluster (perfect match), G_1, G_{11}, and G_{12}, respectively. The two lower levels have nodes with least feature similarity, e.g., nodes V_{inAC} and nodes V_{n1} form individual groups within the respective cluster (zero matching). The dissimilarity of nodes V_{inAC} is due to symbolic expressions introduced by the decoupling sequence that transforms the coupled model into a decoupled one [25]. For more complex circuits, each node contains additional edges that represent the multi-variable input equivalent correlations of the uncoupled macromodel.

The ordered representation helps in getting insight on an OpAmp's flexibility in setting its pole and zero positions and their degree of separation as compared to other OpAmps. This can be important for compensation and obtaining a required phase margin. For example, considering the CM input cluster's level of the representation in Figure 3.5, circuits C_3 (or C_4) and C_5 differ by the symbolic expressions for their pole's capacitive components:

$$G_2: \ PC = \{C_{gd} + C_{db} + C_{gs} + C_{gd} + C_{gb} + C_{gs} + C_{gb} + C_{db}\}$$
$$G_4: \ PC = \{C_{gd} + C_{db} + C_{gs} + C_{gd} + C_{gb} + C_{gs} + C_{gb} + C_{db} + C_{gd} + C_{gd}\}$$

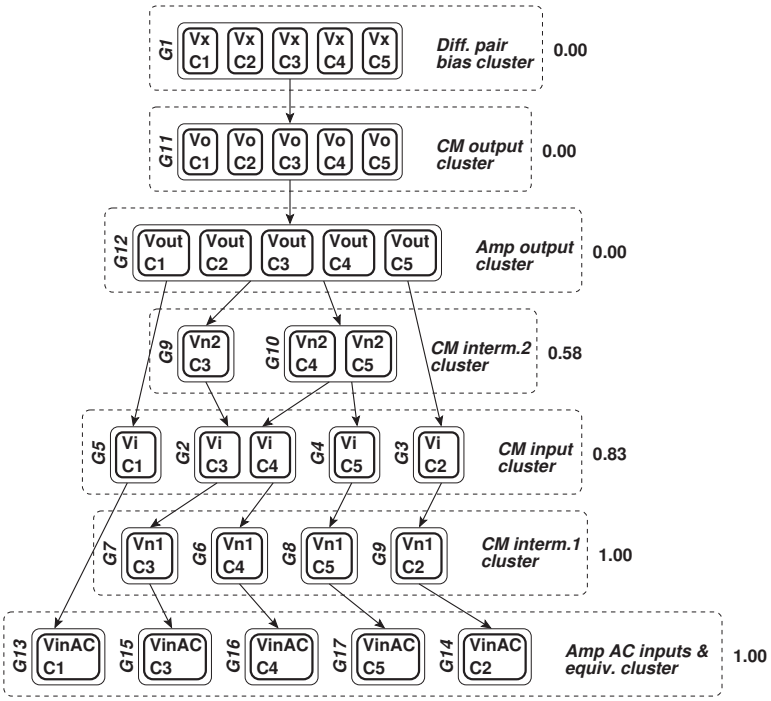

Figure 3.5: Entropy-based ordered feature clustering for five OpAmps

The component of the node's pole of circuit C_5 from group G_4 is defined by two additional device parameters, namely two C_{gd} variables. This suggests that circuit C_5 offers more flexibility than circuit C_3 (or C_4 from group G_2) in controlling the node's pole position. The increased number of variables in the pole's expression can offer more possibilities for setting its position on the frequency axis, even though this position may be closer to the origin than for circuit C_3 (or C_4). Similarly, for the first intermediate CM node level, circuits C_3 and C_4 are distinguished by the associated outgoing edge. The added dependence on a g_{mg} variable for circuit C_4 potentially allows better control of the related zero position than for circuit C_3, including for pole-zero cancellation.

3.4 Experiments

This section presents experiments on creating ordered node clustering representations (ONCRs) for two sets of ten and fifty analog circuits, respectively. The circuits considered are state-of-the-art amplifiers [3–5, 50, 52, 55, 59, 60, 62–66, 68–70, 78–100]. The design set includes voltage and current-mode amplifiers used in applications ranging from general-purpose to ADC-related and audio signal amplifiers. The small-signal UBBB models for all circuits were built using the methods discussed in Section 3.3.

3.4.1 Generation of ONCRs

Topological Node matching

Figure 3.6 shows, for a typical run of the algorithm, the evolution of the matching cost toward the optimal solution. The algorithm initially explores solutions that minimize the matching error. In the later stages, as the error and number of matched sets components of the cost function become similar, the algorithm attempts to minimize the total number of sets and to control the total error, such that a precise final node partitioning is achieved. The execution time on a dual core 2.1 GHz machine was about 26 minutes for the ten circuit set.

Next we studied the importance of the ϵ error value on node matching. First, a precise matching constraint ($\epsilon = 0$) was used for the fifty amplifier design set. The matching procedure distributed a total of 609 circuit nodes into an optimal partitioning, which contains 288 matched groups. 215 of the groups have a single node. These nodes cannot be precisely matched with any other node in terms of the symbolic parameters defining either their pole or edge expressions. The remaining matched groups up to size 7 are distributed as follows: 38 groups have 2 nodes, 9 groups contain 3 nodes, 3 groups have 4 nodes, 7 groups have 5 nodes, 3 groups have 6 nodes, and 2 groups have 7 nodes. The largest group in the solution is of size 38. In general, the higher cardinality groups consist of signal inputs, input structure nodes, and output nodes. Internal circuit nodes from the decoupling sequence account for the

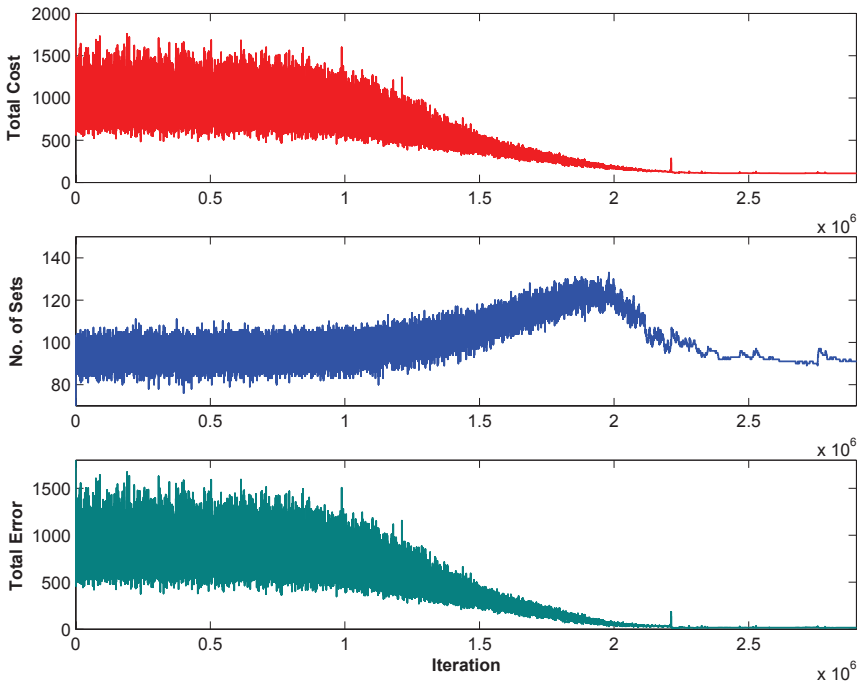

Figure 3.6: Evolution of the matching cost (top: matching cost, center: number of groups component, bottom: total matching error component)

majority of single node groups. The observation suggests that the variety incorporated into circuit topologies is often realized at the level of the internal nodes.

Next, matching experiments considered imprecise matching ($\epsilon \neq 0$) for the poles' and graph edges' symbolic expressions. For poles, PC and PR are the absolute allowed error in terms of number of different type-C and type-R terms, respectively. Similarly, EC and ER represent the permitted number of different symbolic type-C and type-R terms between edge expressions. By varying PC, PR, EC, and ER, we observed the evolution of group sizes in terms of the accepted symbolic error. The matching solution's distribution of circuit node groups up to size 7 is illustrated in Figure 3.7. The precise matching configuration was also included for comparison.

The distribution of matched groups, with respect to the number of contained nodes, changes as more larger node groups are found when error ϵ increases. Runs 1, 2, and 3 in Figure 3.7 indicate that small errors between

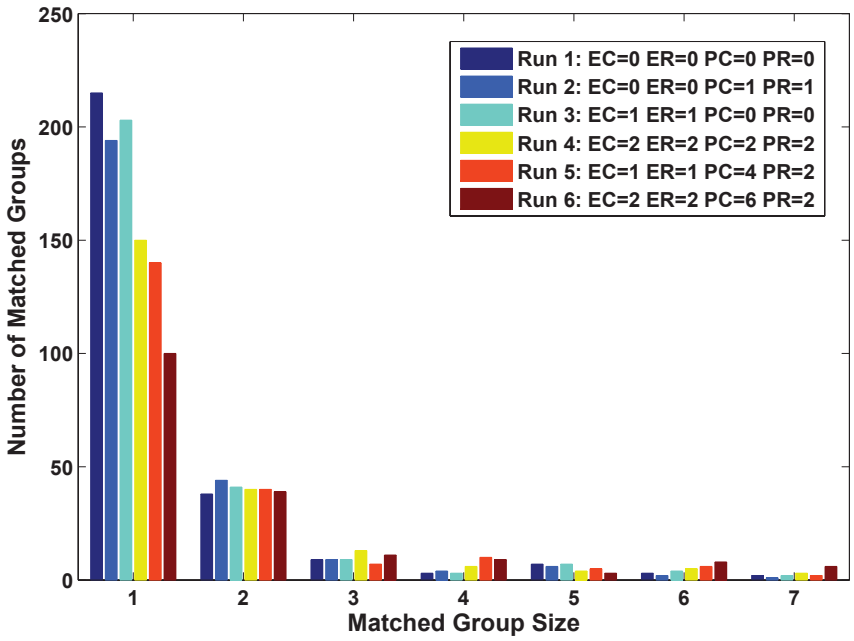

Figure 3.7: Distribution of matched circuit node groups for a precise and multiple imprecise matching algorithm runs (EC/PC, ER/PR - searched edge/pole ϵ-matching for type-C and type-R terms, respectively)

symbolic expressions do not have a major impact on the final distribution of the matched groups. A more significant difference appears only for runs 4, 5, and 6. The higher error reduces the number of unmatched nodes (group size 1) while generally increasing the number of groups of larger sizes. For example, comparing run 1 ($\epsilon = 0$) with run 4 indicates that the number of unmatched nodes is reduced by more than 30% while more groups of six or seven nodes are found. For run 6, the number of unmatched nodes is further reduced by 54% from that of run 1.

The edge errors ϵ were kept the same for runs 4 and 6 and was reduced for run 5, while the pole expression errors for the three cases were progressively increased. The distribution for run 5 shows similar behavior to those of runs 1-3, with the exception of unmatched single nodes. Results for higher-order groups when small edge errors of 0 or 1 are used show little variance even for larger allowed pole errors (runs 1-3 and 5). This indicates that the allowed edge error is the dominant factor to determine the amount of possible node

matching in the runs. Only by increasing the edge error to 2 symbolic terms is additional matching possible in runs 4 and 6. In this two scenarios, increasing the number of groups of larger sizes can be achieved by allowing larger pole expression errors (e.g., run 6 in Figure 3.7). Higher errors are acceptable in this case as pole expressions include as many as 12 symbolic terms. Small errors ϵ correlate two or three small-signal design parameters. For the largest error (e.g., run 6 in Figure 3.7), up to 24 variables were correlated. Increasing the allowed symbolic error for edge expressions to values larger than 2 terms does not produce a better matching solution. This is due to two factors. First, the majority of UBBB model nodes have edge expressions defined by at most three symbolic terms. Hence, increasing the number of different terms accepted does not impact the distribution of matched groups if the nodes' pole expressions error ϵ is constant. In addition, allowing a large error would undermine the concept of matching as symbolic differences of 100% between edges would be routinely accepted by the matching procedure. The matching step can also help identify conditions under which two structurally different circuits have similar small-signal performance, when unmatched terms can be reduced with respect to common expressions.

ONCR construction

Figures 3.8-3.9, A.1-A.2, and A.3-A.4 present the ONCRs generated for the ten amplifier design set (C_1-C_{10}) for precise matching ($\epsilon = 0$, run 1), and imprecise matching corresponding to run 4 (EC=2, ER=2, PC=2, PR=2) and to run 6 (EC=2, ER=2, PC=6, PR=2), respectively (Figures A.1-A.4 are shown in Appendix A). Equations (3.7)-(3.10) represent the four separation criteria that were studied and the separation cost values are indicated for each level in the schemes. Ordering the representation based on the separation cost illustrates increasing metric values and allows traversing the structure from similar to distinct features present at different circuit nodes with respect to the analyzed set of designs. Due to the increased complexity of the figures, directed edges linking the same circuit in different clusters were omitted from the illustrations. However, the node sequence of a specific circuit (C_i) can be

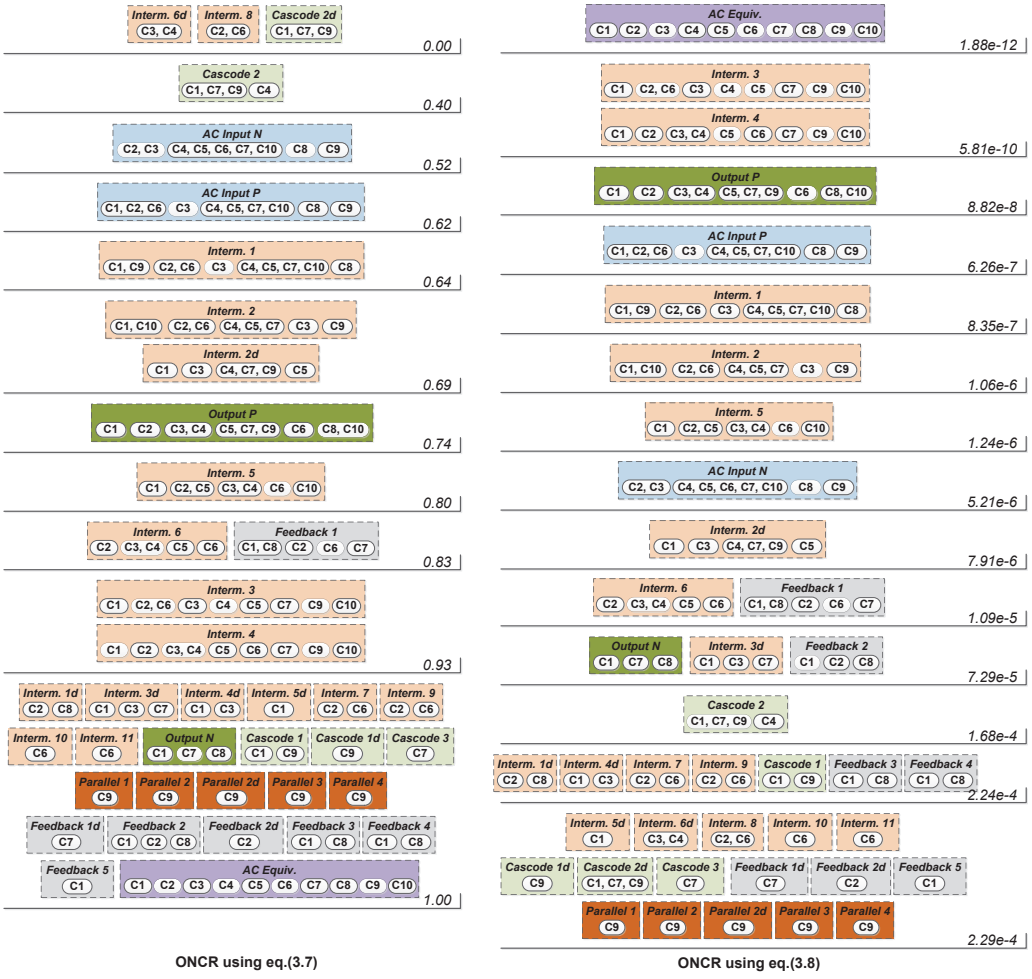

Figure 3.8: ONCR of the ten amplifier design set for precise matching run 1 using entropy-based (eq. (3.7)) and item characteristics-based (eq. (3.8)) separation criteria

found by identifying the respective entry among the groups of each cluster. In a designer usage scenario, the ONCR can be presented in fragments which relate to a subset of the known designs. Chapter 6 presents such an ONCR fragment for circuits that are highly similar to the classic Miller two-stage amplifier from the fifty circuits set.

The results of run 1 for ten designs shows a total of 109 matched groups for a total of 146 nodes. For run 4, the number of groups is reduced to 92,

while the higher allowed symbolic error for run 6 further reduces the number of matched groups to 80. The number of clusters is 39 for all runs since matching is performed only on nodes within the same cluster. The clusters of a specific error run are ranked by the separation criteria from equations (3.7)-(3.10) to generate different ordering and representation depths (two representations are shown in each Figure 3.8-3.9, A.1-A.2, and A.3-A.4).

Considering the ONCR structures and distributions in Figures 3.8-3.9, A.1-A.2, and A.3-A.4, it can be observed that while precise matching successfully identifies exact equivalences between nodes of different circuits, the complexities of the resulting schemes yield little information about similarities between the analyzed circuits. Many circuit nodes remain unmatched or are only grouped in pairs. Complete circuit building blocks cannot be matched (sequences of matched nodes). This supports the necessity and benefits of using approximate matching, as common and relevant dissimilar structures are better illustrated between designs implementing similar functionality.

In the case of the entropy-based separation criteria (equation (3.7)), highly common circuit features among the designs in each cluster are shown first in the ONCRs (lower separation cost), while distinct aspects are shown last (higher separation cost). The metric favors clusters composed of groups of larger sizes, hence better matching. Clusters with a high number of smaller groups, illustrating distinct node features, occupy lower levels of the representations in Figures 3.8, A.1, and A.3.

By comparison, the separation score based on Bayesian classifiers (equation (3.10)) favors clusters consisting of relatively few matched circuit nodes and groups when the ONCR is built in increasing cost order (as shown in Figures 3.9, A.2, and A.4). Lower level clusters, with high metric scores, are formed by an increasing number of groups, which dominates the metric value. The amount of matching does not necessarily increase at these lower levels, for example the *AC Equiv.* cluster has the largest score while having zero matching.

We observed that while producing a separation cost within a different range of values, the ONCR based on item characteristics (equation (3.8)) in

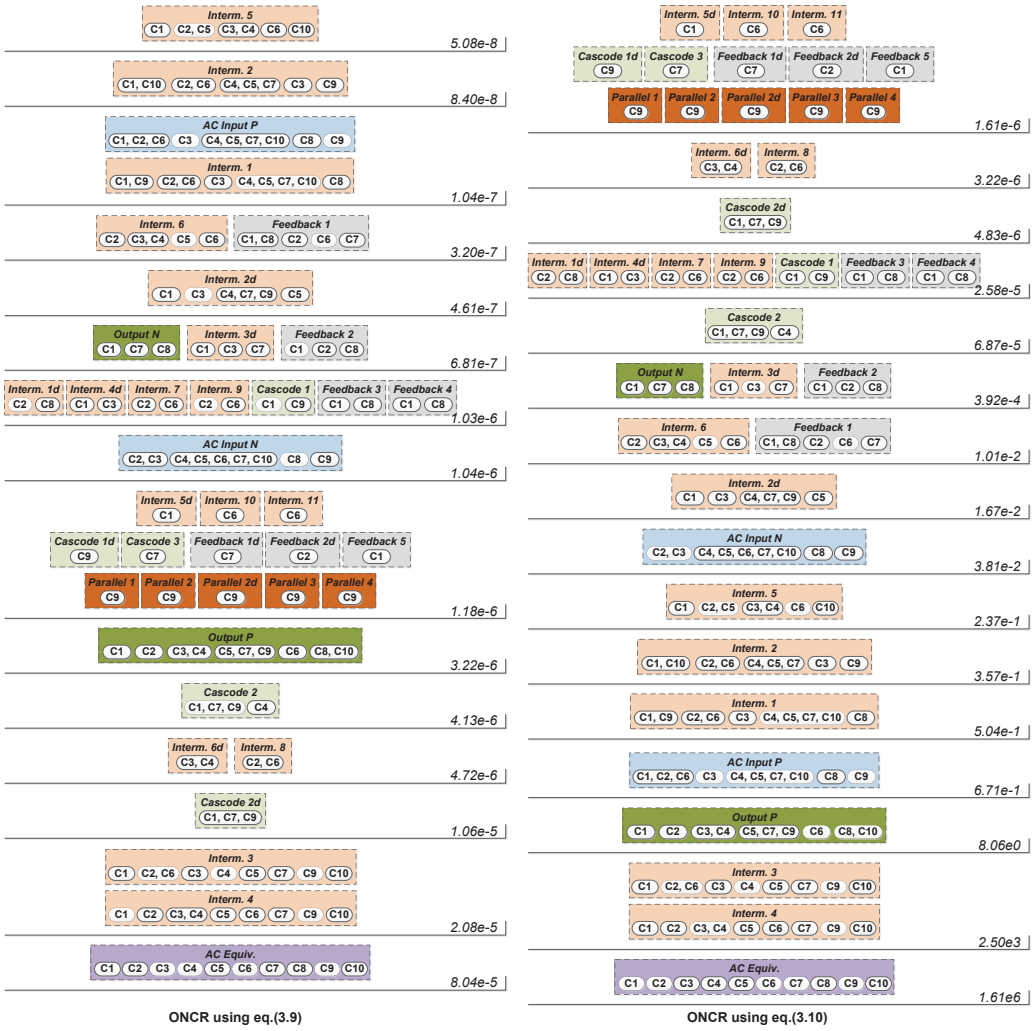

Figure 3.9: ONCR of the ten amplifier design set for precise matching run 1 using category characteristics-based (eq. (3.9)) and Bayesian classifier-based (eq. (3.10)) separation criteria

Figures 3.8, A.1, and A.3 generates an almost mirrored cluster ordering compared to the Bayesian-based classifier (equation (3.10)). One difference is that this item characteristics metric cannot distinguish between clusters that are formed by a single group, regardless of group size. For example, in Figure 3.8, clusters containing a single node or three matched nodes are ranked with the same score. However, the potential of attribute inference increases at lower

levels of the ordering scheme, as smaller clusters are encountered. This enables identification of distinct design aspects from the design set, in a similar fashion to the results produced by the entropy-based separation criteria.

We also examined the ability of the different separation costs to produce ONCRs that consistently isolate highly distinct circuit features in the representation. The results in Figures 3.8, 3.9, A.1, A.2, A.3, A.4 suggest that the entropy-based metric from equation (3.7) and the item characteristics-based metric from equation (3.8) are preferable. For example, consider the cluster for *Interm. 5d* in Figures 3.8-3.9. The features at this node are unique to a single circuit in the analyzed set (C_1) and are therefore highly distinct structures. Both metrics place these clusters on the lowest level of the ONCR, as seen in Figure 3.8. In contrast, the simple category characteristics metric (equation (3.9)), shown in Figure 3.9, places the unmatched distinct clusters at the center of the ordering, without a clear differentiation from the surrounding clusters containing matched features. A similar behavior is also noted for the other analyzed scenarios. Metrics from equations (3.7) and (3.8) can consistently identify the higher rank intermediate node structures with dissimilar circuit features.

With respect to the capability of finding common/matched circuit features, entropy (equation (3.7)) is preferred. In contrast to item characteristics which favors clusters based on the number of groups, the entropy-based metric creates clusters with fewer groups and better matching. A limitation of entropy is in that it does not consider the cluster size. For example, in Figure 3.8, *Interm. 6d* shows perfect matching and is placed on the first level. However, the similarities of a cluster instantiating only two of the ten circuits from the investigated set yields little information about common features among all designs. Better information is provided for larger clusters, instantiating many (or all) circuits from the set, like the *Interm. 3* cluster.

The experiment was repeated for the set of fifty amplifier circuits, $C_1 - C_{50}$. Tables 3.1, A.1, A.2 summarize the results in terms of the identified circuit feature clusters, number of groups in each cluster, number of nodes in the cluster, and the associated metric scores (equation (3.7)-(3.10)). Tables A.1

Table 3.1: Cluster separations scores for run 1 on fifty designs

Cluster	# Groups	# Nodes	S0	S1	S2	S3
AC Equiv.	48	50	9.86E-01	9.50E-83	9.13E-03	2.59E+77
AC Input P	7	50	2.74E-01	7.06E-12	1.07E-07	1.90E+04
AC Input N	6	49	2.28E-01	1.51E-10	2.39E-07	5.56E+02
Output P	11	50	4.56E-01	1.82E-17	1.55E-05	2.66E+10
Output N	6	16	5.12E-01	4.92E-09	2.55E-08	5.58E+00
Interm. 1	12	50	2.86E-01	2.64E-21	2.49E-05	2.34E+14
Interm. 1d	5	5	1.00E+00	5.34E-07	1.84E-08	9.48E-03
Interm. 2	16	47	5.33E-01	5.92E-26	8.65E-05	2.18E+19
Interm. 2d	13	35	5.31E-01	3.38E-20	1.83E-05	1.60E+13
Interm. 3	20	42	6.66E-01	1.20E-31	1.81E-04	1.77E+25
Interm. 3d	11	12	9.54E-01	1.95E-14	8.95E-07	5.95E+06
Interm. 4	21	35	8.16E-01	2.44E-31	1.55E-04	8.25E+24
Interm. 4d	5	6	8.71E-01	4.30E-07	2.65E-08	1.41E-02
Interm. 5	14	26	6.79E-01	1.38E-20	1.44E-05	3.56E+13
Interm. 5d	3	3	1.00E+00	2.32E-05	4.71E-08	2.95E-05
Interm. 6	15	20	8.67E-01	6.93E-21	1.17E-05	6.63E+13
Interm. 6d	2	3	5.79E-01	6.30E-05	1.22E-07	3.28E-06
Interm. 7	6	6	1.00E+00	5.06E-08	3.59E-09	2.04E-01
Interm. 7d	1	1	1.00E+00	7.23E-05	5.70E-08	1.21E-07
Interm. 8	3	4	7.50E-01	1.95E-05	8.38E-08	4.66E-05
Interm. 9	4	4	1.00E+00	4.26E-06	3.47E-08	4.97E-04
Interm. 9d	2	2	1.00E+00	7.09E-05	5.42E-08	1.94E-06
Interm. 10	3	3	1.00E+00	2.32E-05	4.71E-08	2.95E-05
Interm. 10d	2	2	1.00E+00	7.09E-05	5.42E-08	1.94E-06
Interm. 11	1	1	1.00E+00	7.23E-05	5.70E-08	1.21E-07
Cascode 1	2	6	2.51E-01	3.94E-05	4.88E-07	1.05E-05
Cascode 1d	1	4	0.00E+00	7.23E-05	9.12E-07	4.85E-07
Cascode 2	6	16	5.12E-01	4.92E-09	2.55E-08	5.58E+00
Cascode 2d	2	7	2.11E-01	3.47E-05	6.64E-07	1.39E-05
Cascode 3	2	3	5.79E-01	6.30E-05	1.22E-07	3.28E-06
Cascode 3d	2	2	1.00E+00	7.09E-05	5.42E-08	1.94E-06
Cascode 4	1	1	1.00E+00	7.23E-05	5.70E-08	1.21E-07
Cascode 5	1	1	1.00E+00	7.23E-05	5.70E-08	1.21E-07
Cascode 5d	1	1	1.00E+00	7.23E-05	5.70E-08	1.21E-07
Feedback 1	8	11	8.22E-01	1.13E-10	6.56E-08	3.81E+02
Feedback 1d	3	3	1.00E+00	2.32E-05	4.71E-08	2.95E-05
Feedback 2	3	4	7.50E-01	1.95E-05	8.38E-08	4.66E-05
Feedback 2d	1	1	1.00E+00	7.23E-05	5.70E-08	1.21E-07
Feedback 3	3	3	1.00E+00	2.32E-05	4.71E-08	2.95E-05
Feedback 4	2	2	1.00E+00	7.09E-05	5.42E-08	1.94E-06
Feedback 5	1	1	1.00E+00	7.23E-05	5.70E-08	1.21E-07
Parallel 1	4	6	6.93E-01	2.52E-06	7.81E-08	1.26E-03
Parallel 1d	1	1	1.00E+00	7.23E-05	5.70E-08	1.21E-07
Parallel 2	3	5	6.55E-01	2.00E-05	1.31E-07	5.69E-05
Parallel 2d	3	5	6.55E-01	2.00E-05	1.31E-07	5.69E-05
Parallel 3	1	2	0.00E+00	7.23E-05	2.28E-07	2.43E-07
Parallel 4	1	2	0.00E+00	7.23E-05	2.28E-07	2.43E-07

and A.2 are shown in Appendix A. A total of 609 circuit nodes are organized in 47 clusters. Precise matching (run 1) produces a total of 288 node groups. Increasing the allowed symbolic errors reduces this number to 232 and 188 for run 4 and run 6, respectively. For example, the *Interm. 1* cluster (instantiating nodes from all 50 circuits) has 12 node groups for run 1. Matching is improved in run 4 and the number of groups (for the same 50 nodes) is now 9, while in run 6 additional matching is possible and only 7 groups are created.

The results show similar matching characteristics as for the ten amplifier set. Circuit inputs, low order intermediate nodes, and circuit output structures have the most common features. Also, cascode structures are well matched. As the intermediate order increases, fewer circuits are instantiated and the amount of possible matching decreases. For example, the *Interm. 4* cluster contains nodes only from 35 of the 50 circuits. As many as 21 groups are found in this cluster (run 1), which indicates reduced matching. In terms of feedback structures, only 11 circuits employ them. In addition, only 3 out of these circuits have a feedback sequence of length 3 (*Feedback 3*), and relatively low matching was observed among these nodes. Out of the 50 circuits, only 6 use complementary differential features shown in *Parallel* clusters. The results suggest that circuits are predominantly differentiated by features of the internal nodes or feedback structures, while designer's usually utilize common input and output features.

In terms of the separation capability, entropy (S_0, equation (3.7)) is again preferable. Its behavior is superior to that of the item characteristics-based metric (S_1, equation (3.8)) for identifying and ranking common/matched features. Consider the case of clusters *Interm. 2d* and *Interm. 4* from Tables 3.1, A.1, and A.2. Both clusters contain 35 nodes, but different amounts of matching: *Interm. 2d* has fewer groups than *Interm. 4*, and better matching among its nodes. However, only the entropy-based separation score manages to consistently rank the *Interm. 2d* cluster before the *Interm. 4* cluster in the ONCRs to indicate that more common features exist for these structures.

3.4.2 Insight from ONCR Models and Application Examples

ONCR models present the common and unique topological features of the schematics of an analog circuit population. The impact of each features on specific circuit performance, e.g., AC performance and noise, can be precisely characterized using the technique given in Chapter 4 to find the performance trade-offs, opportunities, and limitations of a circuit compared to others. This analysis is important for devising a new generation of analog design tools which incorporate aspects of designer reasoning in the synthesis flow. Methods for topology synthesis (like the ones discussed in Chapter 6) and design verification can be devised, even though novel techniques for transistor sizing and layout design can be envisioned too. Furthermore, ONCRs can offer the support to characterize and systematically expand building block libraries of existing synthesis tools [21, 23, 101].

Circuit topology synthesis has been traditionally tackled using various optimization-related approaches, including evolutionary algorithms [8, 14, 23] and template-based synthesis [28]. In spite of some noted success, many approaches arguably fail to match the versatility and creativity of human designers. For instance, automatically produced topologies through template-based systems include quality solutions but are usually constrained to a specific category of circuits, e.g., $\Delta\Sigma$ ADCs [28], with only a relatively small number (tens) of topologies being explored. In contrast, early evolutionary methods [14] are not constrained to a specific circuit type and explore a large number of different topologies through successive generations. However, this technique incorporates structural features that are less justified from the stand point of functionality or performance, which are not part of manually constructed topologies.

The genetic programming-based (GP) synthesis method in [14] creates designs characterized by long decoupling sequences e.g., with 25 internal nodes. In contrast, the most complex amplifier in the analyzed set, C_1, has only 20 internal nodes. Furthermore, the synthesized amplifiers contain multiple long and isolated signal paths. The manually-designed circuits do not include

such structures. Also, the amplifier input and output nodes of the synthesized circuits are strongly coupled to the rest of the circuit, e.g., some output nodes are coupled to 9 intermediate nodes. The output node's pole expression is complex, containing 5 resistive and 14 capacitive variables. By comparison, the analyzed amplifiers contain on average only 3 couplings to the output node. The output of amplifier C_6 is closest to this design, still, 17 symbolic variables distinguish the two designs.

The synthesis method in [8] constrains the evolved topologies to structures with more traditional features by introducing a correction mechanisms based on current flow analysis. The generated designs are only moderately complex, with the longest decoupling sequence containing 10 nodes. These results are similar to the reference circuits, where the majority of designs show comparable decoupling sequence length. In terms of coupling and pole expressions, similar structures are also found. For example, most of the designs can be matched (pole and coupling) with the outputs of amplifiers $C_1 - C_5$, C_9, and/or C_{10}. Also, starting with good embryonic circuits yields the *Interm. 1* node structure in Figure 3.10(a), one of the more popular solutions among the 50 reference amplifiers. Nevertheless, the constrained synthesis method requires significant designer knowledge, and tends to generate (specialize) only a limited type of topologies. Furthermore, the included set of constraints does not prevent the method from producing some *unusual* designs, like four-stage amplifiers.

More recent techniques utilize a library of well-known, *trusted* building blocks in the synthesis process. In [21], domain knowledge is encoded as a set of rules to ensure correct connectivity, biasing, and region of operation of the well-known library elements. However, unusual design features that are not included in the reference manual designs from the ONCR are still introduced in the solution (e.g., *series* signal flows through current mirrors to implement the output stage of a simple differential pair amplifier).

In [23], the hierarchical organization of the designer-specified building block library results in generation of only well-known, trusted topologies. The tool searches through thousands of different single-stage and two-stage ampli-

fier topologies which include nodal features that are also commonly seen in the ONCR (e.g., structure of *Interm. 1* from Figure 3.10(a)). Differences are only noted with respect to the resistive source degeneration from the building block library which is present in active form in the ONCR circuits (Figure 3.10(c)). The scope of the technique from [23] is only limited by the variety of library elements. For example, the library needs to be extended to permit exploration of a topology with a cascoded current source to bias a differential pair (like in Figure 3.10(b)).

An extension of the previously discussed tool addresses this limitation by introducing mutations of the originally synthesized topologies if their performance is insufficient [23]. The objective function controls the amount of changes (novelty) in the trusted topologies by minimizing the number of performed transformations. The technique therefore achieves desired performance through the smallest change possible in the design (e.g., only add a zero-compensating resistor to a trusted topology).

For difficult problems, random mutation alone can potentially lead to drastic transformations of otherwise *trustworthy* designs into *usual* topologies in an effort to achieve performance. Consider a scenario in which a three-stage amplifier is needed for the performance requirements. There is no guarantee that mutation of a trustworthy two-stage topology results in a trustworthy three-stage design with a complex compensation scheme (when such elements are not originally present in the library). In addition, the process of randomly mutating a circuit over many generations has arguably no correlation to the process used in manual design to refine a topology (other than the ultimate goal of achieving performance). Designers usually reason on how to precisely modify an existing circuit to achieve the performance. For example, the amplifier C_{10} [3] is based on the simple Class A circuit in Figure 3.2 to which C_{10} adds an intermediate node structure that couples between nodes V_3 and V_o. This small, local structural feature transforms the initial design into a Class AB stage with improved slew-rate and unity-gain frequency [3]. We believe that the ability to reason such precise design decisions and create trusted new topologies is key to developing next generation analog design tools.

ONCR models are an important first step towards enhancing topology synthesis and refinement techniques such that precise structural features are successively introduced or modified through a reasoning process. The sequence of tackled features acts as a design plan used to understand, verify, and validate a new topology under specific performance requirements and implementation constraints. For example, based on ONCR schemes like in Figures 3.8-3.9, a collection of local features and their impact on performance can be built at each cluster level of the representation. This information is then used to suggest alternative structural features for a given circuit design, so that its performance improves. In addition, ONCR models indicate the alternatives that have not been considered by a given design set, hence suggest possible places at which new structural features can be introduced. ONCR models also complement library-based synthesis techniques like [21, 23] by expanding their building block set, hence enabling them to tackle a larger variety of design problems. In a practical scenario, an ONCR can be generated for a collection of circuits that includes the set of trustworthy synthesizable topologies from [23] and circuits extracted from recent publications. Leveraging the ONCR insight on common and distinct nodal structures, *new* circuit structures can be systematically identified. These are then used to expand the hierarchical library with additional designer-trusted blocks and options for combining them. Iterating through the process by adding new publications can continuously keep the searchable space of [23] up-to-date with novel human designer contributions.

The remainder of this section presents a set of examples on how ONCR models can be used to systematically suggest alternative circuit structures. Some additional case study application examples are given in Chapter 6. Let's consider the *Interm. 1* nodes cluster in Figure 3.8. Possible nodal structures are shown in Figure 3.10 with their corresponding groups of nodes from Figure 3.8. In terms of coupling between nodes, the most common feature in the 10 amplifier set is the simple differential pair configuration in Figure 3.10(a). V_1 is the first intermediate node in the decoupling sequence and influences linearly the subsequent nodes V_2 and V_3 through g_{ms2} and g_{ms1} coupling, re-

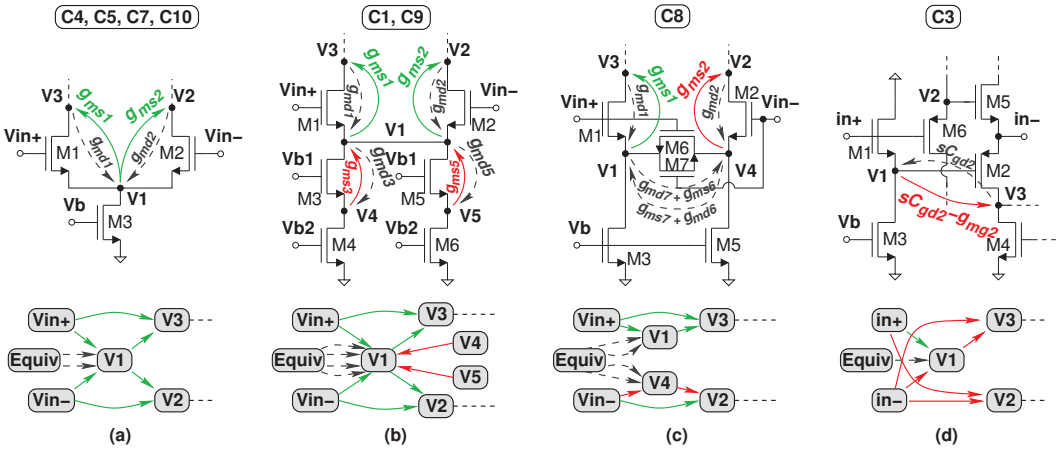

Figure 3.10: Different nodal structures of amplifier input stages and the resulting coupling from V_1 (*Interm. 1* node cluster in Figure 3.8) to other circuit nodes (decoupled UBBB influences shown with dashed arrows): (a) simple differential pair, (b) cascode current source biased differential pair, (c) source degenerated differential pair, and (d) current feedback amplifier input stage

spectively, while being influenced only by the input nodes and *AC Equiv.* This coupling scheme appears in circuits C_4, C_5, C_7, and C_{10} in Figure 3.8. These circuit nodes are grouped together in the ONCR model, thus illustrate the frequent use of the feature. For the 50 circuit set, this feature appears in 38 designs. If performance is insufficient, topology synthesis can use the ONCR model to indicate possible alternatives. An option for the *Interm. 1* node is to couple it to other nodes in the circuit through additional linear influences. Figure 3.10(b) depicts the approach used in circuit C_1 and C_9. Node V_1 is now also influenced by V_4 and V_5 through g_{ms3} and g_{ms5}. Alternatively, the feature in amplifier C_8 can be used for linear couplings of node V_1. Figure 3.10(c) shows the introduced source degeneration, which removes the coupling of V_1 to V_2 and shifts it to node V_4. Node V_4 (*Interm. 1d*) influences V_2 through g_{ms2}. The addition of more node couplings enables greater flexibility in achieving the needed performance. By introducing more, less constrained, design variables in a circuit topology, certain constraints can be relaxed and superior performance is achieved.

Another option for topology refinement is to expand coupling beyond linear influences. This solution is suggested from the pool of structures identified by ONCR for the *Interm. 1* cluster in Figure 3.8. In most cases of the 10 amplifier set, V_1 is coupled only through linear influences to the rest of the circuit (g_{ms}). The three schemes shown in Figure 3.10(a)-(c) cover 7 out of the 10 circuits. However, node coupling is also implemented through rarer frequency-dependent influences (i.e. sC). ONCR identifies this uniqueness in the case of the current feedback amplifier C_3, which couples V_1 to V_2 through the gate of a transistor. In Figure 3.10(d), the structure results in the frequency-dependent influence $sC_{gd2} - g_{mg2}$. This alternative also removes certain couplings since V_1 does not couple to V_2. Compared with the performance of common input stages and linear coupling, such as those of conventional voltage amplifiers in Figures 3.10(a)-(c), this topology improves the design's overall bandwidth at the expense of some loop gain and higher current noise [5]. Circuits C_2 and C_6 (also current feedback amps) exhibit a similar input structure, which is matched to that of C_3 when approximate matching is performed. This suggests the frequency-domain input stage coupling is better suited for high speed applications, and linear coupling produces higher gain designs.

Apart from changing the coupling between nodes, circuit topologies can be also modified to include additional devices at a specific node to address the constraints due to the node poles. For example, for the *Interm. 1* nodes, the ONCR model presents different alternatives of connecting devices at node V_1, like source-source-drain, source-source-drain-drain, and source-drain-gate connections. In Figures 3.10(a) and (b), the pole's symbolic expressions at node V_1 are changed by introducing transistor M_5. For Figure 3.10(a), the resistive and capacitive pole expressions corresponding to group C_4, C_5, C_7, C_{10} in Figure 3.8 are:

$$R_{V_1} = 1/(g_{ms1} + g_{ms2} + g_{md3})$$
$$C_{V_1} = C_{gs1} + C_{sb1} + C_{gs2} + C_{sb2} + C_{gd3} + C_{db3}$$

while for Figure 3.10(b), the expressions corresponding to group C_1, C_9 in Figure 3.8 are:

$$\begin{aligned} R_{V_1} &= 1/(g_{ms1} + g_{ms2} + g_{md3} + g_{md5}) \\ C_{V_1} &= C_{gs1} + C_{sb1} + C_{gs2} + C_{sb2} + C_{gd3} + C_{db3} + \\ &\quad + C_{gd5} + C_{db5} \end{aligned}$$

The new design variables related to device M_5 are g_{md5}, C_{gd5}, and C_{db5}. Their inclusion changes the position of the pole, and increases the design's flexibility as there are more variables. In terms of pole expressions, this structure matches that in Figure 3.10(c) (which corresponds to group C_8 in Figure 3.8, where the source of M_6 is equivalent to that of M_2 and the drain of M_7 to that of M_5 from Figure 3.10(b)). However, together with the differences in coupling, the structures offer different performance benefits. The cascode current source biasing in Figure 3.10(b) gives increased output impedance for a more stable output current, but limits voltage swing for the input transistors. In contrast, for the active source degeneration in Figure 3.10(c), an equivalent cross coupling between V_1 and V_4 exists through g_{md}/g_{ms} of transistors M_6 and M_7 (decoupled UBBB edges). Overall, the structure improves the stages linearity by extending the allowable input signal range.

Finally, by analyzing the symbolic expressions for coupling and poles of node groups in ONCRs, one can also identify design alternatives unused by the current design set. Such alternatives can be presented as suggestions to add/modify devices and node couplings to expand the design space. This option is valuable if none of the topologies captured by an ONCR achieves the desired performance. For example, let's consider that the analyzed 10 design set does not contain current feedback amplifiers C_2, C_3, and C_6. In this case, the ONCR's features for the *Interm. 1* cluster are only those in Figure 3.10(a)-(c). The analysis of the associated symbolic expressions shows that frequency domain dependent coupling is not implemented by any of the designs. Thus, transistor connections that include sC can be suggested. For example, frequency domain coupling in the signal path can be achieved only by

gate-to-drain or gate-to-source connections. Since the assumed ONCR does not contain symbolic expressions corresponding to these connections (structures of Figure 3.10(a)-(c)), it can be inferred that a device gate needs to be placed at node V_1 to explore sC coupling options. By investigating such alternatives, the design space is expanded beyond the initial circuit set. Ultimately, this exploration can identify *new* amplifier topologies, such as the current-mode circuit C_3 with the *Interm. 1* structure in Figure 3.10(d).

3.5 Summary

This chapter described an automated symbolic technique for generating circuit models called ordered node clustering representations (ONCRs) that indicate the main similarities and differences between structurally different analog circuits. The method includes three main steps: identifying the possible sets of separation criteria, analyzing the criteria sets with respect to their potential of distinguishing the circuits, and building the ordered clustering scheme to maximize the separation among dissimilar circuits. Four separation scores were studied for circuit feature clustering: entropy, item characteristics, category characteristics, and Bayesian classifiers. Experiments used ten and fifty state-of-the-art operational amplifier circuits.

Entropy identifies the highest number of common and distinguishing features for a circuit set. The separation criteria based on entropy and item characteristics produce clustering schemes favoring more groups of larger sizes. Clusters with many groups of small sizes occupy the lower levels of the schemes. The separation score based on category characteristics and Bayesian classifiers favors clusters with relatively few matched circuit nodes.

ONCRs offer insight, through symbolic expressions, about the similar and dissimilar circuit features, including topological structures, and the common and distinct symbolic sub-expressions. The design variables (e.g., g_m, C_{gs}, C_{gd}, etc.) that appear in the distinguishing symbolic expressions indicate the available flexibility in positioning poles and zeros.

Clustering schemes are also useful for synthesizing topologies and refining existing circuit structures to tackle new performance requirements. This includes reusing solutions of coupling circuit nodes through linear and frequency-dependent connections, adding new devices at nodes, and replicating signal flow sub-structures for circuit nodes. ONCRs indicate design options that are not covered by a given circuit set and could serve as possible design options that can also be employed to extend the set of basic building blocks for other existing synthesis techniques.

Chapter 4

Generation of Systematic Comparison Data for Analog Circuits

The concepts introduced in Chapter 3 are extended in this part with a novel technique for systematically generating comparison data between two analog circuits. The comparison data presents the similar and distinguishing performance characteristics of circuits with respect to DC-gain, bandwidth, common-mode rejection ratio (CMRR), noise, and sensitivity. The comparison data is important for getting insight about the common and unique benefits of a circuit, selecting fitting circuit topologies for system design, and refining and optimizing circuit topologies. The technique utilizes matching of both the topologies and symbolic expressions of the compared circuits to find the nodes with similar electric behavior. The impact on performance of the unmatched nodes is used to express the differentiating characteristics of the circuits.

4.1 Introduction

Existing macromodeling methods can successfully tackle a large variety of performance attributes, including small-signal AC [25, 102, 103], weakly

nonlinear performance [104–107], and large-signal nonlinear attributes [108, 109]. The utilized modeling techniques include regression analysis [75, 110, 111], symbolic analysis [7], neural networks [74], piecewise-linear approximation [112], optimization-based symbolic descriptions [113], Support Vector Machines [107], system identification [109], and model-order reduction [72, 114].

However, there has been limited work on developing macromodeling methods to relate (compare) the performance of two analog circuits, e.g., DC gain, bandwidth, noise, common-mode rejection ratio (CMRR), and sensitivity. Such comparisons are important to highlight how different topological structures impact circuit electrical behavior and performance, including the nature and complexity of design trade-offs, the design variables available to decide the trade-offs and set each individual performance attribute, and the design conditions under which two circuit topologies present similar or unique behavior and performance. The insight obtained through circuit comparison includes understanding the capabilities and limitations of a circuit compared to other options [5] and selecting the best circuit topology for a given specification [72]. Other possible applications are incremental topology refinement, and circuit optimization and reuse.

It is not trivial to compute the performance similarities and differences between two circuits, and to relate these characteristics to the structural differences of the circuits, including the trade-offs and design variables of each structure. Simulating and/or modeling individually each circuit gives some insight but accurate understanding of the link between topological variations and performance differences requires detailed analysis [5].

Previous work has compared circuits using their performance space descriptions [23, 72, 115–117]. Performance space descriptions relate mathematically the performance attributes of structures, like DC gain, 3dB frequency, and slew rate. Descriptions are constructed either starting from circuit equations [116] or using a synthesis tool that produces the Pareto fronts of the performance space [23, 115, 117]. In [115], a linear approximation of the feasible performance region is constructed. The resulting polytope descriptions of different topologies are overlapped for comparison and enable topology selec-

tion or are used to set achievable performance requirements of blocks in system design. In [23], the Pareto front is presented in a series of 2-D performance plot combinations highlighting the different types of synthesized topologies for comparison. Data mining these results produces spec-to-topology decision trees. Nonlinear sensitivity analysis is used to characterize the relative impact of topology choice and sizing on performance. Symbolic equations relating the performance of the optimal solutions are automatically generated through the technique from [113].

However, performance space descriptions like polytopes, scatter plots, and decision trees abstract all design variables and focus only on numerical performance values. These representations lose the underlying reasons of *why* a topology can only achieve such performance in relation to the other alternatives. We believe this information is crucial to *understanding* the design and these methods lack this insight unless substantial expert manual analysis of the results is performed. Symbolic equations based on performance trade-offs [23] do not improve this aspect as the relations are in terms of performance with no direct link to the structures used in the Pareto optimal designs. Sensitivity analysis based on sizing variables and topology choice [23] offers some insight. But this method does not provide correlated trade-off expressions. Furthermore, applying the technique only on the optimally sized circuits limits the available insight with respect to circuit structure. For example, there are more than 17000 Pareto front solutions, but only 150 different topologies are used. More than 3000 possible topologies in the library remain uncharacterized. Overall, previous work on comparing designs does not offer sufficient insight into how topological differences in circuits introduce new design variables that create novel trade-offs and thus new opportunities (flexibility) for improving performance. This insight is important not only for circuit topology selection but also for design reuse, including circuit optimization for new requirements, incremental topology changes for novel applications, and design migration to different fabrication processes. Systematic comparison of topologies also enables design reasoning. It provides a mechanism to understand the differences between solutions and their implications on circuit performance.

This chapter complements existing characterization techniques and proposes a technique for systematically producing comparison models for two analog circuits. The models present the similar and distinguishing topological features as well as a set of symbolic performance constraints that create a link between the design parameters and trade-offs. Characteristics of the circuits with respect to DC gain, bandwidth, noise, CMRR, and sensitivity are considered. The technique utilizes a dual matching approach of both topologies and symbolic expressions to find the nodes with similar electric behavior in different circuits. The distinguishing aspects of the unmatched behavior are also found for the circuits. A set of constraints relate the behavioral descriptions to performance attribute modification. The final step of the method characterizes how topological and behavioral differences modify trade-offs in a design, availability of free (orthogonal) variables to set performance attributes, and achievable performance values. The presented method focuses on AC performance, but as the structural macromodeling technique [25] used to describe circuits can also tackle weakly nonlinearities, we feel that it should be possible to extend the comparison models to weak nonlinearities too.

The chapter has the following structure. Section 4.2 presents the addressed problem. Sections 4.3 and 4.4 detail the model and proposed algorithm for circuit comparison. Section 4.5 offers experimental results.

4.2 Comparing Electrical Behavior and Performance of Analog Circuits

Comparing the electrical behavior and the performance of two analog circuits requires identifying all related design variables, characterizing the impact of similar and distinguishing variables on circuit behavior and performance attributes, and then relating the resulting performance plots. Intuitively, two circuits can be compared by separately changing the design variable values within their ranges and plotting the values of the relevant performance attributes. Figure 4.1(a) illustrates the process. Performance attributes $Perf_i$ and $Perf_j$ are plotted for various values of variable g while other design parame-

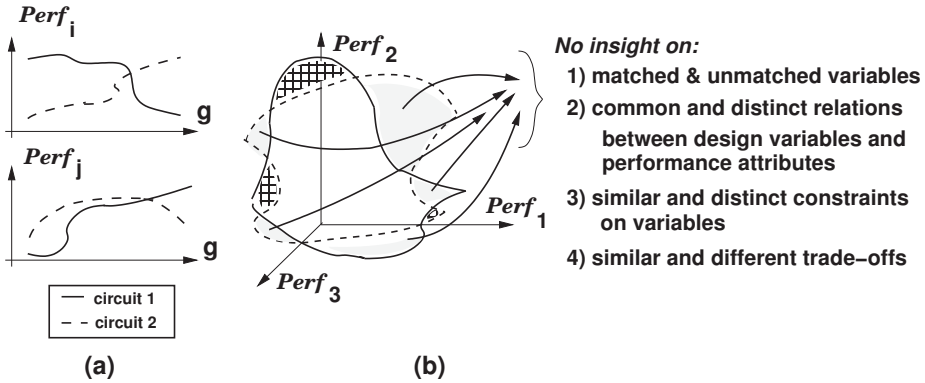

Figure 4.1: Design insight based on circuit comparison

ters are kept constant. The process is repeated for all parameter combinations. The analysis relates the individual performance attributes and their sensitivity with respect to design variables. Performance trade-off surfaces are also generated to present common and distinct performance values. In Figure 4.1(b), the differences between the performance of the two circuits are shadowed. The common performance space is shown without shadow.

In this approach, it is difficult to relate the topological similarities and differences between two circuit schematics to the changes in behavior and performance, including any common and distinguishing behavior of the structural elements of the circuits (e.g., circuit nodes and sub-circuits), and their implications in having similar and distinct design trade-offs and performance. For example, in Figure 4.1(b), the precise reasons that produce the performance space differences for $circuit_2$ compared to $circuit_1$ (the five gray regions) are difficult to establish, including the sets of design variables with matched and unmatched effects, the common and distinct relations linking performance attributes to (matched and unmatched) variables, the similar and distinct constraints on the variable values, and the similar and different trade-offs in the two circuits. Specifically, there is no indication about how design-specific constraints improve performance, such as certain pole-zero placements, or constraints on device parameters, e.g., transconductance and capacitance values being sized according to a certain ratio. In an automated synthesis flow, this insight is useful in incremental circuit topology synthesis, design optimization

and reuse, and topology selection. As shown in Section 4.5, performance attributes and design trade-offs are linked to sets of design variables through non-trivial symbolic expressions and constraints, which are hard to identify and characterize based only on numerical simulation data.

Instead, the proposed circuit comparison method tackles the above difficulties by symbolically relating the mathematical expressions describing the electrical behavior, performance trade-offs, and performance attributes of two circuits. It finds the topologically similar and distinct circuit sub-structures as well as the nodes with similar electrical behavior. Two nodes have similar behavior if there are conditions under which the symbolic transfer functions (TFs) between inputs and nodes can be matched, such that the two TFs represent the same mathematical expression. Examples of such enabling conditions include requirements that certain device parameters are equal, or some devices are much larger (or smaller) than others. Finally, the modifications of performance attributes due to topological and behavioral similarities and differences in two circuits, e.g., ΔDC gain, Δbandwidth, ΔCMRR, and Δnoise, are used to compare trade-offs in a design, availability of free variables to control performance attributes, and achievable performance ranges.

4.3 Circuit Description for Systematic Comparison

This section presents the description used to systematically compare two circuits. The description defines the common and distinguishing electric behavior in two circuits by identifying matched nodes with similar voltages and coupling expressions. The description starts from the UBBB macromodels [25] presented in Chapter 3 of two circuits. This gives explicit details about the nodal behavior of the circuits.

Figure 4.2 depicts the schematics and model representations for a two-stage Miller amplifier and a class AB two-stage amplifier [3]. UBBBs are directed, acyclic signal-flow graphs, in which vertices are circuit nodes, and edges represent the signal coupling between nodes. The resistive and capacitive

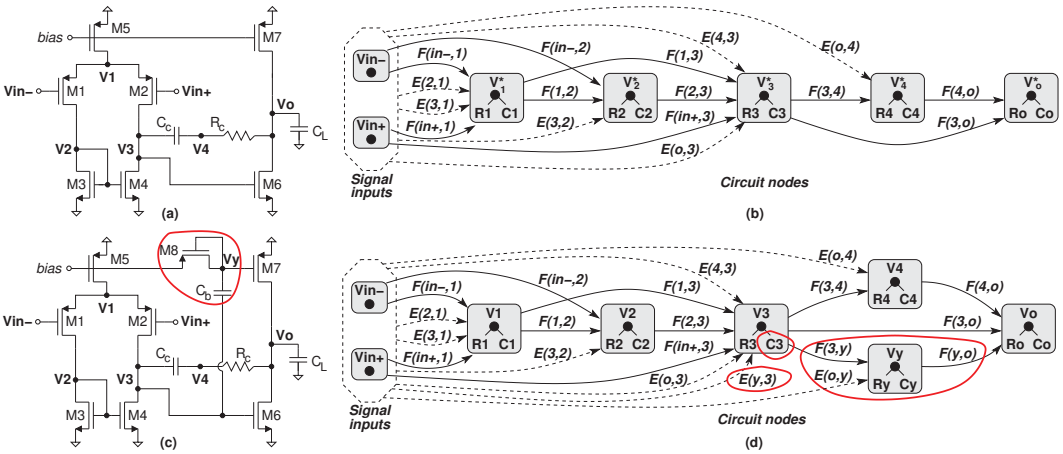

Figure 4.2: Schematic (a) and UBBB signal-flow graph (b) of two-stage Miller amplifier; schematic (c) and UBBB signal-flow graph (d) of class AB two-stage amplifier [3]

components of the poles at circuit nodes and the relations associated to edges are symbolic expressions defined over the small-signal parameters of circuit devices. The symbolic expressions of UBBBs give insight into the electrical behavior of specific circuit structures.

For example, using the concept of *symbolic sets* introduced in Chapter 3, node V_1^* of the UBBB signal-flow graph in Figure 4.2(b) is described as pair $[P_1, E_1]$ with $P_1 = PR_1 \cup PC_1$, $PR_1 = \{g_{md5} + g_{ms1} + g_{ms2}\}$, $PC_1 = \{C_{gd5} + C_{db5} + C_{gs1} + C_{sb1} + C_{gs2} + C_{sb2}\}$, and $E_1 = \{F(1,2)\} \cup \{F(1,3)\} = \{g_{ms1}\} \cup \{g_{ms2}\}$. g_{md} and g_{ms} are small signal terminal transconductance parameters of the uncoupled device model of a MOSFET device. C_{gs}, C_{sb}, C_{gd} and C_{db} are the gate-to-source, source-to-bulk, gate-to-drain, and drain-to-bulk capacitances of a MOSFET.

The concept of ϵ-isomorphism defines an approximate matching of two symbolic sets within a given matching error. The concept is important to capture situations in which the common features of two circuits are more dominant than their distinguishing elements.

Definition (ϵ-isomorphism): For value ϵ, an ϵ-isomorphism of two symbolic sets S_1 and S_2 is the injective mapping $f : S_1 \rightarrow S_2$, such that:
$ers(s, f(s)) \leq \epsilon$, $\forall s \in S_1$,

where $ers(s, f(s))$ is the *matching error* function from Chapter 3 which captures the number of different symbolic terms.

Definition (minimal ϵ-isomorphism): An ϵ-isomorphism $f : S_1 \rightarrow S_2$ is minimal, if for all ϵ-isomorphisms $g : S_1 \rightarrow S_2$ and $g \neq f$ we have:
$\sum_{\forall s_i \in S_1} ers(s_i, f(s_i)) \leq \sum_{\forall s_i \in S_1} ers(s_i, g(s_i))$.

The definition states that a minimal ϵ-isomorphism produces the smallest cumulative matching error computed over all pairs of matched symbolic expressions of the two sets.

Definition (ϵ-matched nodes): Two nodes $V_1 = [P_1, E_1]$ and $V_2 = [P_2, E_2]$ are ϵ-matched if the following three ϵ-isomorphisms exist:
ϵ-isomorphisms $f_1 : PR_1 \rightarrow PR_2$, $f_2 : PC_1 \rightarrow PC_2$, and
minimal ϵ-isomorphism $g : E_1 \rightarrow E_2$.

Definition (ϵ-matched circuits): Given two circuits C_1 and C_2 and value ϵ, matching the two circuits within error ϵ requires finding the maximal sets of ϵ-matched nodes from the two circuits, such that for any two pairs of matched nodes, e.g., node $V_j \in C_1$ ϵ-matches node $W_k \in C_2$ and node $V_i \in C_1$ ϵ-matches node $W_p \in C_2$, the lexicographical ordering of nodes V_j and V_i in the UBBB model of circuit C_1 is the same as the lexicographical ordering of nodes W_k and W_p in the UBBB model of circuit C_2 (e.g., V_j precedes V_i in C_1's UBBB and W_k precedes W_p in C_2's UBBB, or V_i precedes V_j and W_p precedes W_k).

Intuitively, two matched circuits have similar signal flows through their matched nodes, hence signals pass in the same order through the matched nodes. In the above definition, the similarity of the signal flows is captured by the conditions regarding the lexicographic ordering of matched nodes.

The maximal sets of ϵ-matching two circuits describe the common electrical behavior of the circuits while unmatched nodes express the distinguishing aspects of the circuits.

Let's consider the maximal set for the matching of circuits C_1 and C_2, and a pair of matched nodes $V \in C_1$ and $V^* \in C_2$. For the lexical ordering of the nodes in the two UBBB models, we define that nodes $V_j \in C_1$ and $V_j^* \in C_2$ are the immediate predecessors of V and V^*, if V_j precedes V, V_j^*

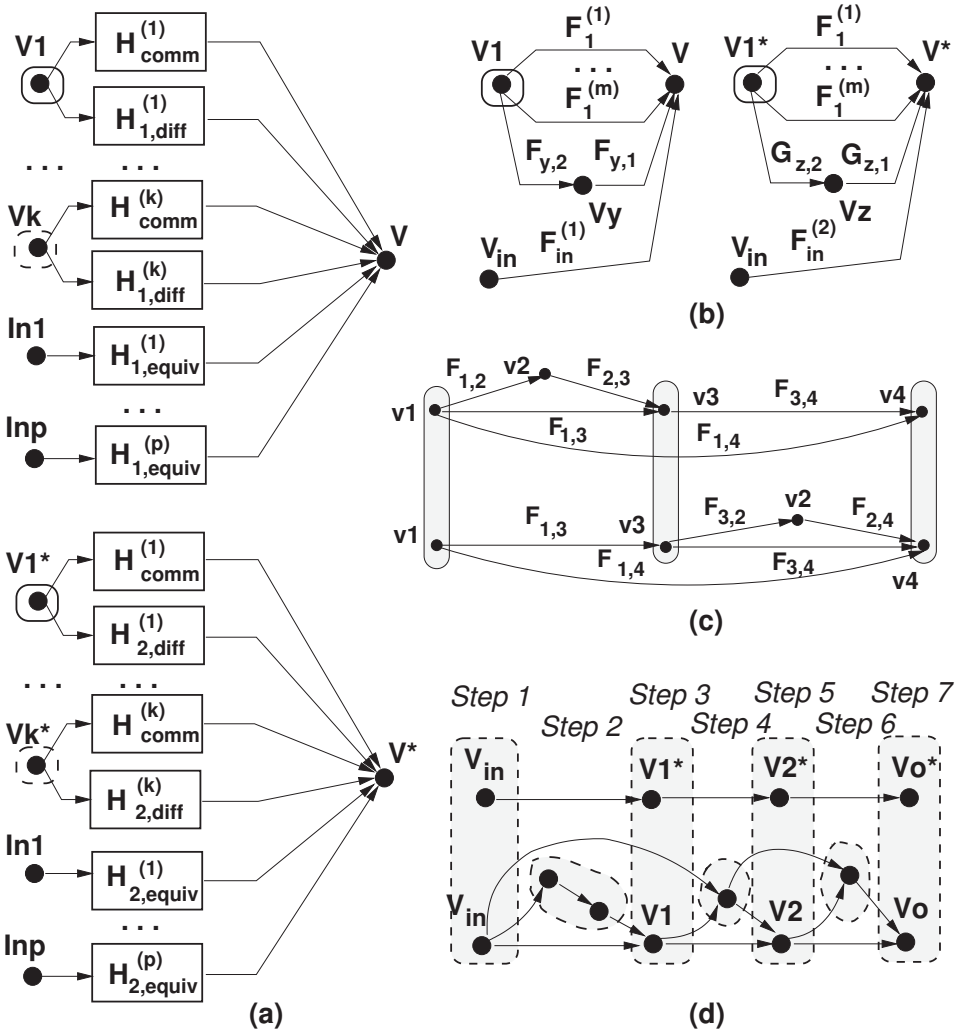

Figure 4.3: Electrical behavior description for comparison

precedes V^*, V_j and V_j^* are matched, and there are no other matched nodes between nodes V_j and V, and between nodes V_j^* and V^*. Let set $Prec_V$ be the set of all immediate predecessors of node V and set $Prec_{V^*}$ be the set of all immediate predecessors of node V^* (e.g., nodes $V_1 \in Prec_V$ and $V_1^* \in Prec_{V^*}$, ..., $V_k \in Prec_V$ and $V_k^* \in Prec_{V^*}$ are pairwise matched).

Lemma: The matched nodes $V \in C_1$ and $V^* \in C_2$ can be expressed as in Figure 4.3(a), where for any pair of matched immediate predecessors $V_i \in Prec_V$ and $V_i^* \in Prec_{V^*}$, $H_{comm}^{(i)}$ are the transfer functions produced by the edges directly connecting nodes V_i (V_i^*) and V (V^*); $H_{1,diff}^{(i)}$ ($H_{2,diff}^{(i)}$) are the transfer functions produced by the edges connecting V_i (V_i^*) and V (V^*) through unmatched nodes; and $H_{1,equiv}^{(q)}$ ($H_{2,equiv}^{(q)}$) are the transfer functions of the paths connecting inputs In_q ($q = 1, p$) and node V (V^*) without passing through any $V_i \in Prec_V$ ($V_i^* \in Prec_{V^*}$).

Proof: Due to superposition principle, we can consider a single input In and a single predecessor in sets $Prec_V$ and $Prec_{V^*}$. Let's assume that the lemma is false, hence there is a signal path that cannot be added to the transfer functions H_{comm}, H_{diff}, and H_{equiv}. However, every signal paths in a UBBB starts from an input In, thus the path should at least be part of the corresponding H_{equiv}. Hence, the assumption is incorrect.

Example: Figure 4.3(b) presents an instance of the general case in Figure 4.3(a). Nodes V_1 and V_1^* are assumed to be matched, thus set $Prec_V = \{V_1\}$ and set $Prec_{V^*} = \{V_1^*\}$. Nodes V_y and V_z are unmatched. Then, $H_{comm}^{(1)} = \sum_{i=1}^{m} F_1^{(i)}$, $H_{1,diff}^{(1)} = F_{y,1}F_{y,2}$, $H_{2,diff}^{(1)} = G_{z,1}G_{z,2}$, $H_{1,equiv} = F_{in}^{(1)}$, and $H_{2,equiv} = F_{in}^{(2)}$.

Example: Let's consider nodes V_o^* and V_o of the two amplifiers in Figure 4.2. Their immediate ϵ-matched predecessors are V_3^* and V_3, respectively. The common TF is $H_{comm}^{(1)} = F(3,o)P_3P_o$. For the Miller amplifier, $H_{1,diff}^{(1)} = H_{1,equiv} = 0$ (no unmatched node). For the class AB design $H_{2,diff}^{(1)} = F(3,y)F(y,o)P_3P_yP_o$ and $H_{2,equiv} = E(o,y)F(y,o)P_yP_o$, due to unmatched node V_y. P_i is the pole at node i.

The following lemma relates the voltages of two circuits in which the immediate predecessor sets *Prec* of the matched nodes include a single node.

Figure 4.3(d) shows such a case.

Lemma: In the s domain, the voltages at matched nodes V and V^* are linked as follows:

$$V = A(s)V^* + \sum_{j=1}^{p} B_j(s)V_{in,j} \tag{4.1}$$

with

$$A(s) = A_1(s)(1 + \frac{H_{1,diff} - H_{2,diff}}{H_{comm} + H_{2,diff}})$$
$$B_j(s) = [(H_{comm} + H_{1,diff})B_{1,j}(s) + H^{(j)}_{1,equiv} - A(s)H^{(j)}_{2,equiv}].$$

TFs H_{comm}, $H_{1,diff}$, $H_{2,diff}$, $H^{(j)}_{1,equiv}$ and $H^{(j)}_{2,equiv}$ are defined as in Figure 4.3(a). Terms $A_1(s)$ and $B_{1,j}$ are those in expression (4.1) set up for the matched immediate predecessors of nodes V and V^*. p is the number of inputs.

Proof: The proof is by induction. Let's consider the circuit structures in Figures 4.3(b), which correspond to the representation in Figure 4.3(a) for $k = 1$. Let's assume that the voltages at nodes V_1^* and V_1, the predecessors of nodes V^* and V, are related as in expression (4.1),

$$V_1 = A_1(s)V_1^* + \sum_{j=1}^{p} B_{1,j}V_{in,j}.$$

We prove the formula for nodes V^* and V.

$$V = (H_{comm} + H_{1,diff})V_1 + \sum_{j=1}^{p} H^{(j)}_{1,equiv}V_{in,j} \text{ and}$$
$$V^* = (H_{comm} + H_{2,diff})V_1^* + \sum_{j=1}^{p} H^{(j)}_{2,equiv}V_{in,j}$$

Hence, $V_1^* = \frac{V^* - \sum_{j=1}^{p} H^{(j)}_{2,equiv}V_{in,j}}{H_{comm} + H_{2,diff}}$. After replacing V_1^* in the expression of voltage V_1,

$$V_1 = A_1(s)\frac{V^* - \sum_{j=1}^{p} H^{(j)}_{2,equiv}V_{in,j}}{H_{comm} + H_{2,diff}} + \sum_{j=1}^{p} B_{1,j}V_{in,j}.$$

Next, V_1 is substituted in the above expression of V, hence

$$V = (H_{comm} + H_{1,diff})[A_1(s)\frac{V^* - \sum_{j=1}^{p} H_{2,equiv}^{(j)} V_{in,j}}{H_{comm} + H_{2,diff}} + \sum_{j=1}^{p} B_{1,j} V_{in,j}] +$$
$$+ \sum_{j=1}^{p} H_{1,equiv}^{(j)} V_{in,j}.$$

With $\frac{H_{comm}+H_{1,diff}}{H_{comm}+H_{2,diff}} = 1 + \frac{H_{1,diff}-H_{2,diff}}{H_{comm}+H_{2,diff}}$ and after rewriting,

$$V = A_1(s)(1 + \frac{H_{1,diff} - H_{2,diff}}{H_{comm} + H_{2,diff}})V^* +$$
$$+ \sum_{j=1}^{p}[(H_{comm} + H_{1,diff})B_{1,j} + H_{1,equiv}^{(j)} -$$
$$- A_1(s)H_{2,equiv}^{(j)}(1 + \frac{H_{1,diff} - H_{2,diff}}{H_{comm} + H_{2,diff}})]V_{in,j}.$$

This proves the lemma.

Example: This example considers the two-stage Miller amplifier in Figure 4.2(a) and the two-stage class AB amplifier [3] in Figure 4.2(c). The UBBB models of the two circuits are shown in Figure 4.2(b) and Figure 4.2(d), respectively.

The following symbolic expressions correspond to equation (4.1) for matched nodes V_4 and V_4^*. Their matched immediate predecessors are nodes V_2 and V_2^*. Nodes V_3 and V_3^* are not matched (nodes with $*$ are for the Miller amplifier):

For the two-stage class AB amplifier:

$$H_{1,diff} = F(2,3)P_3F(3,4)P_4; H_{1,equiv}^{(V_{in-})} = P_4[E(o,4) + P_3F(3,4)$$
$$[E(4,3) + E(o,3) + E(y,3) + P_1[F(in-,1) + E(2,1) + E(3,1)][F(1,3) +$$
$$F(1,2)P_2F(2,3)] + P_2F(2,3)[F(in-,2) + E(3,2)]]]$$
$$H_{1,equiv}^{(V_{in+})} = P_4[E(o,4) + P_3F(3,4)[E(4,3) + E(o,3) + E(y,3) + F(in+,3) +$$
$$P_1[F(in+,1)+E(2,1)+E(3,1)][F(1,3)+F(1,2)P_2F(2,3)]+P_2F(2,3)E(3,2)]].$$

For the two-stage Miller amplifier:

$$H_{2,diff} = F(2,3)P_3^*F(3,4)P_4^*; H_{2,equiv}^{(V_{in-})} = P_4^*[E(o,4) + P_3^*F(3,4)$$
$$[E(4,3) + E(o,3) + P_1^*[F(in-,1) + E(2,1) + E(3,1)][F(1,3) +$$
$$F(1,2)P_2^*F(2,3)] + P_2^*F(2,3)[F(in-,2) + E(3,2)]]]$$
$$H_{2,equiv}^{(V_{in+})} = P_4^*[E(o,4)+P_3^*F(3,4)[E(4,3)+E(o,3)+F(in+,3)+P_1^*[F(in+,1)+$$
$$E(2,1) + E(3,1)][F(1,3) + F(1,2)P_2^*F(2,3)] + P_2^*F(2,3)E(3,2)]].$$

Variables P_i (P_i^*) denote the pole of node V_i (V_i^*), with $P_i = \frac{R_i}{(1+sR_iC_i)}$. $H_{comm} = 0$ considering predecessors V_2 and V_2^*.

Lemma: The transfer function of the sub-graph induced by the nodes in the maximal set of ϵ-matched nodes describes the common part H_{comm} of the transfer functions of the two circuits. The induced sub-graph includes the nodes in the maximal sets and the arcs that connect these nodes.

Proof: Let's assume that the common part H_{comm} of the two transfer functions is not captured by the maximal set of matched nodes. Hence, there are unmatched nodes that contribute to function H_{comm}. But an unmatched node has resistive, capacitive, or coupling components that do not occur in the other circuit. Thus, the components cannot be part of function H_{comm}.

Example: Figure 4.3(c) presents the UBBBs of two circuits. The matched nodes are highlighted. The sub-graph induced by the matched nodes includes V_1, V_3, and V_4, and the arcs labeled as $F_{1,3}$, $F_{3,4}$, and $F_{1,4}$. The transfer function of the sub-graph is $F_{1,3}F_{3,4}P_1P_3P_4 + F_{1,4}P_1P_4$. Expression P_i defines the pole at node V_i.

Example: For the two amplifiers in Figure 4.2, the sub-graph induced by the perfectly matched nodes ($\epsilon = 0$) includes the signal inputs, and nodes V_1^* (V_1), V_2^* (V_2), V_4^* (V_4), and V_o^* (V_o). The set of associated arcs is composed of all F-labeled edges in Figure 4.2, except the encircled ones. TF H_{comm} is constructed from the expressions of all paths across these sets, such as $F(in-,1)F(1,2)F(2,3)P_1P_2$, $F(in-,1)F(1,3)P_1$, and $F(3,4)F(4,o)P_4P_o$.

Lemma: The transfer function of the sub-graph induced by the unmatched nodes of a circuit expresses TFs H_{diff} and H_{equiv}, the distinguishing part of that circuit compared to the second circuit. The sub-graph induced by the unmatched nodes includes the unmatched nodes, the set of direct arcs

between the unmatched nodes, the paths from inputs to the unmatched nodes, and the paths from the unmatched nodes to outputs.

Proof: The transfer function of the sub-graph induced by the unmatched nodes represents the paths that remain in the UBBB model after eliminating the paths of the sub-graph induced by the matched nodes. The paths represent the distinguishing features of the circuit compared to the second circuit.

Example: For the top circuit in Figure 4.3(c), the sub-graph induced by the unmatched nodes includes nodes V_1, V_2, V_3, and V_4, and arcs $F_{1,2}$, $F_{2,3}$, and $F_{3,4}$. The corresponding transfer function is $H_{1,diff} = F_{1,2}F_{2,3}F_{3,4}P_1P_2P_3P_4$. Similarly, for the bottom circuit, the induced graph includes nodes V_1, V_2, V_3, and V_4. The arcs are $F_{1,3}$, $F_{3,2}$, and $F_{2,4}$. The transfer function is $H_{2,diff} = F_{1,3}F_{3,2}F_{2,4}P_1P_3P_2P_4$.

Example: For the class AB amplifier (compared to the Miller amplifier), the set of unmatched nodes includes V_3 and V_y (for $\epsilon = 0$) with unmatched edges $F(3, y)$, $F(y, o)$. Examples of input-output paths contained by the overall $H_{2,diff}$ are $F(in-, 1)F(1, 2)F(2, 3)F(3, y)F(y, o)P_1P_2P_3P_yP_o$ and $F(in-, 1)F(1, 2)F(2, 3)F(3, 4)F(4, o)P_1P_2P_3P_4P_o$.

Lemma: For two circuits, the transfer functions H_{comm}, H_{diff}, and H_{equiv} have the following expression:

$$H = \sum_{p \in P} \frac{\prod_{t \in p} F_t(s)}{\prod_{V_j \in p} \frac{1}{R_j}(1 + sR_jC_j)}. \tag{4.2}$$

P are the signal paths of the following sub-graphs: the sub-graph induced by the matched nodes for H_{comm}, and the sub-graphs induced by the unmatched nodes for H_{diff} and H_{equiv}. V_j represents the nodes of a path p, t are the edges of a path p, and F_t are the edge labels.

Proof: The proof results from Mason's rule applied to signal-flow graphs that do not have feedback structures.

Example: The following transfer functions TF exist for the two structures in Figure 4.3(c). TF $H_{comm} = \frac{F_{1,3}F_{3,4}}{\prod_{j \in \{1,3,4\}} \frac{1}{R_j}(1+sR_jC_j)} + \frac{F_{1,4}}{\prod_{j \in \{1,4\}} \frac{1}{R_j}(1+sR_jC_j)}$, where P_i are the symbolic expressions of the pole in node i. $F_{i,j}$ is the sym-

bolic expression defining the connection between nodes i and j. TF $H_{1,diff} = \frac{F_{1,2}F_{2,3}F_{3,4}}{\prod_{j\in\{1,2,3,4\}}\frac{1}{R_j}(1+sR_jC_j)}$ is the difference between the top and bottom structure, and TF $H_{2,diff} = \frac{F_{1,3}F_{3,2}F_{2,4}}{\prod_{j\in\{1,2,3,4\}}\frac{1}{R_j}(1+sR_jC_j)}$ distinguishes the bottom and top parts.

Example: This property can be observed for the two amplifiers in Figure 4.2 when the expressions of the two input-output paths are combined to form $H_{2,diff}$.

The procedure to describe the impact of structural differences on performance attributes considers attributes $\mathcal{P}$ defined based on the circuit TFs. Such attributes are differential and common-mode gain, output transfer phase, output sensitivity to design parameters, circuit noise due to MOSFET device thermal and flicker noise, power supply rejection ratio, voltage swing limits at individual circuit nodes, and bandwidth.

4.4 Systematic Comparison Method

Figure 4.4 presents the proposed circuit comparison method. Inputs are the UBBB models of two circuits C_1 and C_2, the acceptable matching error, the performance attributes of interest, and any other relevant design constraints, e.g., variable ranges. The method includes four steps. Nodal matching, the first step, computes for every node $V_j \in C_1$ the lists of nodes in C_2 that are ϵ-matched. The lists form the possible matching space. The second step, circuit matching, finds the maximal set of ϵ-matched nodes for the two circuits using the lists of matched nodes computed in step one. Then, it relates the electrical behavior of each pair of matched nodes in the maximal set by computing TFs H_{comm}, H_{diff}, and H_{equiv} for the two circuits. The third step, constraint generation, produces symbolic constraints that relate the TFs computed in step two to the performance attributes of interest, e.g., DC gain, bandwidth, noise, CMRR, and sensitivity, and the modifications of the attributes due to the topological differences of the circuits. Equations (22)-(41) illustrate the constraints. Finally, performance characterization describes the capability of a design to meet the specified performance, including the free and trade-off variables available in each circuit, the trade-offs of the circuits, and the

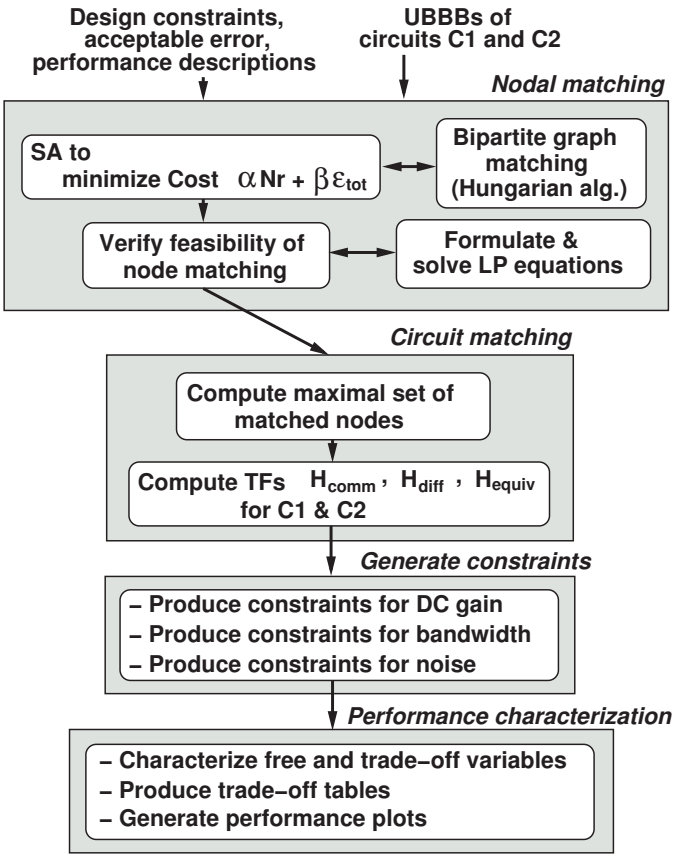

Figure 4.4: Systematic comparison method

performance plots. These four steps are detailed next.

4.4.1 Topological Nodal Matching

Nodal matching identifies the lists of nodes in circuit C_2 that are ϵ-matched to each node in circuit C_1. Inputs are the UBBB models of the two circuits. Outputs are the lists of ϵ-matched nodes for every node in the two circuits. Note that a node can be matched to several nodes in the other circuit if their symbolic sets meet the matching constraints.

The algorithm implements Simulated Annealing (SA) to produce the best matching for a given allowed error. The error counts the number of unmatched symbolic terms in the pole and edge expressions of the nodes.

Similarly to the method from Chapter 3, the SA cost function to be minimized is as follows:

$$Cost_{matching} = \alpha \times N + \beta \times \epsilon_{tot}. \tag{4.3}$$

Term N represents the total number of matched groups in the current solution. Note that each unmatched node counts as a separate group. Term ϵ_{tot} is the cumulative matching error for all pairs of matched nodes. It counts the number of unmatched resistive (e.g., transconductance) and capacitive terms (e.g., C_{gs}) in the pole expressions, the difference in number of edges for the two nodes, and the number of unmatched capacitive and resistive terms of the edge expressions. α and β are weights associated with the two terms. The first term of the cost function aims to find as many node matchings as possible while the second term controls the overall matching error.

Computing the cumulative matching error ϵ_{tot} requires first finding the minimum ϵ-isomorphism for all pairs of matched nodes, and then counting the number of unmatched terms of their symbolic sets. Finding the minimum ϵ-isomorphism of two nodes is difficult as it is harder than topological matching, an NP-hard problem. We expressed the problem as minimum weight bipartite graph matching. Figure 4.5(a) illustrates an example. Each node to be matched represents a partition, and every symbolic expression of a node is a vertex in the partition. For example, vertices e_1 and e_2 correspond to the graph partition describing node V_1, and vertices e_3 and e_4 are in the partition for node V_2. Each vertex (in one partition) is connected to all vertices from the other partition. The weight of each edge is the matching error between the symbolic expressions of the vertices. The objective is to find the edges that connect every vertex in one partition to exactly one vertex in the other partition, such that the overall matching error is minimum. These edges define the minimum ϵ-isomorphism between the two nodes. We used the Hungarian algorithm [118] to solve this problem as it has polynomial time complexity.

Every node matching solution found by SA is verified for feasibility. The verification step finds the unmatched terms, and then extracts the constraints that must be imposed on design variables of the symbolic expressions, so that the matching is valid. Otherwise, the unmatched terms would be dominant

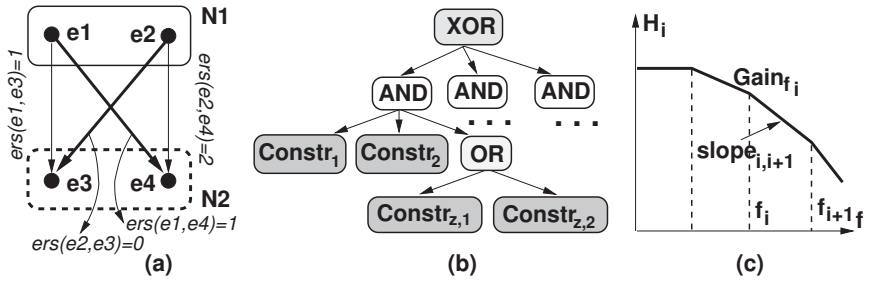

Figure 4.5: Minimum weight bipartite graph matching (a) for minimum ϵ-isomorphism; set of constraints (b); approximation for noise constraints (c)

and significantly change the behavior of the nodes. The feasibility of the extracted constraints is checked by solving the corresponding linear program (LP) formulation. The verified node matching is infeasible if the LP equations do not have a solution, and is feasible if the LP system is unbounded or has a single solution.

Example: Let's consider two nodes with the following unmatched edges: edge e_1 of node V_1 has the symbolic expression $sC_{gd6} - g_{mg6}$, and edge e_2 of node V_2 has the expression $sC_{gd11} - g_{mg11} + sC_2$. The pole resistive expressions for the two nodes are: PR_1 of node V_1 is $g_{md10} + g_{md12} + g_{mg12}$, and PR_2 of node V_2 is $g_{md4} + g_{md14}$. Finally, the pole capacitive expressions are: PC_1 of node V_1 is $C_{gs5} + C_{gd5} + C_{gb5} + C_1$, and PC_2 of node V_2 is $C_{gs7} + C_{gd7} + C_{gb7} + C_2 + C_3$.

The edges differ by one term, C_2. Similarly, the poles differ by one resistive term (g_{mg12}) and one capacitive term (either C_2 or C_3). Constraint extraction generates the following symbolic equations for which the two nodes can be matched:

$$C_2 \rightarrow \gamma, \text{ such that } e_1 \equiv e_2$$
$$g_{mg12} \rightarrow \gamma, \text{ such that } PR_1 \equiv PR_2$$
$$C_1 = C_2 + C_3, \text{ such that } PC_1 \equiv PC_2.$$

The first two constraints indicate that the nodes are matched, if C_2 and g_{mg12} can be sized to be negligible with respect to the matched components (γ is the acceptable approximation error). The last constraint defines the possibility of

matching either capacitance of node V_2 with that of node V_1.

For the above example, the LP formulation is as follows:

$$\begin{aligned}
\text{minimize: } & |0 - C_2| + |g_{mg12} - 0| + |C_1 - (C_2 + C_3)| \\
\text{subject to: } & C_2 \leq \gamma_{Clow} \\
& g_{mg12} \leq \gamma_{Rlow} \\
& |C_1 - (C_2 + C_3)| \leq \gamma_{Clow} \\
& C_2 \geq \gamma_{Chigh} \\
& g_{mg12} \geq \gamma_{Rhigh} \\
& C_1 \geq \gamma_{Chigh} \\
& C_2 + C_3 \geq \gamma_{Chigh}.
\end{aligned}$$

The objective function minimizes the overall errors of all unmatched variables of the pole and edge expressions. Constraints $\leq$ state that individual errors must be negligible, while constraints $\geq$ indicate that unmatched variables must still exist in the expressions, even though their values are small. They are needed to preserve the circuit node structure by avoiding to eliminate parameters or devices from the design. The boundary conditions, $\gamma_{Rlow(high)}$ and $\gamma_{Clow(high)}$, are set using typical transconductance and capacitance ranges for a technology.

4.4.2 Circuit Matching

The circuit matching step identifies the maximal set of ϵ-matched nodes in two circuits. Finding maximal sets is NP-complete as it is similar to best cost matching in directed graphs. The procedure in Algorithm 4.1 takes as inputs the UBBBs of two circuits C_1 and C_2 and the lists LV of ϵ-matched nodes in C_2 corresponding to every circuit node in C_1 (the lists are produced by nodal matching). It outputs the maximal set. The method computes the maximal set by matching a node $V \in C_1$ with a node $V^* \in C_2$ that is the first node in breadth-first order that is ϵ-matched with V and meets one of the following two conditions: (i) all input nodes of V and V^* are also matched in

Algorithm 4.1 Circuit Matching Heuristic

Inputs: Circuits C_1, C_2; List of matched nodes LV;
Output: Maximal set of ϵ-matched nodes of C_1 and C_2;
Match inputs of C_1 and C_2;
For all nodes V in circuit C_1
    Find $V^* \in C_2$ in *matched_list(V, LV)* as the first node
        in breadth-first order ***such that***
            All inputs of V and V^* are matched ***OR***
            Node V^* has smallest number of inputs;
    If $V^* \neq$ NULL ***then***
        Match nodes V^* and V in maximal set;
    Select next $V \in C_1$ in breadth-first order;

the maximal set, or (ii) V^* has the least number of inputs. The user indicates the matched inputs. Node V^* is in the list of ϵ-matched nodes identified for node V by nodal matching. Node V is unmatched if its list LV is empty. The method generates the maximal set of ϵ-matched nodes in a sequence.

Example: Figure 4.3(d) illustrates the algorithm. Let's assume that nodes V_1 and V_2 both have $\{V_1^*, V_2^*\}$ as their lists of ϵ-matched nodes. The input nodes are matched. Then, nodes V_1 and V_1^* are matched in the maximal set because V_1^* precedes V_2^* in the breadth-first traversal. Nodes V_2 and V_2^* are matched as this is the only matching alternative for V_2. Finally, outputs V_o and V_o^* are matched. Note that the nodes encircled with dashed line are unmatched. Also, the signal-flow structures between consecutively matched nodes correspond to Figure 4.3(b).

The maximal sets of matched nodes are used to compute TFs H_{comm}, H_{diff} and H_{equiv} for each circuit, as described in Section 4.3.

4.4.3 Constraint Generation

For two circuits, constraint generation computes their common and distinct constraints that link performance attributes to design variables. Inputs are TFs H_{comm} and H_{diff} calculated by circuit matching (for brevity of nota-

tion, we assumed that H_{diff} also includes H_{equiv}). The impact on performance attribute $\mathcal{P}erf_i$ (e.g., DC gain, bandwidth, noise, CMRR, and sensitivity) due to topological and TF differences are estimated using TFs H_{comm} and H_{diff} for every matched cluster of the circuits. Each TF generates a set of constraints that must be met to satisfy performance $\mathcal{P}erf_i$. Equations (22)-(41) are samples of constraints.

1. DC gain. A series connection of TFs H_{comm} and H_{diff} produces a DC gain of $DC\ gain_{H_{comm}} \times DC\ gain_{H_{diff}}$. A parallel connection creates a DC gain of $DC\ gain_{H_{comm}} + DC\ gain_{H_{diff}}$.

2. Bandwidth. The relation between the TFs H_{comm} and H_{diff} and bandwidth is estimated using Loop-Gain-Poles product (GPP) [119]:

$$\omega_{max} \approx (|1 - DC\ gain| \prod_{i=1}^{n} P_i)^{\frac{1}{n}}. \tag{4.4}$$

ω_{max} is the estimated maximum bandwidth, and n is the number of dominant poles P_i. The bandwidth corresponding to TF H_{comm} has the following upper bound:

$$\omega_{max}^{H_{comm}} \approx (|1 - DC\ gain_{H_{comm}}| \prod_{k=1}^{m} P_k)^{\frac{1}{m}} \tag{4.5}$$

where P_k are the m dominant poles of the common TF.

The difference TF H_{diff} modifies the bandwidth expression ω_{max} depending on how H_{comm} and H_{diff} are connected with each other, e.g., series or parallel.

For series connection, bandwidth corresponding to TF $H_{comm} \times H_{diff}$ is equal to the following value:

$$\omega_{max}^{H_{comm}H_{diff}} \approx (|1 - DC\ gain_{H_{comm}} DC\ gain_{H_{diff}}| \prod_{k=1}^{m+n} P_i)^{\frac{1}{m+n}} \tag{4.6}$$

where TF H_{diff} has n dominant poles that are not among the m dominant poles of TF H_{comm}.

The change in bandwidth due to TF H_{diff} is equal to the following expression:

$$\frac{\omega_{max}^{H_{comm}H_{diff}}}{\omega_{max}^{H_{comm}}} \approx \left(\frac{(DC\ gain_{H_{diff}} \prod_n P_i)^m}{(DC\ gain_{H_{comm}} \prod_m P_i)^n}\right)^{\frac{1}{m(m+n)}}. \tag{4.7}$$

The above expression indicates that the resulting bandwidth increases if the DC gain of H_{diff} is higher than for H_{comm}, and the distance of the dominant poles to the origin is higher for TF H_{diff} than for H_{comm}.

For parallel connection, the bandwidth change due to $H_{comm} + H_{diff}$ is estimated as follows. Let's assume that each TF is expressed as $H_i = \frac{\prod_j z_j}{\prod_i P_i}$, where z_j are zeros and P_i are poles. The two bandwidths relate as in the next expression:

$$\frac{\omega_{max}^{H_{comm}+H_{diff}}}{\omega_{max}^{H_{comm}}} \approx \left[\frac{[(1 + \frac{DC\ gain_{H_{diff}}}{DC\ gain_{H_{comm}}}) \prod_n P_i)]^m}{(DC\ gain_{H_{comm}} \prod_m P_i)^n}\right]^{\frac{1}{m(m+n)}}. \tag{4.8}$$

Expressions (4.7) and (4.8) are used repeatedly for generalized products and sums of TFs.

The overall bandwidth also changes because some of the dominant poles of TFs H_{comm} and H_{diff}, respectively, are canceled by the zeros of H_{diff} and H_{comm}. The bandwidth increase is higher if the poles are close to the origin [119]. Moreover, for TF sums $H_{comm} + H_{diff}$, pole-zero cancellations are possible only if H_{comm} and H_{diff} have at least one common pole. That common pole can be canceled out by the resulting zero. For example, if TFs $H_{comm} = \frac{z_1}{P_1 P_2}$ and $H_{diff} = \frac{z_2}{P_1 P_3}$ then the distinguishing poles P_2 and P_3 cannot be canceled out by the resulting zero $z_1 P_3 + P_2 z_2$, but the common pole P_1 can be eliminated. Additional bandwidth related constraints state that the secondary poles should be well separated from the origin and that the sum of the dominant poles is close to the origin [119].

The produced constraints can be expressed as shown in Figure 4.5(b). Nodes *OR* describe alternatives of constraints, which may or may not be used in design. For example, constraints for pole and zero cancellation can be optional. Nodes *AND* indicate sets of compulsory constraints, such as constraints expressing the dominant poles of TFs H_{comm} and H_{diff}. Nodes *XOR*

define mutually exclusive alternatives, such as the constraint sets created for each possible dominant pole set i.

3. Noise. Increasing the signal-to-noise ratio (SNR) requires decreasing the noise power $Power_{noise}$ in the frequency band of interest Δf. The noise power of noise source i is $Power_{noise} = \int_{\Delta f} S_i |H_i|^2 df$, where S_i is the power spectral density of the source and H_i is the noise TF. Let's assume that the noise TF H_i is approximated as shown in Figure 4.5(c), where each segment has a slope of -20$\frac{dB}{dec}$, and $P_{n,i}$ are the dominant poles of TF H_i. Then, $Power_{noise} \approx \sum_{f_i, f_{i+1}} S_i(Gain(f_i) - slope_{i,i+1} f)^2 df$. Frequencies f_i and f_{i+1} correspond to the consecutive poles $P_{n,i}$ and $P_{n,i+1}$. $Gain(f_i)$ is the gain at frequency f_i. The slope of the segment, $slope_{i,i+1}$, depends on the position of pole P_i, assuming that every pole introduces a slope change of -20$\frac{db}{dec}$.

For thermal noise, $S_i = 4kTcg_m$, hence $Power_{noise} = 4kTcg_m \times \sum_{f_i, f_{i+1}} (Gain(f_i)^2 \Delta f - Gain(f_i) slope_{i,i+1} \Delta f^2 + \frac{slope_{i,i+1}^2 \Delta f^3}{3})$. If $Gain(f_i) > \frac{slope_{i,i+1} f_{i+1}}{2}$ then $Gain(f_i)$ must decrease to reduce the noise power $Power_{noise}$. This originates a trade-off for gain $Gain(f_i)$ as lower gain produces a smaller noise power but affects other performance attributes, like bandwidth. The constraint analysis for the noise power of flicker noise is similar.

4.4.4 Performance Characterization

Performance characterization identifies the impact of the constraints deduced during the previous steps on circuit performance. The deduced constraints include those created by nodal matching (e.g., the conditions under which two nodes can be ϵ-matched), constraint generation process (i.e. pole and zero placement, pole - zero cancellation, and so on), and constraints imposed by the requirements of the application. Performance characterization uses these constraints to identify (i) free and trade-off variables, (ii) requirements for the variable values, such as variables that must be close to zero or have very large value, and (iii) variables that must be much smaller or larger than others. Free variables are variables that can improve performance attributes without worsening other performance attributes or affecting other variables. Trade-off variables improve certain attributes while damaging oth-

ers. The constraints on variable values and their nature (like free or trade-off variables) is used to infer their impact on the individual performance attributes. The produced impact data ranks the two circuits with respect to their capabilities in achieving certain performance values.

First, the set of constraints is used to identify the free and trade-off variables as well as requirements for their values. The impact of the variables on individual performance attributes is summarized through tables that present how the variable must be changed (e.g., increased or decreased) in order to improve that attribute. Tables 4.1 and 4.2 in Section 4.5 illustrate the concept. Second, the dependency of the performance attributes on free and trade-off variables is computed. The widths of the devices setting the free and trade-off variables are varied over their range. Note that the method presents the relative performance changes of two circuits, and not the absolute performance values (though this could be easily included). The analysis considers two cases for the values of matched parameters in the two circuits: common parameters are (i) large or (ii) small compared to the distinguishing parameters that are varied. Bias currents of circuit branches containing matched devices are kept constant to ensure that the common path is not altered by varying device sizes. For systematic comparison, the output branch of each circuit is also considered at fixed biasing.

Figures 4.7-4.8 exemplify the analysis results. Every attribute $\mathcal{P}erf_i$ is shown as a plot presenting its dependency on variable var_j. As shown in the figures, the dependency can indicate little correlation with the variable (e.g., pole P_1), linear dependency (i.e. pole P_3), and non-linearity of various gradients (such as poles P_2 and P_4). Note that the nature of the dependency plots depends not only on the nature of the constraints defining the variables but also the value ranges of the constants. Section 4.5 discusses these aspects in detail.

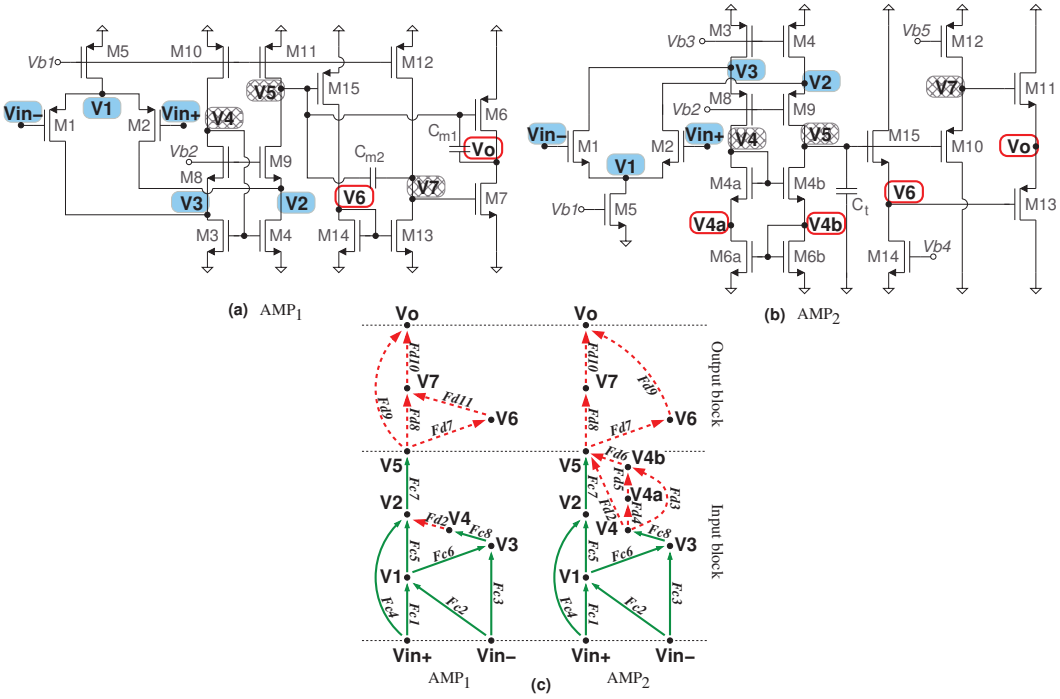

Figure 4.6: Two folded cascode amplifiers, (a) AMP_1 [4] and (b) AMP_2 [5], and (c) their UBBB models

4.5 Experiments

We illustrate the method by comparing the amplifier circuit AMP_1 [4] with the voltage amplifier AMP_2 [5]. Figure 4.6 shows the two folded cascode amplifier topologies. Figure 4.6(c) depicts the UBBB models of the two circuits. Appendix B.1 discusses an additional comparison data generation experiment for two low voltage amplifiers.

The execution time of the most computationally intensive parts, SA with Hungarian algorithm for nodal matching, is ≈300 seconds. The execution time of LP equation solving for checking the feasibility of a matching solution is about 0.1 seconds. The execution time was measured on a dual-core 2.0 GHz machine.

A. Nodal matching. In Figure 4.6, the perfectly matched circuit nodes are shown fully filled. The differential input stage nodes V_{in+}, V_{in-} (signal inputs), V_1, V_3, and V_2 in AMP_1 and AMP_2 share the same symbolic pole and

coupling expressions (Fc_i, $i = \overline{1,8}$) in both amplifiers. The partially matched nodes are shown with hashed fill (nodes V4, V5, V7 in AMP_1 and AMP_2). The unmatched nodes are encircled: circuit nodes V_6 and V_o (output) differ significantly between the two designs as their symbolic expressions cannot be matched. In addition, nodes V_{4a} and V_{4b} from AMP_2 have no equivalents in AMP_1. For the UBBB model graphs in Figure 4.6(c), the common node couplings (Fc_i) are presented with solid lines and the different couplings (Fd_j) are shown with dashed lines.

The set of matched devices (i.e. with all matched parameters like g_{mg}, C_{gd}, etc.) includes $M_{1,2}$, M_5, $M_{3,4}$, and $M_{8,9}$. Indexes are the same for both amplifiers. The other devices cannot be fully-matched and their parameters account for the different TFs. For example, at the partially matched node V_4, for the resistive pole component, $g_{md4a} + g_{mg4a}$ in AMP_2 cannot be matched to g_{md8} in AMP_1. Note that the matched edge Fc_7 is also considered in the expression of $H_{1,diff}$, due to the lack of a direct coupling from node V_4 to V_5 in AMP_2.

B. Circuit matching. The *input* block contains distinguishing sub-structures for poles at partially matched nodes V_4 and V_5, with an unmatched coupling F_{d2} from node V_4. The additional nodal structures of V_{4a} and V_{4b}, with the respective different graph edges Fd_j, $j = \overline{3,6}$, are specific only to AMP_2. The *output* block is characterized only by distinguishing attributes: the same number of nodes are encountered in both amplifiers, but with different sub-structures (V_6, V_7, and V_o). Different coupling between the output stage nodes are found in AMP_1 and AMP_2. For example, there is no coupling $V_6 \rightarrow V_7$ (F_{d11}) in AMP_2, while the output node is no longer linked to the block input node (V_5) but to the internal node V_6.

Using the matched and distinguishing structures, the method produces the set of symbolic transfer functions (TFs) for each circuit block, defining both the common and distinguishing symbolic terms.

The TFs to node V_5 of the *input* block of AMP_1 and AMP_2 are as follows:

$$\text{AMP}_1 : H_{V_5} = H^{(1)}_{comm} \times H^{(1)}_{1,diff} + H^{(2)}_{comm} \times H^{(2)}_{1,diff} \tag{4.9}$$

$$\text{AMP}_2 : H_{V_5} = H^{(1)}_{comm} \times H^{(1)}_{2,diff} + H^{(2)}_{comm} \times H^{(2)}_{2,diff} \tag{4.10}$$

where $H^{(1)}_{comm}$ and $H^{(2)}_{comm}$ are the common signal paths in both amplifiers and $H^{(i)}_{1(2),diff}$ $(i = \overline{1,2})$ captures the differences of the two *input* blocks:

$$H^{(1)}_{comm} = Fc_7P_2[(Fc_4 + P_1Fc_5Fc_1)V_{in+} + (P_1Fc_5Fc_2)V_{in-}] \tag{4.11}$$

$$H^{(2)}_{comm} = Fc_8P_3[(P_1Fc_6Fc_1)V_{in+} + (Fc_3 + P_1Fc_6Fc_2)V_{in-}] \tag{4.12}$$

$$H^{(1)}_{1,diff} = \frac{R_5}{1 + sR_5C_5},\ H^{(2)}_{1,diff} = \frac{R_5R_4Fd_2Fc_7}{(1 + sR_5C_5)(1 + sR_4C_4)} \tag{4.13}$$

$$H^{(1)}_{2,diff} = H^{(1)}_{1,diff},\ H^{(2)}_{2,diff} = \frac{R_5R_4\left(Fd_2 + A\right)}{(1 + sR_5C_5)(1 + sR_4C_4)} \tag{4.14}$$

where

$$P_i = \frac{R_i}{1 + sR_iC_i} \text{and } A = \frac{R_{4b}Fd_6}{1 + sR_{4b}C_{4b}}\left(Fd_3 + \frac{R_{4a}Fd_4Fd_5}{1 + sR_{4a}C_{4a}}\right).$$

The *output* blocks of the two designs are composed only of unmatched structures, resulting in *distinguishing* transfer functions to node V_o:

$$\text{AMP}_1 : H^{(3)}_{1,diff} = \frac{R_o}{1 + sR_oC_o}\left(Fd_9 + B\right) \tag{4.15}$$

$$\text{where } B = \frac{R_7Fd_{10}}{1 + sR_7C_7}\left(Fd_8 + \frac{R_6Fd_7Fd_{11}}{1 + sR_6C_6}\right)$$

$$\text{AMP}_2 : H^{(3)}_{2,diff} = \frac{R_o}{1 + sR_oC_o}\left(\frac{R_7Fd_8Fd_{10}}{1 + sR_7C_7} + \frac{R_6Fd_7Fd_9}{1 + sR_6C_6}\right). \tag{4.16}$$

C. Generate constraints. The impact of the common TFs on performance is characterized by first eliminating the impact of the distinguishing TFs, e.g., imposing the conditions that $H^{(2)}_{1,diff}$ match $H^{(2)}_{2,diff}$ or that the effect of $H^{(2)}_{1,diff}$ and $H^{(2)}_{2,diff}$ can be neglected.

Then, the DC gain improvement constraints for the common parts is equal to:

$$H_{comm}^{(1)} \equiv H_{comm}^{(2)} : \frac{g_{mg1}g_{ms8}}{g_{md1}+g_{md3}+g_{ms8}}(K_{diff}^{(1)}+K_{diff}^{(2)}) \nearrow . \tag{4.17}$$

$K_{diff}^{(i)}$ represent the constant values of the corresponding different TFs. There is limited DC gain improvement due to the common TFs as only device M_3 is not part of both numerator and denominator in equation (4.17). Also, setting the two poles of the common TFs (P_1, P_2/P_3) to be dominant with respect to those of distinguishing TFs in the *input* block of the amplifiers generates the constraints:

$$\frac{1}{2g_{ms1}+g_{md5}} \nearrow \text{ and } 2(C_{gs1}+C_{sb1})+C_{gd5}+C_{db5} \nearrow; \tag{4.18}$$

$$\frac{1}{g_{md1}+g_{md3}+g_{ms8}} \nearrow \text{ and}$$

$$C_{gd1}+C_{db1}+C_{gd3}+C_{db3}+C_{gs8}+C_{sb8} \nearrow . \tag{4.19}$$

Another trade-off appears with the constraints imposed for improving noise performance of the common TFs, namely with:

$$\frac{g_{ms1}}{(2g_{ms1}+g_{md5})(g_{md1}+g_{md3}+g_{ms8})} \searrow . \tag{4.20}$$

In this case, all g_m variables are trade-off variables with respect to the dominant pole and DC gain constraints. The trade-off between gain and noise with respect to g_{ms8} can be eliminated by allowing the variable to be sufficiently large, e.g., $g_{ms8} >> g_{md1}+g_{md3}$. A trade-off with the dominant position of pole P_2 (P_3) in constraint (4.19) still exists.

Transfer expressions (4.9)-(4.14) show that the *input* blocks of circuits AMP_1 and AMP_2 differ because of the poles at nodes V_5, V_4, V_{4a} and V_{4b} and the coupling between nodes $V_4 \rightarrow V_2$ in AMP_1 and $V_4 \rightarrow V_5$, $V_4 \rightarrow V_{4a} \rightarrow V_{4b} \rightarrow V_5$, and $V_4 \rightarrow V_{4b} \rightarrow V_5$ in AMP_2. For the *input* block of AMP_1, it produces the following gain improvement constraint:

$$\frac{K_1}{K_2+g_{md11}}+\frac{K_1K_3}{(K_2+g_{md10})(K_2+g_{md11})} \nearrow . \tag{4.21}$$

For AMP_2, the gain improvement is expressed as:

$$\frac{K_1}{K_2 + g_{md4b}} + \frac{K_1 g_{mg4b}}{(K_2 + g_{md4a} + g_{mg4a})(K_2 + g_{md4b})} C \nearrow, \tag{4.22}$$
$$\text{where } C = 1 - \frac{g_{ms4b}}{g_{ms4b} + g_{md6b} + g_{mg6b}}.$$

Constants K_i include matched parameters:

$$K_1 = \frac{g_{mg1} g_{ms8}}{g_{md1} + g_{md3} + g_{ms8}}, \; K_2 = g_{md8},$$
$$K_3 = \frac{g_{mg3} g_{ms8}}{g_{md1} + g_{md3} + g_{ms8}}. \tag{4.23}$$

The matching of common devices of the differential stage, i.e. $M_1 \equiv M_2$, $M_3 \equiv M_4$, and $M_8 \equiv M_9$, was considered.

DC gain of the *output* block of AMP_1 improves relative to the gain of the same block of AMP_2 if the following constraint is met:

$$\frac{1}{g_{md6} + g_{md7}} \left(g_{mg6} + \frac{g_{mg7} g_{mg13}}{K_4 + g_{md13}} D \right) \nearrow, \tag{4.24}$$
$$\text{where } D = \frac{g_{mg15}}{g_{md14} + g_{mg14} + g_{md15}}.$$

In the case of AMP_2, the *output* block source follower configuration's gain can be improved if:

$$\frac{1}{g_{ms11} + g_{ms13}} \left(\frac{g_{mg10} g_{mg11}}{K_4 + g_{ms10}} + \frac{g_{mg13} g_{mg15}}{g_{md14} + g_{ms15}} \right) \nearrow, \tag{4.25}$$

For both designs, $K_4 = g_{md12}$.

For improving CMRR, the underlying constraint involves parameters related only to matched devices:

$$\frac{g_{md5}}{g_{md5} + g_{ms1} + g_{ms2}} << 1, \; \searrow . \tag{4.26}$$

The differences in the two circuits impact differential and common-mode gain in the same manner, thus resulting in similar CMRR for both circuits.

Two dominant poles were considered for comparing the gain-poles product (GPP) and bandwidth of the two circuits. Topologies can have two poles located before the unity gain frequency, and the pole relative positioning and separation impacts significantly the AC performance. For brevity reasons, the discussion refers only to the output block, but a similar analysis was conducted for the input block too. The complete list of constraints is given in Appendix B.2.

The *output* block of AMP_1 is characterized by the dominant pole set P_o and P_7 (with P_6 non-dominant). The constraints for this set are as shown next:

$$\frac{1}{g_{md6}+g_{md7}} \nearrow \text{ and } K_{10}+C_{gd6}+C_{db6}+C_{gd7}+C_{db7} \nearrow, \tag{4.27}$$

$$\frac{1}{K_4+g_{md13}} \nearrow \text{ and}$$
$$K_{11}+C_{gd13}+C_{db13}+C_{gs7}+C_{gd7}+C_{gb7} \nearrow, \tag{4.28}$$

$$\frac{1}{g_{md14}+g_{mg14}+g_{md15}} \searrow \text{ and}$$
$$C_{gd15}+C_{db15}+C_{gs13}+C_{gd13}+C_{gb13}+$$
$$+C_{db14}+C_{gs14}+C_{gb14} \searrow \tag{4.29}$$

based on the distinguishing parameters in the configuration of poles P_o, P_7, and P_6. The circuit block GPP improvement constraints requires:

$$\begin{aligned} &K_{10}+C_{gd6}+C_{db6}+C_{gd7}+C_{db7} \searrow \text{ and} \\ &K_{11}+C_{gd13}+C_{db13}+C_{gs7}+C_{gd7}+C_{gb7} \searrow \text{ and} \\ &g_{mg6}+\frac{g_{mg7}g_{mg13}g_{mg15}}{g_{md14}+g_{mg14}+g_{md15}} \nearrow \text{ and } \frac{1}{K_4+g_{md13}} \searrow . \end{aligned} \tag{4.30}$$

The common parameters provide constants:

$$K_{10}=C_{m1} \text{ and } K_{11}=C_{gd12}+C_{db12}+C_{m2}. \tag{4.31}$$

The *output* block of AMP_2 is described by three feasible dominant pole sets: (1) P_6, P_7, (2) P_o, P_6, or (3) P_o, P_7. For the first set, the constraints on distinguishing variables are:

$$\frac{1}{g_{ms15}+g_{md14}} \nearrow \text{ and}$$
$$C_{gs15}+C_{sb15}+C_{gd14}+C_{db14}+C_{gs13}+C_{gd13}+C_{gb13} \nearrow; \tag{4.32}$$
$$\frac{1}{K_4+g_{ms10}} \nearrow \text{ and}$$
$$K_{12}+C_{gs10}+C_{sb10}+C_{gs11}+C_{gd11}+C_{gb11} \nearrow; \tag{4.33}$$
$$\frac{1}{g_{ms11}+g_{ms13}} \searrow \text{ and } C_{gs11}+C_{sb11}+C_{gs13}+C_{sb13} \searrow \tag{4.34}$$

for poles P_6, P_7, and P_o, respectively. For the remaining two pole sets, constraints (4.32)-(4.34) are reversed based on considered dominant and non-dominant poles.

The noise-related comparison of the two circuits is as follows. It includes the noise contribution of different features, while also providing the mechanism to reduce total output noise. The noise performance of the *output* block in AMP_1 is improved when:

$$\frac{g_{mg13}g_{mg15}}{g_{md15}+g_{md14}+g_{mg14}} \searrow \text{ and } \frac{g_{mg7}}{K_4+g_{md13}} \searrow \text{ and}$$
$$\frac{g_{mg6}}{g_{md6}+g_{md7}} \searrow \text{ and } K_{10}+C_{gd6}+C_{db6}+C_{gd7}+C_{db7} \nearrow \text{ and}$$
$$K_{11}+C_{gd13}+C_{db13}+C_{gs7}+C_{gd7}+C_{gb7} \nearrow \text{ and}$$
$$C_{gd15}+C_{db15}+C_{gs13}+C_{gd13}+C_{gb13}+$$
$$+C_{db14}+C_{gs14}+C_{gb14} \nearrow \tag{4.35}$$

Table 4.1: Performance trade-offs in AMP_1 output block

Variables	**Gain**	**Noise**	**Pole Set**	**GPP**
g_{md13}	$\searrow$	$\nearrow$	$\searrow$	$\nearrow$
g_{mg13}	$\nearrow$	$\searrow$	-	$\nearrow$
$C_{gd13} + C_{db13}$	-	$\nearrow$	$\nearrow$	$\searrow$
$C_{gs13} + C_{gd13} + C_{gb13}$	-	$\nearrow$	$\searrow$	-
$g_{md14} + g_{mg14}$	$\searrow$	$\nearrow$	$\nearrow$	$\searrow$
$C_{db14} + C_{gs14} + C_{gb14}$	-	$\nearrow$	$\searrow$	-
g_{md15}	$\searrow$	$\nearrow$	$\nearrow$	$\searrow$
g_{mg15}	$\nearrow$	$\searrow$	-	$\nearrow$
$C_{gd15} + C_{db15}$	-	$\nearrow$	$\searrow$	-
g_{md6}	$\searrow$	$\nearrow$	$\searrow$	-
g_{mg6}	$\nearrow$	$\searrow$	-	$\nearrow$
$C_{gd6} + C_{db6}$	-	$\nearrow$	$\nearrow$	$\searrow$
g_{md7}	$\searrow$	$\nearrow$	$\searrow$	-
g_{mg7}	$\nearrow$	$\searrow$	-	$\nearrow$
$C_{gd7} + C_{db7}$	-	$\nearrow$	$\nearrow$	$\searrow$
$C_{gs7} + C_{gd7} + C_{gb7}$	-	$\nearrow$	$\nearrow$	$\searrow$

while for the *output* block of AMP_2, the noise impact of distinguishing parameters is reduced if:

$$\begin{aligned}
&\frac{g_{mg10}g_{mg11}}{K_4 + g_{ms10}} \searrow \text{ and } \frac{g_{mg13}g_{mg15}}{g_{md14} + g_{ms15}} \searrow \text{ and} \\
&\frac{1}{g_{ms11} + g_{ms13}} \searrow \text{ and } C_{gs11} + C_{sb11} + C_{gs13} + C_{sb13} \nearrow \text{ and} \\
&C_{gs15} + C_{sb15} + C_{gd14} + C_{db14} + C_{gs13} + C_{gd13} + C_{gb13} \nearrow \text{ and} \\
&K_{12} + C_{gs10} + C_{sb10} + C_{gs11} + C_{gd11} + C_{gb11} \nearrow
\end{aligned} \tag{4.36}$$

D. Performance characterization. The *output* block variables and the related trade-offs are summarized in Table 4.1 for AMP_1 and Table 4.2 for AMP_2. The *output* block of both amplifiers have only trade-off variables. All distinguishing parameters, in either pole set configuration, have at least one

Table 4.2: Performance trade-offs in AMP_2 output block

Variables	**Gain**	**Noise**	**Pole Set**			**GPP**		
			1	**2**	**3**	**1**	**2**	**3**
g_{ms10}	↘	↗	↘	↗	↘	↗	↘	↗
g_{mg10}	↗	↘	-	-	-	↗	↗	↗
$C_{gs10} + C_{sb10}$	-	↗	↗	↘	↗	↘	-	↘
g_{md14}	↘	↗	↘	↘	↗	↗	↗	↘
$C_{gd14} + C_{db14}$	-	↗	↗	↗	↘	↘	↘	-
g_{ms15}	↘	↗	↘	↘	↗	↗	↗	↘
g_{mg15}	↗	↘	-	-	-	↗	↗	↗
$C_{gs15} + C_{sb15}$	-	↗	↗	↗	↘	↘	↘	-
g_{ms11}	↘	↗	↗	↘	↘	↘	-	-
g_{mg11}	↗	↘	-	-	-	↗	↗	↗
$C_{gs11} + C_{sb11}$	-	↗	↘	↗	↗	-	↘	↘
$C_{gs11} + C_{gd11} + C_{gb11}$	-	↗	↗	↘	↗	↘	-	↘
g_{ms13}	↘	↗	↗	↘	↘	↘	-	-
g_{mg13}	↗	↘	-	-	-	↗	↗	↗
$C_{gs13} + C_{sb13}$	-	↗	↘	↗	↗	-	↘	↘
$C_{gs13} + C_{gd13} + C_{gb13}$	-	↗	↗	↗	↘	↘	↘	-

conflicting variation. For example, in AMP_1, improving noise performance as in (4.35) and setting dominant pole position as in (4.27) by increasing $C_{gd6} + C_{db6}$ degrade bandwidth and GPP according to (4.30).

The performance change due to distinguishing parameters was analyzed next to gain insight on the qualitative and quantitative impact of each variable. Figure 4.7 illustrates the *output* block performance trade-off characterization of AMP_1 and AMP_2 when considering devices M_{13}, M_{14} and M_{10}, M_{15}, respectively. For the *output* block of circuit AMP_1, the distinguishing devices' widths W_{13} and W_{14} are varied. The corresponding trade-off variables are illustrated in the figure. Both widths were changed at the same rate and in the same direction, maintaining a constant current mirror ratio. The examined pole scenario is formed of poles P_7 and P_o. The latter was not illustrated as it

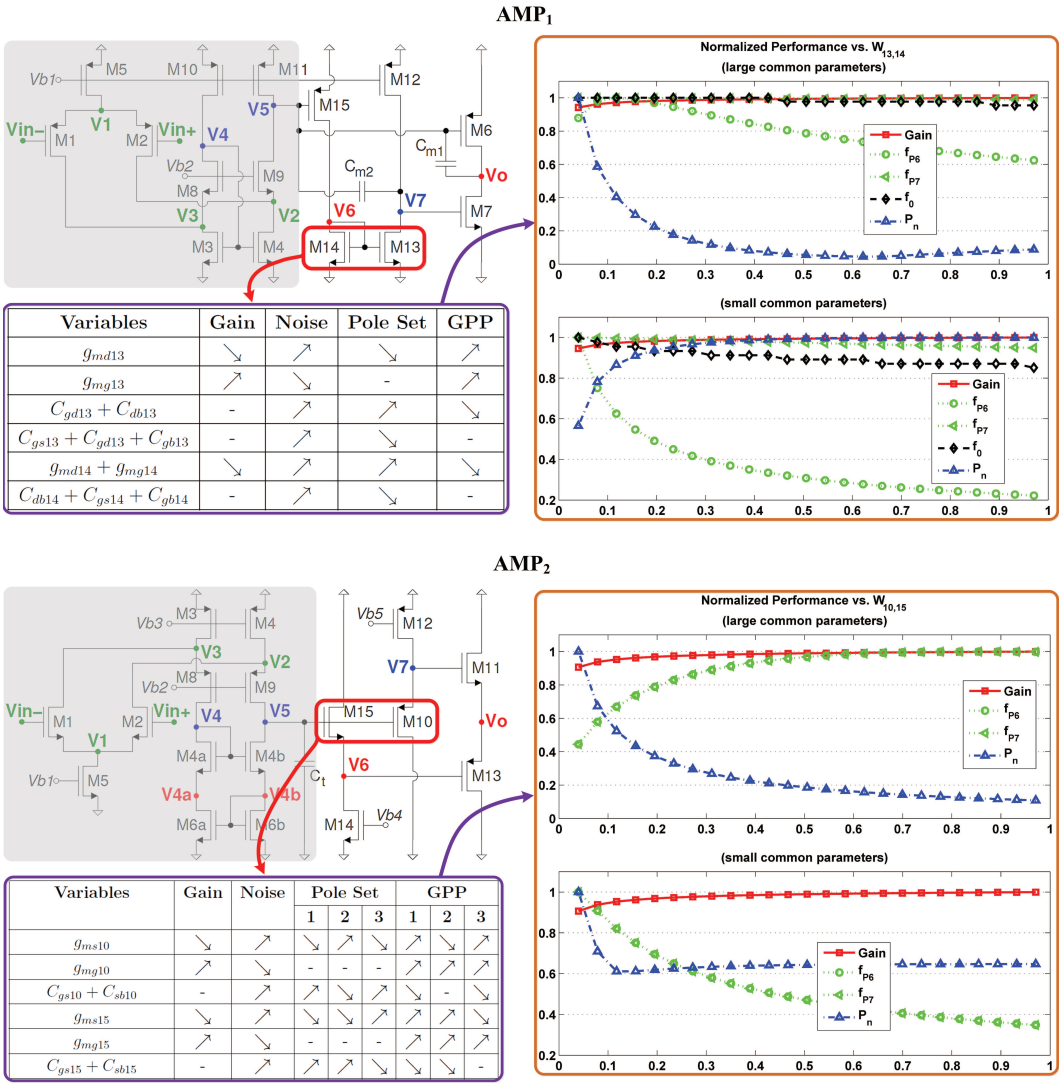

Figure 4.7: Output block performance trade-offs: AMP_1 with respect to widths W_{13} and W_{14} when widths W_{15}, W_6, and W_7 are constant; AMP_2 with respect to W_{10} and W_{15} when W_{14}, W_{11}, and W_{13} are constant

is considered constant in this case. Both poles are located before frequency f_0 on the frequency axis and are dominant. For either common parameter value, gain is not impacted by more than $\approx 5\%$ across the investigated range. For large common parameters, frequency f_{P7} remains relatively unchanged, resulting in a constant distance to frequency f_{Po}. As a result, unity gain frequency is

not degraded by more than $\approx 5\%$ for the maximum reduction in frequency f_{P7}. For small common parameters, a more pronounced degradation results, close to $\approx 15\%$, since frequency f_{P7} can now reduce by $\approx 5\%$. The proximity to the constant frequency f_{Po} transforms the pair of poles into a single second order pole, causing the faster reduction in frequency f_0 when widths W_{13} and W_{14} increase. For noise performance, the non-linear dependence illustrates that the total output noise is reduced when distinguishing parameters become comparable with common constants. Noise remains relatively unchanged after the first third of the analyzed sizing range.

For the *output* block of AMP_2, Figure 4.7 shows the performance variation when W_{10} and W_{15} are both increased at the same rate. The involved trade-off variables are also shown in the figure. As expected, the source follower configuration of the *output* block in AMP_2 exhibits less than unity gain across the investigated range. However, results suggest that an improvement of $\approx 10\%$ is still possible as W_{10} and W_{15} become larger. In terms of bandwidth, the dominant poles are P_7 and P_6. We note that as both device widths are changed, the relative pole separation remains constant with both P_7 and P_6 varying at the same rate. Opposing trends arise for the different common parameters cases, with a decrease in pole frequency for small values. While the resistive component remains relatively unchanged with the same dominant contribution of $g_{ms10,15}$, the capacitance increase in the case of small common parameters enforces the bandwidth performance degradation. Noise follows the same pattern in both scenarios, but is better controlled for large parameters.

Overall, the comparison results from Figure 4.7 suggest that for the considered distinguishing devices, the *output* block of circuit AMP_2 offers favorable trade-off behavior. In the case of large common parameters, the performance trends allow for the highest gain to be obtained while maximizing bandwidth and better limiting the noise impact of the distinguishing parameters. By comparison, gain and noise behavior are similar in circuit AMP_1, but bandwidth can deteriorate by up to 40%.

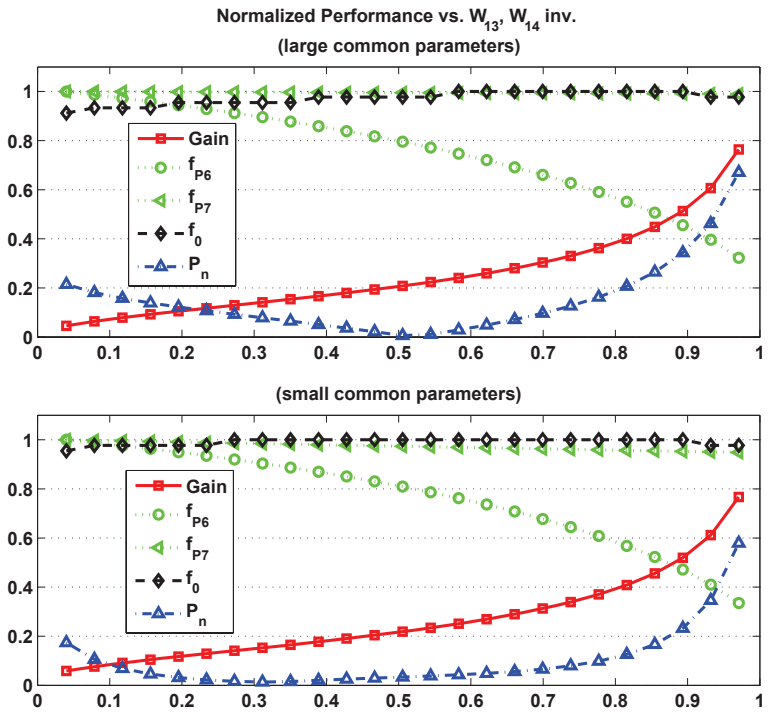

Figure 4.8: Output block performance trade-offs for AMP_1 when widths W_{13} and W_{14} vary in opposing direction

The performance trends for varying the current mirror M_{14} and M_{13} ratio of AMP_1 are given in Figure 4.8. For this analysis, we increase W_{13} while reducing W_{14}. Notable changes are exhibited in the behavior of gain. As expected, DC gain can now be increased as the current mirror ratio increases and is maximized for the highest ratio W_{13}/W_{14}. The trade-off with noise is relaxed for the initial half of the variation range, when the W_{13}/W_{14} ratio is less than unity. However, in the second half, when the ratio becomes greater than one, the noise performance is dominated by the increasing value of W_{13}. The small common parameter case is favorable as an extended range of values of the variables offers lower noise. In either scenario, as the current mirror ratio approaches the investigated maximum, the gain-noise trade-off becomes dominated by noise which worsens faster than gain improves.

Figure 4.9 presents an *input* block comparison of the two amplifiers. For AMP_1, the considered devices are the current sources $M_{10} \equiv M_{11}$ biasing

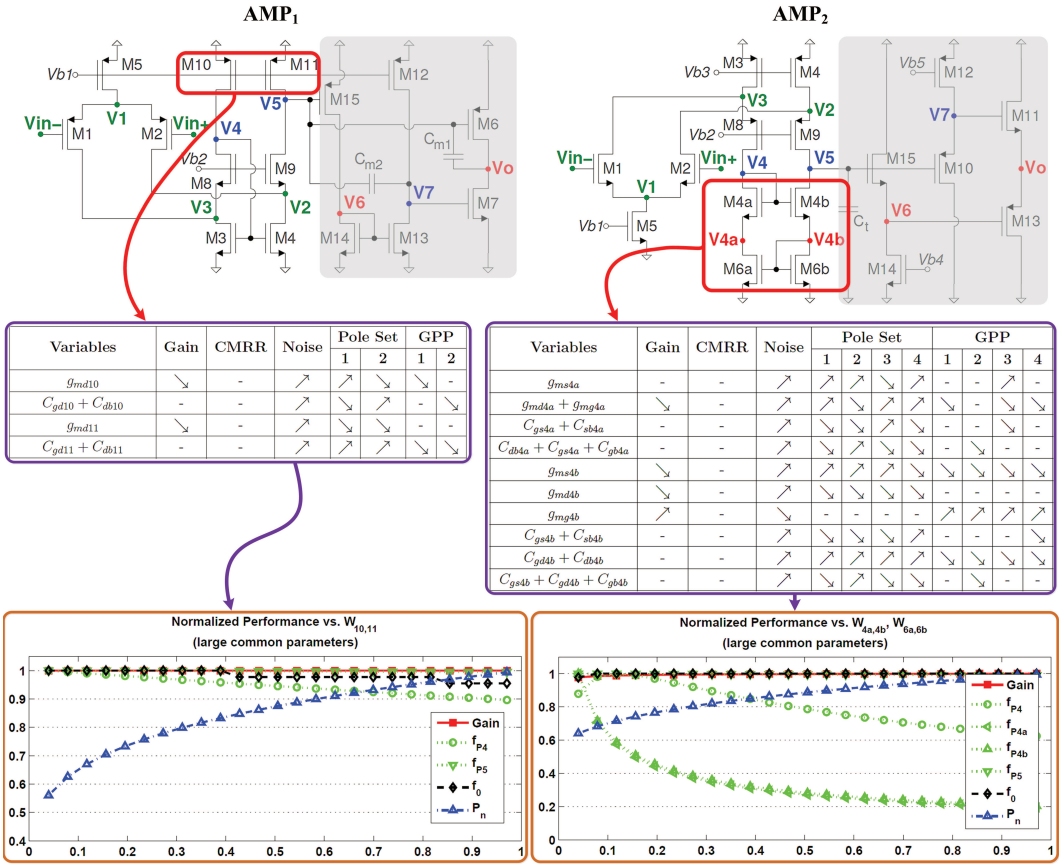

Figure 4.9: Input block performance trade-offs for AMP_1 (devices $M_{10} \equiv M_{11}$) and AMP_2 (devices $M_{4a} \equiv M_{4b}$ and $M_{6a} \equiv M_{6b}$)

the cascode transistors. In the case of AMP_2, we consider the improved Wilson current mirror devices $M_{4a} \equiv M_{4b}$ and $M_{6a} \equiv M_{6b}$. The corresponding trade-off variables related to these devices are shown in Figure 4.9. Normalized performance plots are given for varying the transistor widths at the same rate in each circuit when relatively large common parameters are considered. Side-by-side comparison suggests that this scenario is more beneficial in AMP_1 than in AMP_2. Gain, noise, frequency of pole P_5, and unity gain frequency exhibit highly similar behavior in both designs. However, for AMP_2 pole P_4 frequency (and bandwidth performance) can decrease by up to 40% when $W_{4a} = W_{4b} = W_{6a} = W_{6b}$ widths are increased. In contrast, for AMP_1, the same performance decreases by at most 10% as $W_{10} = W_{11}$ increase.

A detailed description of the *input* block comparison data is offered in Appendix B.2.

4.5.1 Comparison Experiment Summary

The gain of AMP_1 can be controlled by six different device widths through 12 distinguishing small-signal parameters. There are 4 direct and 8 inverse relations between gain value and parameters. In terms of the variations required to improve gain, there are 4 situations of opposing trends (indicating design trade-offs). For noise, the same 6 device widths are involved, influencing a total of 44 distinct transconductance and capacitance parameters. They involve 25 direct (out of which 21 are square-root dependences) and 35 inverse relations, with 10 conflicting variation cases between parameters. In the case of pole sets and bandwidth, the 6 transistor widths control 35 parameters found in 26 direct and 48 inverse relations for all pole sets considered. There are 39 design trade-off expressions.

For AMP_2, gain can be controlled by 7 different device widths through 16 distinguishing small-signal parameters. There are 6 direct and 11 inverse relations. There are 7 opposing trends (indicating design trade-offs). For noise, the same 7 widths are involved, influencing a total of 61 distinct transconductance and capacitance parameters. They involve 30 direct (out of which 24 are square-root dependences) and 44 inverse relations, with 19 conflicting variation cases between parameters. In the case of pole sets and bandwidth, the 7 transistor widths control 50 influencing parameters found in 78 direct and 203 inverse relations for all pole sets considered. There are 136 trade-off expressions.

The comparison suggests that AMP_2 offers greater flexibility in achieving performance improvements since it presents a considerably increased number of distinguishing design variables that can be used to control performance. AMP_2 is likely to perform better for low noise, high bandwidth applications. The input block characteristics are well controlled by parameters related to $M_{6a/6b}$: noise minimization and unity gain frequency increase occurs at node V_5. A lower noise can be transferred to circuit output V_o through the char-

acteristic of the output block, which has additional noise reduction through $M_{10/15}$ while keeping relatively unchanged the bandwidth behavior. The noise of AMP_1 is bounded, hence cannot be improved through distinguishing parameters.

The size of the symbolic expressions was manageable due to the *partitioning* of the circuits into topologically matched sub-structures (like the input and output blocks of the two amplifiers) and separating the symbolic signal paths into common and distinct paths. However, the complexity of the symbolic expressions increases in situations in which there is little matching of topologies and electrical behavior, and therefore, the circuits and their TFs cannot be decomposed. We intend to extend the proposed method to include a more general matching mechanism, in which entire clusters of nodes in a circuit are merged into super-nodes (characterized by TFs and not poles) and edges, also labeled by TFs, connect the super-nodes. The matching steps are to be conducted on this more abstract representation. We expect that a critical problem is to understand how node merging must be controlled to obtain good quality comparison results.

The imprecision of the circuit comparison method is mainly due to the nodal and circuit matching steps. Certain symbolic terms are neglected as long as the matching error is less than ϵ and constraint feasibility is satisfied. This can result in (small) overestimation of TFs H_{comm} and (small) underestimation of the TFs H_{diff}. Therefore, the constraints between variables and performance attributes might incorporate small inaccuracies. Another source of imprecision is due to considering a limited number of dominant poles for constraint generation (usually 2 or 3 poles). However, the trade-off tables are less affected by imprecision as they offer qualitative descriptions, which are less likely to change once the main trends are captured. UBBB models are accurate compared to Spice simulation [25]. Performance plots use UBBB models, thus are also insensitive to the imprecision of the comparison method. Future work could study the impact of the matching error ϵ on the imprecision introduced during comparison.

In a manual design flow, assuming the UBBB models for circuits are available, the extra effort for using the comparison method relates to correlating the equations of the constraints between variables and performance, the trade-off tables, and the performance plots. Also, effort is needed to select good values for ϵ, and deciding which alternatives to analyze for possible pole placements and pole-zero cancellations.

4.5.2 Applications of Circuit Comparison Method

The proposed circuit comparison method can be utilized for the following three design automation tasks.

1. Incremental topology refinement. The proposed circuit comparison method is useful to identify incremental topology changes that can combine the benefits of each topology. For example, let's consider a high gain requirement. For the *output* block of AMP_2, the distinguishing parameters of devices $M_{10/15}$ do not add gain due to their source follower configuration, which introduces a DC transfer contribution $\propto g_{mg}/(g_{mg} + g_{md})$. By comparison, the common source device M_{15} in AMP_1 increases gain. An incremental change in AMP_2 for device $M_{10/15}$ can impact gain by transforming the DC transfer to $\propto g_{mg}/g_{md}$ (and changing AMP_2 to a 2-stage design). The change still reduces noise for specific sizing strategies. However, flexibility of higher frequency behavior is diminished as the resistive components of the poles at nodes V_6 and V_7 are no longer correlated to the device's $1/g_{mg}$ parameter. In the modified design, $1/g_{md}$ controls this aspect and is primarily set by the current of $M_{12/14}$. Hence, under fixed bias, increasing $W_{10,15}$ to improve g_{mg} and gain would negatively impact the frequencies of poles P_6 and P_7, dominated by the increasing capacitive components.

A similar application is circuit topology feature reuse for new constraints, including those due to design migration to different fabrication process. A topology feature is a small structure of devices that can be added to improve the performance of a circuit without modifying its functionality. The performance trade-offs and performance bottlenecks (limitations) of an existing topology can change when moving to another process. The new bottlenecks

can be tackled by searching a library of previous designs to find topologies with constraints similar to those causing the bottlenecks but also with distinguishing features that compensate for the bottlenecks. The distinguishing features are then reused in the current solution.

2. Circuit optimization. Understanding the nature of the trade-offs is important to find sizing strategies that relax (or even eliminate) some performance trade-offs, and to concentrate on the variable ranges that are more likely to produce high quality solutions. For example, in the case of large common parameters W_{10} and W_{15} for AMP_2, an increase in bandwidth is obtained as W_{10} and W_{15} increase. However, this can only be performed for the first half of the investigated dimension range. The non-linear dependence ends quite quickly the bandwidth growth. Therefore, further increasing the differentiating parameters of AMP_2 only deteriorates power consumption and increases area while posing no advantages for bandwidth. Similarly, in AMP_1, increasing W_{13} and W_{14} beyond the midpoint of the range, while large common parameters are considered (see Figure 4.7), does not further improve noise performance, but decreases bandwidth. This insight allows circuit parameter optimization to focus on the more promising sub-ranges of the variables. In [120], a parameter optimization technique for reconfigurable $\Delta\Sigma$ modulators is presented, in which performance trade-off tables guide the search process.

3. Topology selection. The insight obtained from circuit comparison can be used to infer the relative limits to which performance can be improved through the distinguishing parameters in each design. For example, having small common parameters in AMP_1 shows that while W_{14} is kept greater than W_{13}, gain can be increased by $\approx 15\%$. At the same time, output noise can be kept relatively constant, effectively decoupling the two performances. For large reverse ratios of the devices, in the final quarter of the analyzed range, the trade-off between gain and noise becomes more demanding, as noise deteriorates faster than gain can be improved. For AMP_2, the gain-noise trade-off can be relaxed for a larger portion of the investigated sizing range. This offers AMP_2 greater flexibility in addressing other trade-offs, since a vaster range of relative sizing between devices $M_{4a,4b}$ and $M_{6a,6b}$ can be explored. For

this case, varying the sizing across $\approx 70\%$ of the range increases gain linearly by up to 20% while noise can be relatively improved. The insight is useful in topology selection as it indicates which circuit structure is better suited for a given specification.

4.6 Summary

This chapter proposed a novel technique for systematically producing comparison data between two analog circuits. The data refers to DC gain, bandwidth, noise, CMRR, and sensitivity. The nodes with similar electric behavior in the two circuits are found through a dual matching approach of circuit topologies and symbolic expressions. Dissimilarities are also identified in the process. Next, the method computes the constraints that relate the electric behavior to changes of the performance attributes. Using the constraints, the final step produces the comparison data, which includes modification of design trade-offs, availability of free design variables, and achievable performance values.

Future improvements of the method include extending the analysis to nonlinear performance. Another direction is to improve the circuit matching heuristic, e.g., by using information on the signal paths that are decided as dissimilar to prune the lists of matching candidates of a node. Finally, the circuit similarities and dissimilarities extracted as symbolic expressions can be validated through numeric circuit simulations of the two circuits. This requires a sampling procedure that comprehensively covers the device size ranges, such that the numeric values meet the trade-offs and constraints found by the systematic analog circuit comparison technique.

Chapter 5

A Prototype Framework for Modeling the Analog Circuit Design Feature Variety

This chapter takes preliminary steps towards developing a prototype framework to model the design feature variety in analog circuits, such as the various topological structures present in a set of circuits devised for the same purpose (like OpAmps or OTAs). The insight is important to characterize the novel and similar features in a circuit, the conditions under which existing design features can be reused in new circuits, and the exploration of new conceptual designs. Based on the methods from Chapters 3 and 4, this work describes the four basic operators used in modeling: circuit comparison, circuit instantiation-abstraction, circuit combination, and design feature induction. A case study presents the circuit feature variety modeling for a set of OpAmps.

5.1 Introduction

Most design tools for analog and mixed-signal circuits target tedious but conceptually-well understood, routine activities, like transistor sizing and device placement and routing. Having enough knowledge (insight) on a design

task enables one to formulate explicit, closed-form descriptions of the task, e.g., models and rules [13, 28, 73, 74, 121]. The design task is then accomplished by solving the closed-form descriptions using mathematical solvers or heuristic optimization algorithms.

In contrast, there is less knowledge available for design problems that introduce conceptually new challenges or problems which evolve over time. There are usually no closed-form descriptions or specific design rules available unless a significantly large number of conceptually-similar designs are solved first manually. The solving process involves reasoning and decision making in an effort to address open-ended issues and create the missing domain knowledge. In particular, circuit topology design and refinement for novel applications requires significant conceptual design for finding new principles of signal processing and control. New ways of connecting structurally the devices, novel rules for constraining the device operation, and new substructures might emerge during reasoning. Devising a representation model to express expanding and evolving circuit design knowledge is a first step towards creating new design tools that can effectively tackle a wide range of problems without closed-form descriptions.

Analog circuit topology design has been challenging to automate due to the hardness of specifying the related design space and identifying rules and algorithms to explore the space [73]. There is arguably no known closed-form expression of the unrestricted design space. For particular cases, there exist algorithms that utilize a customized set of design rules [16] or a closed-form representation of a class of possible topologies [28]. Another popular option is evolutionary algorithms. Early unconstrained techniques [14] relied on stochastic search in large populations, over successive generations to compensate for the missing domain knowledge. However, there was no guarantee that feasible topologies would be created. Improved, higher quality results are obtained by constraining the search through various amounts of domain-specific rules [8]. The study in Chapter 2 and the analysis of ONCRs from Chapter 3 have shown that even such techniques still produce some *unusual* designs having different structures than manual designs and which human de-

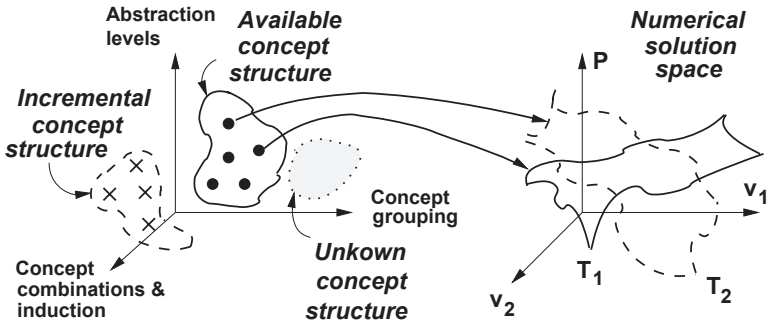

Figure 5.1: Concept structure model and traditional design space model

signers do not generally accept as quality solutions. The approach in [23] overcomes this aspect by evolving single-stage and two-stage OpAmp topologies from a designer-specified building block library. The resulting designs are *trustworthy by construction* as the hierarchical library ensures correct connectivity of well-known structures. An inherent limitation is the diversity of the set of basic building blocks in the library. For new applications, the set of blocks may not present any combination with sufficient performance. An extension in [23] attempts to address this by introducing controlled GP operators on the Pareto optimal topologies of an original run. Small changes are preferred to prevent drastically transforming the original trustworthy topologies into unusual designs. However, the random nature of the operators does not offer reusable insight on any novel conceptual designs that were explored during the evolutionary process.

This chapter presents a formal model for defining concept structures to describe domain knowledge in analog circuit design. The knowledge can be used in synthesis and refinement of analog circuit topologies through a process that mimics expert designer reasoning or to systematically characterize and enhance the set of building blocks of library-based synthesis techniques. Figure 5.1 shows that concept structures expand the traditional design space model, used by design tools for transistor sizing and layout generation. Concept structures express symbolically the design features that can create new conceptual solutions (e.g., circuit topologies, signal flow graphs, etc.) at various levels of abstraction. Each conceptual solution (or concept) originates

specific performance trade-off surfaces between the related design variables, like surfaces T_1 and T_2 in Figure 5.1 defining the trade-offs between performance P and variables v_1 and v_2. Trade-off surfaces are part of the traditional design space model, and are explored through well-known circuit design methods, including optimization-based techniques.

The concept structure model expresses the design feature variety of analog circuits. The concept structure model has two basic operators, (1) circuit comparison to relate the topological, behavioral and performance characteristics of different circuits, and (2) circuit instantiation-abstraction to organize the features as conceptual abstractions and instances at various levels. In addition, two operators are defined to express the extension of a concept structure: (3) circuit feature combination to create new concepts based on present circuit features, and (4) design feature induction to deduce more features following the same patterns as the existing ones. The concept structure characterizes the common and unique features in a circuit compared to other designs, the conditions under which existing features can be reused to meet new specifications, and the exploration of new conceptual designs.

In previous work, an objective-driven topology design transformation in the form of a design rule guides the synthesis search mechanism [22]. The most relevant transformations are probabilistically chosen based on their expected improvement which is heuristically estimated from the performance of the current population of solutions. Similarly, the proposed combination and induction operators discussed in this chapter only return feasible new circuit concepts that can improve performance or relax/eliminate trade-offs. In our proposed modeling framework, operators can be applied at different levels of abstraction to derive new conceptual solutions and can be used to systematically address the performance limitations without a stochastic mechanism. For example, based on the systematic comparison operator, the circuit feature that relates to a performance bottleneck is precisely identified. Only combinations of new features that change the nature of the bottleneck are accepted and added to the concept structure model. The topology refinement procedure presented in Chapter 6 constitutes an example of the process.

In [23], the designer-specified building block library is organized by means of *flexible blocks* in a similar fashion to the way in which the proposed abstraction-instantiation operator is used in the concept structure model. The flexible blocks select among their possible instances through *OR* operators similarly to the proposed modeling framework instantiating different branch concepts based in the specific signals and structures used. Parameters (structure and behavior) relating to higher levels propagate downwards through the hierarchical structure. The abstract description differentiates the two methods. In [23], the description of a flexible block abstracts all details of the underlying possible implementations and only keeps the generic functionality and port configuration (e.g., a current mirror flexible block contains no information about the details of its three possible instances). In our approach, a structural description is used at all levels of the representation. In the abstraction process, differentiating aspects among instances are replaced by abstract signals and structures. We maintain the common attributes of all instances to the highest level possible in the representation (e.g., a current mirror abstract concept always has at least one simple current mirror as part of any of its instances). The structural description present at any abstraction level enables a compact characterization of a class of circuit concepts (i.e., summary of performance achievable by its instances). This facilitates the development of more efficient search mechanisms that can *knowledgeably* explore/ignore partitions of the concept structure which do/don't present the mechanisms to achieve desired performance and focus only on promising regions.

The chapter has the following structure. Section 5.2 offers an overview of the proposed concept structure model by introducing the four basic operators and briefly describes an envisioned synthesis flow utilizing the proposed model. Section 5.3 discusses a case study for the concept structure of OpAmp circuits.

5.2 Operators for Creating Concept Structure Design Knowledge Representations

Given a specification (application) Ψ and a set of circuits Ω that implement Ψ, the goal is to construct a knowledge representation that distinguishes the circuits $C_i \in \Omega$ based on the conceptual steps used in realizing specification Ψ as well as the constraints under which the functionality is achieved.

The proposed knowledge representation is called a concept structures. It has two basic operators for building the structure: (1) circuit comparison and (2) circuit instantiation-abstraction. Two other operators, (3) concept combination and (4) feature induction are used to extend the concept structure. The four operators are discussed next.

5.2.1 Circuit Concept Comparison

Comparing two circuits $C_1, C_2 \in \Omega$ finds the common and distinct signal flow paths of the two circuits, and then computes the common (e.g., transfer function H_{comm}) and the distinguishing (e.g., transfer functions $H_{1,diff}$, $H_{2,diff}$) electrical behavior of the circuits, and characterizes the impact of the common and distinguishing behavior with respect to specification Ψ.

Based on the techniques for topological and symbolic matching presented in Chapters 3 and 4, the impact of H_{comm} and H_{diff} on circuit performance is found, i.e. gain, bandwidth, noise, and CMRR. The trade-off expressions of each circuit are also produced. These explicitly show the performance benefit of a circuit compared to another as well as its performance bottlenecks.

Performance Bottleneck Example: Concept $D3$ from Figure 5.8, a simple differential pair, presents a bottleneck for gain performance. It involves the DC component of the direct coupling variables from the signal input attribute $(-g_{mgx})$ and the pole resistive component $Rp3 = 1/(g_{mdx}+g_{md})$ (variables g_{mgx} and g_{mdx} relate to the input device M_x.). For identical differential paths, the expression of the gain bottleneck in concept $D3$ is given by $Gain_{D3} = g_{mgx}Rp_3$. Figure 5.2 (top plot) illustrates the normalized gain behavior with respect to

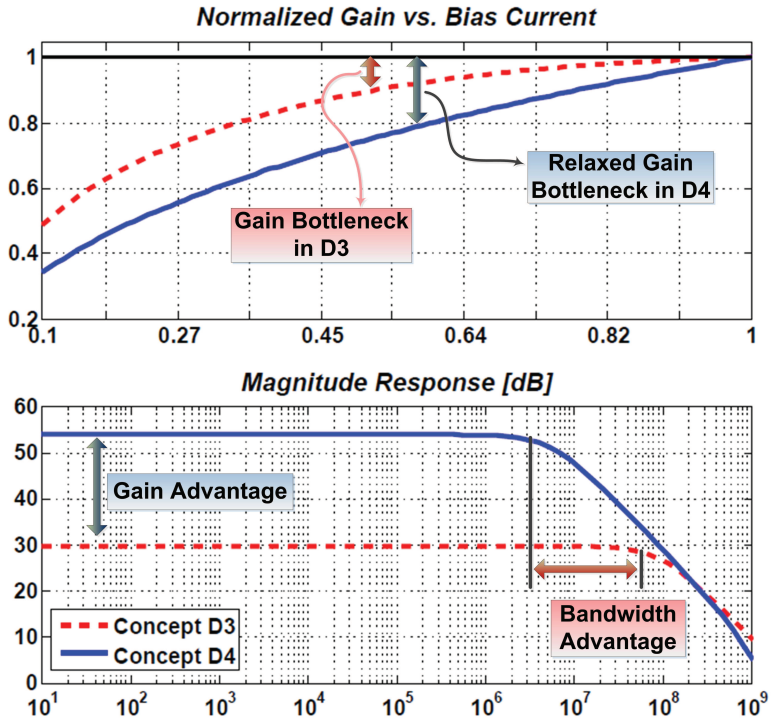

Figure 5.2: Bottleneck and trade-offs in two differential input concepts

variables g_{mgx} and g_{mdx} for a tenfold variation of the tail biasing current.It can be observed for the second half of the bias current range, gain begins to saturate and only 10% improvement is achived.

In contrast, concept $D4$ from Figure 5.8 (folded cascode differential input) relaxes the gain bottleneck of concept $D3$ by adding the g_{ms}/g_{md} cross-coupling to the additional node with pole $P4$. The bottleneck expression is changed to $Gain_{D4} = g_{mgx}Rp_3g_{ms}Rp_4/(1 - g_{md}g_{ms}Rp_3Rp_4)$, where Rp_3 is changed to include the cascode device's contribution $Rp_3 = 1/(g_{mdx} + g_{md} + g_{ms})$. Shown in Figure 5.2 (top plot) for the same tail biasing conditions, the gain now varies over an extended range. Moreover, concept $D4$ presents a more linear change in gain, suggesting greater flexibility in finding suitable values.

Modifying the gain bottleneck in concept $D4$ changes the trade-offs with other performances. Figure 5.2 (bottom plot) presents the magnitude response in the case of maximum tail current. The gain advantage of concept

$D4$ is $\approx 25dB$. However, the relaxed gain bottleneck in concept $D4$ impacts its bandwidth performance. In this regard, concept $D3$ exhibits the advantage and shows improved $3dB$ frequency behavior. Characterization of different concept performance bottlenecks and trade-offs is performed with the methods introduced in Chapters 3 and 4.

The comparison operator also identifies the correspondence between the circuit nodes with similar behavior and the conditions under which expressions H_{comm} and H_{diff} are computed, e.g., conditions that keep the transistors in the right operation region or the conditions under which two different device parameters have the same effect. The correspondence set is described as Cor. The conditions set is denoted as En. Based on the circuit comparison operator, circuit C_1 is expressed with respect to circuit C_2 as follows:

$$< H_{comm}, H_{1,diff}, Cor, En > \tag{5.1}$$

and similarly, circuit C_2 is described with respect to circuit C_1 as:

$$< H_{comm}, H_{2,diff}, Cor, En > . \tag{5.2}$$

5.2.2 Circuit Concept Instantiation-Abstraction

Instantiation-abstraction is the operator that replaces signals or blocks in a design through clusters of signals or blocks with the same behavior, such that at least one of the following four conditions is met: (i) the modified circuit is closer to the physical implementation than the starting design, (ii) the behavior of the resulting circuit offers a better matching to specification Ψ than the original design, (iii) the constraints of the original design are relaxed in the new circuit, and (iv) the specification-relevant trade-offs are changed in the new circuit. The original circuit is called abstraction and the new circuit is its instance.

Instantiation Example: Figure 5.3 illustrates the instantiation operator. Figure 5.3(a) presents the block structure of a MOS device pair for which the output is the differential current. The concept has the abstract

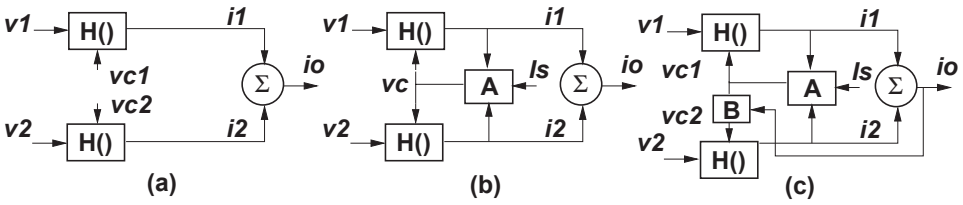

Figure 5.3: Instantiation operator example for differential inputs

functionality of an OTA with $i_o = f(v_1 - v_2)$. Abstract signals v_{c1} and v_{c2} in Figure 5.3(a) are used to control the behavior of the MOS device's $H()$ transfer. In Figure 5.3(b), the two signals are instantiated as $v_{c1} = v_{c2} = v_c$ with block $A()$ generating both (equal) signals in correlation with the differential output currents and an additional variable, I_S. The conceptual model maintains functionality corresponding to a simple common source current biased differential pair OTA and is an instance of the abstract parent from Figure 5.3(a). Similarly, in Figure 5.3(c), the two abstract signals v_{c1} and v_{c2} are now instantiated (generated) by the structure including blocks $A()$ and $B()$. This results in $v_{c1} \neq v_{c2}$ and the new circuit concept is also an instance of the abstract concept in Figure 5.3(a). It implements OTA functionality and corresponds to a source degenerated transconductor. Details on the conceptual OTA models illustrated in Figure 5.3 are provided in Appendix C.

Set $Assoc$ defines the association between the more abstract signals and blocks in abstraction C and their corresponding signals or clusters of signals in its instance C_1. For example, in Figure 5.3(a), the abstract signals v_{c1} and v_{c2} are instantiated as the structure generating them in Figures 5.3(b) and (c).

In general, a circuit C_i is expressed with respect to the set of circuits Ω as follows:

$$< H_{abstr}, H_{inst}, Assoc, En > \tag{5.3}$$

where H_{abstr} is the transfer function of the abstraction of circuit C_i produced using the circuits in set Ω. H_{inst} is the instantiation introduced by circuit C_i for its abstraction. $Assoc$ is the association list between signals and blocks in the abstract concept and C_i. En are the constraints under which the mathematical

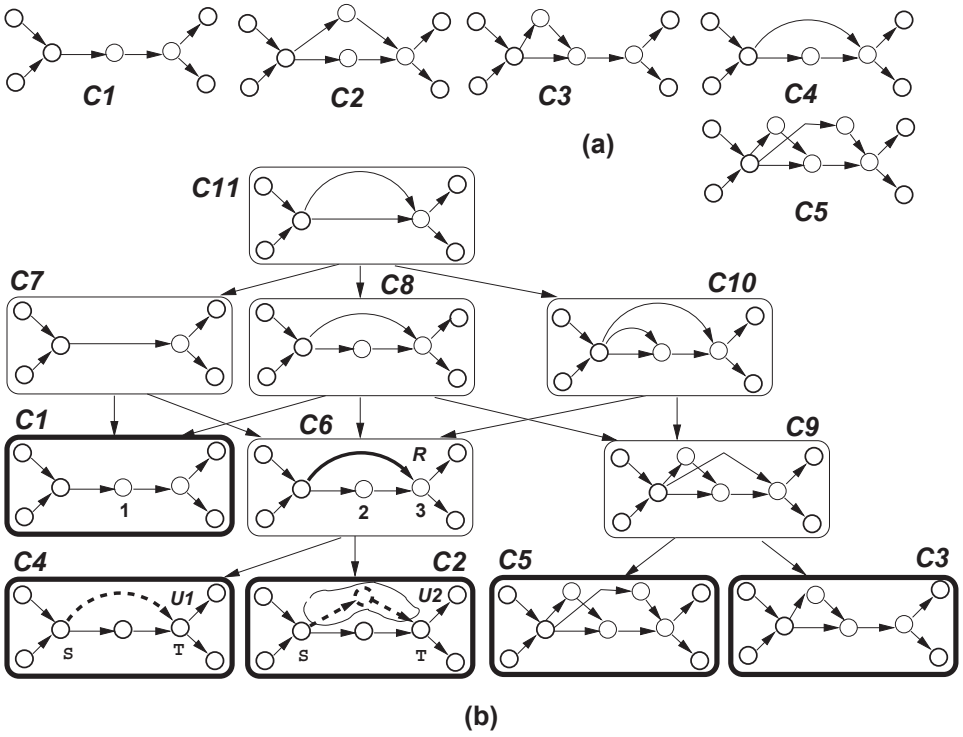

Figure 5.4: Concept abstraction example

expressions are valid.

During the abstraction process, two associated, unmatched symbols or sub-expressions v_1 and v_2 are replaced by a new symbol R with a domain equal to the reunion of the domains of v_1 and v_2. Thus, symbol R acts as a place holder for both v_1 and v_2.

Abstraction Example: Figure 5.4 illustrates the abstraction procedure for a set of five designs ($C_1 - C_5$) described in Figure 5.4(a) as their signal flow graphs. The concepts produced by abstraction are show in Figure 5.4(b). Each of the initial designs is highlighted with bold line. Concepts $C_6 - C_{11}$ are the abstractions. For example, concepts C_2 and C_4 originate the abstract concept C_6. Matched symbols and expressions correspond to the transfer functions of the two circuits and include the pole and coupling expressions of the matched nodes in the two circuits. The matched nodes are shown with bold line. Unmatched expressions between C_2 and C_4 correspond to the

subgraphs shown in bold dotted line. Let's denote these two expressions as U_1 and U_2. Then, for abstract concept C_6, unmatched paths (expressions) U_1 and U_2 from C_2 and C_4, respectively, are replaced by the arc labeled R which defines an abstract place holder capturing the behavior and domain of both U_1 and U_2.

Note that multiple abstractions can result for a set of instances. For example, concepts C_1 and C_6 create two abstractions, C_7 and C_8. Multiple abstractions result, if matching the expressions generates multiple associations that produce a similar (or same) error of the unmatched symbols. For example, node 1 in C_1 can be associated either with node 2 or with node 3 in C_6. This in terms creates two different sets of unmatched structures, and thus the two possible abstractions.

The method to construct the abstractions for a set of circuits C_1, C_2, ..., C_n implementing the same functionality (e.g., OTA or OpAmp) is based on the matching and comparison techniques from Chapters 3 and 4. The result is description H_{abstr} of the abstraction, e.g., its signal flow graph or transfer function. The first step compares the circuits and produces the symbolic expressions of H_{comm}, $H_{j,diff}$, and the sets of ϵ-matched and unmatched nodes. Then, H_{abstr} is initialized as H_{comm}, the common part of all circuit concepts C_i compared. A set S contains the matched nodes with outgoing coupling to unmatched nodes. Similarly, set T contains matched nodes with ingoing coupling from unmatched nodes (sets S and T are indicated in Figure 5.4(b) for C_2 and C_4). Set Q of signal paths originating at nodes in S and ending at nodes in T produces the additional sub-graphs that must be included in H_{abstr} (set Q is shown with bold dashed line for C_2 and C_4 and corresponds to U_1 and U_2). Separate sub-graphs are created for each subset of paths in set Q, such that each path is from a different C_i. Each sub-graph includes any remaining matched nodes on the considered signal paths, the arcs between matched nodes, and a set of new arcs R built as follows. Each arc R corresponds to paths in distinct C_i from the matched node $n \in S$ to matched node $p \in T$, such that the paths pass through at least one unmatched node. The label of arc R is the symbolic expression corresponding to matched structures

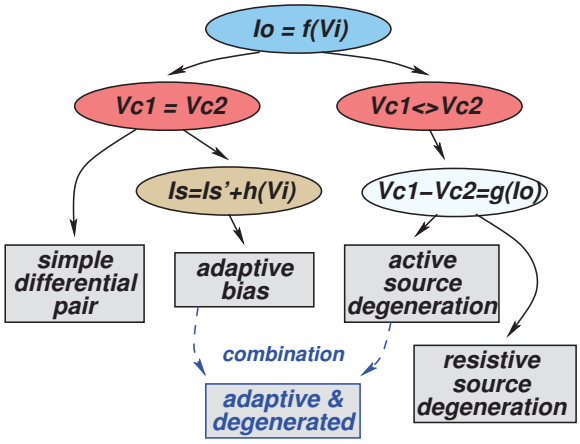

Figure 5.5: A simplified OTA concept structure example

of the considered paths as well as the place holders created for the unmatched sub-expressions of the paths. The bold arc with label R in C_6 is such an arc.

A Simple OTA Concept Structure Example: Figure 5.5 illustrates a simplified concept structure built for 4 OTA circuits. The information about the similar and dissimilar features of the circuits is used to construct the representation in which leaf nodes represent circuit designs, and intermediate nodes express the abstract design features common of the children. The children of an arbitrary node describe a sampling of the conceptual space represented by the node. The top level concept, common to all circuits, guarantees that the transconductor functionality is implemented, $I_o = f(V_i)$, where I_o and V_i are the differential output current and input voltage, respectively. The node corresponds to the abstract OTA concept in Figure 5.3(a). Child concepts add details to the structure through instantiation. One alternative, as previously discussed, is to use the same control voltage for both differential branches ($V_{c1} = V_{c2}$). This corresponds to the conceptual OTA model of Figure 5.3(b). One direct leaf instance of this concept is the simple differential pair transconductor topology. Improving linearity, the alternative instance of node $V_{c1} = V_{c2}$ maintains the same control voltage, but adds an input dependence to the tail biasing current, $I_S = I'_S + h(V_i)$. The concept corresponds to the representation of Figure 5.7(b) and a circuit topology instance is the

adaptive bias transconductor. Another option is the concept utilizing different source voltages for the input transistors (node $V_{c1} <> V_{c2}$). One child of this concept correlates the difference in control voltages to output I_o. Node $V_{c1} - V_{c2} = g(I_o)$ in the OTA concept structure corresponds to the model of Figure 5.3(c). It can be further instantiated as either resistive or active source degeneration topologies.

Figure 5.5 also illustrates a mechanism to extend the concept structure. For example, combining the features of the adaptive bias and source degeneration transconductors can produce a highly linear design [42]. Operators used to extend concept structures are introduced next.

5.2.3 Operators to Extend Concept Structures

Circuit Concept Combinations

Concept combination produces a new circuit concept for specification Ψ by mixing the features of two existing circuit concepts. The resulting design has the property that new features cannot be produced by any instances of the original combined concepts. In addition, the combined concept must maintain functionality and improve at least one performance aspect (eliminating performance bottlenecks, changing trade-offs or increasing flexibility by introducing new design variables). These conditions define a feasible concept combination.

Example: The concept combination in Figure 5.6 produces concept C_4 which combines features from both concepts C_2 and C_3 without being an instance of any of the two. Concept C_4 has two nodes v_g and v_{g1} that can be connected to a number of alternative circuit nodes shown with dashed lines. In contrast, each of the combined concepts, C_2 and C_3, has a single node with variable connections. Concept C_2 allows alternative connections only for node v_g, while concept C_3 allows alternatives only for node v_{g1}. As their topology is more constrained, none of the two concepts can instantiate alone concept C_4 which offers greater flexibility than either the original concept. Concept C_5 is an instance of concept C_4 where the connections of nodes v_g and v_{g1} are now decided.

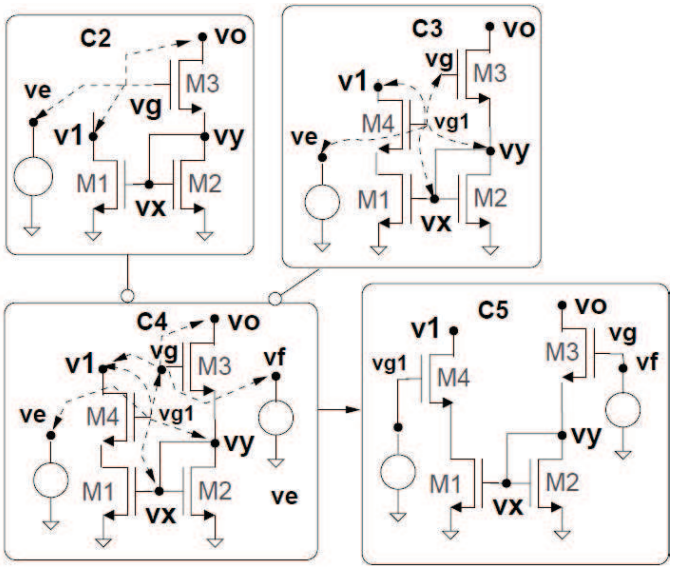

Figure 5.6: Concept combinations example

A similar example is the combination shown in Figure 5.5. The adaptive bias and source degeneration OTA design cannot be directly instantiated by any of the two combined concepts. The adaptive bias OTA concept and the source degenerated concept are on different branches of the structure. The resulting concept improves the linearity performance of both combined concepts [42]. Additional examples of combining concepts are illustrated in the amplifier design case study from Section 5.3.

To determine the set of possible concept combinations for two circuit concepts, the designs are compared. Concept combinations can then be found by combining H_{comm}, the common part of the two circuits, with subsets of nodes and arcs that correspond to the differences in each circuit, $H_{j,diff}$. The combinations that are feasible (e.g., those that modify the trade-offs to improve performance or relax the constraints) are then used to extend the original concept structure.

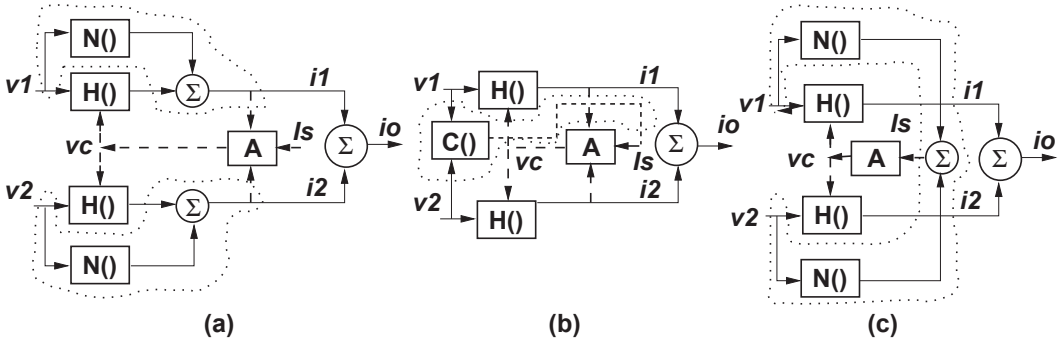

Figure 5.7: Design feature induction for transconductor inputs with improved linearity

Design Feature Induction

The induction operator explores the instance space of an abstraction, where the instance space includes all possible instances that can be devised for the abstraction. Let's assume set Λ of existing instances, where each instance j is characterized by $< H_{j,abstr}, H_{j,inst}, Assoc_j, En_j >$ from equation (5.3). The induction operator uses the existing information on design feature variety of the expressions H_{inst} to create new expressions H_{inst}.

For example, the complementary property of mathematical operators, like equal and different, summation and difference, integration and differentiation, can be used to induce new H_{inst}. The instance in Figure 5.3(b) for the abstraction in Figure 5.3(a) has $v_{c1} = v_{c2}$, which induces the situation in which $v_{c1} \neq v_{c2}$, thus the design in Figure 5.3(c). This is illustrated by the separate branches of the simple concept structure from Figure 5.5.

Finding induction operators based on set Λ involves first identifying the structures corresponding to the different $H_{j,inst}$, such as the structures marked with dotted lines in Figures 5.7(a) and (b). The two concepts are instances of the abstraction in Figure 5.3(b) with different input signal configurations for block $A()$. Then, a generic structure can be fitted for the set of $H_{j,inst}$, such that each $H_{j,inst}$ results by selecting some of the blocks of the structure and dropping others. In addition, the generic structure must preserve the common functionality of the existing instances and the abstract parent. Any new in-

stance $H_{inst} \notin \Lambda$ is based on the generic structure and serves the same purpose as the known instances. For example, the dotted structure in Figure 5.7(c) can be induced by the structures in Figures 5.7(a) and (b) following the same patterns to improve transconductor linearity. An overview of the OTA models in Figure 5.7 is given in Appendix C.

5.2.4 Concept Structures for Analog Circuit Synthesis

A novel circuit synthesis flow based on design comparison, learning, combining, and re-using can be envisioned operating on the proposed concept structure models. The main idea is that solving a circuit design problem requires to identify a set of design steps, so that every step is justified by the fact that it improves performance (e.g., at least one performance attribute) or relaxes design constraints (e.g., at least one constraint). Every synthesis step attempts to address the performance bottlenecks of a circuit topology by changing the relations between the design variables of the bottlenecks. Relations are changed by (i) searching for other designs in the concept structure with different bottlenecks and then combining their features with the current solution, or by (ii) exploring orthogonal ways of relating the variables of the bottlenecks through new ways of interconnecting circuit nodes based on the concept induction operator.

The envisioned flow starts by selecting a design of the concept structure (built on a set of known solutions), such that its performance attributes are closest to the current problem description. This design is likely to be efficiently refined and modified to accommodate the requirements of the tackled specification. Next, iterations of the synthesis flow attempt to minimize the miss-matching between the design performance and the specification requirements by conducting the following steps. First, it analyzes the nature of the performance bottlenecks of the current solution from the concept structure and then finds bottom-up the first parent node that does not have the bottlenecks. The comparison operator applied to child-parent pairs is used for this purpose. Then, a different child without the features that cause the bottleneck is used to further attempt to synthesize the solution. Alternatively, the method

can attempt to remove the current bottlenecks by incorporating features that are present in other designs of the concept structure through the combination operator. The produced performance modifications are evaluated by the comparison of the modified and original circuits. A third option is to create new ways of relating the nodal variables of the bottlenecks, so the bottleneck is changed and a better matching to the problem description is possible. This can be performed using the concept induction operator. Finally, any new solutions created during the steps of concept combination or induction are added to extend the concept structure for future re-use.

5.3 Case Study: Amplifier Circuits Concept Structure

This section discusses a case study for constructing the concept structure for a set of modern amplifier (OpAmp) designs [3–5, 52, 63, 65, 66, 69] and the classic 2-stage Miller circuit. The analysis considers AC behavior of the circuits to identify conceptual abstractions and design instances. The structure is utilized to create concept combinations and induce features that are not part of the initial set of circuits.

The AC behavior of the circuits is represented macromodels, which include the cross-coupling between the circuit nodes and the poles at the nodes. Each OpAmp design was divided into three blocks, e.g., differential input, single-ended conversion, and output blocks. A separate concept structure was built for each block type. The top level concepts present more abstract, conceptual attributes which are common to their instances at lower levels.

5.3.1 Differential Input Concept Structure

Figure 5.8 shows the concept structure for the differential input stage of the analyzed amplifier set. The top level concept, D, presents the general input configuration. Matched attributes, present in all designs, are shown in green. They include the gate-source $sC_{gs} + g_{mg}$ coupling from both inputs

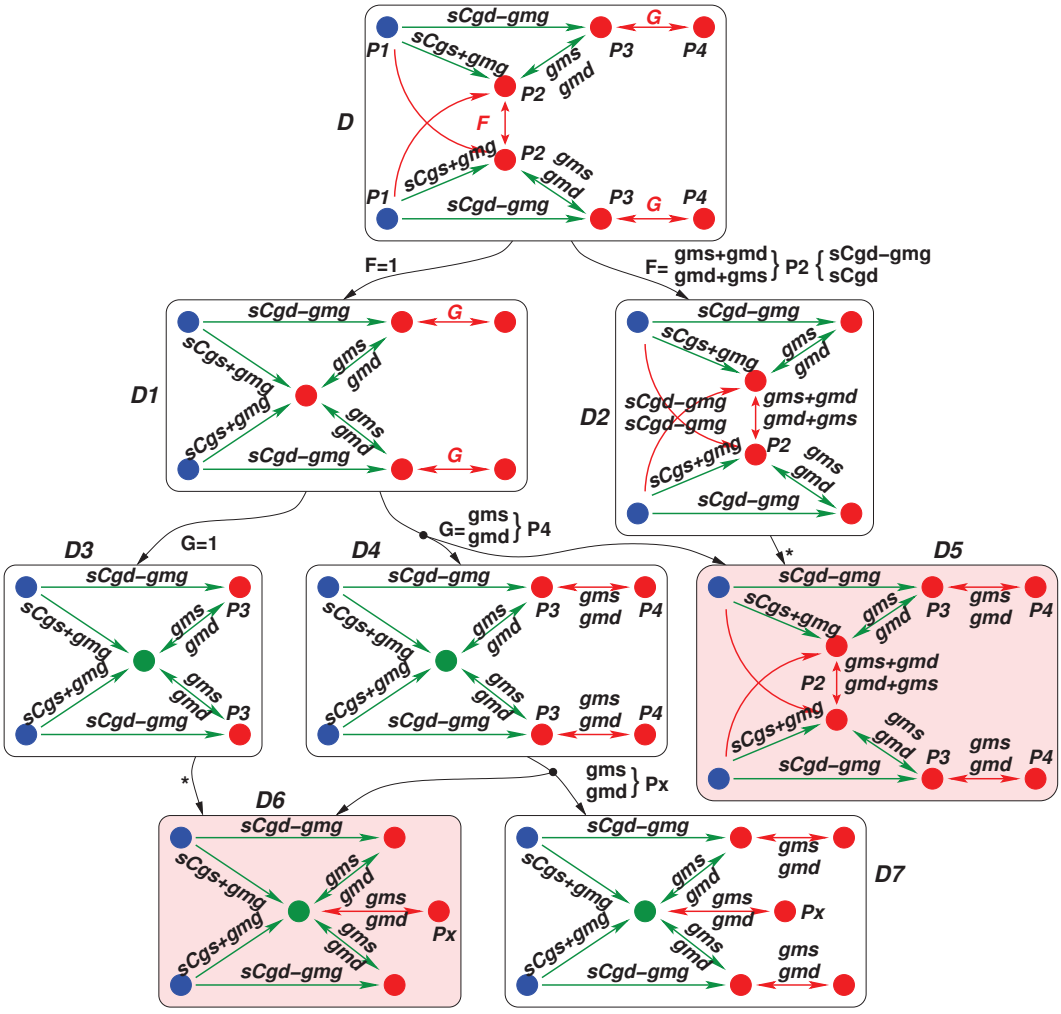

Figure 5.8: Differential input concepts in amplifier circuits

to a center nodal structure, the gate-drain $sC_{gd} - g_{mg}$ coupling on the two symmetrical differential paths, and the cross-coupling from the center structure to the differential paths through g_{ms}/g_{md}. Partially matched poles are found at $P2$ (with matched subexpressions $g_{ms} + g_{md}$ and $C_{gs} + C_{sb} + C_{gd} + C_{db}$ for resistive and capacitive components, respectively) and $P3$ (with matched subexpressions $g_{md} + g_{md}$ and $C_{gd} + C_{db} + C_{gd} + C_{db}$). In addition, the center structure is characterized by abstract attribute F, while the output nodes with poles $P4$ are coupled through abstract function G. Different instantiations of abstract attributes generate the concepts found for the amplifier input block.

One alternative instance of concept D is with $F = 1$ while keeping G abstract, resulting in concept $D1$. The center structure is merged into a single node with its pole expression ($P2$) given by $g_{ms} + g_{ms} + g_{md}$ (resistive part) and $C_{gs} + C_{sb} + C_{gs} + C_{sb} + C_{gd} + C_{db}$ (capacitive part). Concept $D1$ effectively covers any differential input based on the source-coupled transistor pair.

A unique option found in circuit [52] is input concept $D2$. Instantiating $G = 1$ and abstract function $F \neq 1$, active source degeneration is implemented. The two differential devices' sources are no longer identical (as in $D1$), but symmetrically cross-coupled through $g_{ms}+g_{md}$ by the degeneration devices and with additional $sC_{gd}-g_{mg}$ input coupling. The structure of the poles at $P2$ also changes and now includes these two devices' additional contributions as $g_{ms} + g_{ms} + g_{md} + g_{md}$ (resistive part) and $C_{gs} + C_{sb} + C_{gs} + C_{sb} + C_{gd} + C_{db} + C_{gd} + C_{db}$ (capacitive part). The advantage of the structure is improved linearity while increasing the equivalent input capacitance and power dissipation.

Continuing from $D1$, abstract function G can be instantiated to set the block's output structure. With $G = 1$ in concept $D3$, nodes at $P4$ and $P3$ merge, resulting in $g_{md} + g_{md}$ and $C_{gd} + C_{db} + C_{gd} + C_{db}$ pole expressions. The concept represents the simple differential pair with active transistor loads used in designs [3, 63, 65] and the Miller amplifier.

Another alternative found in the amplifier set is to use function G to create additional gain. Concept $D4$ illustrates the structure of a folded cascode differential input implementation. Nodes at $P3$ and $P4$ are cross-coupled through g_{ms}/g_{md} of the cascode devices. The addition of this coupling also impacts the $P3$ configuration (compared to the one in $D3$) by introducing the source parameters of the cascode transistors ($g_{md} + g_{md} + g_{ms}$ and $C_{gd} + C_{db} + C_{gd} + C_{db} + C_{gs} + C_{sb}$ pole expression). The pole at $P4$ is now given by $g_{md} + g_{md}$ and $C_{gd} + C_{db} + C_{gd} + C_{db}$. This circuit concept appears in amplifiers [4, 5, 66, 69].

Only circuit [69] from the set further expands concept $D4$ into $D7$. It adds cascode common source biasing to the differential pair through cross-coupling g_{ms}/g_{md} to another node characterized by pole Px. All other attributes remain unchanged and the advantage is a more constant biasing cur-

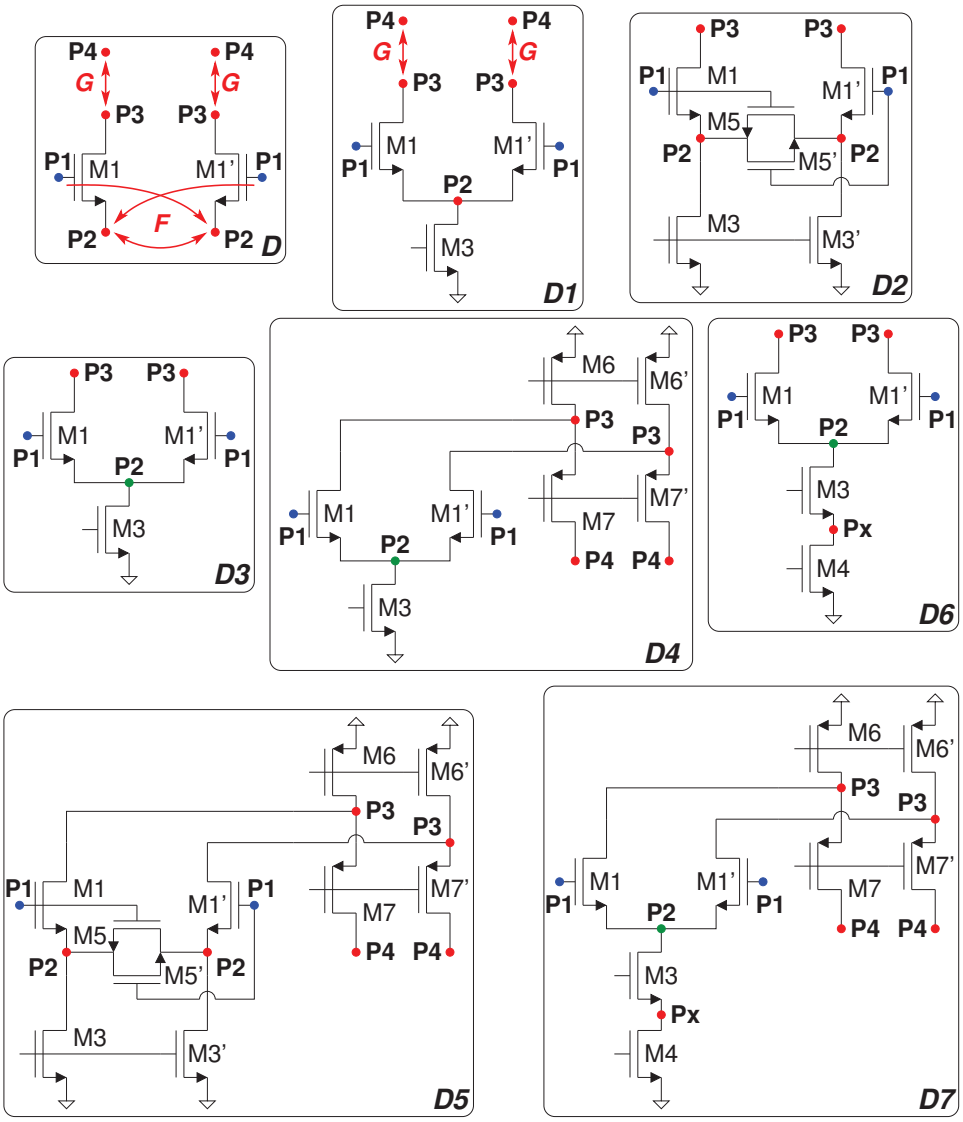

Figure 5.9: Schematic implementations of differential concepts

rent at the expense of an additional non-dominant pole and a reduced input swing. The latter limitation is mitigated in this implementation by using two complementary differential input stages.

The input concept structure in Figure 5.8 also suggests new alternatives which are not covered by the initial amplifier set. One example is the combination of attributes of concept $D2$ with those of $D4$ to create $D5$, a source

degenerated cascode input stage. Similarly, none of the analyzed designs use cascode biasing of a simple differential pair. Illustrated in $D6$, this concept can be found as an application of the unique attribute of $D7$ to the structure of $D3$.

Figure 5.9 illustrates the transistor level implementations for the different explored instantiations of differential input concepts D and $D1$ found in the amplifier circuits set.

5.3.2 Single-ended Conversion Concept Structure

Figure 5.10 shows the single-ended conversion concept structure built from the amplifier set. The top level concept, S, covers all implementations found in the design set. The coupling between the two nodes where the single-ended conversion occurs is denoted with abstract functions F and G which modulate gate-drain cross-couplings $sC_{gd} - g_{mg}/sC_{gd}$. The partially-matched pole structures for $P1$ (input side) imposes sub-expressions g_{md} and $C_{gd} + C_{db}$ (drain connection of one device) for the resistive and capacitive parts, respectively. Pole $P2$ (output side) has the same sub-expressions as $P1$, but is common for all concepts in the structure.

Choosing a single cross-coupling path, with $G = 0$, results in abstract concept $S1$. The same pole structure is maintained. From $S1$, the case of $F = 0$ yields no single ended conversion mechanism (no cross-coupling) in concept $S3$. Pole structures remain unchanged from the top abstract concept. This is the situation of fully-differential implementations, such as amplifiers [3, 52, 66] from the design set.

Also from $S1$, an alternative is instantiating function $F = 1$ to produce concept $S4$. This implements a simple current mirror (SCM) topology. The two nodes are directly cross-coupled through $sC_{gd} - g_{mg}/sC_{gd}$. Node pole structure for $P1$ changes to include the diode connected device and the gate-drain direct coupling. The resistive part becomes $g_{md} + g_{mg}$ (drain and gate connection of diode device) and the capacitive part is $C_{gs} + C_{gb} + C_{db} + C_{gs} + C_{gd} + C_{gb}$ (drain and gate of diode device and gate of output transistor). Amplifiers [3, 63, 65] and the basic Miller utilize this concept.

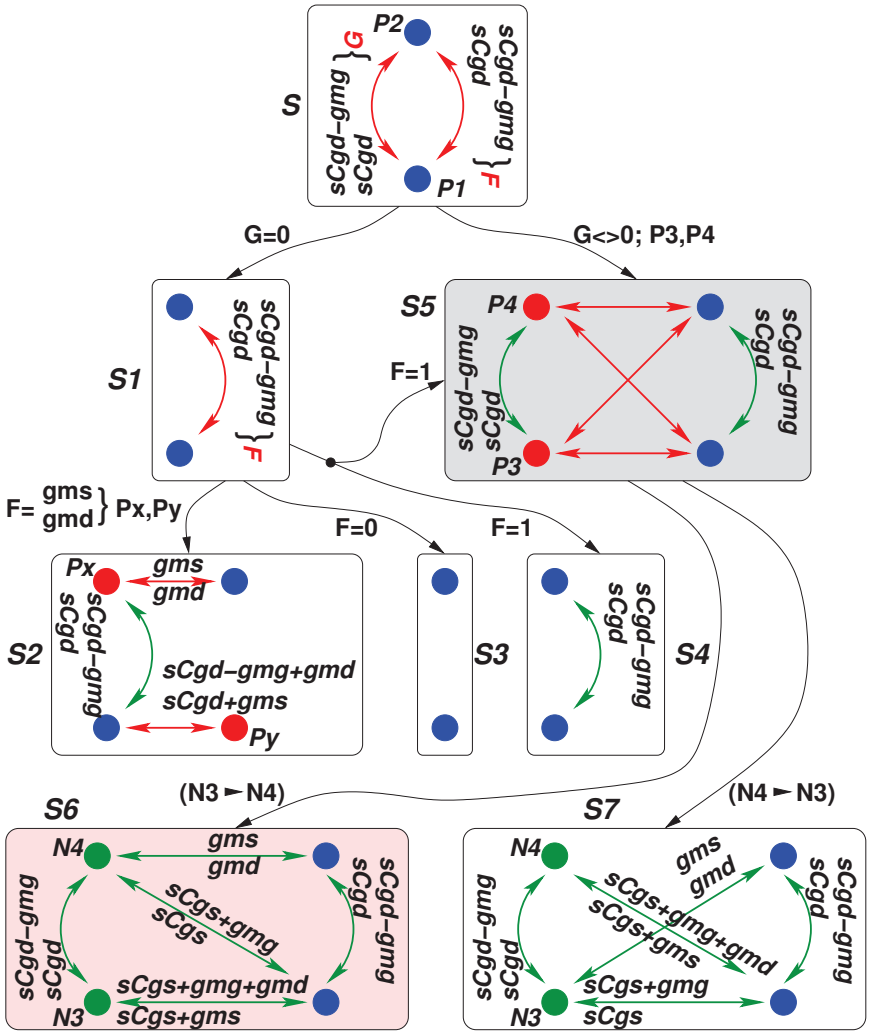

Figure 5.10: Single ended conversion concepts in amplifier circuits

Concept $S2$ instantiates a more complex cross-coupling structure, introducing an intermediate node at Px. $P1$ (input) is cross-coupled to Px through $sC_{gd} - g_{mg}/sC_{gd}$ and then Px is coupled to $P2$ (output) through g_{ms}/g_{md}. The pole introduced at Px is given by $g_{ms} + g_{md}$ and $C_{gs} + C_{sb} + C_{gd} + C_{db}$ (resistive and capacitive parts, drain and source connections of two devices). In addition, symmetry of the structure is preserved by also including intermediate node Py (same expression as Px) cross-coupled to $P1$ through gate-drain and drain-source connections across two devices. The pole structure of $P1$ gets extended

to g_{md} (resistive unchanged) and $C_{gd}+C_{db}+C_{gs}+C_{gd}+C_{gb}+C_{gs}+C_{gd}+C_{gb}$. The capacitive part now includes connections of three distinct devices (one drain - as in the top concept, and two additional device gates). The concept effectively implements a wide-swing cascode current mirror (WSCCM) which improves output resistance while allowing a higher output voltage range. The concept is used in amplifiers [4, 69].

Abstract concept $S5$ uses two cross-coupling paths ($G \neq 0$), one direct and one through two intermediate nodes ($P3$ and $P4$). It is combining two instances of the attributes in concept $S4$ (two SCMs $P1-P2$ and $P3-P4$). The respective pole structures are maintained from concept $S4$. The concept remains abstract as the general nature of the cross-coupling through G illustrates that either orientation of the intermediate SCM ($P3-P4$) is possible.

One alternative is shown in concept $S7$. The orientation of the intermediate current mirror ($P3-P4$) is opposed to that of the main path ($P1-P2$). The output node of the intermediate SCM ($N4$) is not directly coupled to the output of the main SCM ($P2$), but rather to its input node ($P1$). The concept implements the improved Wilson current mirror (IWCM) with the second SCM providing feedback. Amplifier [5] implements this high output impedance topology.

None of the designs in the set implement the alternative $S6$ concept which maintains the input-input, output-output correspondence for the two SCMs in the combined concept. The same cross-coupling expressions are used as in $S7$, but to opposite intermediate nodes, and same pole structure is preserved. $S6$ implements the cascode current mirror (CCM). While having a similar output voltage swing as $S6$ (IWCM), concept $S7$ offers increased output impedance.

5.3.3 Output Stage Concept Structure

Figure 5.11 illustrates the different output structure concepts. The top abstract concept O describes the abstract characteristics of the output blocks of the considered amplifiers. The features of the top concept include

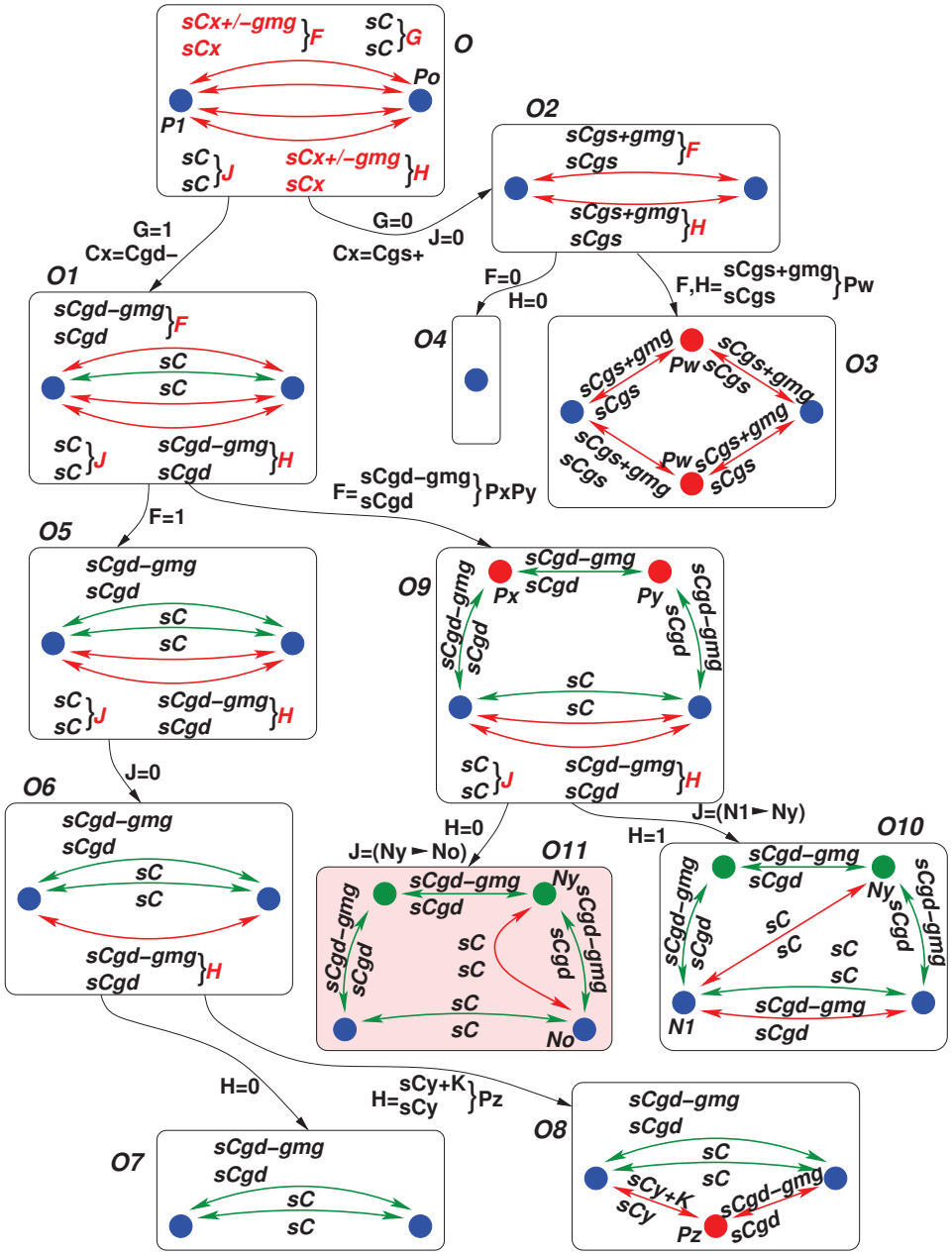

Figure 5.11: Output stage concepts in amplifier circuits

two separate output signal paths characterized by functions F and H, with generic form $Cx \pm g_{mg}$. Also, there are two possible compensation loops. The loops are expressed by cross-coupling sC/sC together with functions G

and J. At this abstraction level, both poles $P1$ (block input) and Po (output) are in generic form. Note that the top-level concept covers a wide range of output stage configurations, including buffers and multi-stage amplifiers with or without class AB outputs.

Concept O has two instances, concepts O_1 and O_2. They separate, based on the implemented concept, the analyzed design set into two categories. Concept O_2 corresponds to single-stage amplifiers or output buffers (with no voltage gain) and compensation loops are eliminated. The pole structures is still generic for this concept. Concept $O1$ describes multi-stage compensated OpAmp designs, and is discussed shortly.

Concept O_2 has two instances. Concept O_4 results from its abstraction O_2 by adding the features $F = 0$ and $H = 0$. Note that concept $O4$ is still conceptual, thus does not represent an implementation. It does not include any additional output structure, and represents the case of the single stage amplifier topology. This concept is used in designs [52, 63].

Concept O_3 is the second instance of concept $O2$. The generic cross-coupling from input to output is instantiated as $C_{gs} + gmg/C_{gs}$ ($Cx = C_{gs}+$) through the intermediate node structures captured by functions F and H. Both functions have the same cross-coupling form across the intermediate node with pole P_w given by expression $g_{md} + g_{ms}$ (resistive component) and $C_{gd} + C_{db} + C_{gs} + C_{sb} + C_{gs} + C_{gd} + C_{gb}$ (capacitive parts component). Concept O_3, with two complementary output paths, corresponds to a buffer design through source followers with no voltage gain (only current gain). Amplifier [5] uses this concept. The dual complementary path ensures a wider range output swing in both positive or negative directions.

The abstract concept O_1, the second instance of the top concept O, represents multi-stage compensated OpAmps. The two different input-output paths are both characterized by the gate-drain cross-coupling $C_{gd} - gmg/C_{gd}$ ($Cx = C_{gd}-$). The abstract functions F and H remain generic, as well as one of the compensation loops through function J. Feature $G = 1$ of the concept illustrates that all instantiated concepts share a direct input-output compensation loop characterized by a symmetric cross-coupling through the compen-

sation capacitor (sC/sC). Concept O_5 is an instance of O_1 for $F = 1$. The concept describes two-stage compensated OpAmps with a common source output gain stage structure (i.e., direct input-output gate-drain coupling through $C_{gd} - gmg/C_{gd}$).

A simple extension of concept O_5 eliminates the second compensation loop, and produces concept O_6. This abstract concept covers both classic and class AB output stages in the amplifier design. For $H = 0$, the alternate output path is eliminated, and concept O_7 represents the output structure found in conventional compensated two-stage amplifiers (class A). The basic configuration is used in the Miller amplifier and circuits [66,69]. OpAmp [69] further expands the concept by using two identical, but complementary, instantiations of the concept. This allows rail-to-rail operation at the expense of additional complexity and power consumption.

In contrast to O_7, concept O_8 keeps the alternate output path and instantiates it through an intermediate node (i.e. P_z) using a cross-coupling of form $sCy + K/sCy$. Concept O_8 corresponds to OpAmps [3, 65] from the set of designs.

Circuit [65] uses $Cy = C_{gs}$ and $K = g_{mg}$ to implement the additional path through a gate-source connection (source follower) to the intermediate node. OpAmp [3] uses a different instantiation of the concept with $C_y = C$ (discrete capacitance) and $K = 0$ to provide the coupling to the intermediate node. This changes the P_1 pole structure to include the extra capacitor $C_{gs} + C_{gd} + C_{gb} + C + C$. Pole P_z is given by a diode connected transistor, extra capacitor, and the gate connection of the added signal path transistor ($g_{md} + g_{mg}$ and $C_{gs} + C_{db} + C_{gb} + C + C_{gs} + C_{gd} + C_{gb}$). While both designs offer better driving capabilities with limited increase in distortion (compared to the conventional case of O_7), the OpAmp in [3] has reduced static power dissipation compared to [65].

Exploring the alternative path from concept O_1, function F can be instantiated through two additional intermediate nodes (P_x and P_y) with gate-drain cross-coupling $C_{gd} - gmg/C_{gd}$ in concept O_9. This introduces an additional cascaded gain stage. The abstract concept can be mapped to various

three-stage compensated amplifiers. Concept O_{11} results by setting $H = 0$ and placing the second compensation path between N_y and output N_o. The concept implements a nested-Miller three stage amplifier output structure. It is not utilized in the considered OpAmp set but can be induced from alternatives to the existing features.

Concept O_{10} is the second instance of concept O_9. It places the second compensation path across input N_1 and N_y and uses a secondary direct input-output path through gate-drain cross-coupling $C_{gd} - gmg/C_{gd}$. This concept implements a positive feedback compensation scheme for three-stage amplifiers. In contrast to concept O_{11}, O_{10} changes input pole P_1 by adding the second compensation capacitor and the gate connection of the secondary output path. OpAmp [4] uses this concept to improve frequency behavior, settling time, and slew rate compared to the nested-Miller design for concept O_{11}.

5.3.4 Discussion on Amplifier Concept Combinations

The concepts from Figures 5.8, 5.10, and 5.11 are combined in the analyzed amplifier set to create the full individual designs. For example, the combination of concepts $D4 - S7 - O3$ generates the structure of amplifier [5]. For the analyzed set of amplifiers, only nine distinct combinations of concepts from Figures 5.8, 5.10, and 5.11 are explored. The generated concept structures could be used to further explore more than 140 distinct concept combination patterns. However, feasibility with respect to the defined specification of each combination needs to be verified. In certain combinations, performance goals cannot be met since the advantages of one concept are diminished when combined with an inappropriate one. For example, combining $D4$ (cascode input) with $S4$ (SCM single-ended conversion) reduces the potential for high gain offered by concept $D4$. Similarly, concept $O4$ (single stage amp) may be infeasible for low voltage, high gain requirements, regardless of the input or single-ended conversion concepts utilized in the combination.

Different concept combination strategies can be envisioned. Figure 5.12 shows two alternatives of combining differential input and single-ended con-

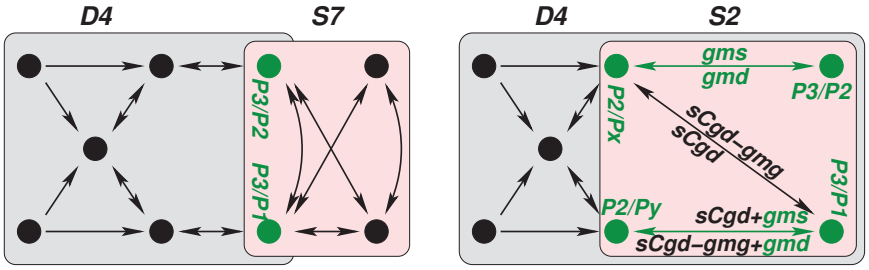

Figure 5.12: Attribute sharing of combined concepts in amplifier circuits

version concepts. In the first example, concept $D4$ (folded cascode input) is combined with concept $S7$ (IWCM). This is one of the most common combination strategies. The output nodes of one concept are shared with the input nodes of a different concept. The pole structure at these nodes changes and includes the attributes of both concepts. Pole $P3$ of $D4$ is merged with $P2$ of $S7$ and is given by $g_{md} + g_{md}$ and $C_{gd} + C_{db} + C_{gd} + C_{db}$. The symmetrical pole $P3$ of $D4$ is merged with $P1$ of $S7$ and is given by $g_{md} + g_{md} + g_{mg}$ and $C_{gd} + C_{db} + C_{gs} + C_{db} + C_{gb} + C_{gs} + C_{gd} + C_{gb}$. No coupling expressions are shared in this case.

Another option involves finding a suitable combination of concepts which can maximize the number of attributes overlapped/shared. The second example in Figure 5.12 shows this method when $D4$ is combined with $S2$ (WSCCM). This combination of concepts enables sharing of all the nodes of concept $S2$ within the structure of concept $D4$. The structure of intermediate nodes of $S2$ (Px and Py) is included in the the differential pair output nodes of $D4$ ($P2$) and enables this overlap. Similarly, the pole structure $P3$ of $D4$ is fully included in that of $P1$ and $P2$ from $S2$. Coupling expressions can also be overlapped: the gms/gmd cross-coupling of the $D4$ output is contained within the cross-coupling of the overlapped nodes in concept $S2$.

The advantages of the merged concept combination approach over a *cascaded* case include a reduced complexity (fewer nodes/poles) and an increased voltage headroom for this design. The disadvantage is in the more closely correlated set of design parameters. For example, the shared cascode devices are controlled by a single biasing voltage and require additional design

effort to exploit gain and voltage swing capabilities. Alternatively, using the *cascaded* approach for concepts $D4$ and $S2$, voltage headroom would be reduced and complexity increased. However, greater design flexibility could be achieved through two different biasing voltages for each set of cascode devices from $D4$ and $S2$. Identification of the advantages and limitations of the different concept combination strategies can be performed with the techniques presented in Chapters 3 and 4.

Concepts can also be combined with themselves as multiple/duplicate copies. *Parallel* combinations can be used to create complementary signal paths which share the output nodes. An example is the implementation of the rail-to-rail amplifier [69]. Alternatively, concept duplicates can be combined in *series*. Examples are the amplifiers [63, 65] which combine in series two identical implementations of single-stage and two-stage amplifiers concepts, respectively. In this case, the output node is shared/overlapped with an input node, creating the current feedback specific to these designs.

5.4 Summary

This chapter introduced the concept structure model to express the design feature variety in analog circuits, a future work direction. The model has four basic operators, circuit comparison, circuit instantiation-abstraction, circuit combination, and design feature induction.

The insight offered by the model is important to characterize the distinct and common features in a circuit and for the exploration of new conceptual designs. For example, the analyzed OpAmp set discussed in the case study implements only 9 distinct topologies. However, there are more than 140 distinct combinations that can result using the concept structures for the OpAmps. The concept structure offers the support to identify alternative signal processing flows which represent feasible novel conceptual designs that can better meet the specification requirements by eliminating performance bottlenecks or by relaxing trade-offs. A case study illustrated circuit concepts for

the input block, single-ended conversion, and output stage of OpAmps as well as new concepts which do not exist in the initial set but could be obtained using the model's concept combination and/or induction operators.

Chapter 6

Analog Circuit Topology Synthesis Examples using ONCRs and Systematic Comparison

This chapter presents a set of approaches to analog circuit synthesis using the concepts introduced in this dissertation. The methods use ordered node clustering representations (ONCR) to identify alternative structural circuit features, circuit concept (feature) combination, and employ systematic circuit comparison to characterize performance trade-offs of the synthesized solutions. The proposed techniques are based on a reasoning-like process. The synthesis procedure precisely identifies the circuit feature that causes a performance bottleneck and aims to locally address the limitation by incorporating only new topological features that are likely to improve performance. This resembles reasoning used by expert designers when developing or selecting analog circuit topologies. Hence, the synthesis output is not only a design, but also the justifications for the performed design decisions which can later be employed in the form of design plans for tackling similar design problems. With respect to existing trustworthy evolutionary techniques [23], the proposed procedures

create the foundation for an alternative approach to analog circuit synthesis. Characterizing the variety of common and distinct circuit structures through ONCRs and correlating symbolically the distinguishing design variables to performance trade-offs creates the premise for cause-effect *understanding* of the solutions. The proposed set of techniques can also be employed to complement library-based numerical search methods [21, 23]. They offer the support to systematically update the library with novel, designer-trusted structures obtained either from current publications or through combinations of existing building blocks, hence increasing the diversity of topologies explored by these tools. Case study examples illustrate applications of the methods using the ONCR of the fifty state-of-the-art amplifier circuits discussed in Chapter 3.

6.1 Overview of Envisioned Methods

6.1.1 Topology Selection Procedure

Algorithm 6.1 illustrates the proposed method of topology selection. The procedure takes as input a reference circuit topology C_k, the set S_C of N known designs for the given application, and the ordered node clustering representation (ONCR) of this set. An additional input, Max_{diff}, is used to control the amount of variance with respect to the reference topology C_k that is considered in the exploration process. The procedure outputs a sorted list L_k of alternative topologies to reference circuit C_k.

Step (1) of Algorithm 6.1 initializes the list of topology selection candidates to the entire set of known solutions, excluding the reference design.

In step (2), the list of candidates L_k is pruned based on the desired degree of differences from reference circuit C_k. Using the ONCR information on circuit node groups, only those designs are kept in L_k for which the number of unmatched circuit structures with C_k is less than or equal to Max_{diff}. This step first identifies the clusters of $C_j \in L_k$ and C_k in the ONCR. For each cluster, the method checks if circuits C_j and C_k have same (or different) node structures by verifying if nodes from C_j and C_k are grouped in the ONCR. After traversal of all clusters, the total number of different nodal structures

Algorithm 6.1 Topology Selection Procedure

Inputs: C_k; $S_C = \{C_i, i = \overline{1, N}\}$; ONCR($S_C$); Max_{diff};
Output: $L_k = \{C_j, C_j = \text{alternative topology for } C_k\}$;
(1) ***Initialize*** $L_k = S_C - \{C_k\}$;
(2) ***For all*** circuits $C_j \in L_k$
    If $|\text{ONCR}(C_j) - \text{ONCR}(C_k)| \leq \text{Max}_{\text{diff}}$ ***then***
        $L_k = L_k - \{C_j\}$;
(3) ***For all*** circuits $C_j \in L_k$
    Generate trade-off profile $T_j = \text{Compare}(C_j, C_k)$;
(4) ***Sort*** L_k based on T_j ***such that***
    Circuit C_j is before circuit C_i in L_k ***if***
        T_j relaxes and/or eliminates more trade-offs than T_i;
(5) ***Return*** L_k;

(cases where C_j and C_k are not in the same group of the ONCR) is tested against Max_{diff} to determine inclusion of circuit C_j in the final candidate list.

Step (3) of the topology selection procedure uses the circuit comparison operator to characterize the performance trade-offs of all circuits from the pruned list of candidates. Comparing circuit $C_j \in L_k$ with the reference circuit C_k generates the trade-off profile T_j of the candidate, which illustrates how the identified differences between the two topologies impact performance such as gain, bandwidth, and noise. The characterization illustrates the relative performance trends with respect to varying design parameters (i.e., transistor width) and is used to rank candidate topologies in step (4) of Algorithm 6.1.

The sorting mechanism in step (4) analyzes the performance trade-off profiles T_j of circuits $C_j \in L_k$ and orders the list L_k with respect to: (i) the performance trade-offs that are eliminated, (ii) the trade-offs that are relaxed, and (iii) the range of design variables over which performance can be improved. For example, a topology relaxing the gain-noise trade-off (e.g., gain improves faster than noise deteriorates) for 70% of the analyzed design variable range is prefered over a topology relaxing the same trade-off only for 25% of the range. The first topology is characterized by higher flexibility to improve performance. Finally, Algorithm 6.1 returns the sorted list of topology selection candidates.

6.1.2 Topology Refinement Procedure

The proposed topology refinement procedure is given in Algorithm 6.2. The procedure implements the concept combination operator introduced in Chapter 5. Inputs are the topology to be refined C_k, the set S_C of known designs for the tackled application, and the ONCR corresponding to S_C. The output is the topology refinement C_k^r (if available). The method consists of two parts: (1) identifying the circuit nodes that relate to the current topology's performance bottlenecks, and (2) finding the alternative nodal structure(s) which remove the performance bottleneck.

Part 1 of the topology refinement procedure uses the trade-off profile T_k (available from the comparison operator) of the input circuit C_k to identify design parameters (i.e., device widths) that correlate to performance bottlenecks that need to be improved. For example, with respect to device M_i, the trade-off profile shows that gain has a logarithmic behavior: as width W_i increases, the circuit's gain saturates to a maximum value. A feasible topology refinement changes this bottleneck to linear or exponential behavior. In Part 1, the topology refinement procedure builds a list of nodes K of circuit C_k to which performance bottleneck devices are connected (based on trade-off profile T_k).

Part 2 of Algorithm 6.2 attempts to find a feasible topology refinement for circuit C_k starting from nodes $n_k \in K$. In steps (1)-(2), the ONCR of known designs S_C is used to find alternative nodal features (structures) for a selected bottleneck node, n_k. First, the cluster containing the group of n_k is found in the ONCR. Then, this cluster is used to identify all unmatched circuit nodes n_p from other circuits C_p (different groups than n_k). These candidates are aggregated in set P. To ensure structural integrity of the refinement process (i.e., generate a *working* circuit topology), only nodes n_p which have the same input edges (matched symbolic expressions) as n_k are included in set P.

The refinement method proceeds in steps (3)-(5) by selecting a node n_p of circuit C_p from the set of candidates P. Its structure then replaces that of n_k in the current refined topology, C_k^r. In step (5), the ONCR signal

Algorithm 6.2 Topology Refinement Procedure

Inputs: C_k; $S_C = \{C_i, i = \overline{1, N}\}$; ONCR($S_C$);
Output: Refined topology C_k^r;
Part 1:
(1) ***Identify*** performance bottleneck of C_k w.r.t. devices M_i using trade-off profile T_k (from comparison operator);
(2) ***Build*** set of circuit nodes K from C_k to which performance bottleneck devices M_i are connected;
Part 2:
(1) ***Select*** $n_k \in K$ and ***find*** ONCR cluster $Cls_k \supset \{n_k\}$;
(2) ***For all*** circuits $C_p \in Cls_k$ ($C_p \neq C_k$, $C_p \in S_C$)
Build set of nodes $P = \{n_p, n_p$ from $C_p\}$ ***such that***
$n_p \neq n_k$ and input_edges(n_p)=input_edges(n_k);
(3) ***Initialize*** $C_k^r = C_k$;
(4) ***Select*** $n_p \in P$ (n_p from C_p) and ***replace*** n_k with n_p in C_k^r;
(5) ***Continue*** adding n_{p+i} from C_p to C_k^r in sequence order ***until*** n_{p+i} from C_p matches any n_{k+j} from C_k ***or*** n_{p+i} is output node of circuit C_p ($i, j \geq 1$);
(6) ***Generate*** trade-off profile $T_k^r = \text{Compare}(C_k^r, C_k)$;
(7) ***If*** bottleneck changed and T_k^r acceptable ***then***
Return refined topology C_k^r;
Else if available do new selection of $n_p \in P$ in step (3)-(4);
Else if available do new selection of $n_k \in K$ in step (1);
Else return *failed*;

path sequence [75] of circuit C_p is followed and additional nodal structures of this circuit (n_{p+i}) are added to C_k^r until one of two stopping criteria are encountered: (i) node n_{p+i} from C_p matches any of the subsequent nodes of n_k from the original design C_k ($n_{p+i} = n_{k+j}$) or (ii) node n_{p+i} is the output of circuit C_p. The two conditions impose that only minimum possible structural changes are introduced from C_p to C_k^r.

In step (6), the comparison operator is invoked to generate the trade-off profile T_k^r of the refined circuit C_k^r with respect to the original C_k. This

characterizes the performance implications of the newly added features.

Analysis of trade-offs T_k^r in step (7) determines whether the current refined topology changes the performance bottlenecks while other trade-offs show acceptable trends. For example, logarithmic gain behavior is changed to exponential by the newly introduced nodal structures, while the gain-noise trade-off can still be controlled over a relatively wide range of design parameter values.

If the current topology refinement solution is not acceptable, the procedures first iterates through other possible candidates in set P at step (4). If still unsuccessful, the method backtracks to step (1) of Part 2 and selects a different node n_k from set K of the input topology C_k and proceeds to refine its structure. The procedure returns a failure after exhaustively trying all refinement alternatives. With respect to the set of known designs S_C, this suggests that topology C_k is the best overall choice for the considered performance bottlenecks since no other solution contains the features that can improve performance or alter trade-off behavior.

6.2 Case Study Topology Synthesis Examples

We now present case study examples of using the novel analog circuit synthesis technique. The method uses the ONCR of fifty state-of-the-art amplifier circuits from Chapter 3 together with the symbolic circuit comparison operator of Chapter 4 to implement topology selection, refinement, and find *new* topologies.

6.2.1 Topology Selection

We illustrate the topology selection procedure in Algorithm 6.1 through an example using the basic two-stage Miller amplifier as a reference topology. In the fifty amplifier design set (S_C), this circuit is labeled C_{11}. With $C_k = C_{11}$, we apply topology selection for $\text{Max}_{\text{diff}} = 2$ to identify alternatives which can be used to improve performance.

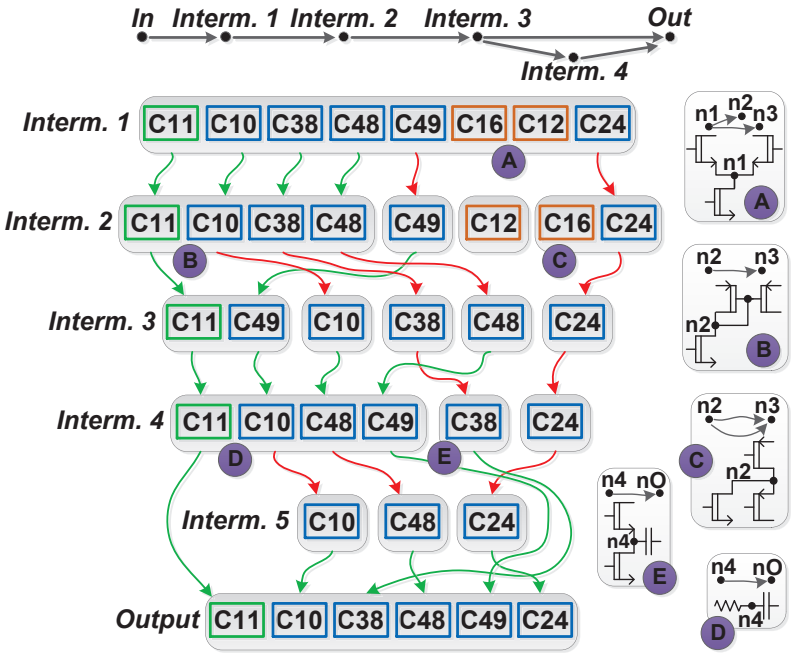

Figure 6.1: Subset of fifty circuits ONCR

Build Candidate List: In step (2) of Algorithm 6.1, the ONCR of known solutions is used to identify topology candidates that satisfy the set Max_{diff} condition. Figure 6.1 illustrates the relevant subset of the fifty circuits ONCR. Reference design C_{11} is highlighted in green while potential selection candidates are marked in blue (C_{10} [3], C_{24} [68], C_{38} [90], C_{48} [98], C_{49} [99]). Six clusters of the ONCR are shown corresponding to the signal path *Interm. 1*-*Interm. 5* and circuit *Output* nodes. Arrows between clusters link nodes of individual circuits. Red arrows indicate situations where the topology selection candidate's nodes are not matched with those of the reference design C_{11} (different groups). For example, in the *Interm. 1* and *Output* clusters all circuits match with C_{11} and form a single group. For *Interm. 2*, topologies C_{49} and C_{24} utilize different structures than C_{11} and are present in different groups. $\text{Max}_{\text{diff}} = 2$ allows at most two different nodal structures with respect to reference C_{11} in this experiment. Using the ONCR information from Figure 6.1,

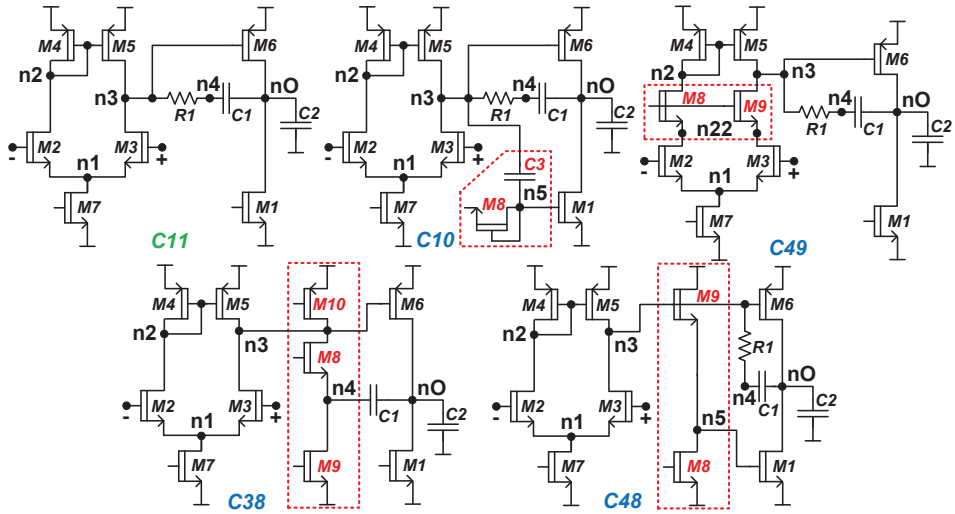

Figure 6.2: Schematics of reference and topology selection candidates

the pruned list of candidates is $L_k = \{C_{10}, C_{38}, C_{48}, C_{49}\}$. For example, C_{48} has two different node structures at *Interm. 3* and at *Interm. 5*, which is an additional node without equivalent in C_{11}. Note that C_{24} is not included in the final pool of candidates as it consists of four different nodal features.

Generate Candidate Trade-offs: In step (3) of topology selection Algorithm 6.1, the list of candidates is compared with the reference design. The symbolic comparison operator correlates the structural differences with performance and generates the circuit's trade-off profile. The schematics of the reference design and topology selection candidates are shown in Figure 6.2. Differences with respect to C_{11} are highlighted for $C_{10}, C_{38}, C_{48}, C_{49}$. The analysis considers the implications on performance of different devices (i.e., devices highlighted in Figure 6.2), common devices through which new signal path attributes are introduced (e.g., M_1 in C_{10}), critical circuit devices (e.g., input pair $M_2 - M_3$), and various combinations of these. Device sizes are varied over a predefined range and the normalized performance plots of gain, CMRR, bandwidth (f_{3dB}), unity gain frequency (f_0), and total noise (P_N) are generated.

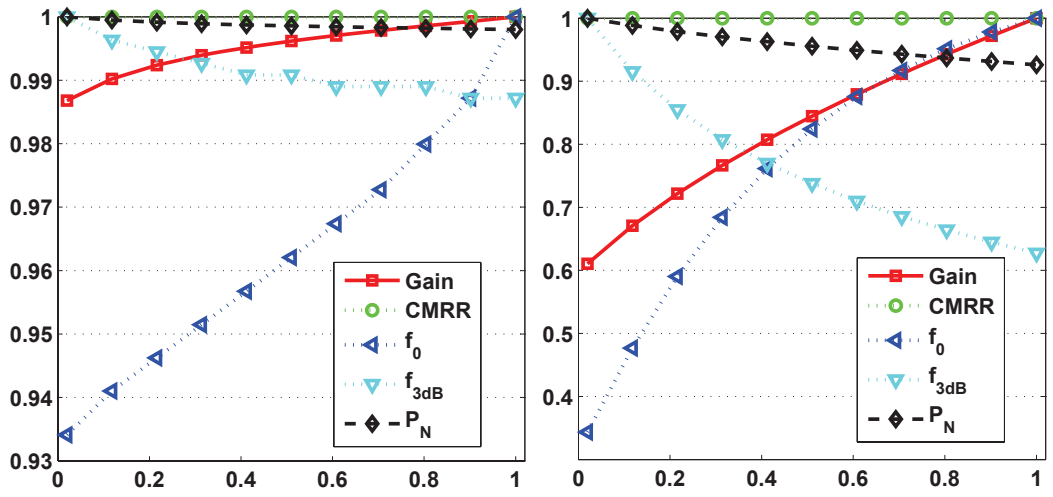

Figure 6.3: Normalized performance of C_{48} with respect to $W_8 \propto W_9$ ($I_8 \searrow$) and W_1 ranges, respectively

C_{48} : Design parameters considered for the analysis include $W_8 - W_9$ (and I_8), W_1, $W_2 = W_3$, and W_6. Device M_1 is included in the set since it introduces a new coupling to the output node in the signal path which is not present in C_{11}. Considering the analysis for different parameters $W_8 - W_9$ (and I_8), we note limited impact on performance. Gain, f_{3dB}, and P_N exhibit variations of less than 1% over the investigated parameter ranges, while CMRR remains unchanged. A slightly more pronounced variation of 7% is obtained for f_0. The scenario is illustrated for proportional variation of $W_8 - W_9$ (and decreasing current I_8) is shown in Figure 6.3 (left). The trade-off profile suggests that these devices can aide in increasing unity gain frequency while maintaining other performance relatively constant. A more favorable scenario for improving performance exists in topology C_{48} when variation of W_1 is also considered. This trade-off profile is shown in Figure 6.3 (right). While in C_{11} W_1 has virtually no impact on performance, in C_{48} the new structure can be used to improve gain by 40%, f_0 by 65% while reducing noise by up to 7%. A trade-off exists however with bandwidth which can decrease by 37%. However, the trade-offs in Figure 6.3 (right) show that the first half of the analyzed range is beneficial to rapidly increasing f_0 for relatively smaller $W_8 - W_9$ and higher current. In the second half of the analyzed range the

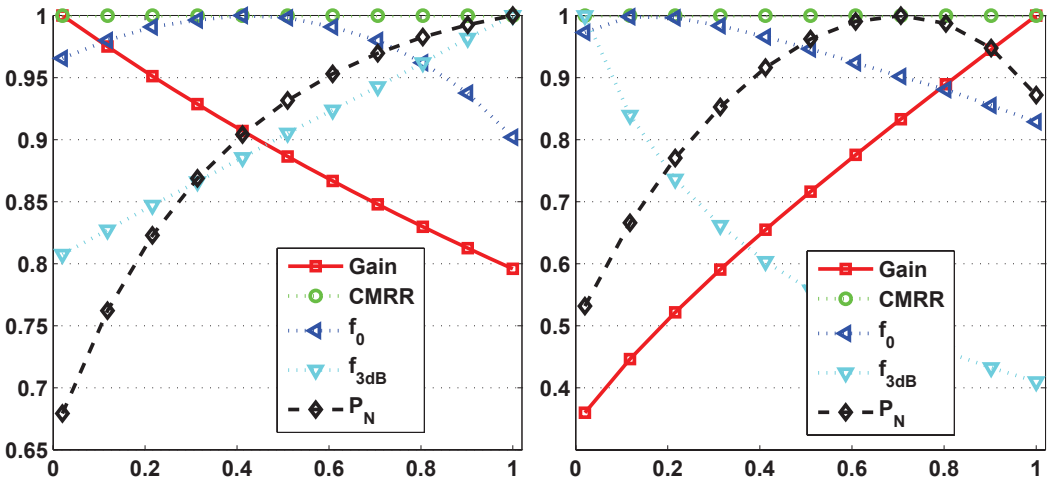

Figure 6.4: Normalized performance of C_{38} with respect to $W_8 \propto W_9 \propto W_{10}$ ($I_8 \nearrow$) and W_6 ($I_8 \searrow$) ranges, respectively

increasing slope reduces and follows the gain performance trend. Analysis of parameter W_6 showed that with respect to C_{11}, this device can also help improve f_0. However, the impact on gain and bandwidth is reduced by 50% when compared to the behavior in C_{11}. For $W_2 = W_3$ a similar performance behavior to that in C_{11} was observed.

C_{38} : Parameters used for the analysis include $W_8 - W_{10}$ (and I_8), $W_2 = W_3$, and W_6. Considering the performance trade-offs with respect to different devices sizing $W_8 - W_{10}$ (and I_8), we observe that $W_9 - W_{10}$ have limited impact. Device sizing W_8 and its biasing current I_8 have the dominant contribution. The trade-off profile is shown in Figure 6.4 (left). Compared to C_{11}, CMRR remains unchanged and the new variables introduce a symmetric gain-bandwidth trade-off with both performances showing closely linear variations of 20% in opposing directions. Unity gain frequency exhibits a relative maximum around the midpoint of the analyzed range. In the second half of this range it decreases nonlinearly by up to 10%. For this scenario, the P_N trade-off exhibits a pronounced variation of 32%. In the first half of the range (lower width and current), it increases sharply as gain linearly decreases. The increase in noise is also at a higher rate than that of f_{3dB}. The second half of the analyzed rage presents a better trade-off pattern as noise tends to saturate

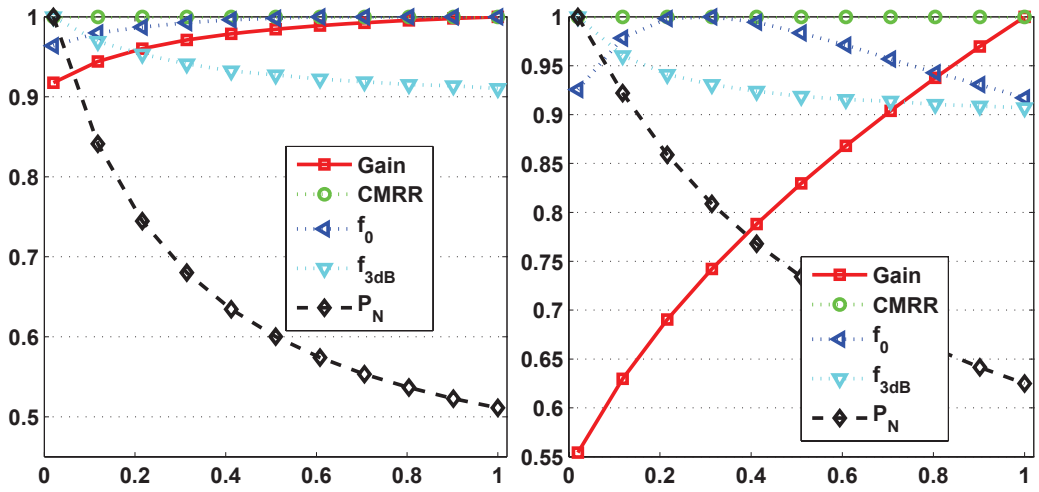

Figure 6.5: Normalized performance of C_{10} with respect to $W_8 \propto C_3$ and $W_1 \propto C_3$ ranges, respectively

towards a maximum value while f_{3dB} continues to increase. When also considering W_6 and a decreasing current I_8, the trade-off profile with respect to C_{11} is changed. Shown in Figure 6.4 (right), gain now increases almost linearly across the range and shows a variation of 65%. In contrast, f_{3dB} decrease across the range by 60% in nonlinear fashion. For the later half of the range (relatively large width, small current), gain increases faster than bandwidth deteriorates. This region is also favorable for controlling P_N as after its maximum increase of 45% (in the first half of the range) it can still be reduced by up to 10% while increasing gain. The maximum of f_0 is almost eliminated in this profile and performance has an accentuated decrese of 18%. The analysis with respect to $W_2 = W_3$ showed that these devices have similar behavior in both C_{38} and C_{11}.

C_{10} : Parameters considered for this topology include W_8, C_3, W_1, $W_2 = W_3$, and W_6. The performance trade-off profile with respect to different variables is shown in Figure 6.5 (left). The parameters have a limited impact on unity gain frequency which exhibits a variation of 5% while CMRR behavior remains unchanged. The gain-bandwidth trade-off shows a 10% variation with both saturating in the second half of the analyzed range (relatively large width and capacitance). The major benefit of this scenario is its noise performance

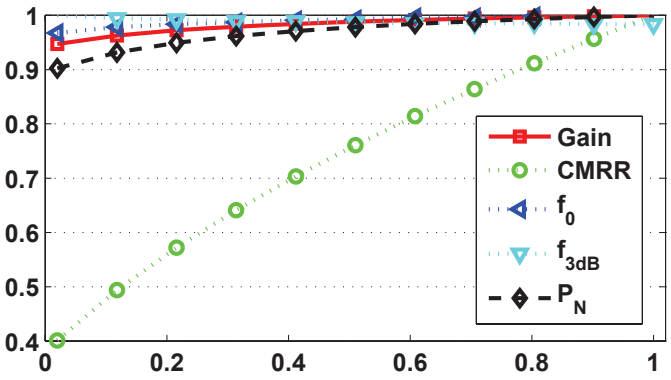

Figure 6.6: Normalized performance of C_{49} with respect to $W_4 = W_5 \propto W_8 = W_9$ range

which can be drastically reduced by up to 50%. The relative benefits of topology C_{10} are illustrated when considering variations of W_8, C_3 together with W_1. Similarly to topology C_{48}, device M_1 introduces a new output coupling in the signal path not found in C_{11}. This trade-off profile is shown in Figure 6.5 (right). Gain can now be increased over a 45% range across the entire range. For the second half of the range, the gain can be continuosly increased while f_{3dB} remains at a relatively constant value which is only 10% smaller than the maximum. While the f_0 maximum is achived for relatively small parameter values (and smaller gain and higher noise) in the second half of the range it is only reduced by 10%. More importantly, the gain-noise trade-off is eliminated as P_N reduces across the range by up to 35%. While considering parameters $W_2 = W_3$, topology C_{10} shows similar behavior to that of C_{11}. The behavior with respect to W_6 in C_{10} is similar to C_{48} since it reduces gain and bandwidth variations while allowing an increase of up to 50% in f_0 across the range. However, combinations of parameters $W_2 = W_3$ or W_6 with W_8 and C_3 present benefits for relaxing both the unity gain frequency and noise trade-offs.

C_{49} : The device sizes considered for trade-off characterization are $W_8 = W_9$, $W_2 = W_3$, $W_4 = W_5$, and W_6. Note that while devices $M_2 - M_5$ are common to C_{11}, they are included in the set of variables due to their impact on different circuit nodes in topology C_{49}. M_6 is included to investigate if the

new structures cause differences in its behavior. Trade-off analysis shows that with respect to $W_8 = W_9$, performance exhibits limited relative variation. Gain and CMRR show the largest variation by increasing 3% across the investigated range. In addition, varying $W_2 - W_6$ in different configurations produces a trade-off profile which is virtually identical to that of C_{11}. Therefore, the topology of C_{49} does not introduce any benefits related to these devices. A slight improvement in gain is obtained when the combination of $W_4 = W_5 \propto W_8 = W_9$ are varied. The trade-offs are shown in Figure 6.6. CMRR, f_{3dB}, f_0, and P_N exhibit the same trends as in C_{11} with respect to $W_4 = W_5$ only. Gain shows the same variation pattern, but in C_{49} it changes over 6%.

Sort Candidate List: Step (4) of the topology selection Algorithm 6.1 sorts the list of candidates based on their trade-off profiles (e.g., Figures 6.3-6.6) such that the topologies with the more pronounced advantages in improving performance of the reference design are preferred. For our example, the ordered list of candidates is $L_k = \{C_{10}, C_{48}, C_{38}, C_{49}\}$. Topology C_{49} is last as its analysis has shown that it does not significantly change the nature of the trade-offs with respect to reference C_{11}. Distinguishing between topologies C_{48} and C_{38} is done based on bandwidth and unity gain frequency behavior. While topology C_{38} presents the mechanism to eliminate the gain-noise trade-off for a fraction of its parameter ranges (when topology C_{48} does not show this benefit), the impact on f_{3dB} and f_0 is more pronounced in this region. Bandwidth is reduced by up to 60% (in contrast to 40% in C_{48}) while also reducing f_0 by 20% (in contrast to increasing f_0 in C_{48}). Overall, topology C_{10} is preferred from the set. It presents the mechanism to eliminate the gain-noise trade-off across the entire analyzed parameter ranges while limiting the reduction in bandwidth to a constant 10% across half of the range. This suggests greater flexibility of this topology in finding relative device sizing conditions that can meet performance requirements. In addition, topology C_{10} requires one of the smallest structural changes with respect to reference C_{11} (two new devices) and does not require additional static power (like the additional current branches in C_{38} and C_{48}).

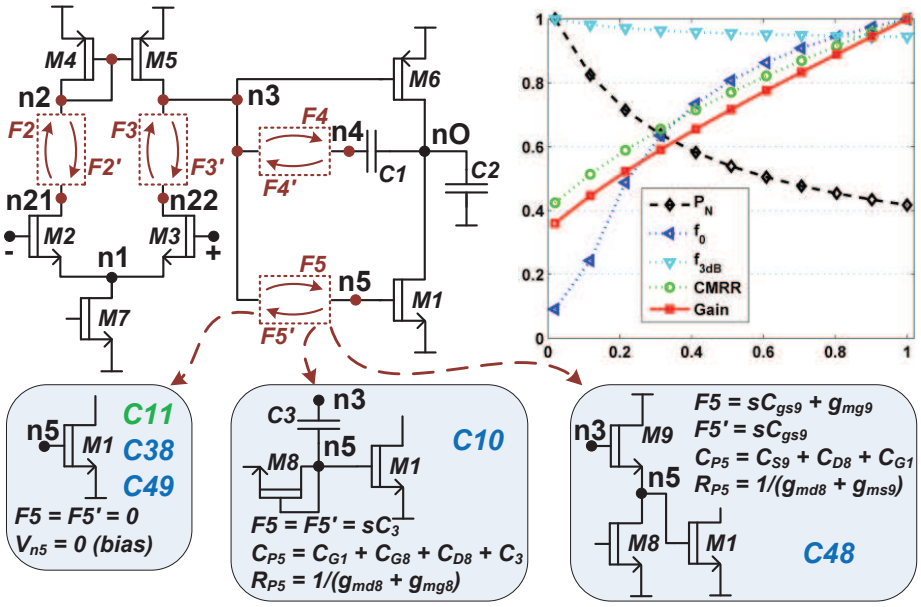

Figure 6.7: Abstraction of circuits $C_{11}, C_{10}, C_{38}, C_{48}, C_{49}$

Build Circuit Class Abstraction: The abstraction of topologies C_{11}, C_{10}, C_{38}, C_{48}, C_{49} is shown in Figure 6.7. The idealized circuit maintains the common structure and devices which are shared by all designs in its class. The common set consists of differential input pair and tail current source (M_2, M_3, M_7), simple current mirror load (M_4, M_5), and output driver pair and capacitors (M_1, M_6, C_1, C_2). Different structures among the designs are replaced by abstract functions F_i which capture both the cross-coupling between nodes and the nodal pole expressions. Specific instances of F_i result in the original set of circuits, like the example for F_5/F_5' in Figure 6.7 showing the different $n_3 \leftrightarrow n_5$ coupling and node n_5 pole resistance and capacitance configurations. In terms of performance trade-offs, the abstraction characterizes the class it represents in terms of the best possible combination which can be obtained from its instances. It's trade-off profile shares attributes from all five circuits and captures the possibility of improving gain, CMRR, unity gain frequency, and noise, while sacrificing only a fraction of the circuit's bandwidth.

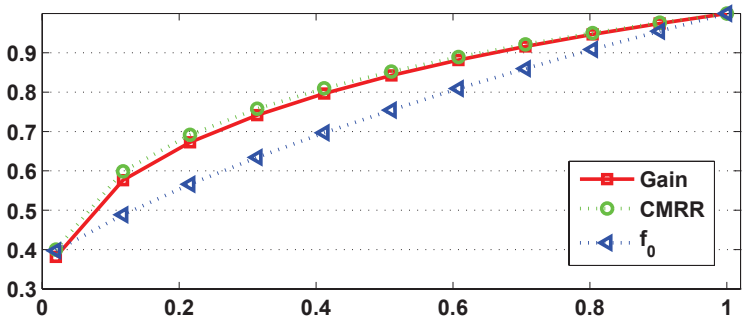

Figure 6.8: Normalized performance of C_{11} with respect to $W_2 = W_3$ range

6.2.2 Topology Refinement

We now illustrate an application of the proposed topology refinement technique to modify the classic Miller two-stage topology (C_{11}) and *discover* folded cascode solutions.

Identify Performance Bottleneck: In Part 1 of topology refinement Algorithm 6.2, the performance bottlenecks are identified using the trade-off profile of the reference design. Figure 6.8 shows the gain, CMRR, and unity gain frequency (f_0) profile of $C_k = C_{11}$, based on varying the input differential devices $M_2 - M_3$ widths over a predefined range. The normalized profile shows that gain and CMRR exhibit a more pronounced limiting behavior as sizes increase. Two thirds of their variation range is covered within only 40% of the width range. To address this limitation, the method identifies nodes $K = \{n_1, n_2, n_3\}$ to which devices $M_2 - M_3$ are connected and proceeds in Part 2 to identify topology refinements.

Find Refinement Candidates: Let's consider that in step (1) of Part 2 (Algorithm 6.2), node $n_2 \in K$ from reference C_{11} is selected for refinement. This selection points to the *Interm. 2* cluster of the fifty circuit ONCR from Figure 6.1. Using the ONCR, step (2) builds the list of refinement candidates consisting of nodes from circuits which are unmatched with C_{11} at this level in the representation. For example, topologies C_{16} [4] and C_{12} [78] are highlighted in orange in Figure 6.1 as potential candidates. The additional input edge constraint from step (2) of Algorithm 6.2 is also satisfied for these two candidates. The *Interm. 2* predecessors in the ONCR are matched for

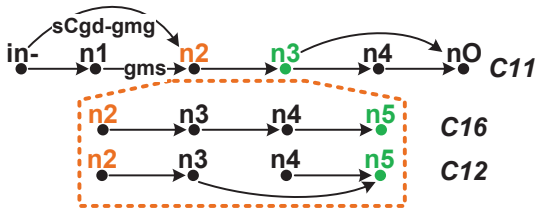

Figure 6.9: Refinement options for C_{11} starting at node n_2

topologies C_{11}, C_{16}, C_{12}: the *Interm. 1* cluster in Figure 6.1 shows a single group of matched nodes containing all three circuits. In addition, the circuit input nodes and their edge expression to n_2 are also matched (not shown in Figure 6.1). Figure 6.9 illustrates the matched input edge structure of node n_2 in C_{11}, C_{16}, C_{12}. This requirement is important to maintain compatibility of original and refined circuit structures. Hence, in step (2), the list of candidate nodes P includes $\{n_2(C_{16}), n_2(C_{12})\}$.

Incorporate Refinement: Steps (3)-(5) of Part 2 in Algorithm 6.2 introduce the features of the candidates to the reference design. Figure 6.9 illustrates the process for node n_2 from C_{11} using circuit structures from C_{16} and C_{12} represented as signal flow graphs. Using topology C_{16}, node n_2 structure of C_{11} is first replaced by that of C_{16}. Following the signal flow and model sequence in C_{16}, the next node reached is n_3. Its structure does not match any of nodes n_3 through n_O of the original C_{11} and is therefore also included in the refined design. Similarly, node n_4 of C_{16} is added to the refined C_{11}. After reaching node n_5 in C_{16}, the refinement process stops. The structure of this node precisely matches that of n_3 in C_{11} as both the symbolic pole and output edge expressions are identical. The remaining nodes in C_{11} (n_4, n_O) are kept unchanged. A similar sequence of steps occurs when the refinement at n_2 according to topology C_{12} is performed. While both refinement alternatives of Figure 6.9 introduce the same number of additional nodes to C_{11}, the corresponding structures are different. Figure 6.10 shows the schematics of the two refinement alternatives. Using the refinement from C_{16} creates a folded cas-

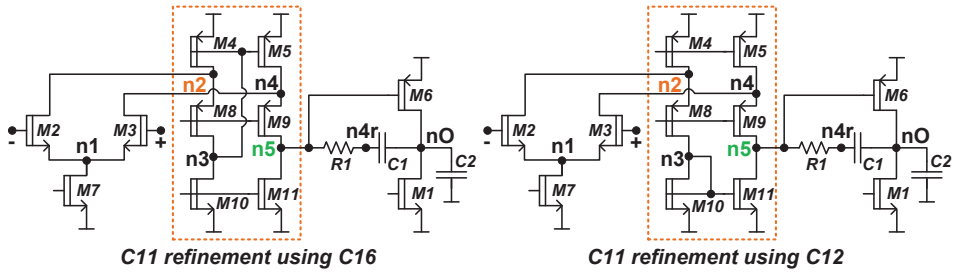

Figure 6.10: Schematics of refined C_{11} topologies

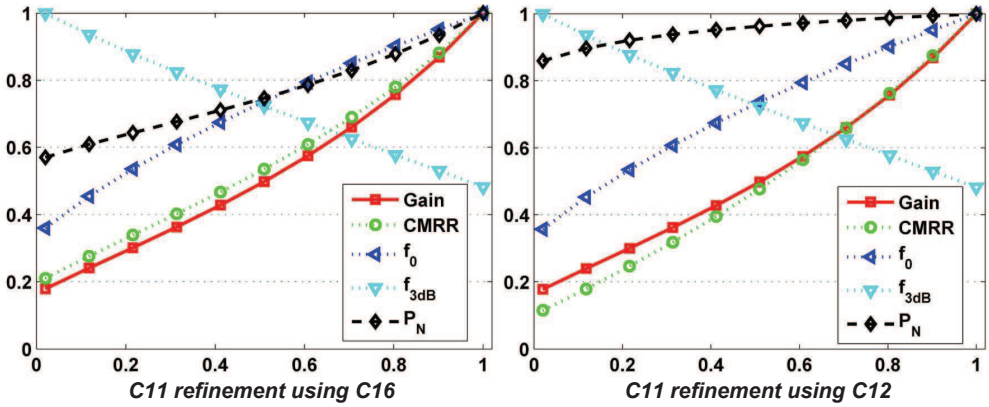

Figure 6.11: Normalized performance of refined C_{11} topologies with respect to $W_2 = W_3, W_8 = W_9, W_{10} = W_{11}$ ranges

code two stage Miller amplifier with wide swing cascode current mirror load. In contrast, the refinement from C_{12} produces a folded cascode amplifier with a simple current mirror load of the input stage.

Characterize Refined Topology: Steps (6)-(7) in Algorithm 6.2 characterize the performance of the refined topologies using the comparison operator. With respect to the reference solution C_{11}, symbolic comparison identifies the additional design variables of new devices $M_8 - M_{11}$ in both refinement alternatives of Figure 6.10. Considering also the original bottleneck devices $M_2 - M_3$, the technique generates the performance trade-off profiles which are used to quantify the advantages of the refined topologies. Figure 6.11 shows the nor-

malized trade-off profiles of the two refined topologies of C_{11} from Figure 6.10. Both topologies include the mechanism to change the gain and CMRR bottleneck of the original design from Figure 6.8 which can now be increased across the entire analyzed design parameter range. Both refined topologies show similar behavior for gain, CMRR, unity gain frequency (f_0), and bandwidth (f_{3dB}). We can observe that the gain-bandwidth trade-off is relaxed as gain increases nonlinearly and faster than bandwidth decreases. In terms of total output noise (P_N), the refined topologies exhibit different behavior. For the refinement based on C_{12}, noise has a relatively limited variation of 15% and saturates towards a maximum value. This suggests that noise can be maintained at relatively constant levels while increasing gain. For the refinement based on C_{16}, noise exhibits a variation of 40% and increases across the range. However, the increase in noise shows a smaller slope than the more pronounced increase of gain. Overall, this suggests that this topology presents greater flexibility in finding a device parameter combination for which both gain and noise performance are acceptable.

6.2.3 Creating New Topologies

The topology refinement procedure from Algorithm 6.2 effectively combines compatible features in the instance space from the existing pool of designs (e.g., nodes of Figure 5.8 where all abstract signals/structures are instantiated). With respect to the known fifty amplifier ONCR, the systematic process can produce a new topology that does not exist in the original design set. The refined topology based on circuit C_{12} from Figure 6.10 is an example of such a design. The topology incorporates relatively common features found in the original topologies: folded cascode differential input, simple current mirror, and common-source output driver. However, none of the existing solutions combine these structural features in this exact manner, making this circuit a *novel* synthesized topology.

In a similar fashion, refinement-of-refinement strategies can also generate new topologies using novel combinations of existing features. An example of two consecutive refinements of the reference two-stage amplifier C_{11} is shown

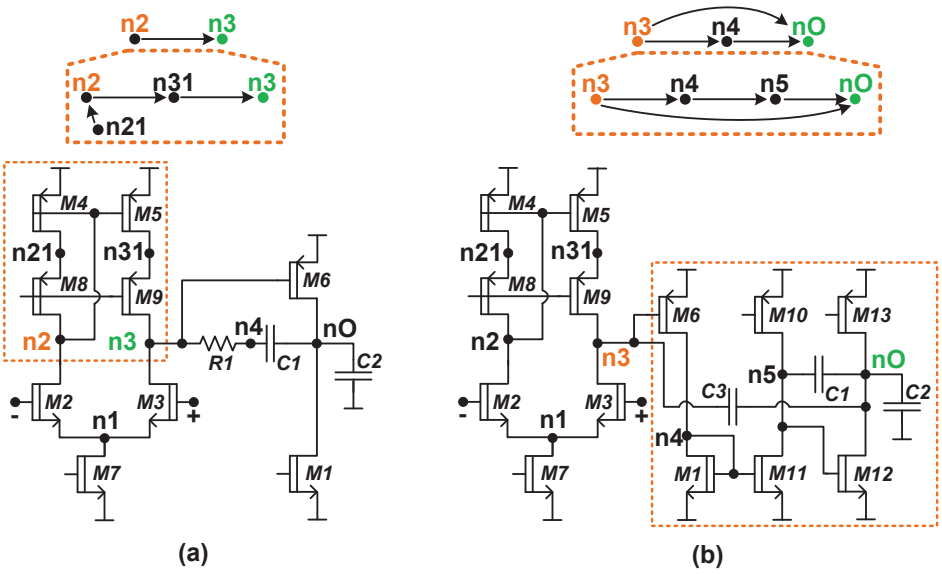

Figure 6.12: Consecutive refinements of C_{11}: (a) first refinement starting at circuit node n_2 and using C_{25}; (b) second refinement starting at circuit node n_3 and using C_{19}

in Figure 6.12. The first refinement step starts at circuit node n_2 and introduces the features of circuit C_{25} [70]. The resulting topology is new to the design set and consists of a two-stage amplifier with a wide swing cascode current mirror load (Figure 6.12(a)). The refinement process is then restarted at node n_3 (the first sequence node matched with reference C_{11}, end of previous refinement) using the features of circuit C_{19} [81]. The procedure transforms the design to create the topology of the three-stage Miller compensated amplifier shown in Figure 6.12(b). This design also constitutes a new topology with respect to the initial set.

Another option to create new topologies is to guide the refinement procedure to include a relatively unique feature in an existing design. Given a reference design, the ONCR information is used to first identify the more common features the circuit employs (i.e., its circuit nodes that form large groups in the ONCR). For the identified nodes, their structure is then replaced

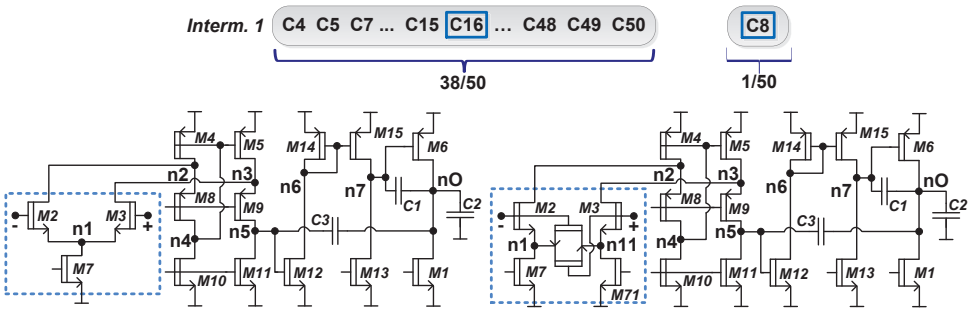

Figure 6.13: New topology found by replacing common input tail bias with *unique* source degeneration

with less common (but equivalent, same ONCR level) features. Figure 6.13 illustrates an example. For the reference nested-Miller folded cascode amplifier C_{16} [4], node n_1 is part of the largest group of nodes of the *Interm. 1* cluster in the fifty circuit ONCR (38 out of 50 circuits). A unique structure for *Interm. 1* is found in the group of design C_8 [52]. In the set, this is the only circuit with the input source degeneration feature. Introducing this feature in the reference design results in a source degenerated three-stage folded cascode amplifier, a topology that was not present in the original fifty circuit set.

Ultimately, a new topology can be created by combining the most common compatible features from ONCR up to a desired level. For example, the procedure starts with the most common feature of the *Interm. 1* cluster. Then it scans the *Interm. 2* cluster in decreasing order of feature popularity to find compatible structures (based on the refinement procedure's criteria) and advances in this manner until a desired circuit complexity is achieved (e.g., *Interm. 6*). Figure 6.14 illustrates the topology using the most common ONCR features up to the *Interm. 5* node. The resulting single-stage folded cascode amplifier with a cascode current mirror load constitutes a new feature combination with respect to the initial amplifier designs set. Combining the most common structures resembles a strategy that reuses well known and trusted features. Arguably, different ONCR scanning strategies can be used to identify new topologies. For example, features could be combined in increasing

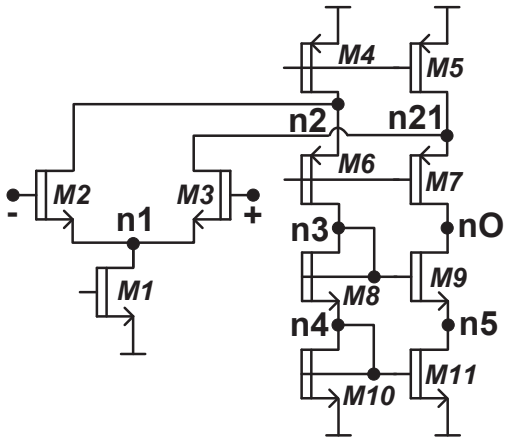

Figure 6.14: Topology resulting from combination of the most common compatible features from ONCR up to *Interm. 4*

order of their popularity, resulting in a circuit that consists of the most unique compatible features.

6.3 Summary

A set of reasoning-based approaches to circuit topology selection, refinement, and synthesis were presented using the concepts presented in Chapters 3, 4 and 5 of this dissertation. The proposed approach conducts steps in which the performance trade-offs and bottlenecks guide the selection and inclusion of new topological features. Every synthesis solution is explicitly justified by the trade-offs and bottlenecks that are improved by the related structural feature. This process resembles reasoning, decision making, and cause-effect understanding involved in manual topology design. Case study examples based on the fifty circuit ONCR of Chapter 3 were used to illustrate the techniques.

Chapter 7

Conclusions

This dissertation presented novel techniques to systematically characterize the analog circuit design space. A preliminary study on measuring innovation in circuit design using metrics from design science illustrated the importance of accurately describing the uniqueness and variety of design features. Based on the insight gained from this study, two main systematic methods were developed for constructing analog circuit design space descriptions: (i) creating ordered node feature clustering representations (ONCR) for large sets of analog circuits based on topology matching and (ii) generating systematic comparison data between analog circuits to capture the performance implications of distinguishing structures. The proposed techniques were used to introduce preliminary work on developing a prototype framework for modeling the analog circuit design feature variety through concept structures that expresses domain knowledge for analog circuits implementing the same functionality. A case study example illustrated application of the proposed methods to a reasoning-based analog circuit topology synthesis alternative.

The study in Chapter 2 investigated the uniqueness and variety of the design features of popular analog circuits by using the set of metrics proposed in the design science literature [1, 2]. The considered circuits include current mirrors, transconductors, and operational amplifiers. The detailed analysis indicated that the metrics are capable of characterizing the uniqueness and

variety of the design features of analog circuits and that popular design features show a decreasing trend in their scores over time. Starting at high values, the scores decrease as more on more new design reuse the feature. In contrast, design features that are not adopted maintained a high uniqueness score, indicating that they are rarely used in future solutions. This suggests that studying the evolution of the metric values over time offers a more reliable insight on the utility of a design feature as it considers not only its uniqueness but also its usefulness for future designs. The analysis of a set of synthesized circuits [8] indicated that it is challenging to automatically produce designs with unique yet useful features. The generated circuits tend to have few novel features. This suggests that devising innovation-related design rules for automated synthesis is an interesting area to explore. Moreover, the uniqueness and variety scores of a design set can give insight on the covered solution space, thus can serve to diversify the search towards unexplored areas but need to be coupled with design usefulness (performance).

While the study presented in Chapter 2 managed to illustrate the importance of accurately describing the uniqueness and variety of design features, the characterization process used was less systematic due to the feature selection mechanism which highly depends on designer expertise and preference. In contrast, Chapter 3 described an automated symbolic technique for generating circuit models, called ordered node clustering representations (ONCR), that indicate the main similarities and differences between structurally different analog circuits. The proposed method discussed three main steps: identifying the possible sets of separation criteria, analyzing the criteria sets with respect to their potential of distinguishing the circuits, and building the ordered clustering scheme to maximize the separation among dissimilar circuits. Four separation scores were studied: entropy, item characteristics, category characteristics, and Bayesian classifiers. Results suggested that entropy is preferable to correctly identify the highest number of common and distinguishing features for a circuit set. It produces clustering schemes favoring more groups of larger sizes. Clusters with many groups of small sizes occupy the lower levels of the schemes.

The generated feature clustering schemes offer insight, through symbolic expressions, about the similar and dissimilar circuit features, including topological structures, and the common and distinct symbolic sub-expressions. The design variables (e.g., g_m, C_{gs}, C_{gd}, etc.) that appear in the distinguishing symbolic expressions indicate the available flexibility in positioning poles and zeros. In addition, clustering schemes are also useful for synthesizing topologies and refining existing circuit structures to tackle new performance requirements. This includes reusing solutions of coupling circuit nodes through linear and frequency-dependent connections, adding new devices at nodes, and replicating signal flow sub-structures for circuit nodes. In other practical applications, ONCRs can also be employed to extend the set of basic building blocks for existing analog circuit topology synthesis techniques.

The concepts introduced in Chapter 3 were extended in Chapter 4 with a novel technique for systematically generating comparison data between two analog circuits. The comparison data refers to DC gain, bandwidth, noise, CMRR. The nodes with similar electric behavior in the two circuits are found through a dual matching approach of both circuit topologies and symbolic expressions. The method computes the constraints that relate the electric behavior to changes of the performance attributes, such as modification of design trade-offs, availability of free design variables, and achievable performance values. Focus is on how identified dissimilar aspects can be exploited to improve performance. The comparison data is important for getting insight about the common and unique benefits of a circuit, selecting fitting circuit topologies for system design, and refining and optimizing circuit topologies. Using the constraints, the produced the comparison data includes modification of design trade-offs, availability of free design variables, and achievable performance values in different relative device sizing scenarios.

In Chapter 5 we introduced the concept structure model to express the design feature variety in analog circuits. The prototype modeling framework is based on the techniques from Chapters 3 and 4. The model uses four basic operators, circuit comparison, circuit instantiation-abstraction, circuit combination, and design feature induction. The insight offered by the model

is important to characterize the distinct and common features in a circuit and for the exploration of new conceptual designs. For example, the original set of circuits used in the detailed case study consists of only 9 distinct topologies. However, there are more than 140 distinct combinations that can result using the proposed concept structures for OpAmps. The concept structure offers the support to identify alternative signal processing flows which represent feasible novel conceptual designs that can better meet the specification requirements by eliminating performance bottlenecks or by relaxing trade-offs.

The concept structure model is envisioned as the main data structure of a reasoning-based synthesis flow for analog circuits. In addition to producing circuit topologies, the method finds alternative signal processing flows which represent different conceptual designs that can meet the specification requirements. Every synthesis step attempts to address the performance bottlenecks of a circuit topology by changing the relations between the design variables of the bottlenecks. Relations are changed by searching for other designs in the concept structure with different bottlenecks and then combining their features with the current solution or by exploring orthogonal ways of relating the variables of the bottlenecks through new ways of interconnecting circuit nodes based on the induction operator. The performance modifications of the new concepts are evaluated through the systematic comparison of the modified and original circuits. If feasible, any new solutions created during the steps of concept combination or induction are added to extend the concept structure for future re-use.

Finally, Chapter 6 presented applications to topology synthesis of the methods proposed in this dissertation. Case study examples illustrated the techniques based on a reasoning-like process. The synthesis procedure precisely identifies the circuit feature that causes a performance bottleneck and aims to locally address the limitation by incorporating only new topological features that are likely to improve performance. Therefore, the synthesis output is not only a design but also the justifications for the performed design decisions. This approach closely resembles an expert designer's style of analog circuit topology refinement and selection and offers an alternative to

current optimization/evolution-based techniques. The proposed set of procedures can also be employed to complement library-based numerical search methods. They offer the support to systematically update the working library with novel, designer-trusted structures obtained either from current publications or through combinations of existing building blocks, hence increasing the diversity of topologies explored by these tools.

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Appendix A

ONCR Results for Imprecise Matching Experiments

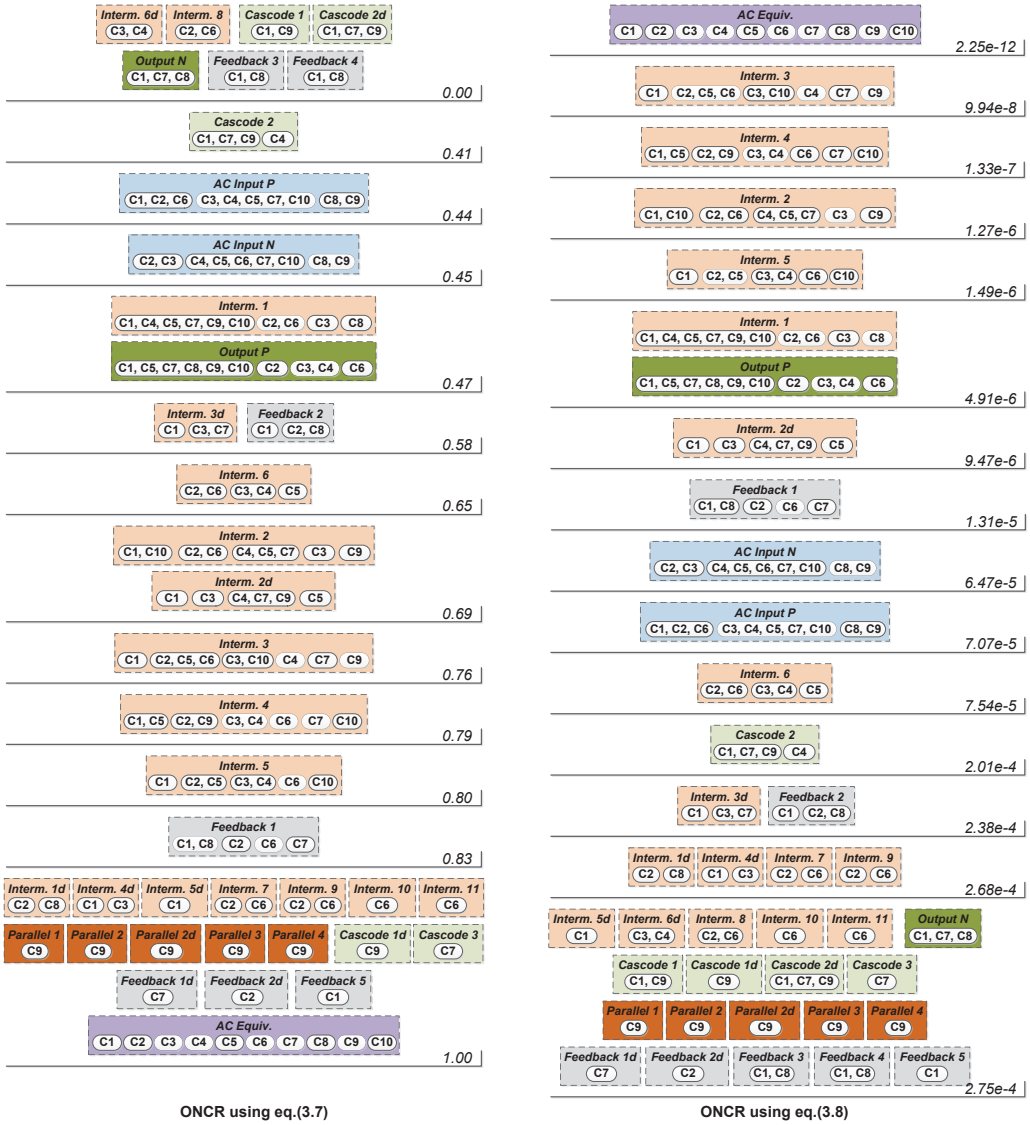

Figure A.1: ONCR of the ten amplifier design set for imprecise matching run 4 (EC=2, ER=2, PC=2, PR=2) using entropy based (eq. (3.7)) and item characteristics based (eq. (3.8)) separation criteria

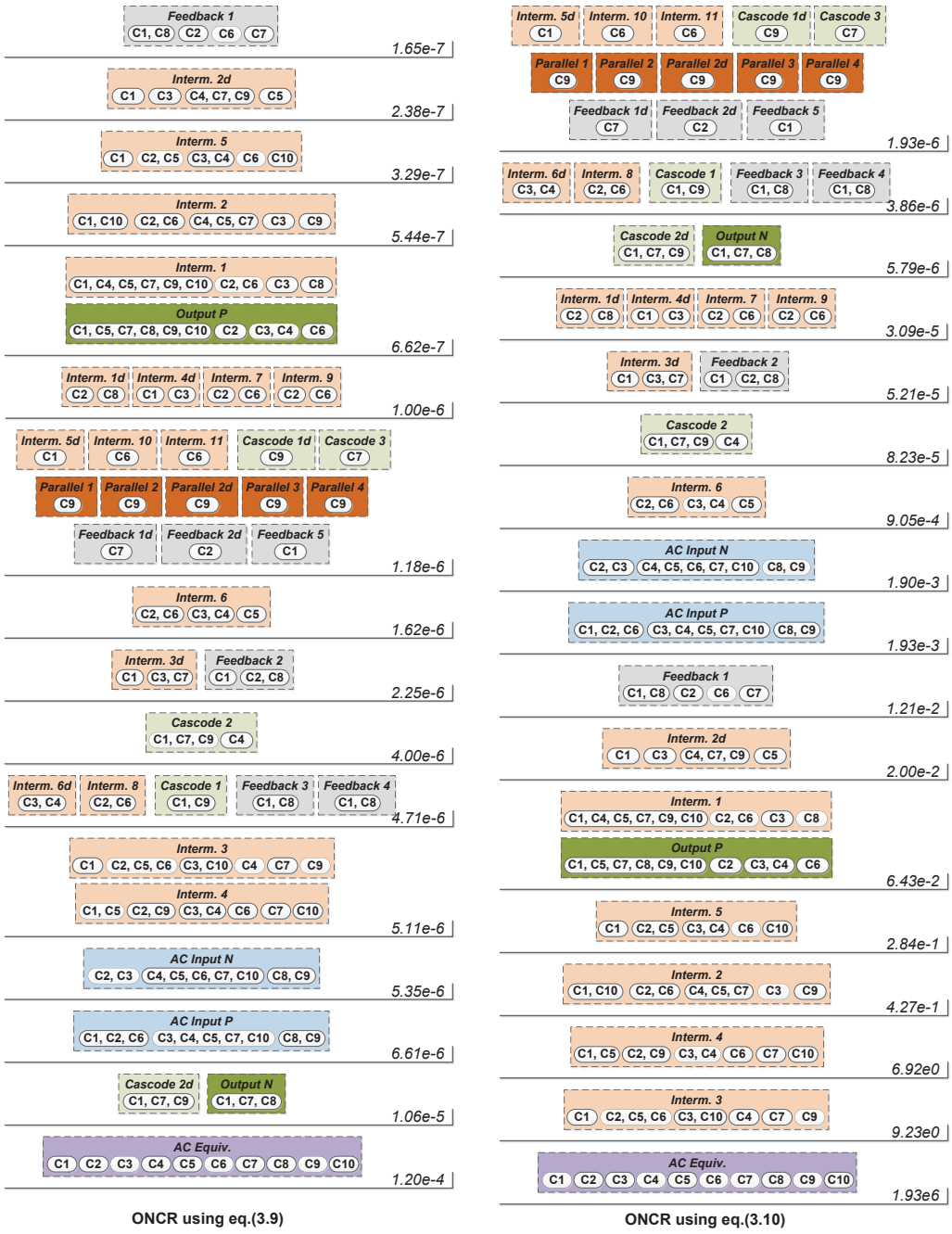

Figure A.2: ONCR of the ten amplifier design set for imprecise matching run 4 (EC=2, ER=2, PC=2, PR=2) using category characteristics based (eq. (3.9)) and Bayesian classifier based (eq. (3.10)) separation criteria

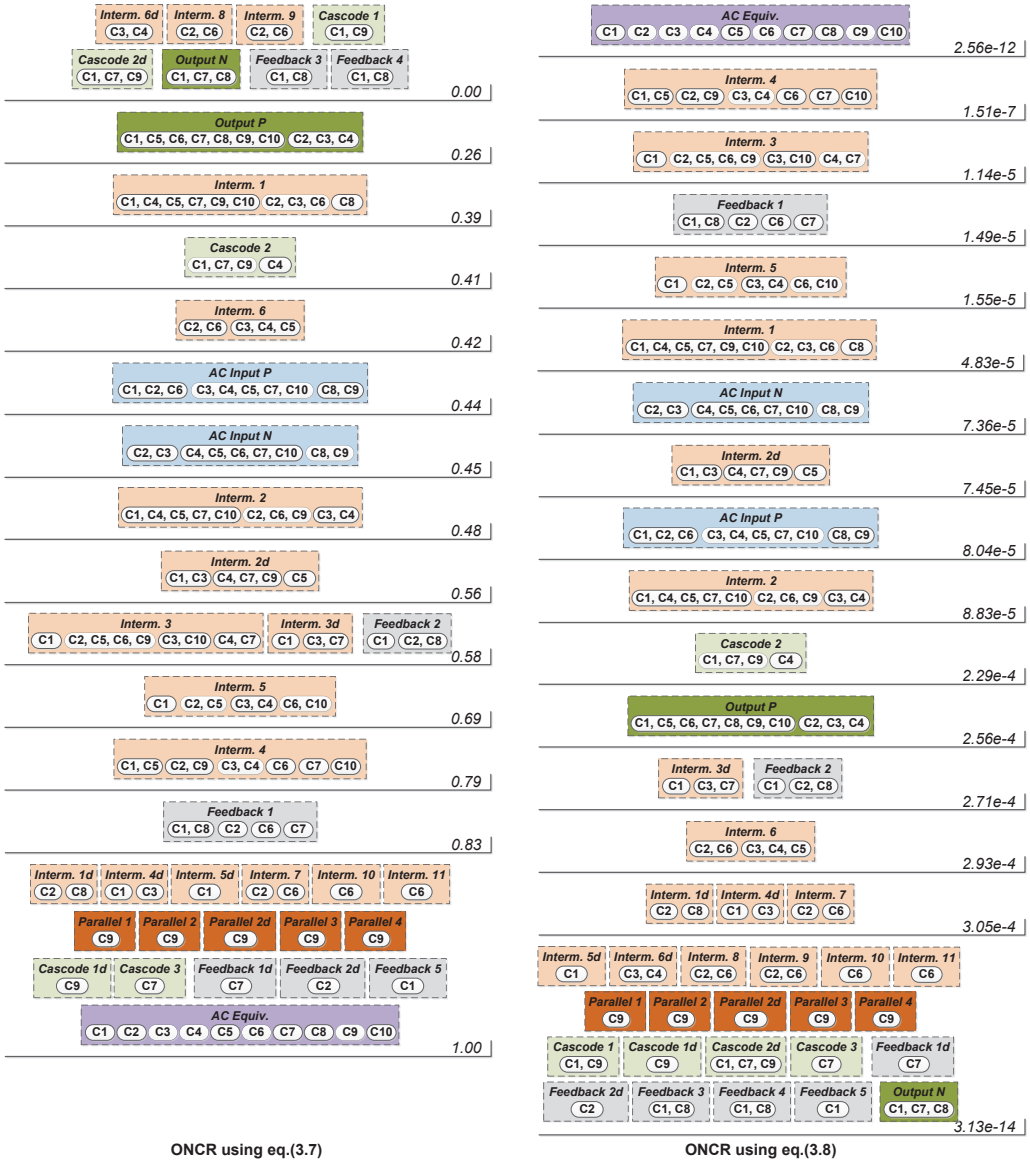

Figure A.3: ONCR of the ten amplifier design set for imprecise matching run 6 (EC=2, ER=2, PC=6, PR=2) using entropy based (eq. (3.7)) and item characteristics based (eq. (3.8)) separation criteria

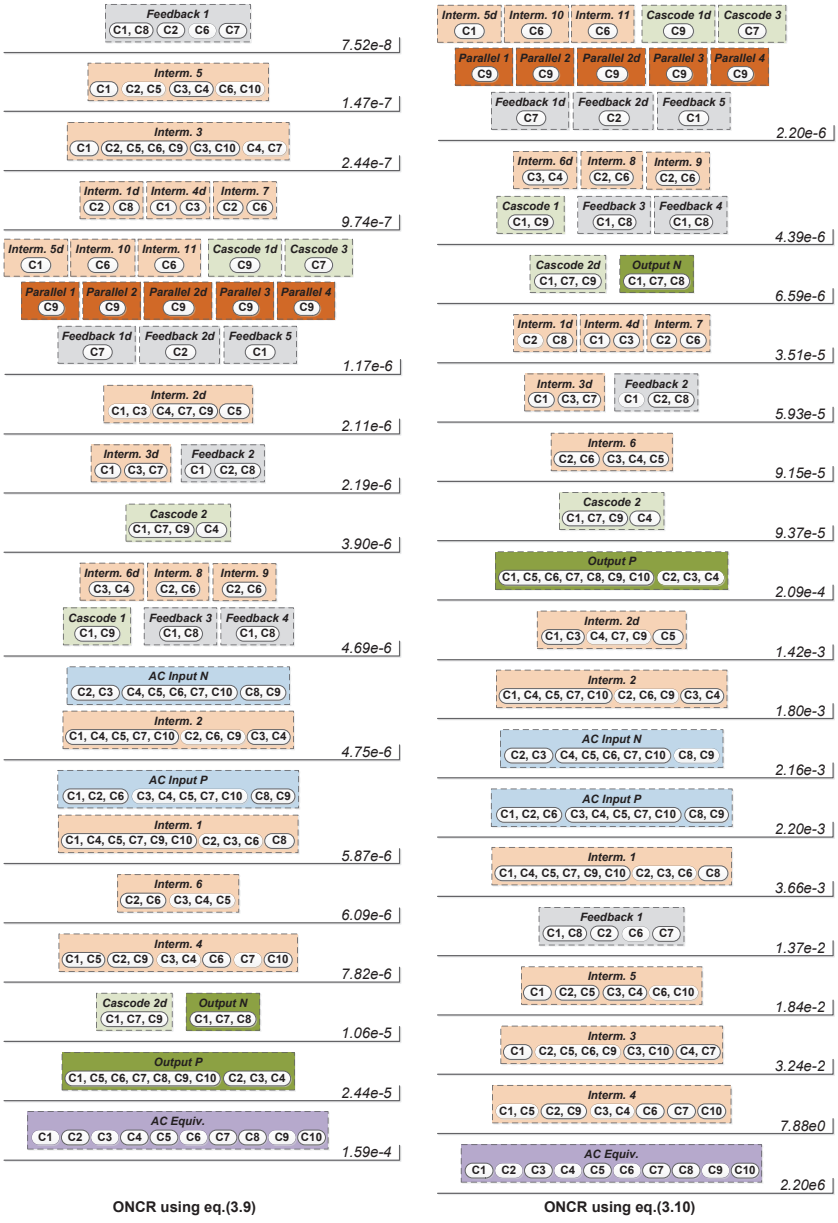

Figure A.4: ONCR of the ten amplifier design set for imprecise matching run 6 (EC=2, ER=2, PC=6, PR=2) using category characteristics based (eq. (3.9)) and Bayesian classifier based (eq. (3.10)) separation criteria

Table A.1: Cluster separations scores for run 4 on fifty designs

Cluster	# Groups	# Nodes	S0	S1	S2	S3
AC Equiv.	48	50	9.86E-01	1.18E-82	1.41E-02	3.21E+77
AC Input P	5	50	2.37E-01	1.43E-08	1.22E-06	5.45E+00
AC Input N	5	49	2.13E-01	7.60E-09	1.17E-06	1.01E+01
Output P	7	50	2.15E-01	2.40E-12	6.70E-07	8.58E+04
Output N	4	16	2.97E-01	4.95E-07	4.81E-07	2.63E-02
Interm. 1	9	50	2.29E-01	3.83E-16	8.13E-06	1.10E+09
Interm. 1d	4	5	8.28E-01	4.33E-06	4.70E-08	9.41E-04
Interm. 2	11	47	4.52E-01	2.43E-17	2.35E-05	2.89E+10
Interm. 2d	8	35	4.35E-01	4.81E-12	1.60E-06	4.40E+04
Interm. 3	14	42	5.54E-01	1.70E-21	6.05E-05	7.21E+14
Interm. 3d	9	12	8.43E-01	7.25E-12	4.68E-07	1.40E+04
Interm. 4	16	35	7.36E-01	7.47E-23	7.61E-05	1.98E+16
Interm. 4d	4	6	6.93E-01	3.13E-06	6.77E-08	1.56E-03
Interm. 5	9	26	5.18E-01	3.59E-13	2.20E-06	6.13E+05
Interm. 5d	3	3	1.00E+00	2.87E-05	4.48E-08	3.66E-05
Interm. 6	10	20	6.96E-01	1.06E-13	2.51E-06	2.14E+06
Interm. 6d	2	3	5.79E-01	7.82E-05	1.20E-07	4.07E-06
Interm. 7	6	6	1.00E+00	6.28E-08	2.73E-10	2.53E-01
Interm. 7d	1	1	1.00E+00	8.98E-05	5.69E-08	1.51E-07
Interm. 8	3	4	7.50E-01	2.43E-05	7.96E-08	5.78E-05
Interm. 9	4	4	1.00E+00	5.28E-06	3.01E-08	6.17E-04
Interm. 9d	2	2	1.00E+00	8.80E-05	5.35E-08	2.41E-06
Interm. 10	3	3	1.00E+00	2.87E-05	4.48E-08	3.66E-05
Interm. 10d	2	2	1.00E+00	8.80E-05	5.35E-08	2.41E-06
Interm. 11	1	1	1.00E+00	8.98E-05	5.69E-08	1.51E-07
Cascode 1	1	6	0.00E+00	8.98E-05	2.05E-06	9.04E-07
Cascode 1d	1	4	0.00E+00	8.98E-05	9.10E-07	6.02E-07
Cascode 2	4	16	3.86E-01	1.01E-06	4.81E-07	1.29E-02
Cascode 2d	2	7	2.11E-01	4.31E-05	6.55E-07	1.72E-05
Cascode 3	2	3	5.79E-01	7.82E-05	1.20E-07	4.07E-06
Cascode 3d	2	2	1.00E+00	8.80E-05	5.35E-08	2.41E-06
Cascode 4	1	1	1.00E+00	8.98E-05	5.69E-08	1.51E-07
Cascode 5	1	1	1.00E+00	8.98E-05	5.69E-08	1.51E-07
Cascode 5d	1	1	1.00E+00	8.98E-05	5.69E-08	1.51E-07
Feedback 1	6	11	6.85E-01	2.65E-08	9.17E-10	1.10E+00
Feedback 1d	1	3	0.00E+00	8.98E-05	5.12E-07	4.52E-07
Feedback 2	3	4	7.50E-01	2.43E-05	7.96E-08	5.78E-05
Feedback 2d	1	1	1.00E+00	8.98E-05	5.69E-08	1.51E-07
Feedback 3	3	3	1.00E+00	2.87E-05	4.48E-08	3.66E-05
Feedback 4	2	2	1.00E+00	8.80E-05	5.35E-08	2.41E-06
Feedback 5	1	1	1.00E+00	8.98E-05	5.69E-08	1.51E-07
Parallel 1	2	6	3.55E-01	7.82E-05	4.81E-07	8.13E-06
Parallel 1d	1	1	1.00E+00	8.98E-05	5.69E-08	1.51E-07
Parallel 2	3	5	6.55E-01	2.48E-05	1.24E-07	7.06E-05
Parallel 2d	3	5	6.55E-01	2.48E-05	1.24E-07	7.06E-05
Parallel 3	1	2	0.00E+00	8.98E-05	2.28E-07	3.01E-07
Parallel 4	1	2	0.00E+00	8.98E-05	2.28E-07	3.01E-07

Table A.2: Cluster separations scores for run 6 on fifty designs

Cluster	# Groups	# Nodes	S0	S1	S2	S3
AC Equiv.	48	50	9.86E-01	1.46E-82	2.15E-02	3.96E+77
AC Input P	5	50	2.37E-01	1.77E-08	6.44E-07	6.72E+00
AC Input N	5	49	2.13E-01	9.38E-09	6.19E-07	1.24E+01
Output P	5	50	2.92E-01	5.14E-08	6.44E-07	2.31E+00
Output N	3	16	3.51E-01	2.24E-05	1.20E-06	3.81E-04
Interm. 1	7	50	2.15E-01	2.97E-12	1.99E-06	1.06E+05
Interm. 1d	4	5	8.28E-01	5.34E-06	3.90E-08	1.16E-03
Interm. 2	7	47	3.47E-01	9.61E-11	1.76E-06	3.07E+03
Interm. 2d	5	35	3.45E-01	5.22E-08	3.16E-07	1.59E+00
Interm. 3	8	42	3.96E-01	2.70E-12	4.70E-06	1.43E+05
Interm. 3d	5	12	6.11E-01	4.94E-07	3.71E-08	5.78E-02
Interm. 4	10	35	6.09E-01	2.05E-13	1.31E-05	2.97E+06
Interm. 4d	3	6	4.84E-01	1.77E-05	1.68E-07	1.81E-04
Interm. 5	6	26	4.81E-01	1.69E-08	2.39E-08	6.22E+00
Interm. 5d	2	3	5.79E-01	9.65E-05	1.18E-07	5.02E-06
Interm. 6	6	20	5.01E-01	9.49E-09	1.41E-08	8.50E+00
Interm. 6d	2	3	5.79E-01	9.65E-05	1.18E-07	5.02E-06
Interm. 7	4	6	7.42E-01	5.15E-06	5.62E-08	1.45E-03
Interm. 7d	1	1	1.00E+00	1.11E-04	5.68E-08	1.86E-07
Interm. 8	3	4	7.50E-01	2.99E-05	7.48E-08	7.14E-05
Interm. 9	3	4	7.50E-01	2.99E-05	7.48E-08	7.14E-05
Interm. 9d	1	2	0.00E+00	1.11E-04	2.27E-07	3.72E-07
Interm. 10	3	3	1.00E+00	3.55E-05	4.21E-08	4.52E-05
Interm. 10d	2	2	1.00E+00	1.09E-04	5.26E-08	2.97E-06
Interm. 11	1	1	1.00E+00	1.11E-04	5.68E-08	1.86E-07
Cascode 1	1	6	0.00E+00	1.11E-04	2.04E-06	1.12E-06
Cascode 1d	1	4	0.00E+00	1.11E-04	9.08E-07	7.43E-07
Cascode 2	4	16	3.86E-01	1.25E-06	3.99E-07	1.59E-02
Cascode 2d	2	7	2.11E-01	5.32E-05	6.44E-07	2.12E-05
Cascode 3	2	3	5.79E-01	9.65E-05	1.18E-07	5.02E-06
Cascode 3d	2	2	1.00E+00	1.09E-04	5.26E-08	2.97E-06
Cascode 4	1	1	1.00E+00	1.11E-04	5.68E-08	1.86E-07
Cascode 5	1	1	1.00E+00	1.11E-04	5.68E-08	1.86E-07
Cascode 5d	1	1	1.00E+00	1.11E-04	5.68E-08	1.86E-07
Feedback 1	6	11	6.85E-01	3.27E-08	4.28E-09	1.36E+00
Feedback 1d	1	3	0.00E+00	1.11E-04	5.11E-07	5.58E-07
Feedback 2	3	4	7.50E-01	2.99E-05	7.48E-08	7.14E-05
Feedback 2d	1	1	1.00E+00	1.11E-04	5.68E-08	1.86E-07
Feedback 3	3	3	1.00E+00	3.55E-05	4.21E-08	4.52E-05
Feedback 4	2	2	1.00E+00	1.09E-04	5.26E-08	2.97E-06
Feedback 5	1	1	1.00E+00	1.11E-04	5.68E-08	1.86E-07
Parallel 1	2	6	3.55E-01	9.65E-05	4.73E-07	1.00E-05
Parallel 1d	1	1	1.00E+00	1.11E-04	5.68E-08	1.86E-07
Parallel 2	2	5	4.18E-01	1.04E-04	3.29E-07	7.74E-06
Parallel 2d	2	5	4.18E-01	1.04E-04	3.29E-07	7.74E-06
Parallel 3	1	2	0.00E+00	1.11E-04	2.27E-07	3.72E-07
Parallel 4	1	2	0.00E+00	1.11E-04	2.27E-07	3.72E-07

Appendix B

Detailed Comparison Data Generation Experiments

B.1 Comparison Data for Two Low Voltage Amplifiers

Figure B.1 shows two low-voltage amplifier circuits denoted as AMP_1 and AMP_2. The first design is a two-stage class-AB topology [3]. The second circuit is a three-stage amplifier with positive feedback compensation [4].

Nodal and circuit matching first found similar and distinct nodes between the two circuits with respect to structure and electrical behavior. Figure B.2 illustrates the nodes and couplings of the amplifiers. Nodes V_{in+}, V_{in-} (signal inputs), V_1, and V_o (output) have identical symbolic pole expressions in both designs. Similarly, the couplings between nodes, Fc_i ($i = \overline{1,9}$), are the same in both circuits. Nodes V_3 and V_7 are only partially-matched due to (small) differences in their symbolic pole expressions.

Enforcing that nodes V_3 have comparable pole components in both

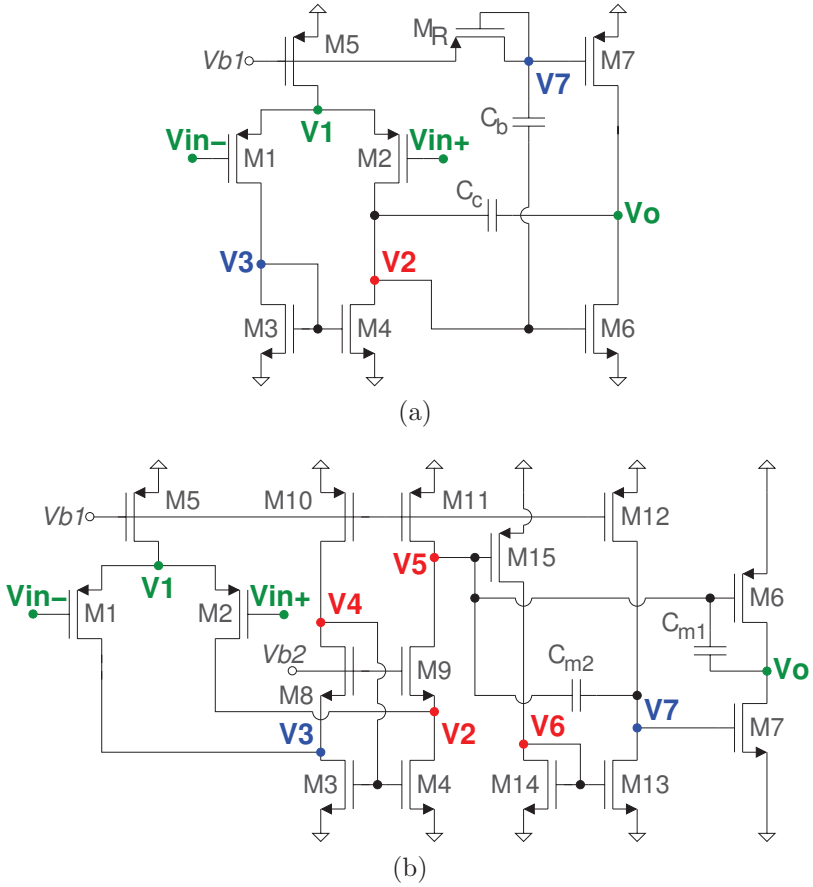

Figure B.1: Two low-voltage differential amplifiers: (a) class-AB 2-stage AMP_1 [3]; (b) 3-stage AMP_2 [4] with positive feedback compensation scheme

circuits results in the following two constraints:

$$g_{mg3}|_{\text{AMP}_1} \equiv g_{ms8}|_{\text{AMP}_2} \text{ and}$$
$$(C_{gs3} + C_{gb3})|_{\text{AMP}_1} \equiv (C_{gs8} + C_{sb8})|_{\text{AMP}_2}, \tag{B-1}$$

when device M_1 parameters are matched between the two circuits, and transistors M_3 and M_4 are functionally matched in AMP_1 (current mirror). Constraints (B-1) imply that device parameters of M_3 in AMP_1 are paired with

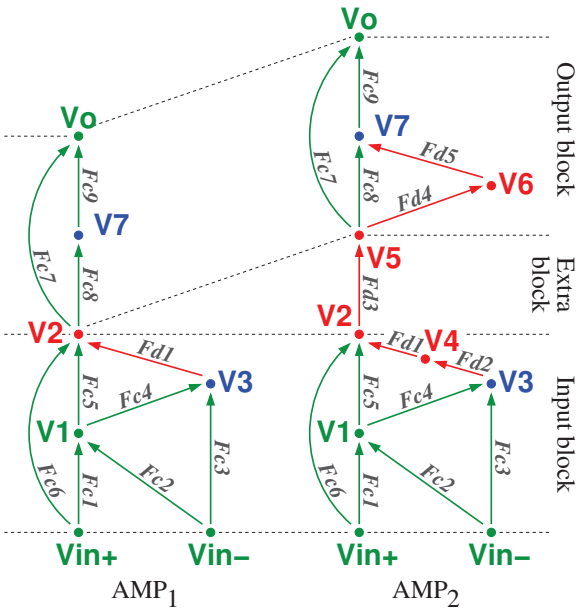

Figure B.2: Model graphs and sub-blocks for AMP_1 and AMP_2

those of device M_8 in AMP_2. Similar constraints exist for the pole at node V_7:

$$
\begin{aligned}
&(g_{mdR} + g_{mgR})|_{\mathrm{AMP}_1} \equiv (g_{md12} + g_{md13})|_{\mathrm{AMP}_2} \text{ and} \\
&(C_{dbR} + C_{gsR} + C_{gbR})|_{\mathrm{AMP}_1} \equiv \\
&\equiv (C_{gd12} + C_{db12} + C_{gd13} + C_{db13})|_{\mathrm{AMP}_2},
\end{aligned} \tag{B-2}
$$

when devices M_7 and capacitances $C_b \equiv C_{m2}$ are matched between the two designs. Constraints (B-2) link the parameters of device M_R in AMP_1 to the combined parameters of two devices, M_{12} and M_{13}, in AMP_2. Hence, the second circuit has greater flexibility to meet the matching conditions (B-2) of the ϵ-isomorphism.

In Figure B.2, the *input* and *output* blocks of AMP_1 and AMP_2 are matched and express similar electrical behavior. There are also *distinguishing* sub-structures present at nodes V_2, V_4, V_5, and V_6 with couplings between the nodes given by symbolic expressions Fd_j, $j = \overline{1,5}$. For example, the additional nodes in AMP_2 (V_4 and V_6) impose different model graph edges: F_{d1}, F_{d2} for the *input* block and F_{d4}, F_{d5} for the *output* block, respectively.

The *extra* block in AMP_2 has no equivalent in AMP_1. Finally, the set of symbolic transfer functions for each circuit block are generated: (i) H_{comm} defines the common symbolic parts of the blocks in both circuits, and (ii) H_{diff} expressing the distinguishing symbolic terms for the blocks in each circuit.

The transfer functions to node V_2 of the *input* block of AMP_1 and AMP_2 are expressed as follows:

$$\text{AMP}_1 : H_2 = H_{comm_1} \times H_{diff_1} + H_{comm_2} \times H_{diff_2} \tag{B-3}$$

$$\text{AMP}_2 : H_2 = H_{comm_1} \times H_{diff_3} + H_{comm_2} \times H_{diff_4}, \tag{B-4}$$

where H_{comm_1} and H_{comm_2} are common signal paths in both designs and H_{diff_i} $(i = \overline{1,4})$ captures the differences of the two *input* blocks:

$$H_{diff_1} = \frac{R_2}{1 + sR_2C_2},\ H_{diff_2} = \frac{R_2Fd_1}{1 + sR_2C_2}, \tag{B-5}$$

$$H_{diff_3} = \frac{R_2}{1 + sR_2C_2},\ H_{diff_4} = \frac{R_2R_4Fd_1Fd_2}{(1 + sR_2C_2)(1 + sR_4C_4)}. \tag{B-6}$$

Expressions (B-3)-(B-6) indicate that the *input* blocks of circuits AMP_1 and AMP_2 differ because of the poles at nodes V_2 and V_4, and the coupling between nodes $V_3 \rightarrow V_2$ and $V_3 \rightarrow V_4 \rightarrow V_2$.

The *extra* block of design AMP_2 has no equivalent in circuit AMP_1 (Figure B.2) and its transfer function to circuit node V_5 is defined only by unmatched components:

$$H_5 = H_{diff_5} = \frac{R_5Fd_3}{1 + sR_5C_5}, \tag{B-7}$$

Figure B.2 shows that the *output* block of AMP_1 is composed of only matched nodes. Hence, only AMP_2 exhibits differences in this circuit block with a transfer function to node V_o defined as follows:

$$H_o = H_{comm_3} + H_{diff_6}, \tag{B-8}$$

where H_{comm_3} represents the common structure (also present in AMP_1).

H_{diff_6} is defined by the unmatched pole and edges related to node V_6:

$$H_{diff_6} = \frac{R_6 F d_4 F d_5}{1 + sR_6 C_6}. \tag{B-9}$$

DC-gain of each circuit sub-structure is characterized by transfer functions $H_{comm_i}(0)$ and $H_{diff_i}(0)$. For analysis, considering $H_{comm_i}(0)$ constant, the constraints on $H_{diff_i}(0)$'s design variables are identified, such that the overall gain is improved. For AMP_2, the *input* block constraint for increasing DC-gain through unmatched variables is as follows:

$$K_1 + \frac{K_2}{K_3(K_4 + g_{md10})} \nearrow . \tag{B-10}$$

K_i are constants induced by common nodes device parameters and are expressed as:

$$\begin{aligned} K_1 &= \frac{g_{mg1}}{g_{md1} + g_{md3} + g_{ms8}},\ K_2 = g_{mg1} g_{mg3} g_{ms8}, \\ K_3 &= (g_{md1} + g_{md3} + g_{ms8})^2,\ K_4 = g_{md8}. \end{aligned} \tag{B-11}$$

Similarly, the DC-gain constraint for the *extra* block of AMP_2 is expressed as:

$$\frac{K_5}{K_4 + g_{md10}} \nearrow, \tag{B-12}$$

with two constants induced by common parameters inherited from adjacent circuit blocks ($K_5 = g_{ms8}$). For the *output* block, the constraint is given by the following expression:

$$K_6 + K_7 \frac{g_{mg15}}{g_{md15} + g_{md14} + g_{mg14}} \nearrow, \tag{B-13}$$

where the common parameter constants are:

$$K_6 = \frac{g_{mg6}}{g_{md6} + g_{md7}},\ K_7 = \frac{g_{mg7} g_{mg13}}{(g_{md6} + g_{md7})(g_{md12} + g_{md13})}. \tag{B-14}$$

Regarding CMRR, we note that both circuits include only matched design parameters. Specifically, the relation between parameters of devices M_5, M_1, and M_2 control this performance. The differences impact DC-gain and CM-gain in the same way. This implies that similar CMRR performance can be expected in AMP_1 and AMP_2 when common signal path variables are precisely matched.

The gain-poles product (GPP) is used to estimate bandwidth [119] in each circuit block by selecting at most two dominant poles. Any remaining poles of the block are considered non-dominant and their constraints are expressed. For the *input* block of AMP_2, two valid sets of dominant poles can be selected: (1) P_2 and P_3 or (2) P_1 and P_4. For the first set, the different parameters are constrained as follows:

$$\frac{1}{K_4 + g_{md10}} \searrow \text{ and } K_8 + C_{gd10} + C_{db10} \searrow, \tag{B-15}$$

with GPP increase constraint expressed by expression:

$$\frac{K_9}{K_4 + g_{md10}} \nearrow . \tag{B-16}$$

For the second *input* block dominant pole set, the constraints of (B-15) are reversed and the underlying GPP becomes:

$$K_8 + C_{gd10} + C_{db10} \searrow . \tag{B-17}$$

The common parameter constants are expressed as:

$$\begin{aligned} K_8 &= C_{gd8} + C_{db8} + 2(C_{gs3} + C_{gd3} + C_{gb3}), \\ K_9 &= g_{mg3} g_{ms8}. \end{aligned} \tag{B-18}$$

For the *extra* block of AMP_2, there is a single dominant pole and the increase constraint implies that:

$$K_{10} + C_{gd10} + C_{db10} + C_{gs15} + C_{gd15} + C_{gb15} \searrow, \tag{B-19}$$

with K_{10} being:

$$K_{10} = C_{gd8} + C_{db8} + C_{gs6} + C_{gd6} + C_{gb6} + C_{m1} + C_{m2}. \tag{B-20}$$

In the case of the *output* block, the only valid dominant pole set is P_o and P_7 introducing the constraint on distinguishing parameters:

$$\begin{aligned} &\frac{1}{g_{md15} + g_{md14} + g_{mg14}} \searrow \text{ and} \\ &K_{11} + C_{gd15} + C_{db15} + C_{db14} + C_{gs14} + C_{gb14} \searrow, \end{aligned} \tag{B-21}$$

The gain-pole product increases when:

$$K_{12} \frac{g_{mg15}}{g_{md15} + g_{md14} + g_{mg14}} \nearrow . \tag{B-22}$$

The constants for this case are expressed as:

$$K_{11} = C_{gs13} + C_{gd13} + C_{gb13}, \;\; K_{12} = \frac{g_{mg7} g_{mg13}}{g_{md12} + g_{md13}}. \tag{B-23}$$

Noise is modeled for each circuit block in the two circuits using the method in [25]. Considering the common path noise fixed, constraints are extracted such that the noise contribution of the differences is diminished. The relevant constraint for the *input* block of AMP_2 is:

$$\frac{1}{K_4 + g_{md10}} \searrow \text{ and } K_8 + C_{gd10} + C_{db10} \nearrow \tag{B-24}$$

For the *extra* block, noise performance is improved when:

$$\begin{aligned} &\frac{1}{K_4 + g_{md10}} \searrow \text{ and} \\ &K_{10} + C_{gd10} + C_{db10} + C_{gs15} + C_{gd15} + C_{gb15} \nearrow \end{aligned} \tag{B-25}$$

Table B.1: Desired variable trends with respect to performance in AMP_2

Variables	**Gain**	**CM**	**Noise**	**Pole**	**GPP**
g_{md10}	$\searrow$	-	$\nearrow$	$\nearrow$, $\searrow$	$\searrow$,-
$C_{gd10} + C_{db10}$	-	-	$\nearrow$	$\searrow$,$\nearrow$	-, $\searrow$
g_{mg15}	$\nearrow$	-	$\searrow$	-	$\nearrow$
g_{md15}	$\searrow$	-	$\nearrow$	$\nearrow$	$\nearrow$
$C_{gd15} + C_{db15}$	-	-	$\nearrow$	$\searrow$	-
$C_{gs15} + C_{gd15} + C_{gb15}$	-	-	$\nearrow$	$\searrow$	-
$g_{md14} + g_{mg14}$	$\searrow$	-	$\nearrow$	$\nearrow$	$\searrow$
$C_{db14} + C_{gs14} + C_{gb14}$	-	-	$\nearrow$	$\searrow$	-

Similarly, the *output* block of AMP_2 is described by:

$$\frac{g_{mg15}}{g_{md15} + g_{md14} + g_{mg14}} \searrow \text{ and}$$
$$K_{11} + C_{gd15} + C_{db15} + C_{db14} + C_{gs14} + C_{gb14} \nearrow \tag{B-26}$$

Table B.1 summarizes the required trends for the *distinguishing* design variables of circuit AMP_2 across the entire amplifier, including *input*, *extra*, and *output* blocks. The trends were computed using constraints (B-10)-(B-26). For example, increasing *input* block DC-gain in AMP_2 by satisfying (B-10) can only be performed by deteriorating noise performance in (B-24). Parameters of device M_{10} have two variations for dominant poles and bandwidth, with respect to each selected set. Design variables g_{mg15} and g_{md15} are bound by conflicting trade-offs. However, both parameters are determined by device M_{15}, as is the case of $C_{gd15} + C_{db15}$, and the common dependence of both transconductance and capacitance on W_{15} correlates these parameters.

The procedure further investigates these parameter correlations and performance trade-offs by evaluating the UBBB model [25] of each individual circuit block. We varied the widths of devices identified by parameters in Table B.1 across a predefined range and present the normalized performance trends. Common parameters and branch bias currents through matched devices are considered constant. This allows us to estimate the performance

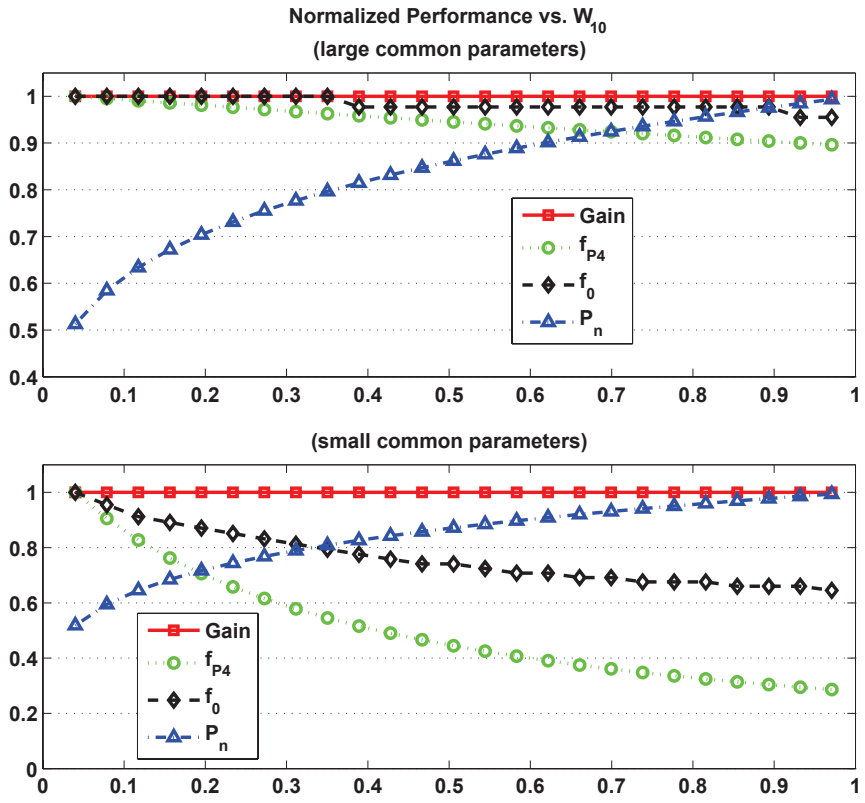

Figure B.3: Input block performance trade-offs for comparing AMP_2 and AMP_1 with respect to W_{10}

sensitivities to *distinguishing* circuit parameters and provides insight about the most appropriate relative sizing strategy that can improve performance.

For the *input* block of circuit AMP_2, design parameters related to device M_{10}, i.e. g_{md10} and $C_{gd10}+C_{db10}$, influence the resistive (R_4) and capacitive (C_4) components of the pole at node V_4. Figure B.3 shows the correlations between W_{10} and gain, pole frequency (f_{P4}), unity-gain frequency (f_0), and total block output noise (P_n). Normalized performance with respect to relative increase in width are presented for two scenarios: when the common path parameters are (i) large or (ii) small with respect to those of M_{10}. For either case, P_4 is the first dominant pole. We can observe that parameters of device M_{10} have virtually no impact on the circuit block's gain when either large or small parameter values are considered. This is due to the constant branch

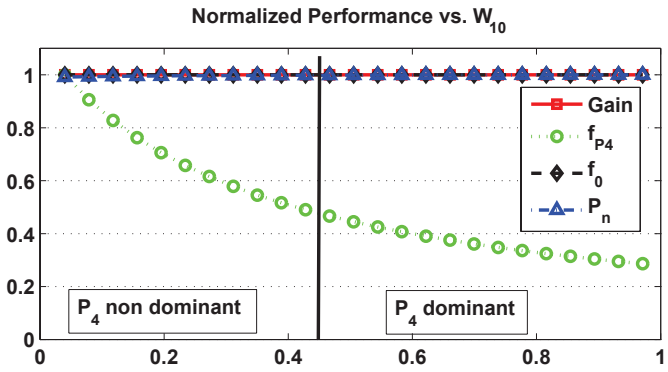

Figure B.4: Input block performance trade-offs for AMP_2 with respect to W_{10} when pole P_4 switches from a non-dominant to a dominant position

current imposed by the matched devices, which in term dictates similar gain in this circuit block for both amplifiers. Total noise exhibits the same sensitivity to M_{10} parameters regardless of the constant parameter values and is minimized for relatively small transistor widths. The variation of 50% across the investigated range suggests that when the common parameters are matched between the two designs, M_{10}'s width should be kept low. This would be required to attempt similar noise performance in both AMP_1 and AMP_2. For pole and unity-gain frequency, W_{10} is again best kept low especially in the case of small common parameters. A deterioration in first dominant pole frequency (equivalent to the -3dB point) of up to $\approx$ 70% from the maximum is noted. Unity-gain frequency is less sensitive, but it can still decrease with up to $\approx$ 35% as the size increases. The opposing trends between total noise and pole and unity-gain frequencies suggests that only g_{m10} is a dominant parameter for noise. $C_{gd10} + C_{db10}$ best controls frequency performance. Appart from the large common parameters scenario, all impacted performance follow a non-linear dependece, provinding a more pronounced variation within the first third of the width range. As W_{10} increases, the trends become closely linear and the impact on performance is reduced.

We also analyzed a situation when P_4 transitions from a non-dominant to a second dominant pole position as W_{10} increases, shown in Figure B.4. However, this scenario is only achievable when some extremely large common

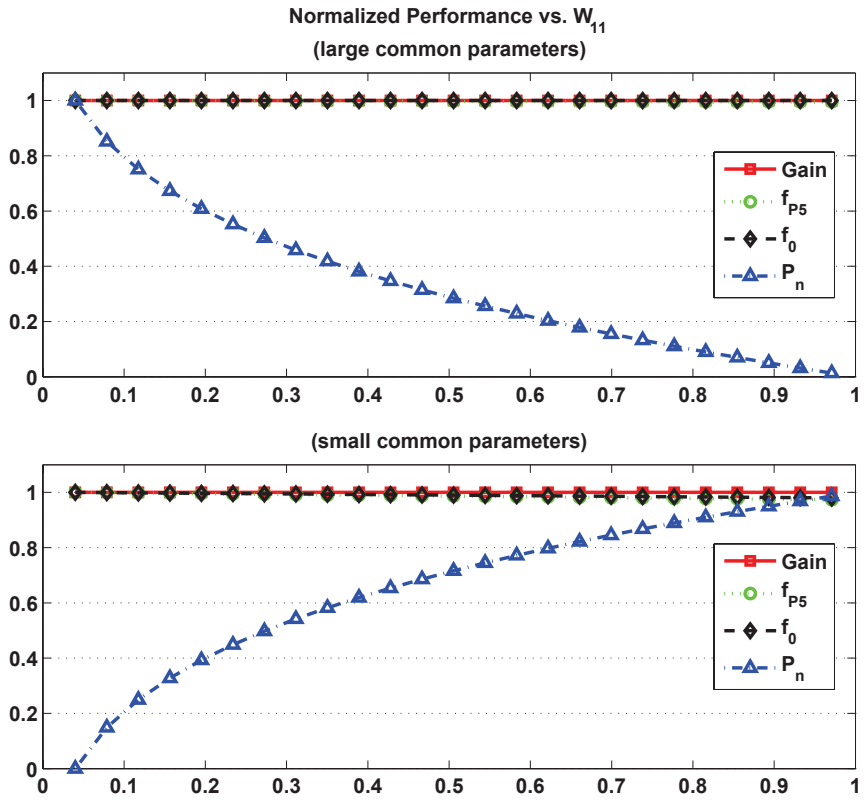

Figure B.5: Extra block performance trade-offs for comparing AMP_2 and AMP_1 with respect to $W_{11} = W_{10}$ when W_{15} is constant

parameters values are used in the block model. This effectively causes the impact of M_{10} parameters on other performance to be eliminated and suggests that this pole set would be infeasible in a physical implementation of AMP_2.

Figures B.5 and B.6 present the performance trends due to the *extra* block of AMP_2 with respect to the sizing of devices $M_{11} \equiv M_{10}$ (due to functional matching) and M_{15}, respectively. The design variables are g_{md11}, $C_{gd11} + C_{db11}$, and $C_{gs15} + C_{gd15} + C_{gb15}$, as part of the pole components at node V_5 (P_5). Figure B.5 indicates that variable W_{11} has virtually no impact on the gain, dominant pole frequency, and unity-gain frequency for either small or large common parameters values. These performances in the *extra* block of AMP_2 are dominated by the matched devices parameters. However, W_{11} does show great impact on total noise in this block. It follows a non-linear depen-

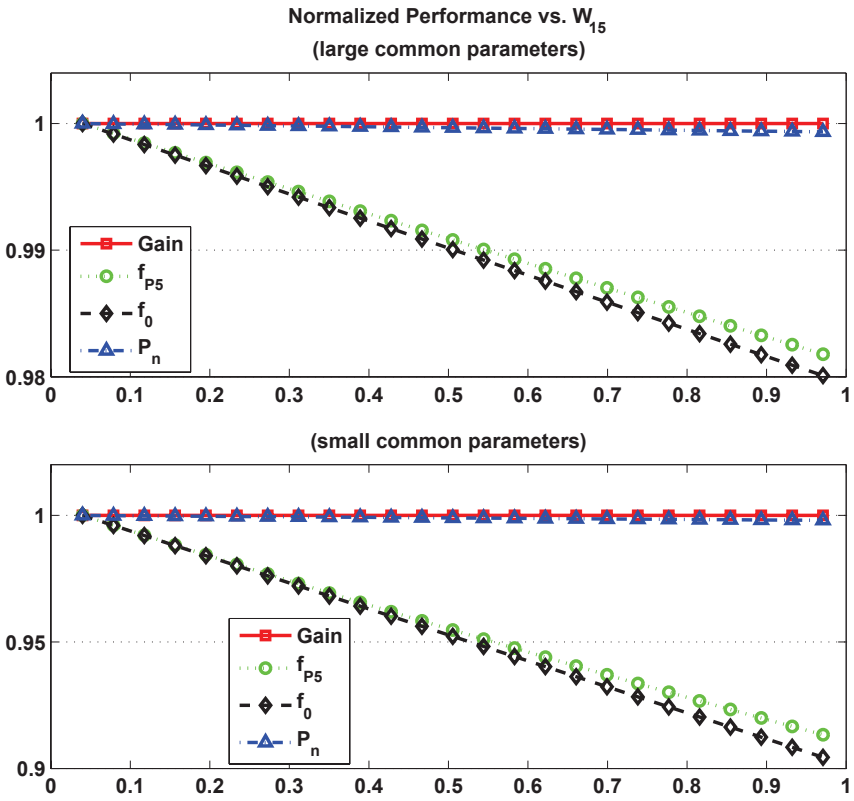

Figure B.6: Extra block performance trade-offs for comparing AMP_2 and AMP_1 with respect to W_{15} when $W_{11} = W_{10}$ is constant

dence and is minimized when W_{11} approaches the values of the common path parameters. For this minimum, the *extra* block of AMP_2 has a reduced noise contribution and the two circuits could be closer matched with respect to this performance. Analyzing the case of device M_{15} in Figure B.6 for dominant pole and unity-gain frequency, W_{15} forces a linear dependence. Furthermore, unity-gain now closely follows the dominant pole trend since P_5 is the single pole in this block of AMP_2. Both performances degrade by a relatively small amount as W_{15} increases: up to 2% and 10% from the maximum in the case of large and small common parameters, respectively. This suggests that small widths are preferred to maintain similar bandwidth between AMP_1 and AMP_2 while keeping the largest possible bandwidth for the unmatched block.

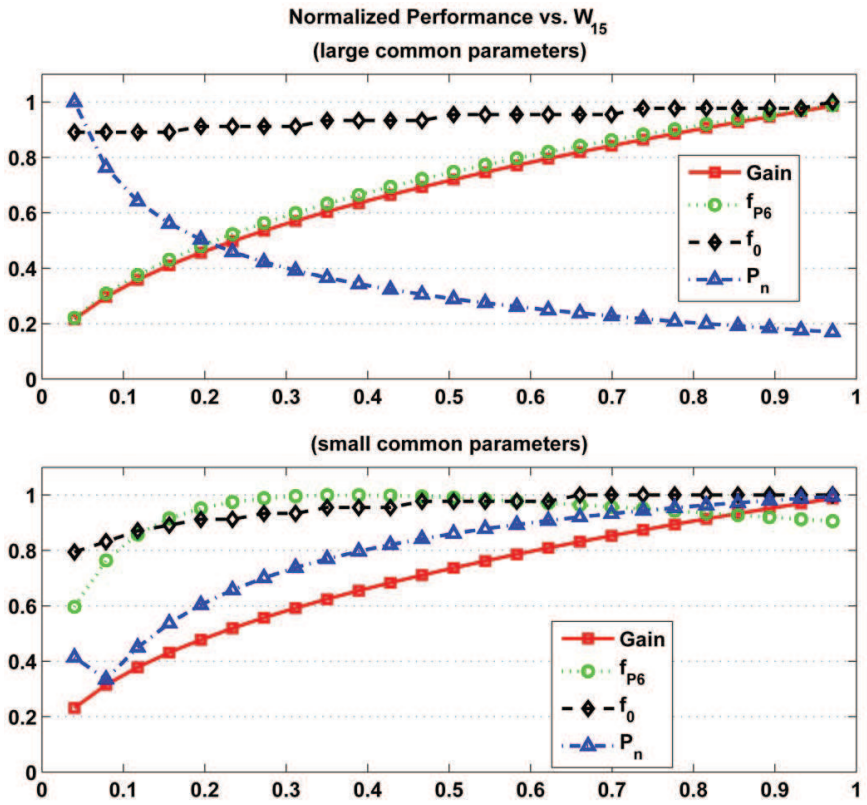

Figure B.7: Output block performance trade-offs for comparing AMP_2 and AMP_1 with respect to W_{15} when W_{14} is constant

Figure B.7 depicts the normalized performance plots for the *output* block of AMP_2, based on the width of device M_{15} when M_{14} is kept constant. The analyzed parameters are g_{md15} and $C_{gd15} + C_{db15}$ controlling the non-dominant pole at node V_6 (P_6) and g_{mg15} defining the coupling between nodes V_5 and V_6. Gain follows the same increasing trend for both small or large common parameters, showing that the impact of W_{15} on this performance is insensitive to common parameters. Furthermore, the increase in gain across the entire analyzed range, suggests that g_{mg15} is the dominant parameter and compensates for the smaller increase in g_{md15}. Also, unity-gain frequency follows similar trends in either case. While f_0 is dominated by the common path attributes, it can still be increased by up to 20% for the maximum analyzed value of W_{15}. For small common parameters, noise can be improved only for

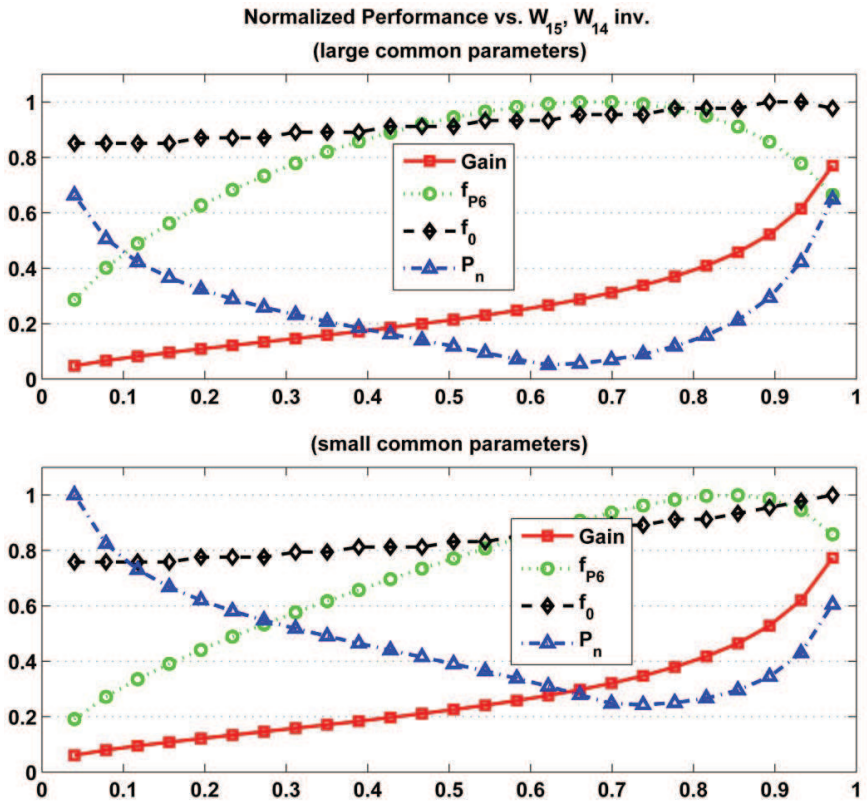

Figure B.8: Output block performance trade-offs for comparing AMP_2 and AMP_1 with respect to W_{15} and W_{14} opposing variation

the first tenth of the analyzed range. After this point the advantage is lost, while gain is still only at $\approx 70\%$ less than the maximum. Beyond this point, noise exhibits a more pronounced variation and deteriorates faster than gain increases.

An interesting situation occurs when W_{14} is also varied, but in opposition to W_{15}, illustrated in Figure B.8. The added parameters of device M_{14} are $g_{md14} + g_{mg14}$ and $C_{db14} + C_{gs14} + C_{gb14}$ influencing the pole at node V_6 (P_6). As in the previous scenario, a limited variation in unity gain is observed, which increases as W_{15} increases and W_{14} decreases. Similarly, gain also increases across the range. However, the impact is more pronounced in the last third of the interval when W_{15} is relatively larger than W_{14}. In the case of noise performance, it is now possible to minimize the impact for both large and small

common path parameters. However, this minimum is no longer achieved when the gain and f_0 are maximized. This suggests that in this scenario gain has to be sacrificed in the *output* block of AMP_2 in order to reduce the noise impact of *distinguishing* features. Overall, the analysis of the output block of AMP_2 suggests that, compared to AMP_1, this topology can exploit the distinguishing attributes to improve performance in this circuit section.

Analyzing the correlations between investigated performance, *distinguishing* circuit parameters' required variation, and transistor widths which influence these parameters can produce insight about the flexibility of a design in achieving specific requirements.

Our analysis shows that AMP_1 is dominated by features also found in AMP_2 and that this second design also includes attributes which can be used to improve its performance. Gain could be controlled in AMP_2 by 3 different transistor widths through 6 *distinguishing* small-signal parameters. For these parameters, there is one direct relation and 5 inverse relations. In terms of required variations, one opposing trend is noted for parameters related to the same width. For noise, the same 3 widths are involved, influencing a total of 23 distinct transconductance and capacitance parameters. They involve 13 direct (12 square-root dependences) and 16 inverse relations, with one conflicting variation between parameters. In the case of pole sets and bandwidth, the 3 transistor widths control 17 parameters found in 6 direct and 16 inverse relations. A total of 11 conflicting variations are found for parameters related to the same device widths. In terms of constants used in our analysis, we observe that a total of 7 common devices influence their value through 24 small-signal parameters. The mathematical dependence on these parameters include 29 direct (with 9 products and 3 squared) and 11 inverse (with 4 products) relations.

While symbolic and topological matching successfully identify the *distinguishing* features present in AMP_2 and present the desired variation trends to improve performance, the performance plots from Figures B.3-B.8 offer important insight about the limitations and the nature of the trade-offs introduced by these design variables. For example, comparing the results from

Figure B.3 with those from Figure B.7, we can infer that parameters related to device M_{10} have no benefits for improving gain when constant cascode currents are used. However, M_{15} can impact gain by up to 80% across the investigated range and its transconductance is dominant for setting this performance. For bandwidth and unity-gain frequency the situation is reversed. Especially in the case of small common parameter values, biasing transistor M_{10} sizing can influence performance by up to 70% and 35% in terms of 3dB frequency (P_4 first dominant pole) and f_0, respectively. Device M_{15} only impacts f_0 by at most 20% and does not influence 3dB frequency (P_6 non-dominant pole). This suggests that if hard requirements are set for gain, M_{15} parameters are the best choice of attempting an improvement, while in the case of f_0, M_{10} is a better candidate. Furthermore, considering the case of M_{15} with small common parameters, we observe that the possible improvement in f_0 saturates over the second half of the analyzed range. This poses a limitation, as further increasing W_{15} will not provide any benefits. Analyzing the trade-off between gain and total noise for this scenario suggests the latter deteriorates as gain increases with W_{15}. However, noise tends to saturate in the second half of the explored range, while gain continues to increase at an almost constant slope. This is important, since it shows that the trade-off between gain and noise is more demanding for relatively small widths of the device. For larger sizing values, noise tends to deteriorate slower. From a design perspective, this suggests that if the noise requirement is relaxed, gain can be more easily increased. This is valid across the investigated range, however, it can be observed that as the sizing increases, gain will eventually saturate to a maximum value.

Our comparison of AMP_1 and AMP_2 has illustrated that the first design is characterized only by common design features, also included in the second amplifier. Furthermore, the method successfully found the *distinguishing* features of AMP_2 and linked these parameters to circuit performance. In this manner, the more appropriate candidates for setting specific performance can be identified and insight about the limitations of each parameter's impact can be inferred while capturing the nature of performance trade-offs.

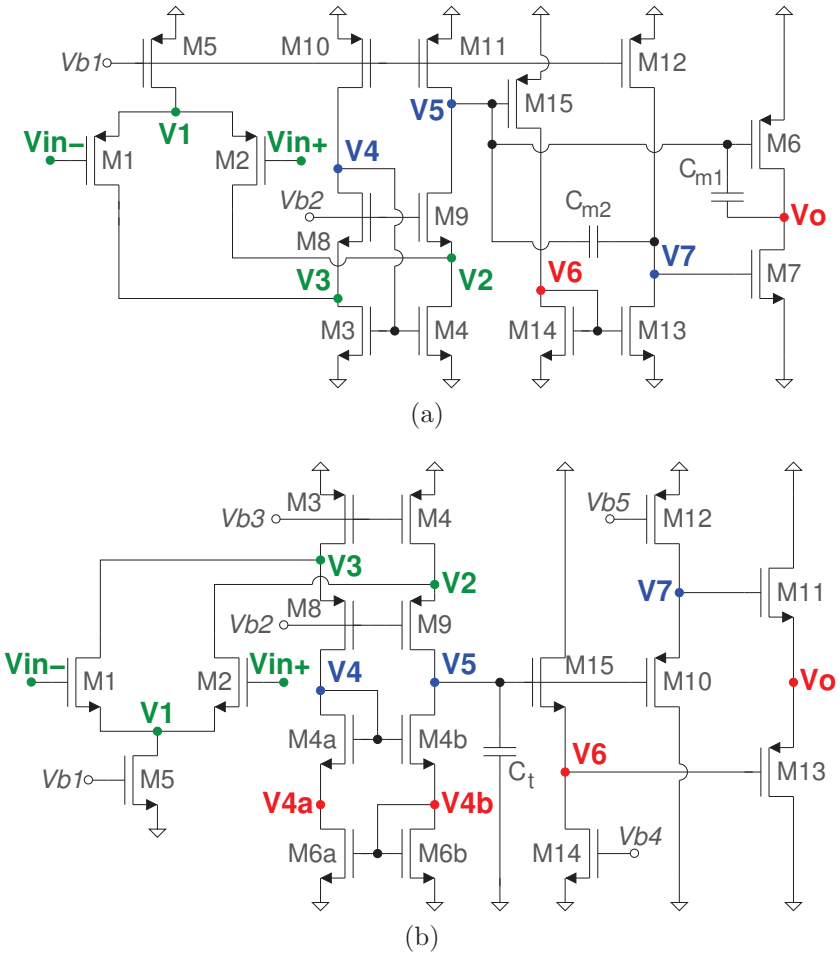

Figure B.9: Two folded cascode amplifiers: (a) AMP_2 [4]; (b) voltage amplifier AMP_3 [5]

B.2 Comparison Data for Two Folded Cascode Amplifiers

We illustrate the methodology by comparing AMP_2 [4] with the voltage amplifier from [5], coined here AMP_3. Figure B.9 shows the two folded cascode amplifier topologies.

Through nodal and circuit matching, we identify the circuit nodes having the same structure and electrical behavior in both designs. Distinct features of each implementation are highlighted at the same time. Figure B.10

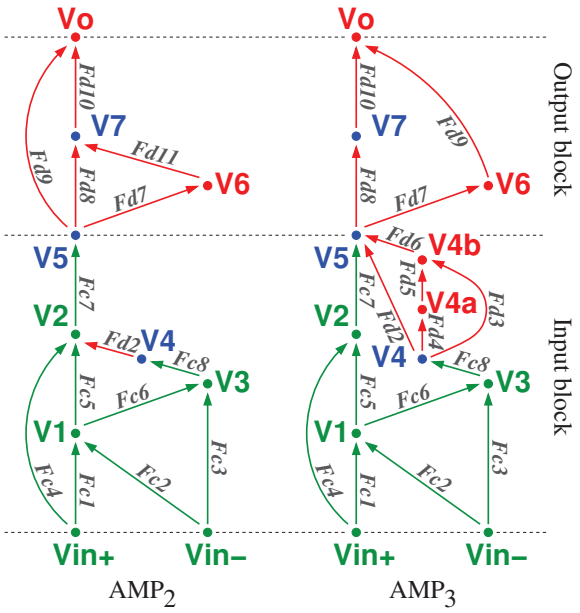

Figure B.10: Model graphs and sub-blocks for AMP_2 and AMP_3

depicts the model representations of AMP_2 and AMP_3. The differential input stage nodes V_{in+}, V_{in-} (signal inputs), V_1, , V_3, and V_2 are perfectly matched and share the same symbolic pole and coupling (Fc_i, $i = \overline{1,8}$) expressions in both amplifiers. Circuit nodes V_6 and V_o (output) differ significantly between the two designs and their associated symbolic expressions cannot be matched. In addition, the method finds that nodes V_{4a} and V_{4b} from AMP_3 have no equivalent in AMP_2.

Nodes V_4, V_5, and V_7 are only partially-matched due to the differences in their symbolic expressions. However, in this experiment, we do not impose the conditions for these nodes to exhibit similar behavior in both circuits. Overall, this allows the method to characterize the designs based on more *distinguishing* features. Furthermore, the scenario of having one amplifier described by only common parameters to both designs is avoided. This allows for comparison information to be produced based on differences in both circuits, for each individual circuit block.

Figure B.10 shows that only two matched circuit blocks with similar electrical behavior are found for these designs. The *input* block contains *dis-*

tinguishing sub-structures for poles at partially matched nodes V_4 and V_5, with an unmatched coupling F_{d2} from node V_4. The additional nodal structures of V_{4a} and V_{4b}, with the respective different graph edges Fd_j, $j = \overline{3,6}$, are specific only to AMP_3. As a result of not enforcing partial-matches, the *output* block is characterized by only *distinguishing* attributes. The same number of nodes are encountered in both amplifiers, but with different sub-structures (V_6, V_7, and V_o). Also different couplings between these output stage nodes are found in AMP_2 and AMP_3. For example, there is no coupling $V_6 \rightarrow V_7$ (F_{d11}) in AMP_3, while the output node is no longer linked to the block input node (V_5), but rather to the internal node V_6.

Using the matched and distinct structures, the method produces the set of symbolic transfer functions for each circuit block, defining the common and distinguishing symbolic terms. The transfer functions to node V_5 of the *input* block of AMP_2 and AMP_3 are given by:

$$\text{AMP}_2 : H_5 = H_{comm_1} \times H_{diff_1} + H_{comm_2} \times H_{diff_2} \tag{B-27}$$

$$\text{AMP}_3 : H_5 = H_{comm_1} \times H_{diff_3} + H_{comm_2} \times H_{diff_4}, \tag{B-28}$$

where H_{comm_1} and H_{comm_2} are common signal paths in both amplifiers and H_{diff_i} ($i = \overline{1,4}$) captures the differences of the two *input* blocks:

$$H_{diff_1} = \frac{R_5}{1 + sR_5C_5},\ H_{diff_2} = \frac{R_5R_4Fd_2Fc_7}{(1 + sR_5C_5)(1 + sR_4C_4)}, \tag{B-29}$$

$$H_{diff_3} = H_{diff_1},\ H_{diff_4} = \frac{R_5R_4}{(1 + sR_5C_5)(1 + sR_4C_4)}\,(Fd_2 + A) \tag{B-30}$$

$$\text{where } A = \frac{R_{4b}Fd_6}{1 + sR_{4b}C_{4b}}\left(Fd_3 + \frac{R_{4a}Fd_4Fd_5}{1 + sR_{4a}C_{4a}}\right).$$

Note that the matched edge Fc_7 is also considered in the expression of H_{diff_2}, due to the lack of a direct coupling from node V_4 to V_5 in AMP_2.

The common transfers are expressed as:

$$H_{comm_1} = Fc_7(P_2Fc_4 + P_2P_1Fc_5Fc_1)V_{in+} + \\ + Fc_7(P_2P_1Fc_5Fc_2)V_{in-} \quad \text{(B-31)}$$

$$H_{comm_2} = Fc_8(P_3P_1Fc_6Fc_1)V_{in+} + \\ + Fc_8(P_3Fc_3 + P_3P_1Fc_6Fc_2)V_{in-} \quad \text{(B-32)}$$

$$\text{where } P_i = \frac{R_i}{1 + sR_iC_i}.$$

For the common TFs in *input* block, the set of equivalent devices (i.e. with all matched parameters among the two design, e.g. g_{mg}, C_{gd}, etc) is composed of $M_{1,2}$, M_5, $M_{3,4}$, $M_{8,9}$. Indexes are the same across both amplifiers. The other devices cannot be fully-matched and their parameters account for the different TFs. For example, at partially matched node V_4, for the resistive pole component, $g_{md4a} + g_{mg4a}$ in AMP_3 cannot be matched to g_{md8} in AMP_2.

Transfer expressions (B-27)-(B-30) show that the *input* blocks of circuits AMP_2 and AMP_3 differ because of the poles at nodes V_5, V_4, V_{4a} and V_{4b} and the coupling between nodes $V_4 \rightarrow V_2$ in AMP_2 and $V_4 \rightarrow V_5$, $V_4 \rightarrow V_{4a} \rightarrow V_{4b} \rightarrow V_5$, and $V_4 \rightarrow V_{4b} \rightarrow V_5$ in AMP_3. The added complexity of the *distinguishing* structures produces more complex relations in the *input* block, especially for AMP_3 as shown in (B-30).

The *output* blocks of the two designs are composed of only unmatched structures (Figure B.10), resulting in *distinguishing* transfers to node V_o for the implementations. $H_o = H_{diff_{5/6}}$ is then expressed as:

$$\text{AMP}_2 : H_{diff_5} = \frac{R_o}{1 + sR_oC_o}(Fd_9 + B) \quad \text{(B-33)}$$

$$\text{where } B = \frac{R_7Fd_{10}}{1 + sR_7C_7}\left(Fd_8 + \frac{R_6Fd_7Fd_{11}}{1 + sR_6C_6}\right)$$

$$\text{AMP}_3 : H_{diff_6} = \frac{R_o}{1 + sR_oC_o}\left(\frac{R_7Fd_8Fd_{10}}{1 + sR_7C_7} + \frac{R_6Fd_7Fd_9}{1 + sR_6C_6}\right) \quad \text{(B-34)}$$

Using expressions (B-27)-(B-34), we characterize DC gain in terms of only the different design parameters between the two amplifiers while consider-

ing constant common parameters. For the *input* block of AMP_2 this produces the gain performance improvement constraint:

$$\frac{K_1}{K_2 + g_{md11}} + \frac{K_1 K_3}{(K_2 + g_{md10})(K_2 + g_{md11})} \nearrow, \tag{B-35}$$

while for AMP_3 this results in:

$$\frac{K_1}{K_2 + g_{md4b}} + \frac{K_1 g_{mg4b}}{(K_2 + g_{md4a} + g_{mg4a})(K_2 + g_{md4b})} C \nearrow, \tag{B-36}$$
$$\text{where } C = 1 - \frac{g_{ms4b}}{g_{ms4b} + g_{md6b} + g_{mg6b}}.$$

Constants K_i are generated by the matched parameters and are expressed as:

$$\begin{aligned} K_1 &= \frac{g_{mg1} g_{ms8}}{g_{md1} + g_{md3} + g_{ms8}}, \; K_2 = g_{md8}, \\ K_3 &= \frac{g_{mg3} g_{ms8}}{g_{md1} + g_{md3} + g_{ms8}}, \end{aligned} \tag{B-37}$$

where functional matching (differential stage) of common devices $M_1 \equiv M_2$, $M_3 \equiv M_4$, and $M_8 \equiv M_9$ is considered.

Constraints for the common TFs can be similarly extracted by conditioning the different TFs. For example, we can impose that the parameters of $H^{(2)}_{1,diff}$ match those of $H^{(2)}_{2,diff}$ and kept constant to extract the DC gain improvement constraints for the common parts:

$$H_{comm_1} \equiv H_{comm_2} : \frac{g_{mg1} g_{ms8}}{g_{md1} + g_{md3} + g_{ms8}} (K^{(1)}_{diff} + K^{(2)}_{diff}) \nearrow \tag{B-38}$$

when functional matching of devices is considered and $V_{in+} = -V_{in-}$. $K^{(i)}_{diff}$ represent the constant values of the corresponding different TFs.

Similarly to the case of differences, the DC gain improvement constraint in equation (B-38) shows that parameters of the same device require different trends. For example, for M_1, g_{mg1} has to increase while g_{md1} needs to decrease. The same occurs for g_{ms8}. However, its influence on DC gain is reduced when it can be ensured that $g_{ms8} >> g_{md1} + g_{md3}$. Therefore, for the DC gain constraint on common TFs, only device M_3 has non-conflicting parameter

required trends.

Setting the two poles of the common TFs (P_1, P_2/P_3) to be dominant with respect to those of different TFs in the *input* block of the amplifiers generates the constraints:

$$\frac{1}{2g_{ms1}+g_{md5}} \nearrow \text{ and } 2(C_{gs1}+C_{sb1})+C_{gd5}+C_{db5} \nearrow; \tag{B-39}$$

$$\frac{1}{g_{md1}+g_{md3}+g_{ms8}} \nearrow \text{ and}$$
$$C_{gd1}+C_{db1}+C_{gd3}+C_{db3}+C_{gs8}+C_{sb8} \nearrow; \tag{B-40}$$

These two constraints are in agreement with the common path DC gain constraint in equation (B-38). However, a trade-off appears with the constraints imposed for improving noise performance of common TFs, namely with:

$$\frac{g_{ms1}}{(2g_{ms1}+g_{md5})(g_{md1}+g_{md3}+g_{ms8})} \searrow \ . \tag{B-41}$$

In this situation, all g_m variables become trade-off variables with respect to the dominant pole and gain constraints. The trade-off between gain and noise with respect to g_{ms8} can be eliminated by allowing the variable to be sufficiently large, as previously discussed for removing gain sensitivity ($g_{ms8} >> g_{md1} + g_{md3}$). However, a trade-off with the dominant position of pole P_2 (P_3) in constraint (B-40) still exists.

For the *output* block of AMP_2, the gain constraint on different parameters is given by the following expression:

$$\frac{1}{g_{md6}+g_{md7}}\left(g_{mg6}+\frac{g_{mg7}g_{mg13}}{K_4+g_{md13}}D\right) \nearrow, \tag{B-42}$$
$$\text{where } D=\frac{g_{mg15}}{g_{md14}+g_{mg14}+g_{md15}}.$$

In the case of AMP_3, the *output* block source follower configuration's *unity* gain can be improved by:

$$\frac{1}{g_{ms11}+g_{ms13}}\left(\frac{g_{mg10}g_{mg11}}{K_4+g_{ms10}}+\frac{g_{mg13}g_{mg15}}{g_{md14}+g_{ms15}}\right)\nearrow, \tag{B-43}$$

where for both designs a common current source defines $K_4 = g_{md12}$.

For improving CMRR, the underlying constraint requires parameters related only to matched devices.

$$\frac{g_{md5}}{g_{md5}+g_{ms1}+g_{ms2}} << 1, \ \searrow . \tag{B-44}$$

Differences impact differential and common-mode gain in the same manner, resulting in no control over CMRR through the identified distinct features.

For characterizing the gain-poles product (GPP) and bandwidth, we select two dominant poles in each circuit block and generate the corresponding constraints.

For the *input* block of AMP_2, there are two feasible pole sets: (1) P_5, P_1 or (2) P_5, P_4. We consider the pole at node V_5 to be always dominant since it contains discrete capacitances and we assume them to have the major contribution over small-signal parameters. For P_2 and P_3, their symmetry forces them to be always considered non-dominant. The constraints on P_5 and P_4 for the first set are expressed as:

$$\frac{1}{K_2+g_{md11}}\nearrow \text{ and}$$

$$K_5+C_{gd11}+C_{db11}+C_{gs6}+C_{gd6}+C_{gb6}+$$

$$+C_{gs15}+C_{gd15}+C_{gb15}\nearrow; \tag{B-45}$$

$$\frac{1}{K_2+g_{md10}}\searrow \text{ and } K_6+C_{gd10}+C_{db10}\searrow . \tag{B-46}$$

Pole P_1 is not constrained since it is only formed of common parameters. For the second set of poles, constrain (B-46) on P_4 is reversed. The resulting

gain-pole-product (GPP) constraints are:

$$K_5 + C_{gd11} + C_{db11} + C_{gs6} + C_{gd6} + C_{gb6} + \\ + C_{gs15} + C_{gd15} + C_{gb15} \searrow \text{ and } \frac{1}{K_2 + g_{md10}} \nearrow \text{ for set 1;} \tag{B-47}$$

$$K_5 + C_{gd11} + C_{db11} + C_{gs6} + C_{gd6} + C_{gb6} + \\ + C_{gs15} + C_{gd15} + C_{gb15} \searrow \text{ and} \\ K_6 + C_{gd10} + C_{db10} \searrow \text{for set 2.} \tag{B-48}$$

The constant parameters impose constants K_5 and K_6, expressed as:

$$K_5 = C_{gd9} + C_{db9} + C_{m1} + C_{m2} \\ K_6 = C_{gd8} + C_{db8} + C_{gs3} + C_{gd3} + C_{gb3} + C_{gs4} + C_{gd4} + C_{gb4}. \tag{B-49}$$

Similarly, for the *input* block of AMP_3, we extract constraints for 4 different dominant pole sets: (1) P_5, P_1, (2) P_5, P_4, (3) P_5, P_{4a}, or (4) P_5, P_{4b}. In the case of the first set, they are expressed as:

$$\frac{1}{K_2 + g_{md4b}} \nearrow \text{ and} \\ K_7 + C_{gd4b} + C_{db4b} + C_{gs10} + C_{gd10} + C_{gb10} + \\ + C_{gs15} + C_{gd15} + C_{gb15} \nearrow; \tag{B-50}$$

$$\frac{1}{K_2 + g_{md4a} + g_{mg4a}} \searrow \text{ and} \\ K_8 + C_{db4a} + C_{gs4a} + C_{gb4a} + C_{gs4b} + C_{gd4b} + C_{gb4b} \searrow; \tag{B-51}$$

$$\frac{1}{g_{ms4a} + g_{md6a}} \searrow \text{ and } C_{gs4a} + C_{sb4a} + C_{gd6a} + C_{db6a} \searrow; \tag{B-52}$$

$$\frac{1}{g_{ms4b} + g_{md6b} + g_{mg6b}} \searrow \text{ and} \\ C_{gs4b} + C_{sb4b} + C_{db6b} + C_{gs6b} + C_{gb6b} + \\ + C_{gs6a} + C_{gd6a} + C_{gb6a} \searrow . \tag{B-53}$$

For the other 3 dominant pole sets, constraint (B-50) for P_5 remains un-

changed. Constraints (B-51) for P_4, (B-52) for P_{4a}, and (B-53) for P_{4b} are reversed for each set in which the respective pole is considered dominant. Combined with gain, we obtain the GPP constraints:

$$K_7 + C_{gd4b} + C_{db4b} + C_{gs10} + C_{gd10} + C_{gb10} + \\ + C_{gs15} + C_{gd15} + C_{gb15} \searrow \text{ and} \\ \frac{K_9 g_{mg4b}}{K_2 + g_{md4a} + g_{mg4a}} \left(1 - \frac{g_{ms4b}}{g_{ms4b} + g_{md6a} + g_{mg6a}}\right) \nearrow \tag{B-54}$$

for set 1;

$$K_7 + C_{gd4b} + C_{db4b} + C_{gs10} + C_{gd10} + C_{gb10} + \\ + C_{gs15} + C_{gd15} + C_{gb15} \searrow \text{ and} \\ K_8 + C_{db4a} + C_{gs4a} + C_{gb4a} + C_{gs4b} + C_{gd4b} + C_{gb4b} \searrow \text{ and} \\ K_9 g_{mg4b} \left(1 - \frac{g_{ms4b}}{g_{ms4b} + g_{md6b} + g_{mg6b}}\right) \nearrow \text{ for set 2;} \tag{B-55}$$

$$K_7 + C_{gd4b} + C_{db4b} + C_{gs10} + C_{gd10} + C_{gb10} + \\ + C_{gs15} + C_{gd15} + C_{gb15} \searrow \text{ and} \\ C_{gs4a} + C_{sb4a} + C_{gd6a} + C_{db6a} \searrow \text{ and } \frac{1}{g_{ms4a} + g_{md6a}} \searrow \text{ and} \\ \frac{K_9 g_{mg4b}}{K_2 + g_{md4a} + g_{mg4a}} \left(1 - \frac{g_{ms4b}}{g_{ms4b} + g_{md6b} + g_{mg6b}}\right) \nearrow \tag{B-56}$$

for set 3;

$$K_7 + C_{gd4b} + C_{db4b} + C_{gs10} + C_{gd10} + C_{gb10} + \\ + C_{gs15} + C_{gd15} + C_{gb15} \searrow \text{ and} \\ C_{gs4b} + C_{sb4b} + C_{db6b} + C_{gs6b} + C_{gb6b} + \\ + C_{gs6a} + C_{gd6a} + C_{gb6a} \searrow \text{ and } \frac{1}{g_{ms4b} + g_{md6b} + g_{mg6b}} \searrow \\ \text{and } \frac{K_9 g_{mg4b}}{K_2 + g_{md4a} + g_{mg4a}} \left(1 - \frac{g_{ms4b}}{g_{ms4b} + g_{md6b} + g_{mg6b}}\right) \nearrow \tag{B-57}$$

for set 4;

Considering discrete capacitances as matched devices ($C_t \equiv C_{m1}, C_{m2}$), the constants are defined as:

$$K_7 = C_{gd9} + C_{db9} + C_t,\ K_8 = C_{gd8} + C_{db8},\ K_9 = g_{ms8}. \tag{B-58}$$

In this experiment, the *output* block of AMP_2 is characterized by the same dominant pole set as in the previous case, P_o and P_7 (with P_6 non-dominant). However, due to the differences in matching with the other folded cascode amplifier, the constraints are now expressed as:

$$\frac{1}{g_{md6} + g_{md7}} \nearrow \text{ and } K_{10} + C_{gd6} + C_{db6} + C_{gd7} + C_{db7} \nearrow, \tag{B-59}$$

$$\frac{1}{K_4 + g_{md13}} \nearrow \text{ and}$$
$$K_{11} + C_{gd13} + C_{db13} + C_{gs7} + C_{gd7} + C_{gb7} \nearrow, \tag{B-60}$$

$$\frac{1}{g_{md14} + g_{mg14} + g_{md15}} \searrow \text{ and}$$
$$C_{gd15} + C_{db15} + C_{gs13} + C_{gd13} + C_{gb13} +$$
$$+ C_{db14} + C_{gs14} + C_{gb14} \searrow, \tag{B-61}$$

based on the *distinguishing* parameters in the configuration of P_o, P_7, and P_6, respectively. The circuit block GPP improvement constraints requires:

$$K_{10} + C_{gd6} + C_{db6} + C_{gd7} + C_{db7} \searrow \text{ and}$$
$$K_{11} + C_{gd13} + C_{db13} + C_{gs7} + C_{gd7} + C_{gb7} \searrow \text{ and}$$
$$g_{mg6} + \frac{g_{mg7} g_{mg13} g_{mg15}}{g_{md14} + g_{mg14} + g_{md15}} \nearrow \text{ and } \frac{1}{K_4 + g_{md13}} \searrow . \tag{B-62}$$

The common parameters provide constants:

$$K_{10} = C_{m1} \text{ and } K_{11} = C_{gd12} + C_{db12} + C_{m2}. \tag{B-63}$$

The *output* block of AMP_3 is described by 3 feasible dominant pole sets: (1) P_6, P_7, (2) P_o, P_6, or (3) P_o, P_7. For the first set, the constraints on

distinguishing variables are expressed by:

$$\frac{1}{g_{ms15}+g_{md14}} \nearrow \text{ and}$$
$$C_{gs15}+C_{sb15}+C_{gd14}+C_{db14}+C_{gs13}+C_{gd13}+C_{gb13} \nearrow; \tag{B-64}$$
$$\frac{1}{K_4+g_{ms10}} \nearrow \text{ and}$$
$$K_{12}+C_{gs10}+C_{sb10}+C_{gs11}+C_{gd11}+C_{gb11} \nearrow; \tag{B-65}$$
$$\frac{1}{g_{ms11}+g_{ms13}} \searrow \text{ and } C_{gs11}+C_{sb11}+C_{gs13}+C_{sb13} \searrow; \tag{B-66}$$

for poles P_6, P_7, and P_o, respectively. For the remaining 2 pole sets, constraints (B-64)-(B-66) are reversed based on considered dominant and non-dominant poles. The GPP is then characterized by the requirements:

$$C_{gs15}+C_{sb15}+C_{gd14}+C_{db14}+C_{gs13}+C_{gd13}+C_{gb13} \searrow \text{ and}$$
$$K_{12}+C_{gs10}+C_{sb10}+C_{gs11}+C_{gd11}+C_{gb11} \searrow \text{ and}$$
$$\frac{1}{g_{ms15}+g_{md14}} \searrow \text{ and } \frac{1}{K_4+g_{ms10}} \searrow \text{ and}$$
$$\frac{1}{g_{ms11}+g_{ms13}}\left(g_{mg10}g_{mg11}+g_{mg13}g_{mg15}\right) \nearrow \text{ for set 1;} \tag{B-67}$$
$$C_{gs15}+C_{sb15}+C_{gd14}+C_{db14}+C_{gs13}+C_{gd13}+C_{gb13} \searrow \text{ and}$$
$$C_{gs11}+C_{sb11}+C_{gs13}+C_{sb13} \searrow \text{ and}$$
$$\frac{1}{g_{ms15}+g_{md14}} \searrow \text{ and } \frac{g_{mg10}g_{mg11}}{K_4+g_{ms10}}+g_{mg13}g_{mg15} \nearrow \text{ for set 2;} \tag{B-68}$$
$$K_{12}+C_{gs10}+C_{sb10}+C_{gs11}+C_{gd11}+C_{gb11} \searrow \text{ and}$$
$$C_{gs11}+C_{sb11}+C_{gs13}+C_{sb13} \searrow \text{ and}$$
$$\frac{1}{K_4+g_{ms10}} \searrow \text{ and } g_{mg10}g_{mg11}+\frac{g_{mg13}g_{mg15}}{g_{ms15}+g_{md14}} \nearrow \text{ for set 3.} \tag{B-69}$$

The matched current source in this circuit block introduces the constant $K_{12} = C_{gd12}+C_{db12}$.

Using UBBB based noise modeling [25], we derive the constraints on *distinguishing* parameters in each design. This illustrates the noise contribution of different features, while also providing the mechanism to reduce total

output noise. For the *input* block of AMP_2, the resulting noise constraints can be expressed as:

$$\begin{aligned}
&\frac{1}{K_2 + g_{md11}} \searrow \text{ and } \frac{1}{K_2 + g_{md10}} \searrow \text{ and} \\
&K_5 + C_{gd11} + C_{db11} + C_{gs6} + C_{gd6} + C_{gb6} + \\
&\quad + C_{gs15} + C_{gd15} + C_{gb15} \nearrow \text{ and} \\
&K_6 + C_{gd10} + C_{db10} \nearrow
\end{aligned} \tag{B-70}$$

Constraint (B-70) captures the requirements such that the noise contribution of the different (unmatched) node structures is reduced while also minimizing the impact on the transfer of this noise to the circuit section output (where total noise is evaluated in the model).

Similarly for the input block of AMP_3, the *distinguishing* parameters are constrained by noise performance as:

$$\begin{aligned}
&\frac{g_{mg4b}}{K_2 + g_{md4b}} \searrow \text{ and } \frac{g_{mg4b} g_{ms4b}}{g_{ms4b} + g_{md6b} + g_{mg6b}} \searrow \text{ and} \\
&\frac{g_{mg4a} + g_{md4a}}{g_{ms4a} + g_{md6a}} \searrow \text{ and } \frac{1}{K_2 + g_{md4a} + g_{mg4a}} \searrow \text{and} \\
&K_7 + C_{gd4b} + C_{db4b} + C_{gs10} + C_{gd10} + C_{gb10} + \\
&\quad + C_{gs15} + C_{gd15} + C_{gb15} \nearrow \text{ and} \\
&K_8 + C_{db4a} + C_{gs4a} + C_{gb4a} + C_{gs4b} + C_{gd4b} + C_{gb4b} \nearrow \text{ and} \\
&C_{gs4a} + C_{sb4a} + C_{gd6a} + C_{db6a} \nearrow \text{and} \\
&C_{gs4b} + C_{sb4b} + C_{db6b} + C_{gs6b} + C_{gb6b} + \\
&\quad + C_{gs6a} + C_{gd6a} + C_{gb6a} \nearrow
\end{aligned} \tag{B-71}$$

The added complexity of the *input* block in AMP_3 imposes a significant increase in the number of constraints and involved design parameters.

Table B.2: Desired variable trends with respect to performance in AMP_2 input block

Variables	**Gain**	**CMRR**	**Noise**	**Pole Set**		**GPP**	
				1	**2**	**1**	**2**
g_{md10}	$\searrow$	-	$\nearrow$	$\nearrow$	$\searrow$	$\searrow$	-
$C_{gd10} + C_{db10}$	-	-	$\nearrow$	$\searrow$	$\nearrow$	-	$\searrow$
g_{md11}	$\searrow$	-	$\nearrow$	$\searrow$	$\searrow$	-	-
$C_{gd11} + C_{db11}$	-	-	$\nearrow$	$\nearrow$	$\nearrow$	$\searrow$	$\searrow$
$C_{gs6} + C_{gd6} + C_{gb6}$	-	-	$\nearrow$	$\nearrow$	$\nearrow$	$\searrow$	$\searrow$
$C_{gs15} + C_{gd15} + C_{gb15}$	-	-	$\nearrow$	$\nearrow$	$\nearrow$	$\searrow$	$\searrow$

Noise performance of the *output* block in AMP_2 can be improved when:

$$\frac{g_{mg13}g_{mg15}}{g_{md15} + g_{md14} + g_{mg14}} \searrow \text{ and } \frac{g_{mg7}}{K_4 + g_{md13}} \searrow \text{ and}$$
$$\frac{g_{mg6}}{g_{md6} + g_{md7}} \searrow \text{ and } K_{10} + C_{gd6} + C_{db6} + C_{gd7} + C_{db7} \nearrow \text{ and}$$
$$K_{11} + C_{gd13} + C_{db13} + C_{gs7} + C_{gd7} + C_{gb7} \nearrow \text{ and}$$
$$C_{gd15} + C_{db15} + C_{gs13} + C_{gd13} + C_{gb13} +$$
$$+ C_{db14} + C_{gs14} + C_{gb14} \nearrow \tag{B-72}$$

while for the *output* block of AMP_3, the noise impact of *distinguishing* parameters is reduced if:

$$\frac{g_{mg10}g_{mg11}}{K_4 + g_{ms10}} \searrow \text{ and } \frac{g_{mg13}g_{mg15}}{g_{md14} + g_{ms15}} \searrow \text{ and}$$
$$\frac{1}{g_{ms11} + g_{ms13}} \searrow \text{ and } C_{gs11} + C_{sb11} + C_{gs13} + C_{sb13} \nearrow \text{ and}$$
$$C_{gs15} + C_{sb15} + C_{gd14} + C_{db14} + C_{gs13} + C_{gd13} + C_{gb13} \nearrow \text{ and}$$
$$K_{12} + C_{gs10} + C_{sb10} + C_{gs11} + C_{gd11} + C_{gb11} \nearrow \tag{B-73}$$

The comparable complexity of both designs in the *output* block produces a similar number of constraints and involved small-signal parameters.

Tables B.2 and B.3 summarize the required variable trends for the *input*

Table B.3: Desired variable trends with respect to performance in AMP_3 input block

Variables	**Gain**	**CMRR**	**Noise**	**Pole Set**				**GPP**			
				1	**2**	**3**	**4**	**1**	**2**	**3**	**4**
g_{ms4a}	-	-	↗	↗	↗	↘	↗	-	-	↗	-
$g_{md4a} + g_{mg4a}$	↘	-	↗	↗	↘	↗	↗	↘	-	↘	↘
$C_{gs4a} + C_{sb4a}$	-	-	↗	↘	↘	↗	↘	-	-	↘	-
$C_{db4a} + C_{gs4a} + C_{gb4a}$	-	-	↗	↘	↗	↘	↘	-	↘	-	-
g_{ms4b}	↘	-	↗	↗	↗	↗	↘	↘	↘	↘	↘
g_{md4b}	↘	-	↗	↘	↘	↘	↘	-	-	-	-
g_{mg4b}	↗	-	↘	-	-	-	-	↗	↗	↗	↗
$C_{gs4b} + C_{sb4b}$	-	-	↗	↘	↘	↘	↗	-	-	-	↘
$C_{gd4b} + C_{db4b}$	-	-	↗	↗	↗	↗	↗	↘	↘	↘	↘
$C_{gs4b} + C_{gd4b} + C_{gb4b}$	-	-	↗	↘	↗	↘	↘	-	↘	-	-
g_{md6a}	-	-	↗	↗	↗	↘	↗	-	-	↗	-
$C_{gd6a} + C_{db6a}$	-	-	↗	↘	↘	↗	↘	-	-	↘	-
$C_{gs6a} + C_{gd6a} + C_{gb6a}$	-	-	↗	↘	↘	↘	↗	-	-	-	↘
$g_{md6b} + g_{mg6b}$	↗	-	↗	↗	↗	↗	↘	↗	↗	↗	↗
$C_{db6b} + C_{gs6b} + C_{gb6b}$	-	-	↗	↘	↘	↘	↗	-	-	-	↘
$C_{gs10} + C_{gd10} + C_{gb10}$	-	-	↗	↗	↗	↗	↗	↘	↘	↘	↘
$C_{gs15} + C_{gd15} + C_{gb15}$	-	-	↗	↗	↗	↗	↗	↘	↘	↘	↘

block of AMP_2 and AMP_3, respectively. The *output* block variables are given in Table B.4 for AMP_2 and Table B.5 for AMP_3. The results are extracted from constraints (B-35)-(B-73). We observe that for the input block of AMP_2, all *distinguishing* design parameters are trade-off variables across the investigated performance. For example, improving DC-gain from (B-35) and total stage output noise from (B-70) through g_{md11} requires opposing variations of the parameter. In AMP_3, we note that the *input* does present free variables. For example, design parameters $g_{md6b} + g_{mg6b}$ require the same variation, without conflict, for all performances in the case of 3 out of the 4 dominant pole sets considered. However, the sensitivity needs to be evaluated in order to quantify the advantages of these variables on the circuit's performance. Furthermore, design variables $C_{db6b} + C_{gs6b} + C_{gb6b}$ are linked to the same device M_{6b} and have opposing variation in all these case. The correlations between the transconductance and capacitance of the same transistors render the parame-

Table B.4: Desired variable trends with respect to performance in AMP_2 output block

Variables	**Gain**	**CMRR**	**Noise**	**Pole Set**	**GPP**
g_{md13}	↘	-	↗	↘	↗
g_{mg13}	↗	-	↘	-	↗
$C_{gd13} + C_{db13}$	-	-	↗	↗	↘
$C_{gs13} + C_{gd13} + C_{gb13}$	-	-	↗	↘	-
$g_{md14} + g_{mg14}$	↘	-	↗	↗	↘
$C_{db14} + C_{gs14} + C_{gb14}$	-	-	↗	↘	-
g_{md15}	↘	-	↗	↗	↘
g_{mg15}	↗	-	↘	-	↗
$C_{gd15} + C_{db15}$	-	-	↗	↘	-
g_{md6}	↘	-	↗	↘	-
g_{mg6}	↗	-	↘	-	↗
$C_{gd6} + C_{db6}$	-	-	↗	↗	↘
g_{md7}	↘	-	↗	↘	-
g_{mg7}	↗	-	↘	-	↗
$C_{gd7} + C_{db7}$	-	-	↗	↗	↘
$C_{gs7} + C_{gd7} + C_{gb7}$	-	-	↗	↗	↘

ters as trade-off variables. The *output* block of both amplifiers exhibits only trade-off variables. All *distinguishing* parameters, in either pole set configuration, have at least one conflicting variation. For example, in AMP_2, improving noise performance from (B-72) and setting dominant pole position in (B-59) by increasing $C_{gd6} + C_{db6}$ will degrade bandwidth and GPP thorough (B-62).

In order to gain additional insight about the *distinguishing* parameter trade-offs, the method proceeds to evaluate the UBBB models of each circuit block. The widths of the distinct devices identified by parameters from Tables B.2-B.5 are varied over a predefined range. This allows the estimation of performance sensitivities to a single or to groups of devices' sizing. Note that our method is focused on presenting the relative performance changes over the investigated range, and not absolute performance values. In this manner, we

Table B.5: Desired variable trends with respect to performance in AMP_3 output block

Variables	**Gain**	**CMRR**	**Noise**	**Pole Set**			**GPP**		
				1	**2**	**3**	**1**	**2**	**3**
g_{ms10}	↘	-	↗	↘	↗	↘	↗	↘	↗
g_{mg10}	↗	-	↘	-	-	-	↗	↗	↗
$C_{gs10} + C_{sb10}$	-	-	↗	↗	↘	↗	↘	-	↘
g_{md14}	↘	-	↗	↘	↘	↗	↗	↗	↘
$C_{gd14} + C_{db14}$	-	-	↗	↗	↗	↘	↘	↘	-
g_{ms15}	↘	-	↗	↘	↘	↗	↗	↗	↘
g_{mg15}	↗	-	↘	-	-	-	↗	↗	↗
$C_{gs15} + C_{sb15}$	-	-	↗	↗	↗	↘	↘	↘	-
g_{ms11}	↘	-	↗	↗	↘	↘	↘	-	-
g_{mg11}	↗	-	↘	-	-	-	↗	↗	↗
$C_{gs11} + C_{sb11}$	-	-	↗	↘	↗	↗	-	↘	↘
$C_{gs11} + C_{gd11} + C_{gb11}$	-	-	↗	↗	↘	↗	↘	-	↘
g_{ms13}	↘	-	↗	↗	↘	↘	↘	-	-
g_{mg13}	↗	-	↘	-	-	-	↗	↗	↗
$C_{gs13} + C_{sb13}$	-	-	↗	↘	↗	↗	-	↘	↘
$C_{gs13} + C_{gd13} + C_{gb13}$	-	-	↗	↗	↗	↘	↘	↘	-

can systematically compare the two designs in terms of the relative impact parameter changes have on circuit performance. This is useful for identifying suitable relative sizing strategies which offer the optimal trade-offs when only a nominal design is known. The analysis considers the same matched parameter values in both designs for two cases: common parameters are relatively (i) large or (ii) small compared to *distinguishing* varied parameters. To ensure that the common path is not altered by varying device sizes, bias currents for circuit branches containing matched devices are kept constant. For systematic comparison, the output branch of each circuit is also considered at fixed biasing.

In Figure B.11, we present the normalized performance trends for the *input* block of AMP_2 when $W_{10} = W_{11}$ varies and W_6, W_{15} are kept constant. The sizing of devices M_{10} and M_{11} are held equal to maintain differential sym-

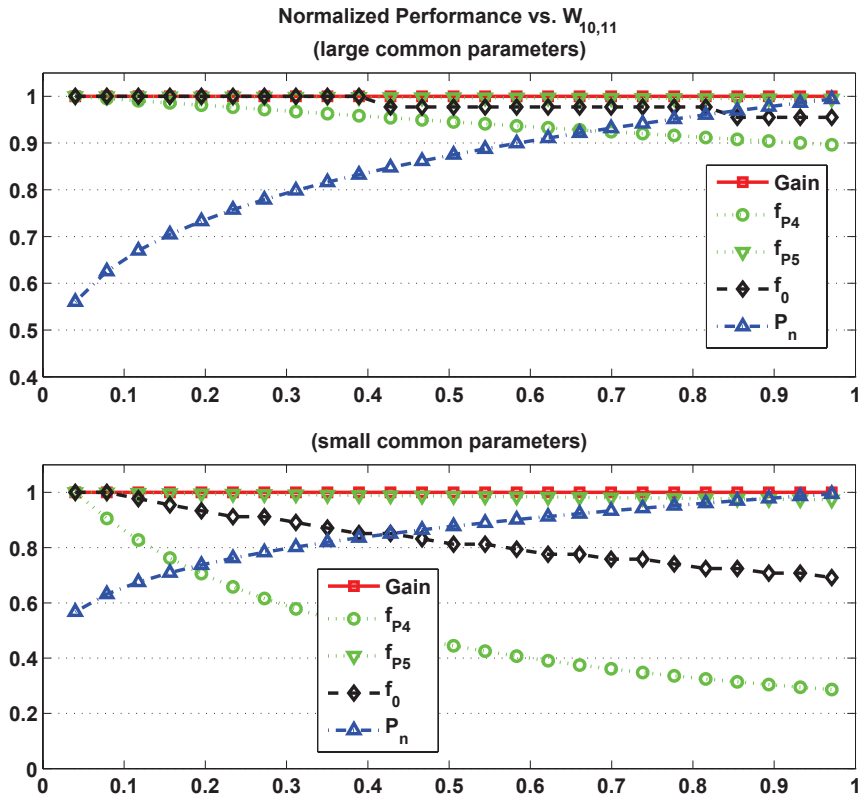

Figure B.11: Input block performance trade-offs for AMP_2 with respect to $W_{10} = W_{11}$ when W_6 and W_{15} are constant

metry (functional matching). The dominant pole set is formed of P_5 and P_4. We observe that gain remains unchanged across the investigates width range for both large and small common parameter values. Due to the matched cascode devices, the branch currents are constant, resulting in fixed g_{md} parameters for the *distinguishing* devices and no relative change in block gain. The total output noise increases with $W_{10} = W_{11}$ in the same non-linear form for either common parameter case. A variation of $\approx 45\%$ from the maximum is noted. In terms of pole frequencies and unity-gain frequency (f_0), the large common parameter case is less sensitive to variations of $W_{10} = W_{11}$. The frequency of the first dominant pole P_5 remains relatively unchanged in either scenario, due to the relatively large discrete capacitance dominating any increase of $C_{gd11} + C_{db11}$. For small common parameter value, the frequency of

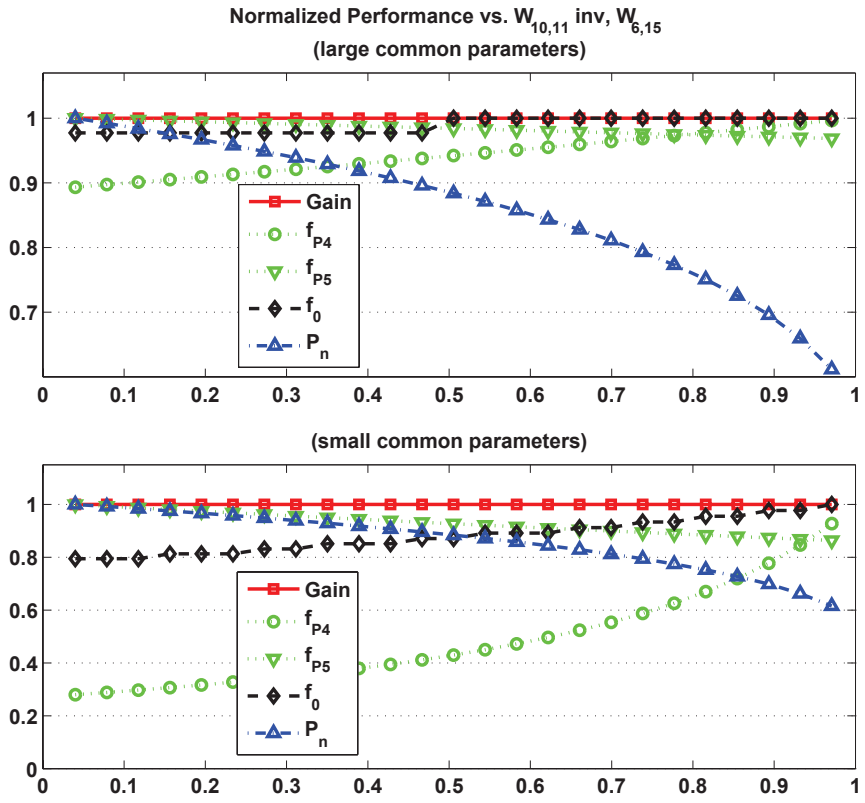

Figure B.12: Input block performance trade-offs for AMP_2 when $W_{10} = W_{11}$ and W_6, W_{15} vary in opposing direction

P_4 and f_0 can reduce by as much as $\approx 70\%$ and $\approx 30\%$, respectively, with f_{P4} exhibiting the major drop in the first half of the investigated range. Overall, the large common parameter scenario is favorable since it better maintains pole separation (important for bandwidth, phase margin, and stability), while offering the same relative noise performance degradation.

In Figure B.12, we depict a scenario when $W_{10} = W_{11}$ is reduced from a maximum value, while W_6 and W_{15} are increased at the same rate. The results closely mirror those of Figure B.11. A more significant change of the first dominant pole (P_5) if observed, while the variation range of unity-gain frequency is now slightly reduced. The capacitive contribution of devices M_6 and M_{15} overpower the decrease of $C_{gd11} + C_{db11}$, causing a noticeable decrease in the pole's frequency. For the small parameter case, this sizing variation

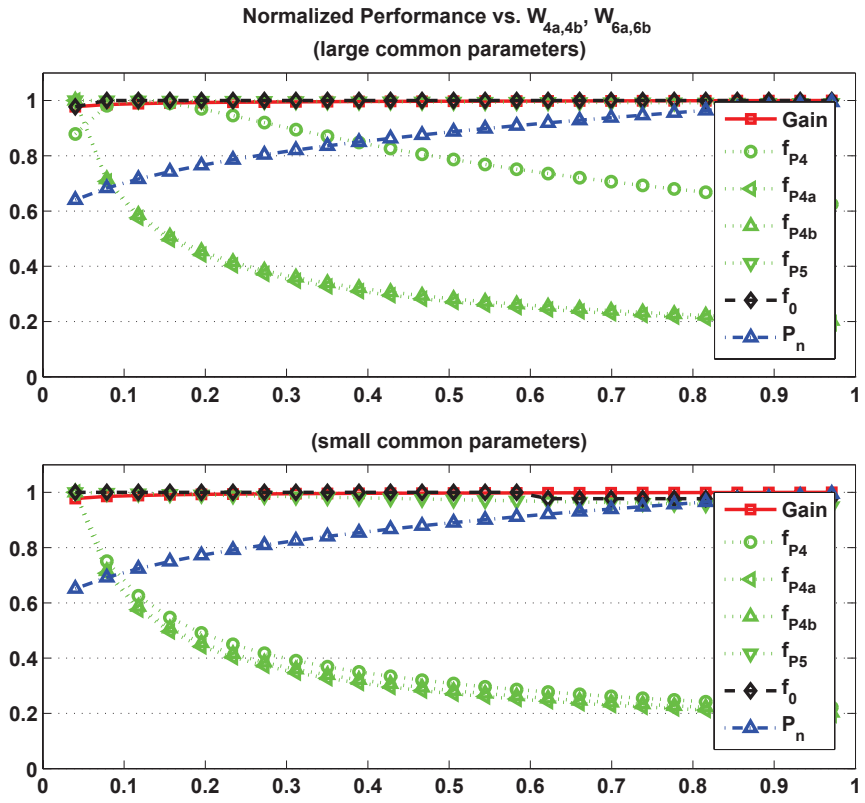

Figure B.13: Input block performance trade-offs for AMP_3 with respect to $W_{4a} = W_{4b}$ and $W_{6a} = W_{6b}$ when W_{10} and W_{15} are constant

pattern provides for a greater separation of the two dominant poles. While frequency point f_{P5} approaches the origin, f_{P4} increases. A reduction of close to 20% in -3dB band may occur, but maximizing f_{P4} can prove advantageous for phase margin.

For the *input* block of AMP_3, Figure B.13 shows the normalized performance changes when $W_{4a} = W_{4b}$ and $W_{6a} = W_{6b}$ are both increased at the same rate, while keeping W_{10} and W_{15} constant. The dominant pole set illustrated is P_5 and P_4. Gain, and noise performance trends are similar to those of AMP_2. The constant gain suggests that this performance has similar, but opposing sensitivities to these devices. An accentuated reduction in the separation of poles is observed. While P_5 remains relatively unchanged, like in AMP_2, a greater variation (reduction) in f_{P4} is found, especially for large

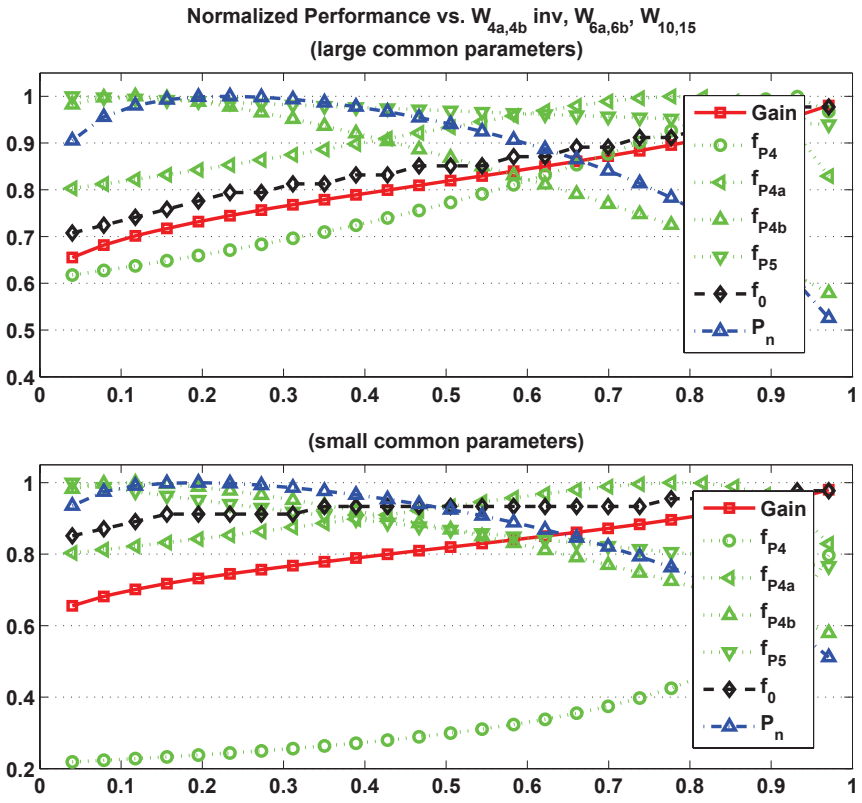

Figure B.14: Input block performance trade-offs for AMP_3 when $W_{4a} = W_{4b}$ and $W_{6a} = W_{6b}$, W_{10}, W_{15} vary in opposing direction

common parameters when compared to AMP_2. For this design, it can vary by up to $\approx 40\%$. Upon closer inspection, we observe that for AMP_3 unity-gain frequency follows the changes in f_{P5} when gain is constant. It is not affected by changes in f_{P4}, as the second pole is located beyond f_0. The virtual insensitivity of gain and bandwidth performance and the degradation of noise suggest that changing $W_{4a} = W_{4b}$ and $W_{6a} = W_{6b}$ in the same direction does not introduce any advantages.

In Figure B.14 we present the results for the input block of AMP_3 when $W_{4a} = W_{4b}$ is varied from maximum to minimum, while $W_{6a} = W_{6b}$, W_{10} and W_{15} follow an opposing trend. In contrast to AMP_2, a close to linear increase in gain can be produced when $W_{4a} = W_{4b}$ decreases and $W_{6a} = W_{6b}$ increases. The maximum performance can be achieved for the maximum value

of $W_{6a} = W_{6b}$ and the minimum of $W_{4a} = W_{4b}$, with $\approx 35\%$ variation across the widths range. In terms of noise performance, the results present a favorable scenario, since it is possible to relatively decrease total output noise as gain increases. For a small portion of the analyzed range, noise follows the increase in $W_{6a} = W_{6b}$. However, the tendency is quickly overpowered by the reduction of $W_{4a} = W_{4b}$. This is due to both devices M_{4a} and M_{4b} controlling not only the noise contribution of *distinguishing* parameters, but also the transfer characteristic to the section's output. In terms of bandwidth, a similar dominant pole scenario is found, where only f_{P5} is located before the unity-gain frequency. More importantly, we note that for large common parameters, f_0 increases at a similar rate with gain, as f_{P5} remains relatively unchanged. It is observed that f_0 can be improved by up to 30%. The advantage is lost for small common parameter values. The greater decrease in f_{P5} for this case partially compensates the same rate of gain increase. Hence, f_0 only varies by $\approx 15\%$. For pole separation, the case of large common parameters follows the increasing tendancy of P_4. For small common parameters, this trend is only preserved for the first two thirds of the parameter ranges. In the last part, P_{4b} becomes more dominant than P_4 and its continued relative decrease degrades pole separation since P_5 changes at a slower rate. The analysis suggests the large common parameter design to be a better overall choice for improving the investigated performance.

A similar analysis and comparison is performed for the *output* blocks of each circuit. Figure B.15 shows the impact on performance in AMP_2 when distinguishing devices M_{13} and M_{14} are varied. This impacts the design parameters from Table B.4 in rows 1 to 6. Both widths were changed at the same rate and in the same direction, maintaining a constant current mirror ratio. The examined pole scenario is formed of poles P_7 and P_o. The latter was not illustrated as it is considered constant in this case. Both poles are located before frequency f_0 on the frequency axis and are dominant. For either common parameter value, gain is not impacted by more than $\approx 5\%$ across the investigated range. For large common parameters, frequency f_{P7} remains relatively unchanged, resulting in a constant distance to frequency f_{Po}. As

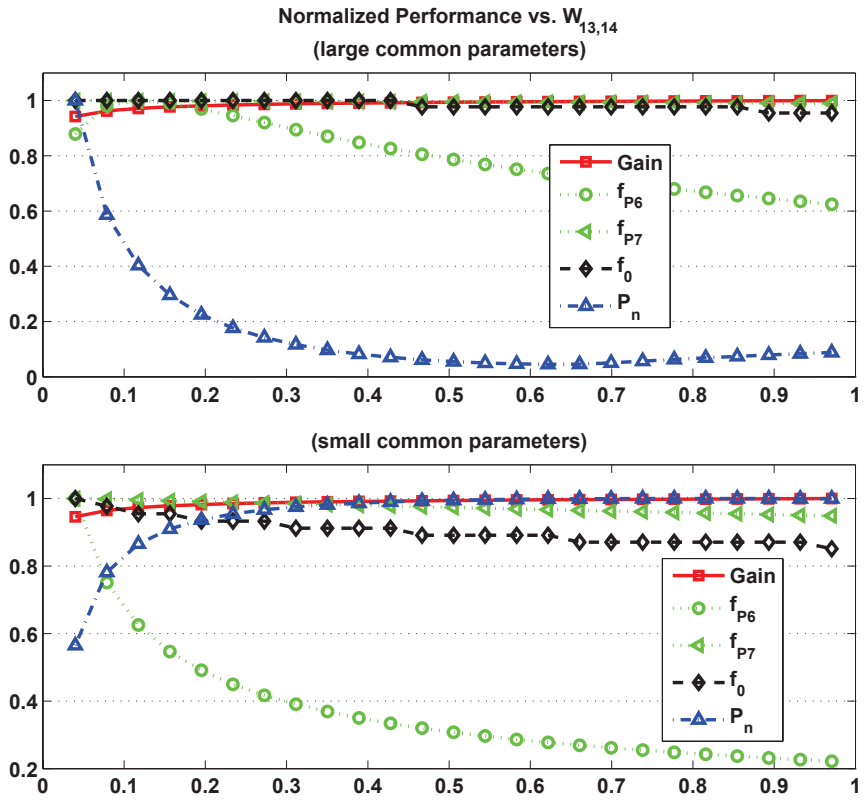

Figure B.15: Output block performance trade-offs for AMP_2 with respect to W_{13} and W_{14} when W_{15}, W_6, and W_7 are constant

a result, unity gain frequency is not degraded by more than $\approx 5\%$ for the maximum reduction in frequency f_{P7}. For small common parameters, a more pronounced degradation results, close to $\approx 15\%$, since frequency f_{P7} can now reduce by $\approx 5\%$. The proximity to the constant frequency f_{Po} transforms the pair of poles into a single second order pole, causing the faster reduction in frequency f_0 when widths W_{13} and W_{14} increase. For noise performance, the non-linear dependence illustrates that the total output noise is reduced when distinguishing parameters become comparable with common constants. Noise remains relatively unchanged after the first third of the analyzed sizing range.

The performance trends for varying the current mirror M_{14} and M_{13} ratio of AMP_2 are given in Figure B.16. For this analysis, we increase W_{13} while reducing W_{14}. Notable changes are exhibited in the behavior of gain. As

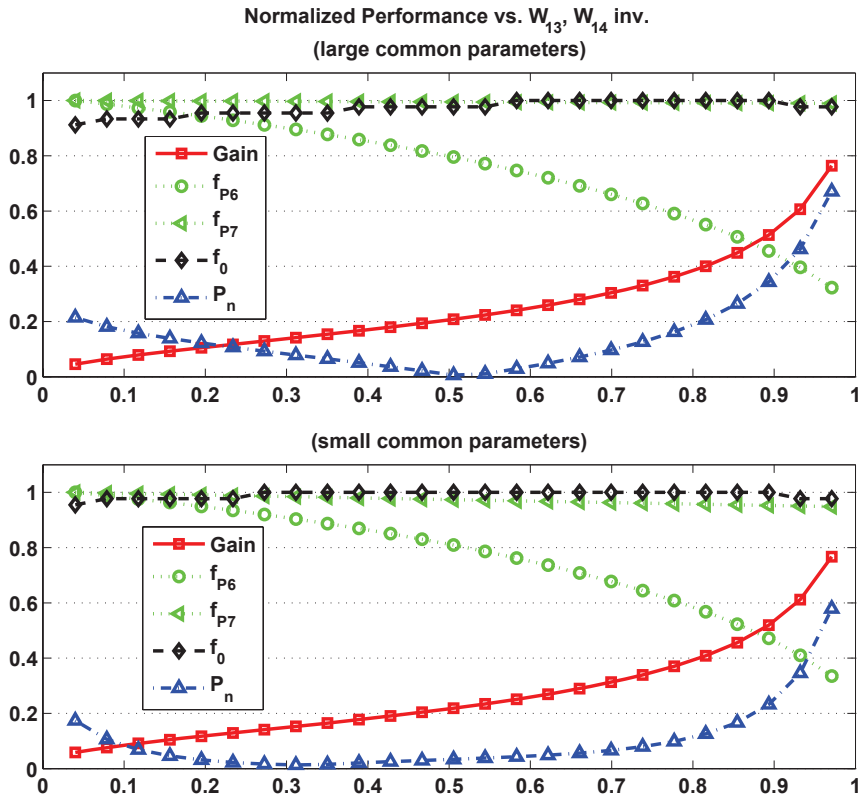

Figure B.16: Output block performance trade-offs for AMP_2 when W_{13} and W_{14} vary in opposing direction

expected, DC gain can now be increased as the current mirror ratio increases and is maximized for the highest ratio W_{13}/W_{14}. The trade-off with noise is relaxed for the initial half of the variation range, when the W_{13}/W_{14} ratio is less than unity. However, in the second half, when the ratio becomes greater than one, the noise performance is dominated by the increasing value of W_{13}. The small common parameter case is favorable as an extended range of values of the variables offers lower noise. In either scenario, as the current mirror ratio approaches the investigated maximum, the gain-noise trade-off becomes dominated by noise which worsens faster than gain improves.

For the *output* block of AMP_3, Figure B.17 shows the performance variation when W_{10} and W_{15} are both increased at the same rate. The impacted variables correspond to rows 1-3 and 6-8 of Table B.5, respectively. As ex-

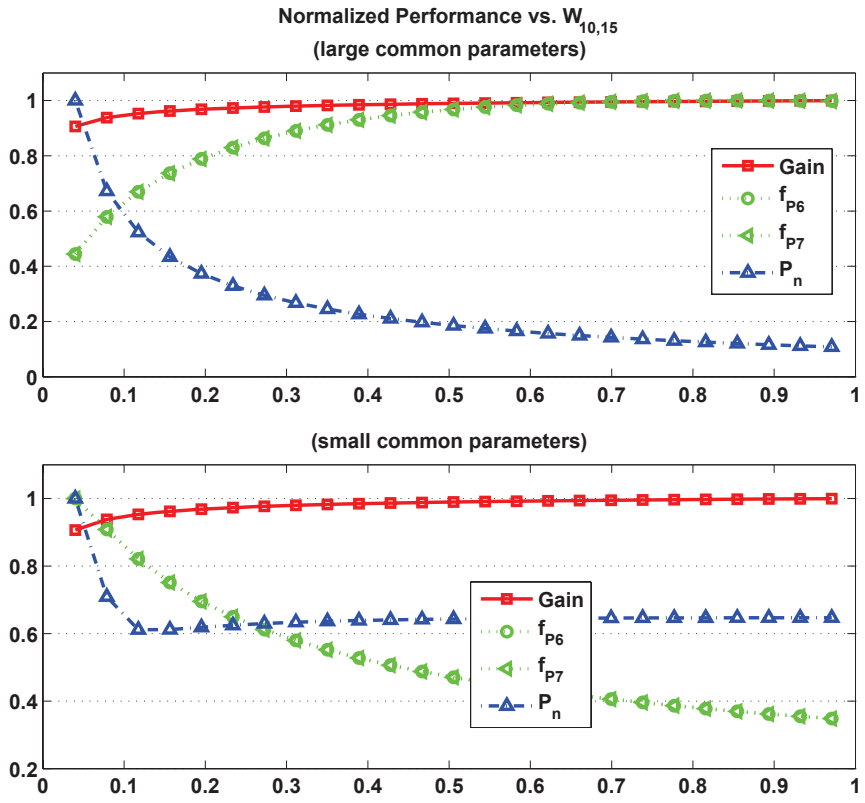

Figure B.17: Output block performance trade-offs for AMP_3 with respect to W_{10} and W_{15} when W_{14}, W_{11}, and W_{13} are constant

pected, the source follower configuration of the *output* block in AMP_3 exhibits less than unity gain across the investigated range. However, results suggest that an improvement of $\approx 10\%$ is still possible as W_{10} and W_{15} become larger. In terms of bandwidth, the dominant poles are P_7 and P_6. We note that as both device widths are changed, the relative pole separation remains constant with both P_7 and P_6 varying at the same rate. Opposing trends arise for the different common parameters cases, with a decrease in pole frequency for small values. While the resistive component remains relatively unchanged with the same dominant contribution of $g_{ms10,15}$, the capacitance increase in the case of small common parameters enforces the bandwidth performance degradation. Noise follows the same pattern in both scenarios, but is better controlled for large parameters. Overall, this suggests that the first combination of pa-

rameters is favorable allowing highest gain to be obtained while maximizing bandwidth and better limiting noise impact of the *distinguishing* parameters.

Comparing the *output* blocks shows that both amplifier designs present combinations for *distinguishing* and common parameters which can be employed to relatively improve bandwidth and noise properties of the circuits. However, in terms of gain, the configuration in AMP_3 is limited by the use of the source follower topology and only minor improvements are achievable.

The gain of AMP_2 can be controlled by six different device widths through 12 distinguishing small-signal parameters. There are 4 direct and 8 inverse relations between gain value and parameters. In terms of the variations required to improve gain, there are 4 situations of opposing trends (indicating design trade-offs). For noise, the same 6 device widths are involved, influencing a total of 44 distinct transconductance and capacitance parameters. They involve 25 direct (out of which 21 are square-root dependences) and 35 inverse relations, with 10 conflicting variation cases between parameters. In the case of pole sets and bandwidth, the 6 transistor widths control 35 parameters found in 26 direct and 48 inverse relations for all pole sets considered. There are 39 design trade-off expressions.

For AMP_3, gain can be controlled by 7 different device widths through 16 distinguishing small-signal parameters. There are 6 direct and 11 inverse relations. There are 7 opposing trends (indicating design trade-offs). For noise, the same 7 widths are involved, influencing a total of 61 distinct transconductance and capacitance parameters. They involve 30 direct (out of which 24 are square-root dependences) and 44 inverse relations, with 19 conflicting variation cases between parameters. In the case of pole sets and bandwidth, the 7 transistor widths control 50 influencing parameters found in 78 direct and 203 inverse relations for all pole sets considered. There are 136 trade-off expressions.

For the 12 constants and CMRR constraint in this experiment, we observe that a total of 5 common devices ($M_{1,2}$, $M_{3,4}$, $M_{8,9}$, M_{12}, M_5, and not considering discrete capacitance) influence their values through 17 different small-signal parameters. The mathematical dependences on these parameters

include 19 direct (with 2 products) and 8 inverse relations. For the extracted constraints, the constants appear in 35 direct, 28 inverse, and 18 equality (for noise) expressions.

Through the proposed circuit comparison methodology, the analysis results presented in Figures B.11-B.17 can be used to also infer the relative limits to which performance can be pushed through the enabling *distinguishing* parameters in each design. For example, in the case of large common parameters of Figure B.17 in AMP_3, an increase in bandwidth can be obtained as W_{10} and W_{15} increase. However, this can only be performed for first half of the investigated dimension range. The non-linear dependence causes the bandwidth to relatively quickly saturate at the maximum. Therefore, it can be inferred that for this scenario, further increasing these differentiating parameters of AMP_3 would only deteriorate power consumption while posing no advantages for bandwidth. Similarly, in AMP_2, increasing W_{13} and W_{14} beyond the midpoint of the range while large common parameters are considered (Figure B.15), does not further improve noise performance and will decrease bandwidth.

The nature of the trade-offs is also captured by the comparison method. This is important as relative sizing strategies can be identified which can relax or even eliminate performance trade-offs. For example, analyzing noise and gain performance in Figure B.16 for small common parameters in AMP_2 shows that while W_{14} is kept greater than W_{13}, gain can be increased by $\approx 15\%$. At the same time, output noise is kept relatively constant. For large reverse ratios of the devices, in the final quarter of the analyzed range, the trade-off between gain and noise becomes more demanding, as gain will deteriorate faster than gain can be improved. Comparing with the small common parameter case in Figure B.14, we can observe that in AMP_3 the gain-noise trade-off can be relaxed for a larger portion of the investigated sizing range. This offers AMP_3 greater flexibility in addressing other trade-offs, since a vaster range of relative sizing between devices $M_{4a,4b}$ and $M_{6a,6b}$ can be explored. For this case, varying the sizing across $\approx 70\%$ of the range increases gain linearly by up to 20% while noise can be relatively improved. The insight is useful in topology selection as

it indicates which circuit structure is better suited for a given specification.

The proposed circuit comparison method is useful to identify incremental topology changes that can combine the benefits of each topology. For example, let's consider a high gain requirement. For the *output* block of AMP_3, the distinguishing parameters of devices $M_{10/15}$ do not add gain due to their source follower configuration, which introduces a DC transfer contribution $\propto g_{mg}/(g_{mg} + g_{md})$. By comparison, the common source device M_{15} in AMP_2 increases gain. An incremental change in AMP_3 for device $M_{10/15}$ can impact gain by transforming the DC transfer to $\propto g_{mg}/g_{md}$ (and changing AMP_3 to a 2-stage design). The change still reduces noise for specific sizing strategies. However, flexibility of higher frequency behavior is diminished as the resistive components of the poles at nodes V_6 and V_7 are no longer correlated to the device's $1/g_{mg}$ parameter. In the modified design, $1/g_{md}$ controls this aspect and is primarily set by the current of $M_{12/14}$. Hence, under fixed bias, increasing $W_{10,15}$ to improve g_{mg} and gain would negatively impact the frequencies of poles P_6 and P_7, dominated by the increasing capacitive components.

In contrast, a reversed situation is noted for the *input* block's behavior. While maintaining constant bias such that the common/matched parameters are constant in both designs, the *distinguishing* features of AMP_2 do not offer gain improvement. In addition, all other performance investigated are deteriorated when $W_{10/11}$ is increased. This suggests that for AC performance of the input stage, the configuration in AMP_3 is preferable. We have observed that this topology offers greater flexibility and presents relative device sizing plans that can aid gain, bandwidth, and noise performance.

The comparison suggests that AMP_3 offers greater flexibility in achieving performance improvements since it presents a considerably increased number of distinguishing design variables that can be used to control performance. AMP_3 is likely to perform better for low noise, high bandwidth applications. The input block characteristics are well controlled by parameters related to $M_{6a/6b}$: noise minimization and unity gain frequency increase occurs at node V_5. A lower noise can be transferred to circuit output V_o through the characteristic of the output block, which has additional noise reduction through

$M_{10/15}$ while keeping relatively unchanged the bandwidth behavior. The noise of AMP_2 is bounded, hence cannot be improved through distinguishing parameters.

Appendix C

Conceptual Models for Linear OTA Functionality

C.1 Basic OTA Concept Functionality Modeling

Basic transconductor functionality can be implemented by a MOS transistor operating in the saturation region. Ignoring secondary effects and subthreshold operation, transfer function of the transistor can be described using the square-law I-V characteristic:

$$H() : \begin{cases} I_o = K\left(V_i - V_c - V_T\right)^2 & \text{if } V_i - V_c > V_T \\ 0 & \text{if } V_i - V_c \leq V_T \end{cases} \tag{C-1}$$

where I_o is the output current, V_i is the input voltage, and V_c is the control voltage. K represents the transistor transconductance parameter and V_T is the transistor threshold voltage. The control voltage V_c is equivalent to the source voltage of the MOS transistor and is viewed here as a control factor for the transfer function, allowing creative alternative design exploration. Equation (C-1) also captures the operating range of this transistor, describing its

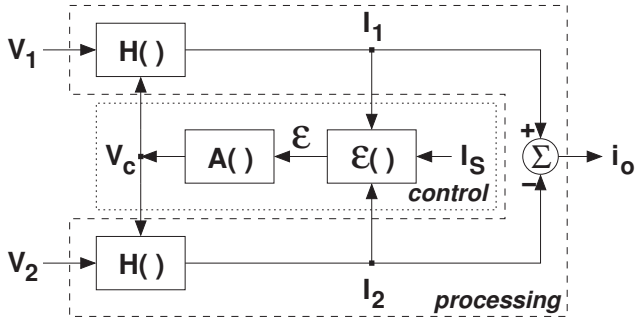

Figure C.1: Simple differential pair conceptual OTA model

relation to the control signal.

The conceptual model representation for a simple differential pair transconductor is shown in Figure C.1. Using this model, the circuit's operation can be described at a conceptual level by two correlated paths: signal processing and control.

Signal processing is defined by two symmetric branches for the differential implementation, each modeled as an $H()$ block described by equation (C-1). The role of the signal processing path is to define the transconductor functionality. Due to the differential and symmetric nature of the model, the overall transfer function of the entire processing path can be expressed as:

$$\begin{aligned} i_o &= I_1 - I_2 = f\left(V_1 - V_2\right) \\ &= \left(V_1 - V_2\right)\sqrt{2K\left(I_1 + I_2\right) - K^2\left(V_1 - V_2\right)^2} \\ &= \left(V_1 - V_2\right)\sqrt{2KI_S - K^2\left(V_1 - V_2\right)^2} \end{aligned} \tag{C-2}$$

where V_1 and V_2 are the input voltages for each branch and I_1 and I_2 are the respective output currents of each branch. Input voltages are considered here as being composed of a small signal variation and a common mode voltage.

The control path of the creative model is employed in adjusting the processing path transfer attributes for the simple differential pair transconductor. As depicted in Figure C.1, the control path makes use of two blocks

described by:

$$\epsilon() : \epsilon = I_S - (I_1 + I_2) \tag{C-3}$$

$$A() : out = V_c \text{ such that } \epsilon \to 0 \tag{C-4}$$

From equations (C-3) and (C-4), the overall control constraint governing the model is:

$$I_S = I_1 + I_2 \tag{C-5}$$

The control voltage V_c needed for each $H()$ block of the model in Figure C.1 is indirectly defined by imposing the control (tail bias) current I_S. This voltage is only defined such that overall control constraints (equations (C-3)-(C-5)) are continuously satisfied given the two input voltages V_1 and V_2, while the current I_S determines the processing path attributes of the model.

To capture the constraints of the model, the processing path transfer given by equation (C-2) is only valid within the limits imposed on the single transistor $H()$ block model. Using equations (C-1), (C-2) and (C-5), the margin of operation for the circuit is given by:

$$|V_1 - V_2| \leq \sqrt{\frac{I_S}{K}} \tag{C-6}$$

This shows that, apart from adjusting processing transfer attributes, the control path is also involved in determining the input voltage values that can be handled by a circuit and still provide an output determined by equation (C-2).

C.2 Improving OTA Concept Linearity

C.2.1 Extending Basic Model Operation Range

Expanding the basic conceptual model's operation range allows for larger input voltage swings. The model from Figure C.1 and related constraints can show basic improvements dependent on the control current I_S and the transistor K parameter. Furthermore, it can be observed that, due to

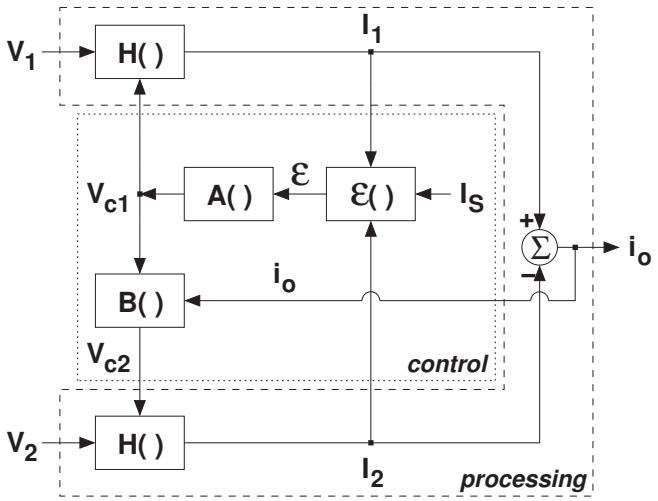

Figure C.2: Conceptual model to extend OTA operating range

the symmetry of the circuit, a reduction of the common control voltage V_c in equation (C-6) is obtained. This suggest using two different control voltages (V_{c1} and V_{c2}) for each processing branch in the basic model.

A *new* circuit conceptual model achieving this requirement is presented in Figure C.2. The basic OTA functionality is maintained through the same processing scheme, $H()$. Since signals V_{c1} and V_{c2} are determined by V_1 (I_1) and V_2 (I_2), respectively, in order to maintain the differential transfer and symmetry of the circuit, the control voltages have to be correlated with each other through the input voltage $V_1 - V_2$ and/or the output current $I_1 - I_2$. Therefore, the transfer of the $B()$ block in Figure C.2 can be described as a function of currents as:

$$B() : V_{c2} = V_{c1} + f\,(I_1 - I_2) \tag{C-7}$$

The obtained operating range constraint of the new model is given by:

$$|V_1 - V_2| \leq \sqrt{\frac{I_S}{K}} + |V_{c1} - V_{c2}| \tag{C-8}$$

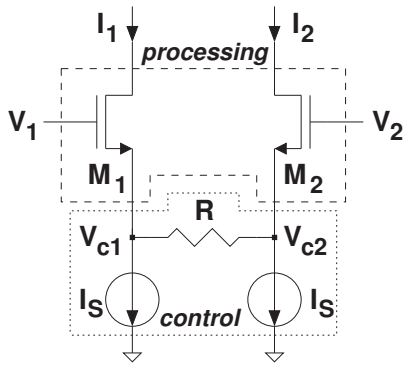

Figure C.3: Resistive source degeneration circuit

The basic model's operating range (equation (C-6)) is now extended by a function dependent on the two separate control voltages used for each processing branch.

The addition of the $B()$ block to the simple differential pair also causes a change in the overall processing transfer function. Using equation (C-1) for each processing branch, the new transfer can conceptually be expressed as:

$$i_o = I_1 - I_2 = f\left(V_1 - V_2, |V_{c1} - V_{c2}|\right) \tag{C-9}$$

where $|V_{c1} - V_{c2}|$ is determined by the $B()$ block transfer.

The conceptual circuit model from Figure C.2 corresponds to the source degeneration principle. Both resistive and MOS transistor source degeneration topologies are covered by this model. Using different transfer functions for the $B()$ block yields the two different implementations. Two transistor circuit topologies implementing this principle are shown in Figure C.3 and Figure C.4.

C.2.2 Compensating Basic Model Nonlinearity

A second improvement of the basic model involves compensating the non-linear term in the overall differential pair processing transfer given by equation (C-2).

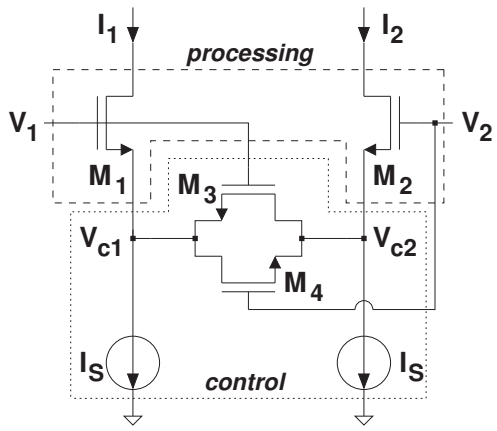

Figure C.4: MOS transistor source degeneration circuit

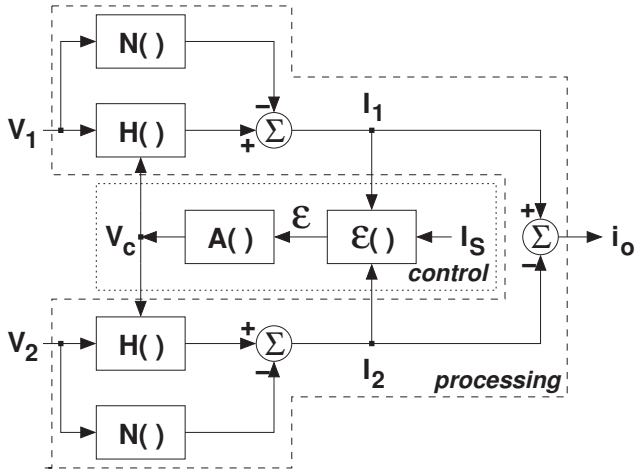

Figure C.5: Conceptual model for OTA nonlinearity compensation using independent corrections for each processing branch

By rewriting equation (C-1) as:

$$H() : \begin{cases} I_o = A_1 + A_2 V_i + A_3 V_i^2 & \text{if } V_i - V_c > V_T, \\ 0 & \text{if } V_i - V_c \leq V_T. \end{cases} \tag{C-10}$$

where A_1, A_2 and A_3 are determined by the control voltage V_c and transistor parameters, the linearity correction model from Figure C.5 can be envisioned. In this case, the abstract $N()$ blocks compensate the non-linear term $A_3 V_i^2$

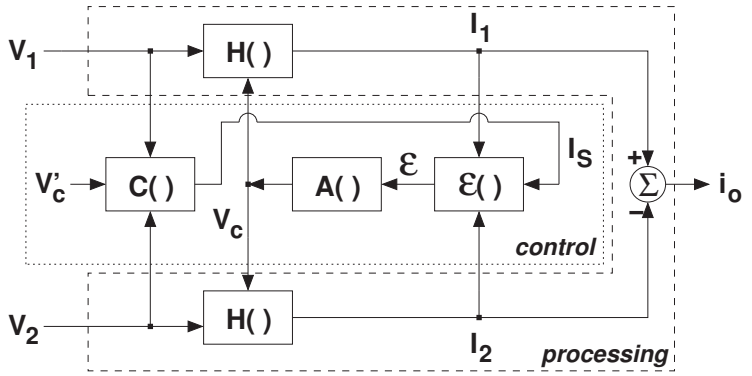

Figure C.6: Conceptual model of OTA nonlinearity compensation using a common correction for both processing branches

of each processing branch. A simplification of this representation is shown in Figure C.6. Observing that the overall control equation of the model in Figure C.5 can be written as:

$$I_1 + I_2 = I_S = I_{DC} + f\left((V_1 - V_2)^2\right) \tag{C-11}$$

when differential input signals are used and I_{DC} is correlated with the common mode voltage of V_1 and V_2. Hence, a single block generating the right-hand side of equation (C-11) by means of an external control signal and the input signals can replace the two $N()$ blocks in Figure C.5 while preserving OTA functionality. These considerations justify the equivalent model from Figure C.6 with a linear overall transfer function.

A transistor level implementation of this model was presented in [41], an adaptive bias transconductor. The circuit schematic is shown in Figure C.7.

The previous linearity correction is rooted in observing and compensating the non-linear term in the individual transistor transfer function. Another correction strategy can be inferred by examining the overall processing transfer of a simple differential pair (equation (C-2)) and, by using equation (C-10), expressing it as:

$$i_o = F_1\left(V_1 - V_2\right) + F_2\left(V_1 - V_2\right)^2 \tag{C-12}$$

This suggests that it is possible to use two independent differential pairs that

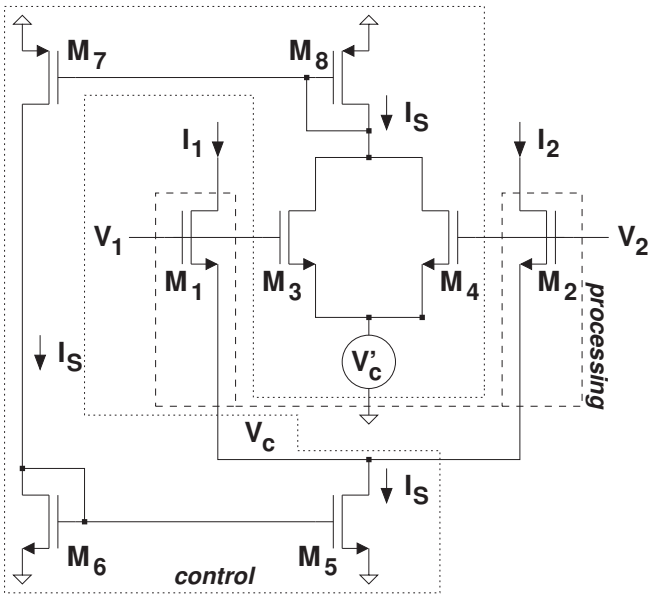

Figure C.7: Adaptive bias transconductor circuit

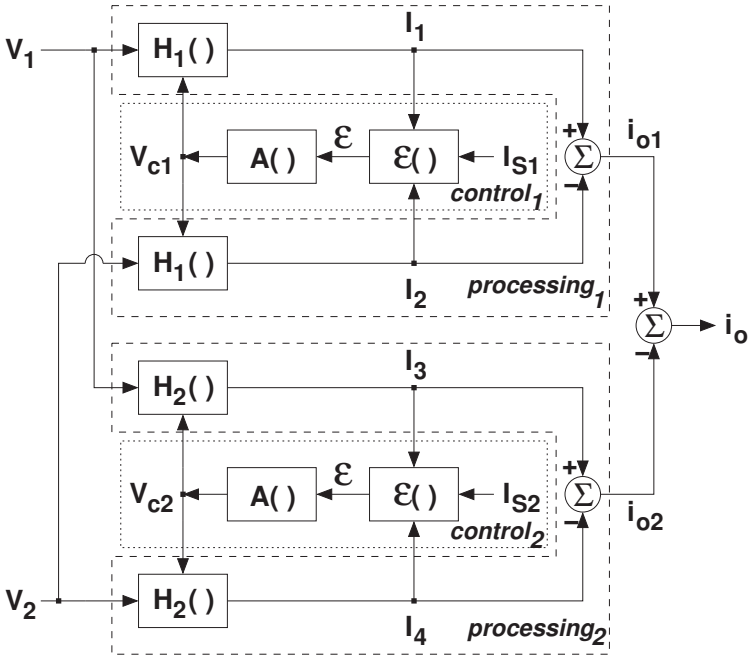

Figure C.8: Conceptual model of OTA nonlinearity compensation derived from overall processing transfer

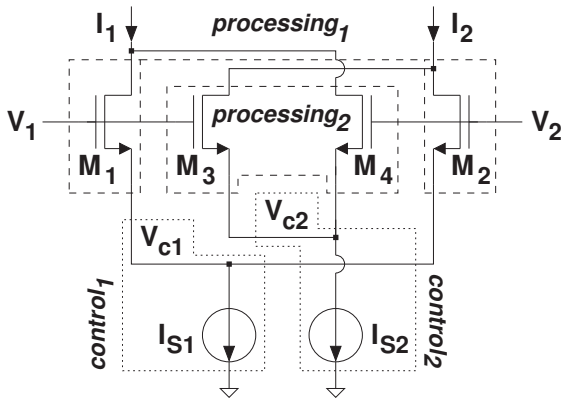

Figure C.9: Cross-coupled differential pairs circuit

share only the input voltages to create a linear behavior of the output current (by proper choice of F_1 and F_2 (for each of the two differential pairs). Both transfer parameters are determined by only the control voltages and transistor parameters used in each of the two basic models, therefore allowing the use of the same input signals on both representations. The model for such a correction is shown in Figure C.8.

Circuit implementations of this corrected basic model generate the cross-coupled differential pair topology. The schematic of this circuit is presented in Figure C.9.

Both non-linearity compensation techniques described here also impact the operating range of the model since this range is determined by the control path implemented in the correction model. Details can be found in [40–43].