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Design of Low-power, Low-noise Readout Circuits for Sensory Microsystems

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Yingkan Lin

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Abstract of the Dissertation

Design of Low-power, Low-noise Readout Circuits for Sensory Microsystems

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A wide range of new applications, especially in the areas of health and environmental monitoring, have become possible due to advances in the sensor technologies over the last decade. To translate those advances in the sensor technologies into sensory microsystems amenable to these applications, novel techniques and design methodologies have to be developed at the sensory interface to address more stringent system constraints and the imperfections in these sensor technologies. We propose and demonstrate the design methodologies and implementations of the sensory microsystems for two novel sensor technologies, selective metal-oxide gas sensor and semiconductor scintillator.

The gas sensing system with a selective metal-oxide gas sensor is developed to discriminate and measure the signaling metabolites in human exhaled breath. The gas sensor indicates the gas density by changing its resistance with the concentration of the target gas. The proposed readout integrated circuits are able to interface the sensors with the baseline resistance from 1 kΩ to 100 MΩ and measures the gas induced resistance change in the range from 0.05% to 10% of the baseline re-

sistance. The high resolution and low power are realized in the proposed readout architecture with an adaptive baseline compensation structure and 13-bit Sigma-Delta ADC. A 0.5 μm CMOS technology prototype integrated chip is taped out and tested to demonstrate the wide dynamic range and low power consumption of the readout circuit.

The radiation detection system is implemented with a large-area epitaxial photodiode integrated on a body of a semiconductor scintillator. The radiation detector is stimulated by the radiation particles and generates electronic charge into the readout circuits. The design of low-noise readout circuit including charge sensitive amplifier, pulse shaper, peak detector and clock-less A/D converter are discussed. The size of the input transistor and the peaking time of the shaper are optimized to obtain a minimum equivalent noise charge (ENC) with a large input load capacitance. A time-based clock-less A/D converter is implemented to minimize the interference from the digital part of the readout system on the low-noise charge-sensitive amplifier. A prototype integrated chip is built in a standard 0.5 μm CMOS technology and the corresponding test printed circuit board (PCB) with chip on board technique is fabricated. An ENC of 334 electrons is measured at 50 pF input capacitance with a slope of 4.5 electrons/pF and the linearity is better than ±1%. The total power consumption of one charge amplification channel is 2.2mW.

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Chapter 1

Introduction

1.1 Readout Circuit for Sensory Microsystems

Sensory microsystems are the systems implemented on miniature wearable or portable platforms with their input signals coming from different kinds of sensor devices. The development of MEMS technology endows sensors with considerable diversity. As a result, sensory microsystems have a significant and pervasive impact on a large number of applications, including medical diagnostics and treatment, disability aids, automotive industry, security and defense sectors, environmental studies, consumer electronics and etc. The design of sensory microsystems focuses on developing high-resolution, high-throughput, high-integration-density and low-power. High resolution ensures the sensing accuracy of the system. High throughput allows for real-time operation in applications with high computational complexity and high data rates. High density of integration yields low cost and small form factor. Low-power designs allow for the use of a miniature battery power supply, wireless power harvesting, or other low-energy power sources. These design requirements ask for a high performance of the readout circuit for the microsystems.

Readout circuit refers to integrated circuit specially used for reading sensors of a particular type. Design of integrated circuit technology is necessary in the

sensory microsystems where the sensitivity is of importance and using a discrete circuit may not be feasible as noise may be large enough to cover up the whole signal. Most sensors produce only low-level signals so that some form of low-noise readout pre-amplification must be employed. Since the amplification electronics has to offer a sufficient gain for low-level signals in order to facilitate further conditioning and processing, its properties are most crucial. One of the critical parameters is its noise performance. The equivalent input referred noise of the readout circuit limits the resolution because it defines the smallest distinguishable signal level. In most cases, signal conditioning has to follow the amplification electronics to facilitate further signal evaluation. Typical functions performed by signal conditioners are pulse shaping, equalization, signal compression, multiplexing and demultiplexing, and A/D conversion. The amplification and conditioning are merged together into a single module as the readout circuit.

This work presents the readout circuits design of two examples of such sensory microsystems for two novel sensor technologies, selective metal-oxide gas sensor and semiconductor scintillator. Both systems have wide application in current society and require high accuracy and low power on their readout circuits.

1.2 Background of Selective Gas Sensing

Detecting and discriminating among signaling metabolites in the exhaled human breath and their measurement in the trace concentrations would lead to a personal breath analyzer, a fast, non-invasive and early diagnostic medical tool [1, 2]. In the Exhaled human breath, there is a mixture of N_2, O_2, CO_2, H_2O, inert gases and hundreds of other trace gases [3]. These trace gases include inorganic molecules such as NO, NH_3 or CO and volatile organic compounds (VOCs) such as acetone, ethane and isoprene, with concentrations ranging from parts-per-billion (ppb) to parts-per-million (ppm). For different people, the composition of breath varies a lot both qualitatively and quantitatively, especially in the field of trace gases. VOCs are products of core metabolic processes while inorganic molecules are related to health conditions and can reflect a potential disease of the individual or a recent exposure to a drug or an environmental pollutant.

Therefore, the abnormality in the concentration of certain trace gases, so-called bio-markers, could potentially provide clues to diagnose corresponding diseases. Identifying these signaling metabolites (disease markers) and measuring them in trace concentrations is not a trivial problem. However, among the current usage, breath analysis typically involves bulky and costly equipment and large sampling volumes or requires ”unhealthy” receptors to be consumed by the patient prior to testing. The main drawback in breath analysis diagnostics till now has been the lack of inexpensive sensor technologies that would detect and monitor the concentration of a single gaseous compound in the complex odor mixture with high specificity and at low trace concentrations, in the presence of numerous interfering compounds. Thus, to meet the promise of an easy, affordable, noninvasive, medical diagnostics technology, a simple, low cost and small gas sensor with accurate and low power integrated readout circuit is needed for breath analysis.

1.3 Background of Radiation detection

As the illicit use of nuclear devices grows into a national security issue, as the threaten of radiological contamination to human health is gradually recognized, to develop more sensitive and accurate radiological detection technology becomes an important subject. The theory of radiation detection is to detect the ionizing events as nuclear radiation and X-ray are all ionizing radiation.

For a typical ionization counter, the total charge produced by the passage of an ionizing particle under a high positive voltage through the active volume can be collected and measured. Different names are used for the devices based on the amount of voltage applied to the center electrode and the consequent nature of the ionizing events. If the voltage is high enough for the primary electron-ion pair to reach the electrodes but not high enough for secondary ionization, the device is called an ionization chamber. The collected charge is proportional to the number of ionizing events, and such devices are typically used as radiation dosimeters. At a higher voltage, the number of ionizations associated with a particle detection rises steeply because of secondary ionizations, and the device is often called a proportional counter. A single event can cause a voltage pulse proportional to the energy loss of the primary particle. At a still higher voltage, an avalanche pulse is produced by a single event in the devices called Geiger counters.

Another radiation detection technology is to use a scintillator: a substance which emits light when struck by an ionizing particle. The scintillation detectors used in the Geiger-Marsden experiment were simple phosphor screens which emitted a flash of light when struck by an alpha particle. Modern scintillation counters may use single crystals of NaI doped with thallium. Electrons from the ionizing event are trapped into an excited state of the thallium activation center and emit a photon when they decay to the ground state. Photomultiplier tubes are used to intensify the signal from the scintillations.

The application of radiation detection has permeated into peoples everyday life. As a small, lightweight, cost effective personnel radiation monitoring device, an electronic dosimeter covers a wide rage of X-ray and Gamma radiation detec-

tion to protect the wearer from the harmful effects of radiation by tracking changes in exposure and keeping an ongoing record of the user's dose over time. Geiger counters are used to detect, locate and quantify any radioactive material in a very short time. Contamination monitors protect critical locations from the trafficking of radioactive sources and ensure that radioactive contamination can be alarmed and eliminated. However, no matter which field radiation detection is applied in, it is required to be accurate, portable, adaptable and real time. These requirements impose high difficulties on the design of radiation detectors as well as the readout circuits.

It is of significance to analyze the design procedure of two systems separately, because the different sensing theories of the sensors lead to very different characteristics of input signals. The resistance of the gas sensor is used as system input and can be seen as a DC signal inside each measurement. On the other hand, the radiation detector generates current pulse into the system which is abrupt and of short duration. The respective design principles and circuit architectures of two systems are elaborately analyzed in the following chapters, related simulation and ASIC test results are presented as well.

Chapter 2

Readout Circuit for Gas Sensing System

2.1 Gas Sensor

The gas sensor adopted in the proposed system is shown in Figure 2.1. It utilizes resistive chemosensing technology which can selectively measure ppb concentrations of target gases [1, 2]. By controlling the microstructure of nanocrystalline metal oxide films of the sensor so as to employ oxide polymorph phases, the sensors that are sensitive to only a specific class of gaseous analytes or even be specific to a single species have been derived. Selective NO, ammonia, and acetone breath analyzer prototypes have been produced. However, there is an inherent property of the gas sensor that their large baseline resistance can be few orders of magnitude higher than the actual sensor resistance change due to the signal response. Moreover, the large baseline resistances vary across sensors and drift over time at a different rate.

The sensitivity required for quantification of the ppb level concentration of these signaling metabolites calls for novel circuit and system techniques in the design of the readout IC system. To achieve the high sensitivity, readout techniques have to address the property of the gas sensors. There is a wide range of pro-

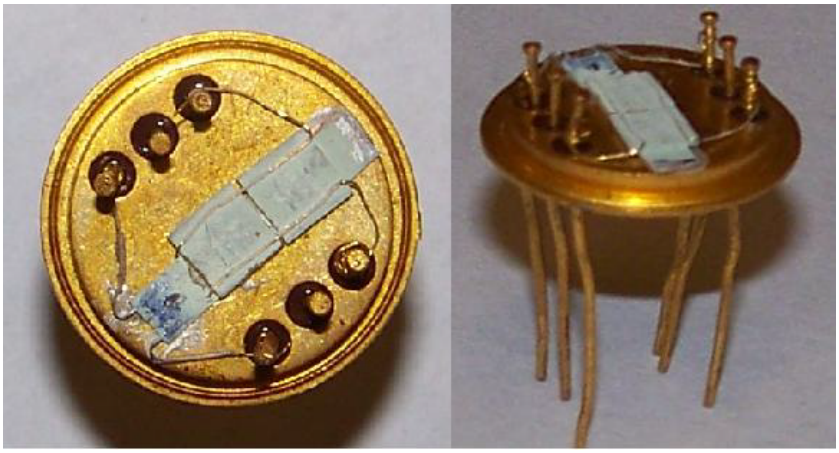


Figure 2.1: Top view and side view of the metal-oxide gas sensor.

posed instrumentation techniques developed for resistance measurement for gas or chemical sensors. A system simply applying current to measure the voltage across the unknown resistor only covers 60dB resistance change range [4]. Implementations based on resistance-to-time conversion [5], in which the oscillation frequency directly depends on the detector resistance, can fit a very wind dynamic range, up to GΩ, but the conversion time increases linearly with the increase of the detector resistance. Moreover, its accuracy is affected by the parasitic capacitance of the sensing device and can hardly be better than 0.5%. The approach which compresses the detector resistance in a logarithmic space [6] by using CMOS parasitic vertical bipolar devices doesn't achieve an accuracy better than 1% because of its intrinsic approximation. Another popular method is to convert the resistance into voltage mode or current mode, amplify the signal and perform the analog-to-digital conversion. By tracking baseline resistance, some developed readout systems achieve around 160dB dynamic range and 0.1% accuracy [7, 8]. Apart from satisfying the sensitivity and dynamic range requirements in presence of large variable baseline resistance for the gas sensor, low power consumption of the readout circuit is another important design constraint for a hand-held, portable and realtime device.

2.2 System Overview

A low-complexity, low-power solution for the measurement of gas concentrations that tracks the baseline resistance is proposed. The readout circuit matches the detector baseline resistance from 1 kΩ to 100 MΩ. The detectable resistance change ration ranges from 0.05% to 10%, which leads to the dynamic range of the system of 166 dB. In addition, the power consumption of the systems is significantly reduced compared to the solutions proposed in the literature. The proposed topology is also amenable to implementation of the signal processing algorithms based on the independent component analysis [9] that can compensate for the variation of the baseline resistance of the detector due to degradation and ageing.

2.2.1 Detector Resistance Composition

A gas sensing system consists of three main parts: an array of gas sensors with temperature control circuit, an electronic read-out circuit and a data processor. Each gas sensor behaves electrically as a resistor. The electrical resistance of each of the detector in the array is composed of two series resistance. The first series resistance is a baseline resistance, R_b. The baseline resistance depends on the sensitive material kind and fabrication technique. It may varies across detector design and even across detectors with the same design. The value of this resistance can be in a wide range that spans over several decades. Due to ageing of the device and temperature gradient, this baseline resistance also demonstrates change over time. The second component of the detector resistance is the resistance related to the presence of the specific gas in the environment, ΔR_{gas}. Thus, the total resistance of a gas sensor in the array is given by:

$$R_{sen} = R_b + \Delta R_{gas} \tag{2.1}$$

where only ΔR_{gas} represents the useful signal, as the ratio of ΔR_{gas} and R_{sen} quantifies the existence and density of the target gas.

The baseline resistance of the gas sensor adopted in the proposed system spans over 5 decades, from 1 KΩ to 100 MΩ. In the presence of gas analytes, the estimated range of the resistance ΔR_{gas} varies from 0.05% to 10% of the baseline resistance R_b, leading to the total dynamic range of resistance R_{sen} of 166 dB. To cover this dynamic range with a single ADC, the number of bit of ADC has to be at least 28 bits which is unrealistic.

2.2.2 System Architecture

In order to realize the large detection dynamic range, a readout system which is insensitive to the baseline resistance and measures only the gas induced resistance change in a specific voltage range around the baseline resistance is an effective implementation. The system block diagram is shown in Figure 2.2. A voltage D/A converter and a current D/A converter are introduced to compensate for the wide variation range of the baseline resistance and to limit the power consumption. The current D/A converter (IDAC) is used for cancelation of the effect of inherent baseline resistance of detector through calibration. The voltage D/A converter (VDAC) provides for a different voltage drop across the sensor and effectively limits the current that flows through the detector which is the power consumption of the readout system. A/D converter, implemented as the current mode incremental $\Delta\Sigma$, is then used to measure the difference between the current that flows through the gas sensor and current of IDAC. The measured current corresponds to the component of the detector resistance sensitive to the change in the gas concentration. As the large portion of the detector current that originated from the baseline resistance is compensated by IDAC, the required resolution of the current ADC is significantly reduced and only moderate resolution is required. In this way, by adjusting the digital input value of the two D/A converters, the readout circuit can be both energy effective and highly accurate.

According to the Figure 2.2, the current difference caused by detector resis-

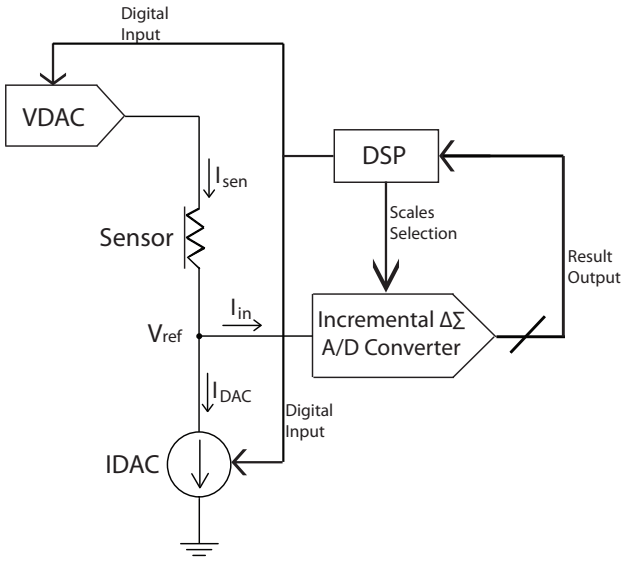


Figure 2.2: Block diagram of gas sensor readout circuit.

tance variation can be expressed as:

$$I_{\Delta} = \frac{V_{DAC} - V_{ref}}{R_b - \Delta R_{gas}} - \frac{(V_{DAC} - V_{ref})}{R_b}, \tag{2.2}$$

where the V_{ref} is set at 0.9V and the voltage range VDAC can supply is from 1V to 2.9V. Thus the electrical potential difference on the sensor ranges from 0.1V to 2V. D/A converters are designed as 5-bit voltage DAC and 8-bit current DAC. First of all, in the field of sensitivity, the system is required to detect as small as 0.05% resistance variation. Considering the maximum baseline resistance, 100 MΩ, and the largest VDAC output, the least significant bit(LSB) of ADC can be calculated according to (2.2) as:

$$I_{lsb,ADC} = \frac{2.9 - 0.9}{100M - 100M \times 0.05\%} - \frac{2.9 - 0.9}{100M} = 10pA \tag{2.3}$$

Secondly, in the field of dynamic range, the up-limit of the detectable-resistance change ratio is 10% which means that the ADC doesn't saturate until the current

caused by 10% detector resistance change flows into the ADC. For the minimum value of the base resistance , 1 KΩ and the smallest VDAC output, the maximum input current of ADC can be obtained by (2.2) again as:

$$I_{max,ADC} = \frac{1-0.9}{1K-1K\times 10\%} - \frac{1-0.9}{1K} = 11.1\mu A \tag{2.4}$$

The corresponding number of bit of the ADC has to be $\frac{log(11.1\mu/10p)}{log(2)}$, approximate 20 bits. Although it is better than 28 bits mentioned at the beginning, it's still a tough performance for an ADC. As a result, the ADC is designed with two measurement ranges. On the other hand, since the residue current of IDAC, which is always smaller than 1 LSB of IDAC, also flows into ADC, the superposition of this residue current and maximum ADC input current has to be within the ADC conversion range. Therefore, IDAC is divided into two scales as well. The baseline resistance range can be seperated into two equivalent parts, 1 K-320 KΩ, 320 K-100 MΩ. The resolution of each scale can be calculated according to (2.2), the LSB of ADC in two measurement scales are 2.85 nA and 9 pA. It's easy to calculate the currently necessary resolution of ADC is 12-bit. Moreover, an addition bit has to be inserted to indicate the direction of the input current. Thus, a 13-bit ADC is implemented in the system which is feasible and reliable. The corresponding two scale 8-bit IDAC has resolution of 400 nA and 1.3 nA respectively.

To demonstrate the accuracy and power consumption of the proposed system architecture, the gas sensing system is simulated in MATLAB. The simulation is run from the calibration mode to the detector resistance measurement mode, the meaning of each mode will be explained in the following section. Resistance thermal noise is also introduced into the system. In Figure 2.3, the baseline resistor is chosen to be 100 MΩ which is the worst case for the system sensitivity due to the smallest current. The change in the detector resistance is from 0.05% to 10%. From Figure 2.3, we can observe that that the maximum error is on the order of 0.045% of the baseline resistance.

To quantify the power consumption of the system, detector resistance change

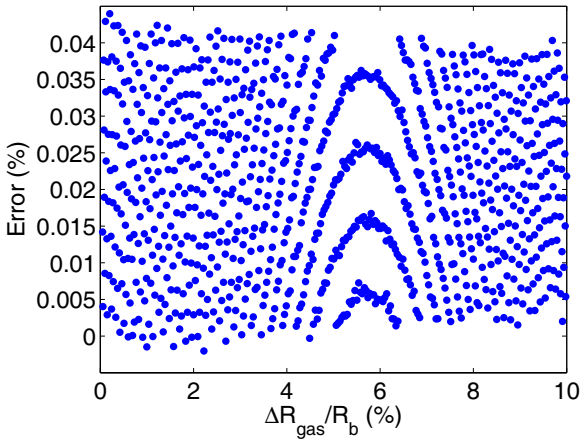


Figure 2.3: The relative measurement error as the function of the ratio between gas induced resistance change and 100MΩ baseline resistance.

ratio is fixed at 10% which incurs the largest current variation. Figure 2.4 shows the power consumption as a function of the baseline resistance at 10% detector resistance change ratio.

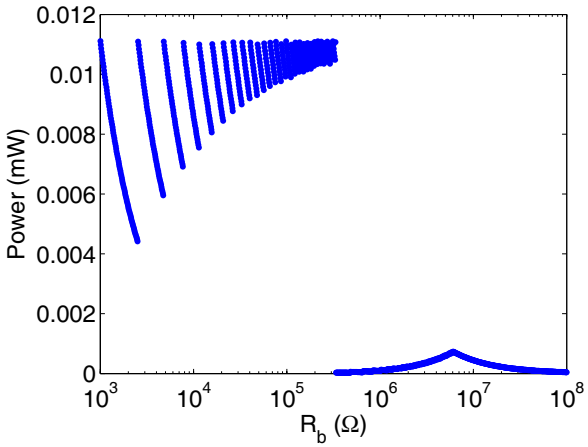


Figure 2.4: Power consumption of the readout system as the function of baseline resistance with $\Delta R_{gas}/R_b = 10\%$.

2.2.3 Operation Modes

To measure the change of the detector resistance, the proposed readout system has two modes of operation, namely calibration and measurement. Calibration is used to set the voltage across the detector to a constant reference voltage in the absence of the target gas, since the baseline resistance may vary across different detectors. Meanwhile calibration sets the biasing current of current DAC to a constant value before data conversion. Thus calibration not only guarantees high accuracy with a moderate resolution of ADC, but also limits the power consumption of the readout system.

Since the approximate value of the sensor baseline resistance is known before calibration begins, the scale of ADC and IDAC can be determined by comparing the expected R_b with the boundary resistance between two scales, 320KΩ. At the same time, the input value of the VDAC can also be set according to R_b. Therefore, in the calibration mode, only the input of the IDAC has to be decided. In this process, the ADC works as a comparator in a 1 bit mode and this output bit represents the direction of the input current. Thus the time consumption of the calibration in worst case is less than 1/16 of the conversion time. According to Figure 2.2, by increasing the output current of the IDAC, the current flowing into the ADC is decreasing until the current direction turn around. At that moment, the digital input of the IDAC has to be reduced by 1 to maintain the current flowing into the ADC. Accordingly, the input current of the ADC is less than 1 LSB of IDAC, and ADC has got its initial value. The calibration is completed.

In measurement mode, the input value of voltage DAC and current DAC stay the same. The change of target gas concentration causes the resistance change of the gas sensor. The ADC works in full-bit mode and converts the analog input current to digital outputs which quantify the present gas concentration.

2.3 Current-Steering D/A Converter

2.3.1 Circuit Architecture

Current-steering D/A converters are based on an array of matched current sources that are switched to the output. There are two basic architectures to implement this array, namely the binary-weighted and thermometer-coded.

Binary-weighted

In the binary implementation, every switch switches a current to the output that is twice as large as the next least significant bit. The digital input code directly controls these switches. The output current of the binary-weighted structure is expressed as:

$$I_{out} = I_{lsb} \sum_{i=1}^{N} b_i 2^{i-1}, \tag{2.5}$$

where N is the number of binary-weighted bits and b_i are the binary-weighted bits. The standard deviation of its output current for the most critical transition is given by:

$$\sigma(\Delta I) = \sqrt{2^N - 1} \frac{\sigma(I)}{I} LSB, \tag{2.6}$$

where $\sigma(I)$ is the standard deviation of an unit current source with a normal distribution and it is a good approximation for the differential nonlinearity(DNL). It's worth noting that the $\sigma^2(\delta I)$ at the most significant bit transition is approximately $2^(N-1)$ times larger than at the least significant bit transition. Therefore, a large DNL error and an increased dynamic error are intrinsically linked with binary-weighted architecture. However, this architecture still takes advantages at its simplicity and the small required silicon area.

Thermometer-coded

In the thermometer-coded architecture, every unit current source is addressed separately. The digital input code has to be converted to a thermometer code that controls the switches. The output current of thermometer-coded structure is expressed as:

$$I_{out} = I_{lsb} \sum_{i=1}^{M} t_i, \tag{2.7}$$

where $M = 2^N - 1$, M is the number of thermometer-coded bits and t_i are the thermometer-coded bits. Its output current standard deviation can be expressed as:

$$\sigma(\Delta I) = \frac{\sigma(I)}{I} LSB \tag{2.8}$$

This equation means that in thermometer-coded structure, the error between two consecutive code is just the deviation on the additional unity current source. The advantages of this architecture are its good DNL error and the small dynamic switching error. With thermometer-coded, DAC has a guaranteed monotonicity since only one additional current source is switched to the output for one extra LSB. However, it suffers from complexity, large chip area and power consumption.

Segmented

To get the best of both worlds, the current mode D/A converter of the proposed system is implemented using segmented current-steering structure [10]. This structure can make use of the advantages offered by both binary-weighted and thermometer-coded current DAC architecture. The segmented current-steering structure separates N-bit binary input data into M less-significant bits with binary-weighted current sources and $(N - M)$ more-significant bits in thermometer-coded structure. In this architecture, a balance between good static and dynamic specifications versus a reasonable decode power, area and complexity can be reached. Since the

segmented architecture is a mixture of the previous two architectures, its standard deviation is:

$$\sigma(\Delta I) = \sqrt{2^{M+1} - 1}\frac{\sigma(I)}{I}LSB \tag{2.9}$$

The segmented 8-bit current-steering D/A converter in the proposed system is implemented with 4 bit thermometer-coded structure and 4 bit binary-weighted structure shown in Figure 2.5. There are 4 current sources in the binary structure while 15 current sources in thermometer architecture. The cascode configuration increases the output impedance to further stable the current output. A binary to thermometer decoder is also needed to translate the 4 more-significant bits from binary value to 15-bit thermometer value. Furthermore, by adding enough delay on the path of 4 less-significant bits in decoder, all the current sources are guaranteed to generate output simultaneously.

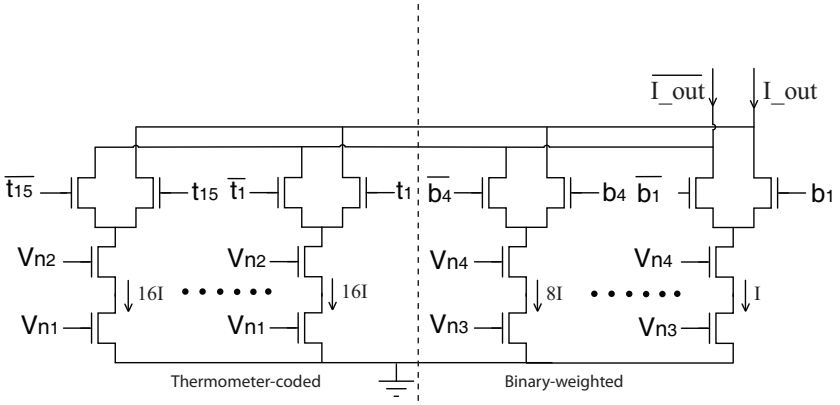


Figure 2.5: Schematic of current mode D/A converter.

2.3.2 Current Cell Mismatch

For a current-steering D/A converter, DNL can be improved by the adoption of segmented structure, another important specification, integral nonlinearity(INL), has to be designed carefully. The INL is mainly determined by the matching behavior of the current sources in the DAC. The parameter, INL yield is defined

as the ratio of the number D/A converters with an INL smaller than $\frac{1}{2}$LSB to the total number of tested D/A converters. The statistical relationship between the INL yield, the resolution and the unit current standard deviation for the DAC is discussed in [11] and given by:

$$\frac{\sigma(I)}{I} \leq \frac{1}{\sqrt{2^{N+2}C}}, \tag{2.10}$$

$$C = inv\_norm_{(-x,x)}(0.5 + \frac{INL_{yield}}{2}), \tag{2.11}$$

where the $inv\_norm(x)$ is the inverse function of the normal cumulative function integrated from $-x$ to x and N is the resolution of the DAC. It can be obtained according to the equation that for an 8-bit D/A converter, to achieve a 99.7% INL yield specification, the unity current-source matching is $\frac{\sigma(I)}{I} \leq 1\%$.

Based on the mismatch model of MOS transistor derived in [12], this can be expressed in terms of the process-matching parameters and the transistor biasing as:

$$\frac{\sigma^2(I)}{I^2} = \frac{4(\sigma^2_{V_T})}{(V_{GS} - V_T)^2} + \frac{\sigma^2_\beta}{\beta^2}, \tag{2.12}$$

where V_T is the threshold voltage of the transistor and $\beta = C_{ox}\mu W/L$ is the current factor. Then the dimensions of the current source transistors are given by:

$$W^2 = \frac{I}{K_n(\frac{\sigma(I)}{I})^2}[\frac{A^2_\beta}{(V_{GS} - V_T)^2} + \frac{4A^2_{VT}}{(V_{GS} - V_T)^4}], \tag{2.13}$$

$$L^2 = \frac{K_n}{4I(\frac{\sigma(I)}{I})^2}[A^2_\beta(V_{GS} - V_T)^2 + 4A^2_{VT}], \tag{2.14}$$

where A_{VT} and A_β are process-related constants and $K_n = \mu_n C_{ox}$. According to INL_{yield} specification $\frac{\sigma(I)}{I}$ has to be smaller than 1%, if the mismatch of width and length is considered across transistors, $\frac{\sigma(I)}{I}$ is set to be 0.5%. Although current source with larger overdrive voltage consumes less area, the saturation operation region of all transistors has to be satisfied. Thus, the overdrive voltage $V_{GS} - V_T$ is

set to be 300 mV. Therefore, the size of the transistors in the current source array in Figure 2.5 can be obtained as the table:

Table 2.1: Transistor sizing in the current-steering D/A converter.

$1I_{lsb}$	$2.7\mu/35\mu$
$2I_{lsb}$	$3.6\mu/24\mu$
$4I_{lsb}$	$5.4\mu/17.4\mu$
$8I_{lsb}$	$7.5\mu/12\mu$
$16I_{lsb}$	$10.5\mu/8.4\mu$

2.3.3 Simulation Result

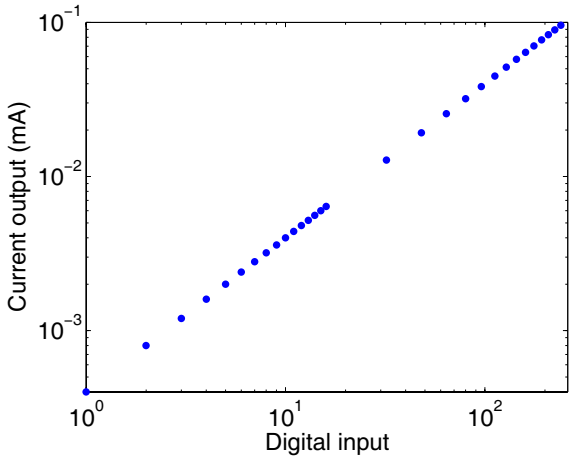


Figure 2.6: Simulated output of segmented current-steering D/A converter.

The segmented current-steering D/A converter is designed under AMI 0.5 μm CMOS technology and simulated in the Cadence Spectre environment. 30 points are selected in the current range from 0 to 100 μA. I_{lsb} for this current range is equal to 400 nA. The output of the DAC is shown in Figure 2.6. Excellent linearity can be observed. The influence of transistor mismatch on the linearity is going to be tested after the fabrication of the converter. The simulated maximum power

consumption of D/A converter complies with the theoretic calculation which is about 367 μ W.

2.4 Incremental $\triangle\Sigma$ A/D Converter

2.4.1 Oversampling A/D Converter

Oversampling occurs when the signals of interest are bandlimited to f_0 and the sample rate is at f_s, where $f_s > 2f_0$. $2f_0$ is the Nyquist rate. The oversampling ratio(OSR) is defined as:

$$OSR = \frac{f_s}{2f_0} \tag{2.15}$$

The quantization noise power of an oversampling ADC can be written as:

$$P_e = \frac{\Delta^2}{12}\frac{1}{OSR}, \tag{2.16}$$

where Δ equals the difference between two adjacent quantization levels. Therefore, doubling OSR decreases the quantization noise power by one-half or equivalently 3 dB.

The system architecture of a delta-sigma oversampling A/D converter is shown in Figure 2.7 [13]. The first stage is a continuous-time anti-aliasing filter and is required to band-limit the input signal to frequencies less than one-half the oversamping frequency, f_s. Following the anti-aliasing filter, the continuous time is sampled by a sample-and-hold module. Then, the hold signal is processed by a delta-sigma modulator, which converts the analog signal into a noise-shaped low resolution digital signal. The last block in the system is a decimator which converts the oversampled digital signal into a high-resolution digital signal at a lower sampling rate. The decimation filter can be conceptually thought of as a low-pass filter followed by a down sampler. In the systems where the delta-sigma modulator is realized with switched-capacitor (SC) circuitry, a separate sample and hold is not reuired, as the continuous time is inherently sampled by the switches and input capacitors of the SC delta-sigma modulator.

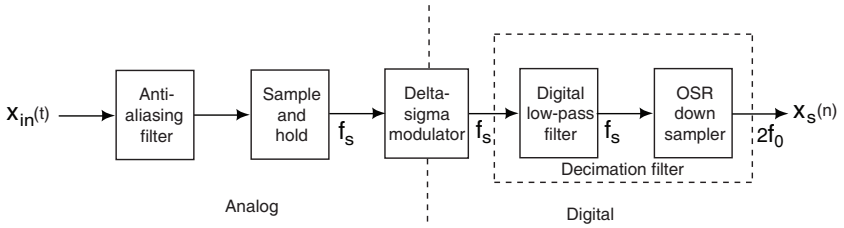


Figure 2.7: Block diagram of an oversampling A/D converter.

2.4.2 Circuit Architecture

The choice of the current-measuring first-order single bit delta-sigma modulator matches the low-frequency content of the signal of interest, which allows high oversampling ratios and trade-off between bandwidth and resolution, and offers additional noise reduction [14]. The incremental delta-sigma ADC used in the system comprises the current integrator, the comparator and the switched-current single-bit D/A converter. The implementation of the integrator and the switched-current DAC is shown in Figure 2.8.

Current Integrator

To achieve high resolution and minimize distortion, the input current is directly integrated onto a capacitor in the feedback loop of a low-noise high-gain voltage amplifier, converting the integrated current into a voltage signal. Since the ADC has two measurement scales for the input current according to the system architecture design, a pair of integrating capacitors C_1' and C_1'' are adopted and selected for difference scale. The choice of their values depend on the input current range and implies a tradeoff between conversion speed and signal-to-noise ratio which will be discussed in section 2.4.4.

Correlated double sampling (CDS) establishes the voltage at the virtual ground input to the integrator though a coupling capacitor C_2 inserted in between the integrator input and the inverting amplifier. The capacitor C_2 samples the difference between the inverting amplifier offset voltage and the externally supplied voltage

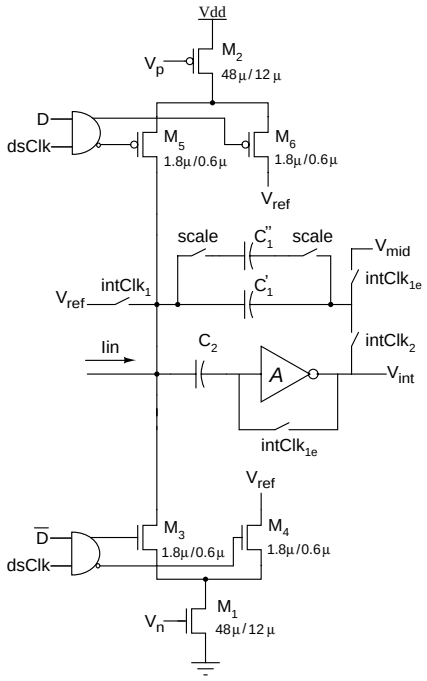


Figure 2.8: Schematic of delta–sigma current integrator with switched-current single-bit DAC.

reference V_{ref} at the beginning of the conversion cycle, activated by the $intCLK$ clock signal. The capacitor C_2 is chosen to be 1 pF to minimize the effect of charge leakage over the duration of the conversion cycle.

The high-gain amplifier is implemented as a low power, single ended, telescopic cascode amplifier. The design of this single stage inverting amplifier is shown in Figure 2.9. For highest energy efficiency, the amplifier is biased on the edge of the subthreshold region, where the amplifier has maximum transconductance to current ratio and low power consumption. The subthreshold operation also provides extended output dynamic range with minimum drain-to-source saturation voltage. The bias current of the amplifier is set to the minimum value that accommodates adequate slew rate relative to the sampling frequency. When the bias current is 250 nA with 1 pF load capacitance and 3.3 V supply, the simulated open-loop DC gain of amplifier is 90dB, the unity gain bandwidth is 900

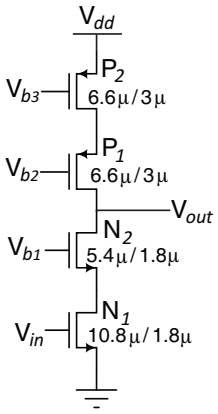


Figure 2.9: Schematic of cascode inverting high-gain amplifier.

KHz and the phase margin is 94 degree. The high gain guarantees the immobility of the virtual ground and large phase margin stabilizes the output integrated voltage.

Current Feedback DAC

Single-bit D/A conversion and duty-cycle modulation in the delta-sigma modulator feedback loop are implemented by a switched current circuit comprising transistors M_1 to M_6. This part of circuit functions as a D/A converter because its input is a digital value from the comparator while its output is an analog current with opposite directions. The switched currents feed directly into the input node where they are integrated along with the input current. The current source transistors M_1 and M_2 are biased with V_p and V_n which are set with an identical external supplied current reference I_{ref}. Therefore, the tail currents they generate at the input node is $\pm I_{ref}$. M_1 and M_2 are sized with large width and length to improve matching between reference currents across channels. Transistors M_3 to M_6 are implemented as minimum-size switches to direct the reference current either into the integrator or to a shunting path at the same reference voltage level V_{ref}. As a result, the current source M_1 and M_2 are always active and their drain voltage is maintained at V_{ref} to decrease the effect of charge injection noise at the integrator

input. The shunting of the current can also be controlled by the duty cycle clock, $dsClk$, which helps to realize the gain modulation.

Comparator

Single-bit quantization in the delta-sigma modulator is implemented by the comparator shown in Figure 2.10. The comparator is reset at the beginning of each integration cycle when clock $intClk1$ is active and coupling capacitor C_3 samples the mid level voltage V_{mid}. The sampling capacitor C_3 is chosen to be 1 pF. In the conversion phase, when $intClk1$ is low, the difference between integrator output voltage V_{int} and V_{mid} is amplified to V_{dd} or 0 by a high-gain cascode inverting amplifier with the same architecture in Figure 2.9. Then the result of comparison is latched on the falling edge of $dsClk$ in the D flip-flop.

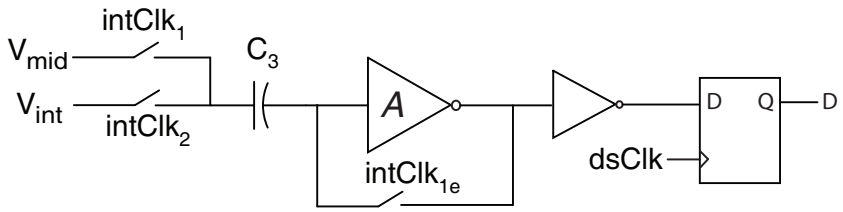


Figure 2.10: Schematic of comparator as a single-bit quantizer in the delta–sigma modulator.

Decimator and Output

The decimator is implemented as the simple accumulate-and-dump circuit. The output bits of delta-sigma modulator that represent logic one are counted every $dsClk$ using a 13-bit counter during one conversion period which is controlled by $intClk$. At the end of each conversion cycle, the counter value is written to output register and a new conversion cycle begins with cleared counter. The register can be read asynchronously by DSP at any time during conversion cycle. The digital data can be readout through parallel 13 wires or shifted by a parallel-serial converter then output through one wire in 13 clock cycles.

2.4.3 Clock Timing Analysis

First of all, the timing of all clocks is generated from a system clock $sysClk$ at sampling rate f_s, nominally 2 MHz. The digital gain modulation clock $dsClk$ is used to control the shunting of the feedback current. When $dsClk$ is high, one polarity of reference current is injected into the integrating node depending on the quantization bit from comparator. When $dsClk$ is low, both currents are diverted to the shunting path and cancel onto the V_{ref} node. $dsClk$ is active for a single cycle in every G cycles, at a rate f_s/G. It also clocks the counter in the decimator. The decimated output is available after OSR cycles of $dsClk$, at a conversion rate $f_s/(G \times OSR)$. From the integrator clock, $intClk$, non-overlapping clocks $intClk_1$ and $intClk_2$ are derived. The clock $intClk_{1e}$ is the replica of $intClk_1$ with rising edge following the rising edge of $intClk_1$ but falling edge preceding the falling edge of $intClk_1$ to prevent the charge injection from the switch across the integrator. Example clock signals are illustrated in Figure 2.11. It can be observed that digital gain $G = 3$ and oversampling ratio $OSR = 4$.

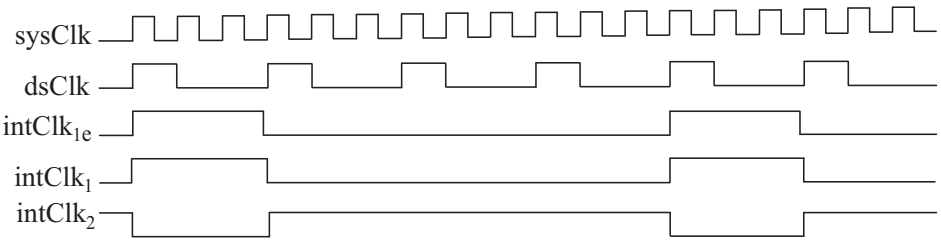


Figure 2.11: Illustration of clock timing sequence.

2.4.4 Performance Analysis

Range and Resolution

The delta-sigma A/D converter resets the integrator at the beginning of each conversion period. At time nT from reset, with $T = G/f_s$ which is the period of

$dsClk$, the integrator output voltage V_{int} can be calculated as:

$$V_{int}[n+1] = V_{int}[n] + (I_{in} - D[n]\frac{I_{ref}}{G})\frac{T}{C_1}, \tag{2.17}$$

where $D[n]$ is the current I_{ref} direction (-1 or $+1$) controlled by the comparator output at time nT with initial conditions $V_{int}[0] = V_{mid} = 0$ and $D[0] = -1$. At the end of the conversion period, after OSR numbers of integration cycles, the integrator voltage reaches its final value as:

$$V_{int}[OSR] = (OSR \times I_{in} - \sum_{i=1}^{OSR-1} D[i]\frac{I_{ref}}{G})\frac{T}{C_1}, \tag{2.18}$$

Therefore, the input current I_{in} (or its average over the integration interval) decomposes into two terms as:

$$I_{in} = \sum_{i=1}^{OSR-1} D[i]\frac{I_{ref}}{G \times OSR} + \frac{V_{int}[OSR]}{OSR}\frac{C_1}{T}, \tag{2.19}$$

where the first term represents the decimated output and the second term represents the quantization error. The decimated output term defines the LSB resolution of the input current as:

$$I_{lsb} = \frac{2I_{ref}}{G \times OSR} \tag{2.20}$$

A constant of 2 has to be added because the values of $D[i]$ are "± 1" instead of "0" and "1". The resolution is thus determined by the reference current I_{ref} scaled by both the digital gain and the oversampling ratio. When $D[i]$ are all "1", their superposition equals to OSR. Consequently, the maximum input current is I_{ref}/G. The same calculation can be made when $D[i]$ are all "-1". Therefore, the input current range is $2I_{ref}/G$. It is worth noting the input range is not related to the oversampling ratio but only scaled by digital gain. The conversion frequency is simply obtained as:

$$f_{conv} = f_s/(G \times OSR), \tag{2.21}$$

which implies a linear tradeoff between resolution and conversion bandwidth.

According to (2.18), when an LSB change in the quantized output, the change of integrated voltage equals:

$$V_{range} = 2\frac{I_{ref}T}{GC_1} = 2\frac{I_{ref}}{f_s C_1}, \tag{2.22}$$

By combining (2.20) and (2.22), the relation between resolution and integrated capacitor can be obtained as:

$$I_{lsb} = f_{conv} C_1 V_{range}, \tag{2.23}$$

To simplify the clock management, the gain modulation stays as 1 in the prototype ASIC design. For the two scales of A/D converter, the sample frequency, f_s, is the system input clock which is set as 2 MHz. The 13-bit ADC decides the oversampling ratio should be 2^{13}. Then the conversion frequency of the ADC can be calculated according to (2.21) as about 245 Hz.

According to the analysis in 2.2.2, I_{lsb} of ADC are 9 pA and 2.85 nA. Considering the charge loss and system stability, the integrating capacitance across the Op Amp can't be either too large or too small. As a result, C_1' is chosen to be 100 fF and C_1'' is chosen to be 6 pF. Based on (2.23), the integrating voltage range for $I_{lsb} = 9pA$ is $\pm$350 mV and the voltage range for $I_{lsb} = 2.85nA$ is $\pm$2V. The current reference of the ADC is simply $OSR/2$ times of the I_{lsb}.

Noise Analysis

The main noise sources of the A/D converter are the amplifier in the integrator and the reference current source. The noise model of the amplifier is usually represented by its input transistor. The thermal noise of the input transistor operated in subthreshold is approximately equal to the shot noise which can be calculated as:

$$v_{amp,th}^2 = \frac{2qI_d}{g_m^2}\Delta f = \frac{2qI_d}{(\frac{I_d}{nV_T})^2}\Delta f = \frac{2qV_T^2 n^2}{I_d}\Delta f, \tag{2.24}$$

where $V_T = kT/q$ is the thermal voltage, n is the slope coefficient, I_d is the drain current of the transistor and Δf is the bandwidth of the amplifier. The contribution of the flicker noise is reduced by the effect of correlated double sampling as it imposes a zero at the origin of frequency [15]. The reference current noise is given by thermal noise from the current sources M_1 and M_2 in Figure 2.8. Since they are operated in strong inversion, their current thermal noise is calculated as:

$$i^2_{ref,th} = \frac{2}{3} 4kTg_m\Delta f \tag{2.25}$$

The flicker noise contributed by M_1 and M_2 is negligible as their large transistor area.

Since the noise from integrator and current source is evaluated at the decimated output at last. According to (2.19), the effect of integrator noise in the digital output merely amounts to a voltage deviation which is even smaller than one LSB, while noise from the reference current which is directly integrated on C_1 is able to affect the decimated output. Therefore, this input referred current noise becomes dominant. By superimposing the noise contribution of each cycle over approximately f_s bandwidth, the total noise power of A/D converter is given by:

$$i^2_{in,n} = \sum_{i=1}^{OSR-1} \frac{i^2_{ref,th}}{G^2 OSR^2} \approx \frac{8}{3} \frac{kTI_{lsb}f_s}{V_{ov}G} \tag{2.26}$$

It is worth noting that if the conversion frequency and the least significant bit of input current are kept same, the advantage of larger gain modulation is improving the signal-to-noise ratio. However, the cost is the increase of the power consumption which will be analysed in the following paragraphs.

Power Consumption

For a hand-held gas sensor facility, power consumption is a very important limiting factor. The approximate power of the whole A/D converter is given by:

$$Power = 2I_{ref}V_{dd} + 2I_dV_{dd} + \frac{1}{G}f_{conv}C_{dec}V_{dd}^2, \tag{2.27}$$

where the first term accounts for the reference current source, the second terms corresponds to the integrator and comparator amplifiers and the last term is the dynamic power of the decimator with equivalent internal capacitive load C_{dec}. According to (2.20) and (2.23), the first term reduces to $G(OSR)C_1f_{conv}V_{range}V_{dd}$. Assume the bias current of the amplifier is just large enough to push the integrated voltage equal to V_{range} in one $dsClk$ cycle, the power consumption can be rewritten as:

$$Power = G\,OSR\,f_{conv}C_1V_{range}V_{dd}(1 + \frac{2}{G}) + \frac{1}{G}f_{conv}C_{dec}V_{dd}^2 \tag{2.28}$$

It can be observed that gain modulation reduces the power consumed by the counter at the cost of larger power of integrator. However, the digital power is usually negligible compared with the analog counterpart. Therefore, the gain modulation suppresses the noise contribution at the expense of power. Moreover, both high resolution and fast conversion rate boost the power dissipation which corresponds with the common sense.

2.4.5 Simulation Result

To verify the design and the current sensitivity, the 13-bit delta-sigma A/D converter is simulated using Cadence Spectre simulator. The scale with 9 pA LSB current is selected with the input current range form -18 nA to 18 nA. The integral nonlinearity error is shown in the Figure 2.12.

As to the power consumption, the scale with I_{lsb} equal to 2.85 nA is simulated. The power of ADC is approximately 21 μW. As demonstrated in Figure 2.4, the

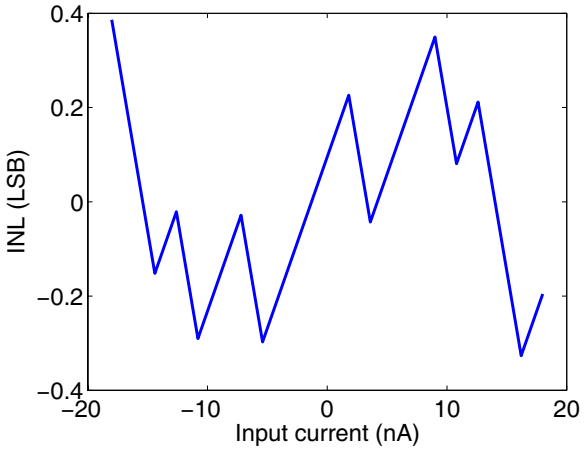


Figure 2.12: Simulated integral nonlinearity (INL) of the incremental $\Delta\Sigma$ A/D converter.

power consumed in the sensor is limited to less than 12 μW for the lowest possible sensor resistance, while the power consumption of the current-steering D/A converter is up to 367 μW which plays an dominant role. As a result, the maximum system power consumption could be 400 μW which is constrained by the current DAC.

2.5 Implemented ASIC

2.5.1 Board Level Verification

In order to conduct the functional verification of the design before ASIC tape out, board level systems based on commercial chips are fabricated. A single channel gas sensing system with Bluetooth data transmission module is shown in Figure 2.13. Another three-channel gas sensing board based on PCI data acquisition (DAQ) card is shown in Figure 2.14. They are both composed with 5-bit D/A converter and 16-bit A/D converter. The output current from the gas sensor is converted to voltage mode and amplified with a programmable voltage gain realized by an Op Amp and a resistance array to cover the large dynamic range. Micro-controller is used to generate data protocol and adjust the voltage gain.

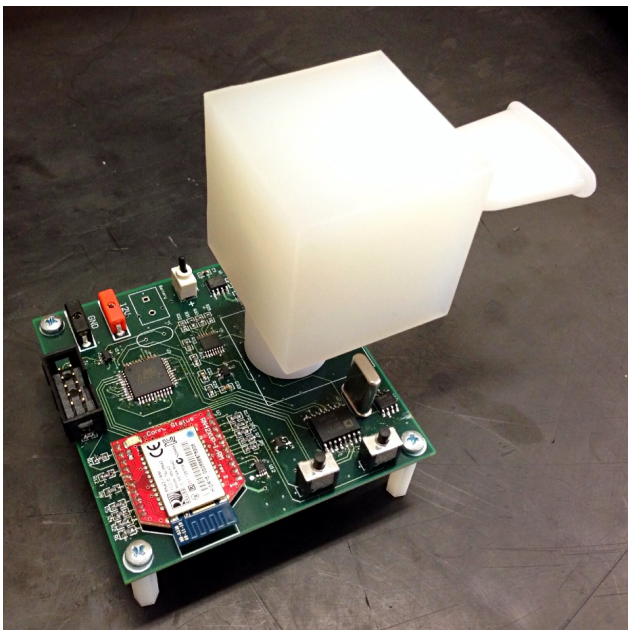


Figure 2.13: Board level gas sensing system with Bluetooth module.

The sensor resistance is randomly chosen for testing. The output of the ADC is sampled once every second and calculated to the sensor resistance. A 100 seconds

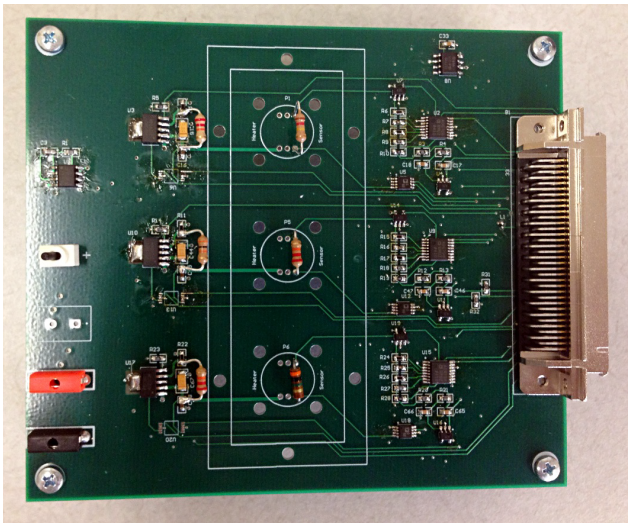


Figure 2.14: Board level three-channel gas sensing system with PCI DAQ.

measurement result of the test board is shown in Figure 2.15. It can be obtained that the standard deviation of the measurements is about 0.067%.

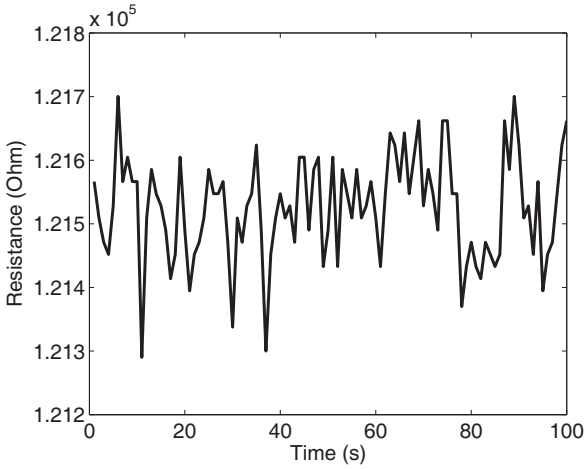


Figure 2.15: Measured resistance of the gas sensor.

2.5.2 ASIC Implementation

The implemented gas sensing ASIC is fabricated through AMI 0.5 μm CMOS technology [16]. The layout of the chip is shown in Figure 2.16.

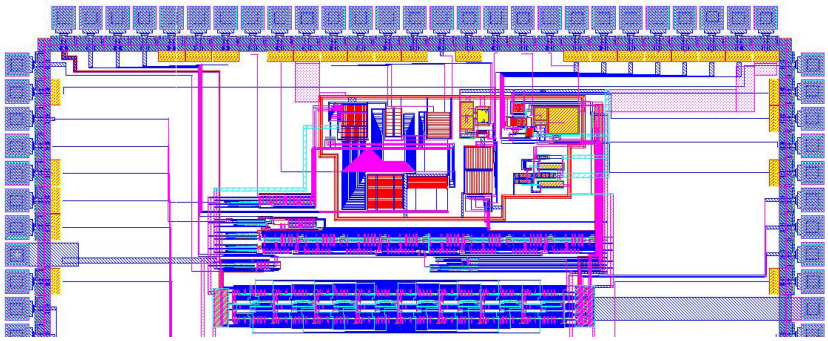


Figure 2.16: ASIC layout of gas sensing system in 0.5 μm technology.

Chapter 3

Readout Circuit for Radiation Detection System

3.1 Radiation detector

Radiation detectors, also know as particle detectors, are adopted to detect, track or identify high-energy particles and measure the energy of the radiation. The radiation of interest may include charged particles like fast electrons and uncharged particles like neutrons, X-rays and gamma-rays. When the radiation energy is high enough to ionize the sensing material in the detector, free charges will be generated. The charges may be single polarity like electrons or dual polarity like electron-hole pairs. As the amount of the free charges are proportional to the radiation energy, to read out the charge, Q, provides an accurate measurement of the radiation energy.

A radiation detector usually has more than two electrodes. By applying a voltage on one side and a common electrode on the opposite side, an electric field can be built in the detector. Under this electric field, the ionized particles are induced to move and generate a current flow. In this way, the detector can be modeled as a current source which generates a current pulse in a very short time and a parallel parasitic capacitor C_{DET}. On the other hand, the detector may have a continu-

ous constant leakage current, I_{leak}, due to the semiconductor material component inside. As a matter of fact, to satisfy the measurement accuracy of contemporary radiation detector, a strict requirement is imposed on the performances of its front-end readout circuit including signal-to-noise ratio, dynamic range, linearity, stability and etc.

Numerous readout ASICs for radiation detection based on different sensors and applications are studied and reported [17]-[26]. However, most of the systems achieving low ENC are developed with relatively small sensor capacitance [17, 18]. The large input sensor capacitance always obstruct the readout circuit to achieve high sensitivity. A readout circuit for CdTe and CdZnTe X-Ray detectors with 20 pF input capacitance is observed with minimum ENC of 900 electrons [19]. A readout integrated circuit for avalanche photo diodes obtains an ENC as 275 electrons plus 10 electrons for every additional pico-farad of the input capacitance [20]. [21] is able to suppress ENC under 100 electrons when there is no input capacitance, but noise raises still too fast along with the increasing of the capacitance. An impressive front-end ASIC for a silicon Compton telescope with 30 pF input capacitance is implemented and achieves 200 electron ENC in [22], but its power consumption is still a concern. [23] has small power at μW order, but the noise is larger than 500 electrons without any input capacitor. Therefore, to achieve high sensitivity without dissipating large power is a challenging work in the design of front-end ASIC.

The radiation detector used in the proposed system is a semiconductor scintillating solid-state detector array with integrated epitaxial photodiode on the body of scintillator, illustrated in Figure 3.1. Its structure guarantees nearly perfect registration of the photons converted from the energy of the incident radiation [27]. Based on the Compton telescope technique, a three-dimensional array of semiconductor scintillator provides an accurate spectroscopic resolution for isotope discrimination and simultaneously an accurate determination of the direction to the source. However, the drawback of this detector array is that the large area of the pixel epitaxial photodiodes leads to an even larger capacitance, measured at

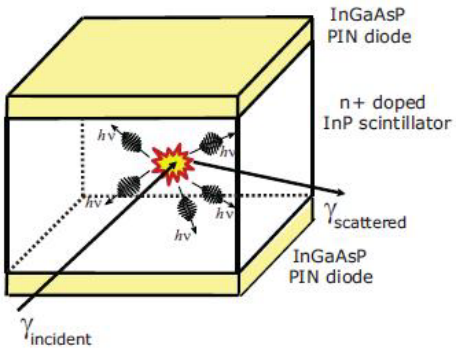


Figure 3.1: Semiconductor scintillator comprising a scintillator body and an integrated photodiodes on top and bottom plates of its surface.

50 pF. Despite the large diode area, the reverse-bias leakage current is rather low, on the order of 10 pA.

Accordingly, careful design of the readout system including charge sensitive amplifier (CSA) and pulse shaper for the proposed detector array is required to optimize the noise under the power and area constraint. Moreover, to obtain the digital value of the output signal, an A/D converter is implemented. We propose implementation of the clock-less ADC to reduce the potential effect of the switching noise on the low-noise CSA.

3.2 System Overview

3.2.1 System Architecture

The radiation detection readout circuit can be implemented in either voltage mode or current mode. In voltage mode, the input current signal is integrated on the detector capacitor, as $V_{in} = Q_{in}/(C_{det})$ and read out with a high input impedance stage, usually a voltage amplifier, which has A times voltage gain. A resistor is added to provide the DC path for the leakage current. The simplified schematic can be seen in the Figure 3.2. In current mode, the input current is directly amplified and read out by a low input impedance stage, a charge amplifier. The charge amplifier is usually composed with a high gain Op Amp, a feedback capacitor and resistor. The simplified schematic can be seen in the Figure 3.3. The AC coupling capacitor is no longer necessary and the leakage current can be provided by the feedback resistor. In this case, a low input impedance stage is preferred, because it guarantees that the sensing node on the detector is biased at a highly stable voltage by creating a virtual ground at that node. On the contrary, the voltage signal may affect the bias of detector during measurement in the high impedance circuit. Therefore, the charge sensitive amplifier(CSA) is chosen in the proposed system.

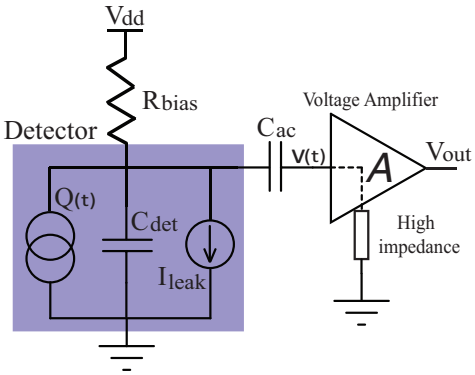


Figure 3.2: High input impedance circuit.

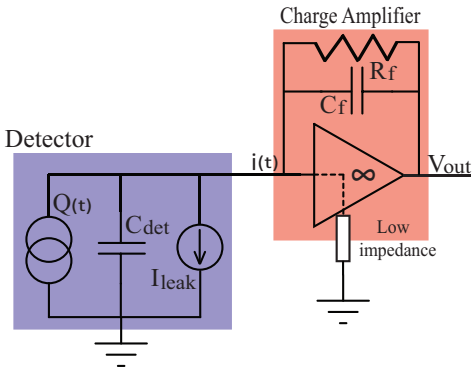


Figure 3.3: Low input impedance circuit.

The current signal coming out of the detector lasts for a very short time due to the event driven electron ionization, the input of the CSA can be modeled as a Dirac current pulse. Although limited by the bandwidth of the amplifier, the rising time of V_{out} in Figure 3.3 is till close to a voltage step equal to Q_{in}/C_f. There are three reasons we need a pulse shaper after CSA to control the bandwidth of the circuit. First of all, limited bandwidth effectively suppresses the output noise and boosts signal-to-noise-ratio. Secondly, a pulse shaper restricts the output pulse width to prevent signal distortion caused by the upcoming event in a moderate or high event trigger environment. At last, the pulse amplitude of interest is easy to read out when the pulse has a relatively slow rising edge. Therefore, the pulse shaper is important in a radiation detection system.

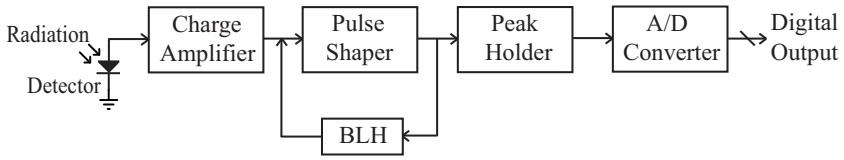


Figure 3.4: Block diagram of radiation detection system.

The overall system architecture can be seen in Figure 3.4. A baseline-holder (BLH) module is adopted across the shaper to stabilize the DC baseline voltage of the output. After the pulse shaper, the amplitude of signal is hold for reading by the peak detector. In the end, an analog-to-digital converter(ADC) converts the captured peak voltage to a digital value which indicates the intensity of radiation.

3.2.2 Noise Analysis

Low noise is always the major concern in the design of a radiation detection system. Instead of signal-to-noise-ratio, the resolution of current mode front-end electronics is usually expressed in terms of Equivalent Noise Charge(ENC) [28]. ENC is defined as the amount of charge that the detector must release to make the signal amplitude equal to the integrated rms noise at the output of readout circuit. To obtain the ENC, the output noise has to be calculated first.

The dominant noise sources in the system includes shot noise of radiation detector as well as thermal and flicker noise of CSA. Without loss of generality, these noise sources can be separated into series noise and parallel noise when looking into the input node of CSA. If the transfer function of the following circuity is $H(f)$, the output noise power contributed by the parallel noise source can be calculated as:

$$v_{ni}^2 = \int_0^\infty S_i |H(f)|^2 \, \mathrm{d}f, \tag{3.1}$$

where S_i is the power spectre density(PSD) of the parallel noise. According to the Thevenin Norton Equivalent theorem, the series noise source can be transformed into parallel noise by dividing the equivalent impedance. The equivalent impedance is the input capacitor at the node including detector parasitic capacitance, amplifier parasitic capacitance and feedback capacitance. Therefore, the output noise power contributed by the series noise source can be calculated as:

$$v_{nv}^2 = \int_0^\infty \frac{S_v |H(f)|^2}{|Z|^2} \, \mathrm{d}f = \int_0^\infty S_v \omega^2 C_{in}^2 |H(f)|^2 \, \mathrm{d}f \tag{3.2}$$

As mentioned in last section, the output of CSA is approximately a voltage step whose amplitude is Q_{in}/C_f. Accordingly, ENC can be calculated as:

$$ENC = \frac{v_n}{V_{o,max}} Q_{in} = \frac{\sqrt{\int_0^\infty S_i |H(f)|^2 + S_v \omega^2 C_{in}^2 |H(f)|^2 \, \mathrm{d}f}}{\frac{1}{C_f}} \tag{3.3}$$

To get the information about the CSA transfer function, fourier transform is applied to the output, the output in frequency domain is:

$$V_o(f) = F(\frac{Q_{in}}{C_f} \Phi(t)) = \frac{Q_{in}}{j 2\pi f C_f} \tag{3.4}$$

Since the input is Q_{in}, the transfer function of CSA is equivalent to:

$$H_{CSA}(f) = \frac{1}{j2\pi f C_f} \tag{3.5}$$

Considering the noise source, the series noise can be separated in to series white noise and series flicker noise. Both series noise come from transistors composing the CSA and they are uncorrelated, so $S_v = S_{vw} + S_{vf}$. On the other hand, the parallel noise is merely the shot noise from the sensor leakage current which is also white. Thus, parallel low frequency noise is neglected here. It is known that white noise is a random signal with a flat power spectre density and flicker noise is approximately linear relationship inverse of frequency. As a result, the integral of ENC can be obtained as:

$$ENC^2 = S_{iw}\frac{1}{4\pi^2}\int_0^\infty \frac{1}{f^2}\,\mathrm{d}f + C_{in}^2(S_{vw}\int_0^\infty \mathrm{d}f + S_{vf1}\int_0^\infty \frac{1}{f}\,\mathrm{d}f) \tag{3.6}$$

S_{vf1} is the series flicker noise power spectre density at 1Hz. It is obvious that for all three terms, the integral goes to infinity instead of converging. Although in the real case, the output noise of CSA can't be infinity because of limit bandwidth of Op Amp, the huge ENC is still unacceptable. Therefore, the pulse shaper stage is quite necessary. For example, the transfer function of a shaper with n coincident poles is:

$$H_{nShaper}(f) = \frac{A_0\tau}{(1 + j2\pi f\tau)^n} \tag{3.7}$$

τ is the time constant of the pulse shaper and A_0 is the gain. The impulse response of this shaper follows:

$$h_{nShaper}(t) = (\frac{t}{\tau})^{n-1}\frac{H_0}{(n-1)!}e^{-\frac{t}{\tau}} \tag{3.8}$$

It's easy to find that $h(t)$ has its maximum when $t = (n-1)\tau$. The ENC of the

system with n^{th} order shaper can be recalculated as:

$$ENC^2 = \frac{S_{iw}\int_0^\infty \frac{A_0^2\tau^2}{(1+\omega^2\tau^2)^n}\,\mathrm{d}f + S_{vw}C_{in}^2\int_0^\infty \frac{A_0^2\omega^2\tau^2}{(1+\omega^2\tau^2)^n}\,\mathrm{d}f + S_{vf1}C_{in}^2\int_0^\infty \frac{A_0^2\omega^2\tau^2}{(1+\omega^2\tau^2)^n}\,\mathrm{d}f}{h_{max}^2} \tag{3.9}$$

Assume the arbitrary time constant τ as the pulse peaking time τ_p which is the time required to rise from 1% of the peak amplitude to the peak. Assume $x = \omega\tau_p$ and use substitution. The integral can be simplified as:

$$ENC^2 = \frac{S_{iw}\frac{\tau_p}{2\pi}\int_0^\infty \frac{1}{(1+x^2)^n}\,\mathrm{d}x + S_{vw}\frac{C_{in}^2}{2\pi\tau_p}\int_0^\infty \frac{x^2}{(1+x^2)^n}\,\mathrm{d}x + S_{vf1}C_{in}^2\int_0^\infty \frac{x}{(1+x^2)^n}\,\mathrm{d}x}{h_{max}^2/A_0^2} \tag{3.10}$$

This equation gives a general idea on the ENC of a radiation detection system with a pulse shaper. It is worth noting that the ENC doesn't converge until the order number of shaper, n, is two or larger. It can also be seen that ENC increases with the circuit and detector noise. Another important observation is that large superposition capacitance at the input node may cause severe ENC deterioration by affecting the series noise terms. Therefore, optimization process is quite necessary to find a possible minimum ENC value. The calculation of PSD function S_{iw}, S_{vw}, S_{vf1} as well as the discussion about the shaper order and peaking time selection will be introduced in the following ENC optimization sections.

3.3 ENC Optimization

3.3.1 Input Transistor ENC Calculation

In a properly designed low-noise amplifier, the dominant noise originates from the input transistor. Therefore, input transistor optimization plays an important role in the readout circuit design. The noise source of the input transistor is shown in Figure 3.5. The noise source on the left is in current mode and on the right in

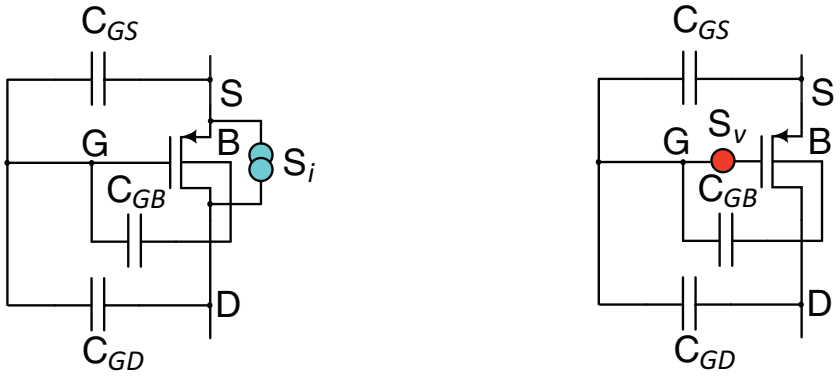


Figure 3.5: Noise source diagram of input transistor.

voltage mode. The power spectre density of S_i can be expressed as:

$$S_i = \gamma n 4kT g_m, \tag{3.11}$$

where γ and n are coefficients which will be discussed later. g_m is the transconductance of the input transistor. The flicker noise is not concerned here. According to the the Thevenin-Norton theorem, voltage mode noise is equal to:

$$S_v = \gamma n \frac{4kT}{g_m} \tag{3.12}$$

It's easy to see that large transconductance is helpful in suppressing the input noise. As we all know, a transistor has different parameter models when it is biased in different region of operation. In order to pick up the suitable model, we need to

decide how to bias the input transistor in the first place. The term of inversion coefficient (IC) [29] is usually used to determine the bias extent of the transistor.

$$IC = \frac{I_D}{2n\mu C_{OX} V_T^2 \frac{W}{L}}, \tag{3.13}$$

where I_D is the drain current, n is the slope factor, μ is the low-field mobility, C_{OX} is the gate oxide capacitance, V_T is the thermal voltage, W and L are the effective channel width and length respectively. When $IC > 10$, the transistor is in strong inversion. When $IC < 0.1$, the transistor is in weak inversion. Considering the low power design constraint, the power consumption of CSA is chosen to be no larger than 1mW. We use 0.5μm CMOS technology, V_{dd} is 3.3V. Then the drain current of input transistor has to be smaller than 300μA. Intuitively, larger current can increase g_m and results in smaller thermal noise of input transistor without any impact on low frequency noise. Therefore, we choose the largest affordable current, 300μA, as the drain current of input transistor.

When biased in strong inversion, the input transistor transconductance is:

$$g_{m,strong} = \sqrt{2 I_D \mu_0 C_{OX} \frac{W}{L}} \tag{3.14}$$

Introduce (3.13) into (3.14), the transconductance can be rewritten as:

$$g_{m,strong} = \frac{I_D}{V_T \sqrt{nIC}} \tag{3.15}$$

On the other hand, when biased in weak inversion, the input transistor transconductance is:

$$g_{m,weak} = \frac{I_D}{nV_T} \tag{3.16}$$

To guarantee the transistor in strong inversion, IC has to be larger than 10, meanwhile, n is close to 1. By comparing (3.15) and (3.16), it can be seen that the thermal noise PSD in strong inversion has to be at least 3 times larger than in weak inversion. Moreover, in spite that the lower W/L ratio in strong inversion under

the same bias current takes advantage at smaller input capacitance, it increases the flicker noise as well. Therefore, in a system with low power constraint, input transistor biased in strong inversion does not offer the best ENC performance.

To keep the transistor stay in the weak inversion, its size ratio, W/L, has to be larger than 4.67×10^4, which means, when length is as small as 4λ, width has to be larger than 56 mm. This is obviously an unacceptable size in area consideration and the input capacitance becomes overflow. Consequently, the operation region between the strong and weak inversion is an efficient choice to obtain good performance in both ENC and power consumption, this region is called moderate inversion.

An advance and relatively accurate model for transistors in moderate inversion is extracted based on the EKV model [30, 31, 32]. First of all, the transistor thermal noise power spectre density is written as:

$$S_{vw} = \alpha_W n\gamma(I_{DW}, L)\frac{4kT}{g_{mW}(I_{DW}, L)W}, \tag{3.17}$$

$$n \approx \frac{g_m + g_{mb}}{g_m}, \tag{3.18}$$

$$\gamma \approx \frac{1}{1+IC}(\frac{1}{2} + 2IC3), \tag{3.19}$$

$$g_{mW} \approx \frac{I_{DW}}{nV_T}(\frac{\sqrt{1+4IC}-1}{2IC}), \tag{3.20}$$

where α_W is the excess noise coefficient, n is the subthreshold slope coefficient, I_{DW} is the drain current per unit of W, g_{mW} is the transconductance per unit of W and IC is the inversion coefficient in Equation (3.13). The transistor flicker noise power spectre density can be written as:

$$S_{vf} = \frac{K_f(L)}{C_{OX}WLf^{\alpha_f}}, \tag{3.21}$$

where coefficient $K_f(L)$ depends on L and the slope depends on the coefficient $\alpha(f)$. The non-1/f slope requires a modification of the integral in Equation (3.10).

The model of gate capacitance which is included in C_{in} is re-estimated by considering the overlap components as well as the operation region of the transistor. The gate capacitance per unit of W is written as:

$$C_{GW} \approx 2C_{OV} + C_{OX}L(\gamma_C(I_{DW}) + \frac{(n-1)(1-\gamma_C(I_{DW})}{n}), \tag{3.22}$$

$$\gamma_C \approx (\frac{3}{2} + \frac{1}{3}\frac{\sqrt{1+4IC}+1}{IC^2})^{-\frac{2}{3}}, \tag{3.23}$$

The power spectre density of the parallel white noise is the shot noise caused by the leakage current of the detector. It can be simply written as:

$$S_{iw} = 2qI_{leak} \tag{3.24}$$

Therefore, introducing (3.17), (3.21), (3.22) and (3.24) in (3.10), the new ENC result follows:

$$ENC^2 = (C_{det} + C_{GW}W)^2[\frac{a_W}{\tau_p}\frac{\alpha_W n\gamma 4kT}{g_{mW}W} + a_f\frac{(2\pi)^{\alpha_f}}{\tau_p^{1-\alpha_f}}\frac{K_f}{C_{OX}WL}] + a_p\tau_p 2qI_{leak}, \tag{3.25}$$

$$a_W = \frac{\int_0^\infty |H(x)|^2x^2\,\mathrm{d}x}{2\pi h_{max}^2},\ a_f = \frac{\int_0^\infty |H(x)|^2x\,\mathrm{d}x}{2\pi h_{max}^2},\ a_p = \frac{\int_0^\infty |H(x)|^2\,\mathrm{d}x}{2\pi h_{max}^2}, \tag{3.26}$$

where the coefficients a_W, a_f, a_p only depend on the order and type of the pulse shaper. It is worth noting that in Equation (3.25), for a selected channel length, ENC can be optimized just by modification of W and τ_p. The appearance of two parameters in both numerator and denominator suggests the possibility of the existence of minimum ENC. By sweeping the acceptable values of W and τ_p and observing the tendency of ENC, the minimum can be found easily. However, before that, we need to take a close look at the coefficients decided by the pulse shaper.

3.3.2 Shaper Type and Peaking Time

Generally speaking, the shaper can be realized using time-variant solution with switch-controlled integrator or via time-invariant solution. A time invariant shaper is more suitable in the front-end electronic because there is no switch activity in the circuit to jeopardize the signal-to-noise ratio. Time invariant shapers are separated into several types according to the poles number, types and positions. First of all, the number of poles, n, defines the order of a shaper. As proved in (3.3), the order of the shaper has to be higher than two to guarantee the convergence of the charge amplification system output noise. Secondly, if the profile of a shaper is always positive, it is called a unipolar shaper. On the contrary, if a shaper has both positive and negative profile, it is a bipolar shaper. The positive part area of a bipolar shaper is equal to its negative part area. This zero-area characteristic provides bipolar shapers better stability of the output baseline, especially at high event rate. However, compared with unipolar shaper, bipolar shaper has obviously worse signal-to-noise ratio performance. At last, a shaper can have n real coincident poles to make it a real shaper or a specific combination of real and complex conjugate poles to make it a complex shaper. The transfer functions of real shapers and complex shapers are as follows [33]:

$$T(s) = \frac{1}{(s+p)^n} \qquad r - shaper, n \geq 2, \tag{3.27}$$

$$T(s) = \frac{1}{(s+p_1)\prod_{i=2}^{(n+1)/2}[(s+r_i)^2 + c_i^2]} \quad c - shaper, n = 3, 5, 7..., \tag{3.28}$$

$$T(s) = \frac{1}{\prod_{i=1}^{n/2}[(s+r_i)^2 + c_i^2]} \qquad c - shaper, n = 2, 4, 6..., \tag{3.29}$$

For complex shaper, r_i and c_i are the real and complex conjugate parts of the roots of the equation $\frac{1}{0!} - \frac{s^2}{1!} + \frac{s^4}{2!} + ...\frac{s^{2n}}{n!} = 0$. The real shapers and complex shapers are designed with these transfer function to make them "semi-Gaussian" as with

the increase of order number, n, the shaper output tends to approximate a Gaussian curve. The semi-Gaussian shaper has already been proven to be a optimum choice of pulse shaper for radiation detection application [34, 35, 36].

In addition to the types, shapers are also characterized by specific time parameters, especially the peaking time τ_p and the width τ_W. τ_p is the time required to rise from 1% of the peak amplitude to the peak. It can be adjusted to minimize the ENC according to (3.25). τ_W is the time required to go from 1% back to 1% of the peak amplitude, which determines how high the event rate can be without degrading the accuracy. From (3.26), coefficients a_W, a_f, a_p as well as the ratio τ_W/τ_p are all set when the shaper is chosen. Their approximate values are concluded in the table shown in Figure 3.6[30]:

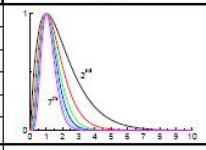
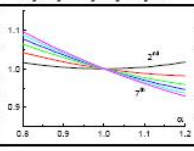
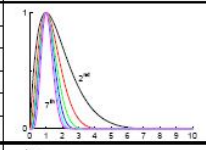
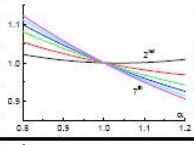
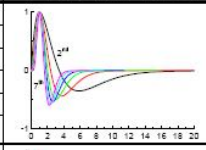
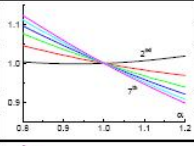
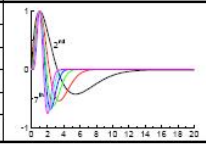
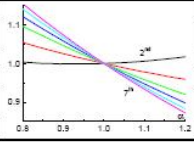
Filter	Shape	a_w	$a_f(1)$	a_p	$\rho_f(\alpha_f)=a_f(\alpha_f)/a_f(1)$	τ_w/τ_p	$-\rho_p$	η_p	λ_p
RU-2		0.92	0.59	0.92		7.49	0.98	-	-
RU-3		0.82	0.54	0.66		5.04	1.85	0.30	1.64
RU-4		0.85	0.53	0.57		4.17	2.50	0.44	1.60
RU-5		0.89	0.52	0.52		3.72	3.01	0.52	1.60
RU-6		0.92	0.52	0.48		3.46	3.40	0.57	1.61
RU-7		0.94	0.51	0.46		3.28	3.74	0.61	1.62
CU-2		0.93	0.59	0.88		6.17	1.05	-	-
CU-3		0.85	0.54	0.61		3.92	2.07	0.31	1.59
CU-4		0.91	0.53	0.51		3.16	2.95	0.48	1.57
CU-5		0.96	0.52	0.46		2.84	3.65	0.58	1.58
CU-6		1.01	0.52	0.42		2.66	4.22	0.63	1.60
CU-7		1.04	0.52	0.40		2.55	4.71	0.65	1.62
RB-2		1.03	0.75	1.01		16.6	0.34	0.29	-
RB-3		1.11	0.78	0.76		9.87	0.69	0.41	-
RB-4		1.30	0.81	0.66		7.67	0.98	0.47	-
RB-5		1.47	0.85	0.62		6.61	1.20	0.51	-
RB-6		1.61	0.87	0.59		5.96	1.39	0.54	-
RB-7		1.74	0.90	0.57		5.53	1.55	0.56	-
CB-2		1.08	0.80	1.02		12.9	0.47	0.33	-
CB-3		1.27	0.86	0.76		7.29	0.91	0.45	-
CB-4		1.58	0.93	0.67		5.58	1.32	0.52	-
CB-5		1.87	0.98	0.62		4.80	1.66	0.56	-
CB-6		2.10	1.03	0.60		4.39	1.92	0.58	-
CB-7		2.33	1.06	0.57		4.10	2.15	0.61	-

Figure 3.6: Waveforms and coefficients for semi-Gaussian shapers of different order.

It can be observed in the table that under the same shaper order and peaking time, complex shapers returns to baseline faster than real shapers. Under the same shaper order and pulse width, complex shapers rise slower than real shapers.

3.3.3 ENC Simulation and Optimization

With the accurate equation for ENC calculation and all coefficients related to the shaper, the minimum ENC can be obtained by finding the optimal design parameters of the input transistor and shaper. As mentioned in the previous section, to maintain the low power design, drain current of input transistor is set at 300 μA. Channel length of the input transistor is chosen to be 4λ, considering the area constraint. PMOS is used as the input transistor since it has much less flicker noise than NMOS. The shapers with complex conjugate poles are not taken into account because of complexity in realization. The scintillating solid-state detector used in the proposed system leads to 50 pF detector capacitance and 10 pA leakage current.

First of all, a third order shaper is adopted. There are two variables can be tuned to search for the minimum. We sweep the channel width from 30 μm to 30 mm and choose 5 typical values for the peaking time from 1 μs to 100 μs. The simulated ENC result is shown in Figure 3.7. The curves indicate that ENC

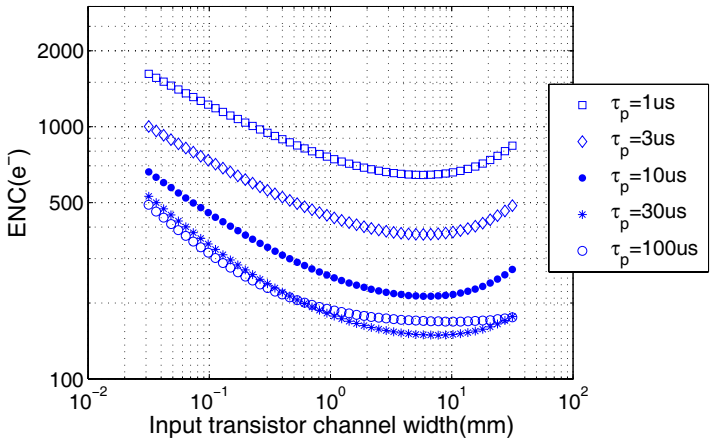


Figure 3.7: Simulated ENC vs different channel width and peaking time.

is suppressed with the increase of channel width and reaches the minimum, then it bounces back again. The same tendency appears when peaking time changes.

ENC drops until peaking time reaches 30 μs and bounces back. It is trivial to prove that minimum ENC exists in this peaking time range. What's more important is that in the peaking time range from 30 to 100 μs, the minimum ENC is obtained when channel width is around 8 mm. This width can be decided as the optimal choice. Recalculate the inversion coefficient in (3.13), $IC = 0.7$ which exactly sets the input transistor in the moderate inversion.

After picking up the width of the input transistor, we set the width to 8 mm and change the shaper order from 2 to 5 and sweep the peaking time from 1 μs to 1 ms. The simulated ENC result is shown in Figure 3.8. It is obvious in the figure that higher order shaper can lower ENC. However, it also shows that the ENC improvement is getting smaller as the order becomes higher. Considering the extra cost of area, power and complexity, to implement a high order shaper is not a promising and worthy effort. Therefore, a third order real poles pulse shaper could be an efficient choice for the proposed system.

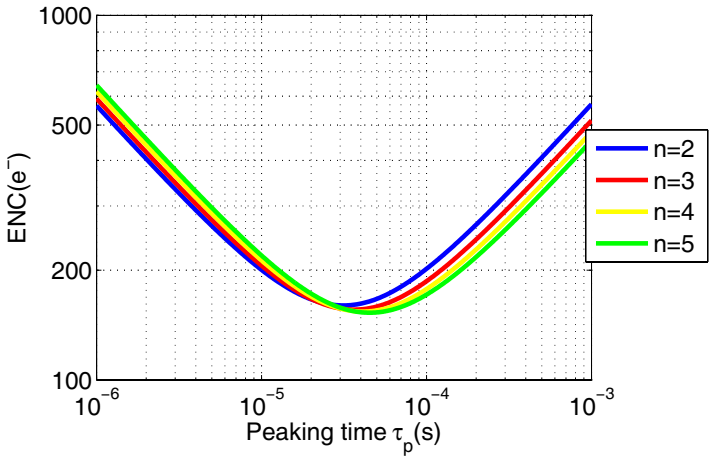


Figure 3.8: Simulated ENC vs shaper order and peaking time for W=8mm.

Figure 3.9 shows the tendency of each term in ENC changes with the peaking time of a third order shaper. Parallel white noise is linearly proportion to the peaking time, while series white noise is opposite. Flicker noise is almost a flat line because coefficient α_f is very close to 1. The contribution of flicker noise is

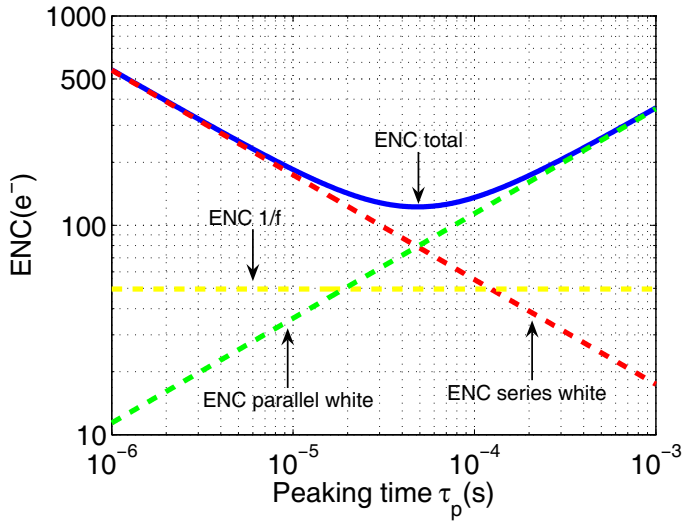


Figure 3.9: Simulated ENC vs peaking time of a 3^{rd} shaper for W=8mm.

much smaller than the thermal noise due to the large size of the input transistor. When parallel white noise is equal to series white noise, the minimum ENC can be obtained. The peaking time at this point is approximately 48 μs. The simulated minimum ENC is about 130 electrons.

3.4 Charge Sensitive Amplifier

A charge sensitive amplifier is composed of a voltage amplifier, a feedback capacitor, reset network and compensation network. By providing a virtual ground at the input node, the amplifier stabilizes the potential of the sensor electrode and converts the charge input to voltage output by integrating the input charge on the feedback capacitor. The block diagram of CSA is shown in Figure 3.3.

3.4.1 Voltage Amplifier

A folded cascode implementation of the high gain voltage amplifier is shown in Figure 3.10. One major advantage of the folded cascode amplifier is the bias current of output branch can be much smaller than the input branch. A higher current through input transistor achieve a larger input transconductance, while a lower current through output transistors achieve a larger output resistance. Due to the gain of cascode Op Amp is approximately $(g_m r_o)^2$, it's easier to reach a high voltage gain. Nevertheless, folded cascode Op Amp is weak at stability because an additional pole exists at the intersection node of three branches.

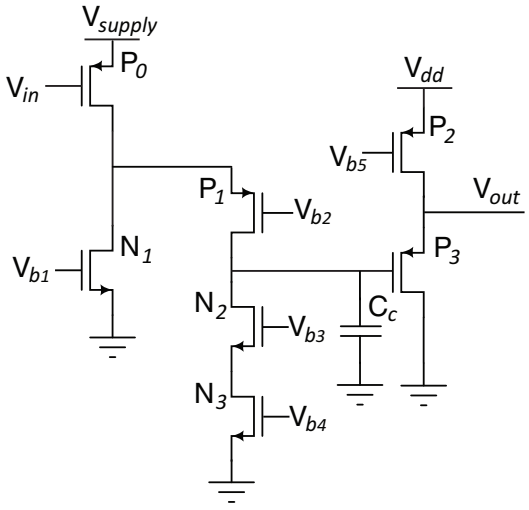


Figure 3.10: Schematic of a cascode high gain voltage amplifier.

It can be seen in the figure, P type MOSFET is chosen as the input transistor due to its lower flicker noise. A source follower is used as a voltage buffer to isolate the voltage amplifier and guarantee enough current output. The dominant pole lies at the node connecting amplifier and source follower. In order to achieve a better stability, a compensation capacitor is inserted between two stages to increase the phase margin. Although the size of the input transistor P_0 has already been decided in last section to optimize ENC performance, the left transistors still need to be designed properly to make their noise contribution as small as possible. Due to the cascode effect, the noise generated by P_1 and N_2 is usually negligible. As to N_1 and N_3, their noise contribution at the input node is approximately $V_n^2 g_{m,x}^2 / g_{m1}^2$. V_n is the input referred noise at the gate of each transistor and $g_{m,x}$ is their transconductance. While g_{m1} is the input transistor transconductance. Large g_m of input transistor biased in moderate inversion effectively scales down the noise contribution of other transistors. On the other hand, to bias N_1 and N_3 in deep strong inversion to guarantee their small g_m, their gate voltages are set as high as possible according to available voltage headroom. With the fixed current, the W/L ratio is obtained. Then width and length are increased at the same time to make flicker noise negligible compared with thermal noise. However, the Op Amp stability sets the up-limit of transistors size. The size of each transistor in the amplifier are listed in the following table:

Table 3.1: Transistor sizing in the voltage amplifier.

P_0	8m/1.2μ
P_1	189μ/1.2μ
P_2	60μ/1.8μ
P_3	90μ/1.8μ
N_1	14.7μ/12.6μ
N_2	731μ/2.4μ
N_3	37.8μ/6μ

The frequency response of the whole voltage amplifier is shown in Figure 3.11.

According to the figure, the DC gain of the amplifier is around 78 dB, which is high enough to set the virtual ground. The phase margin is about 40 degree to decrease the ringing and overshoot at the output.

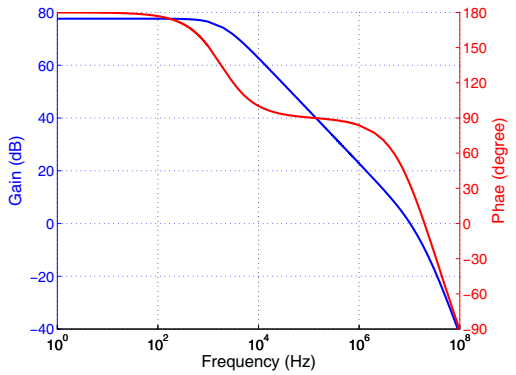


Figure 3.11: Amplitude and phase response of voltage amplifier.

3.4.2 CSA Structure

The structure of a charge sensitive amplifier is shown in Figure 3.12: A feed-

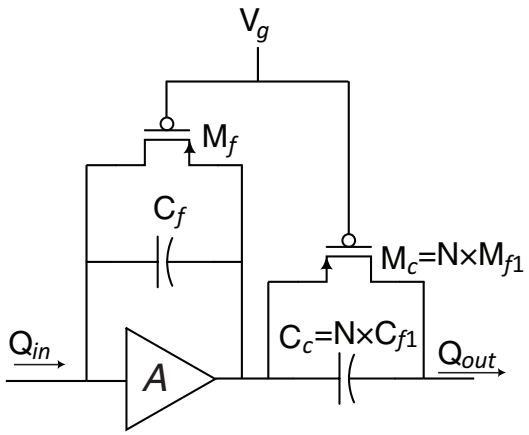


Figure 3.12: Schematic of the charge amplifier.

back is connected across the voltage amplifier to integrate the input current. The

reset network is needed to provide dc stabilization of the amplifier, discharge of the feedback capacitor after each event and a dc path for the detector leakage current. To implement the reset network, a time-variant switch can be used to periodically discharges C_f. However, the time-variant solution introduces extra switch interference in the sensitive circuit as well as integrates leakage current on the feedback capacitor to satisfy the output if its period is not frequent enough. Thus, a continuous time option is preferred [37]. Ideally, a simple resistor R_f in parallel to C_f could be adopted, as illustrated in Figure 3.3. The noise contribution of this resistor is a parallel thermal noise to the input node of CSA. Its PSD is simply $4kT/R_f$. To make it contribution comparable to the unavoidable detector shot noise, the feedback resistor has to satisfy:

$$R_f \geq \frac{4kT}{2qI_{leak}} \tag{3.30}$$

As the leakage current in the proposed system is 10 pA, the resistor has to be larger than 5 GΩ. This value is not practical in the fabrication due to the chip area constraint. Therefore, a transistor is used as substitution, as illustrated in Figure 3.12.

The transistor M_f is connected between the input and output of the Op Amp, with a fixed gate voltage. When the channel length of M_f is much larger than the width, the transconductance of the transistor can be very small, in another word, very high resistance. Moreover, in this configuration, a very small changes at source voltage can make M_f adapt to a wide range of leakage current. In low noise consideration, it's ideal to bias M_f in strong inversion for its smaller g_m. However, when the leakage current is as small as 10 pA, the transistor is more likely to move into subthreshold unless an incredibly long channel is adopted. In the proposed CSA, A feasible 1/40 width to length ratio is chosen for M_f which is biased in subthreshold region. Hence, the noise contribution of the reset transistor is almost the same as detector shot noise, the PSD of which is $2qI_{leak}$.

It can be seen in the Figure 3.12, the circuit consists of an Op Amp, C_f and

M_f just converts the input current mode signal to the voltage mode output. In order to realize the charge amplification, compensation network has to be included. Transistor M_c and capacitor C_c, which are the N times replicas of M_f and C_f respectively, compose the compensation network of CSA. Compensation network has two functions, gain compensation and linearity compensation. As the same voltage change at C_f and C_c which is V_o at the output of Op Amp, the output charge can be written as:

$$Q_{out} \approx C_c V_o = N \times C_f V_o = N \times Q_{in} \tag{3.31}$$

N times capacitance implements N times charge gain. However, according to the Kirchhoff laws, a nonlinearity term from leakage current will be added to the output charge if M_c is not applied. The specialty of M_c is that it shares the same source, drain and gate voltage with M_f, because their sources and source are connected together, their drains are set by the virtual ground of same Op Amp. It's easy to see that drain current of M_c is always N times of M_f. As a result, the mirror effect guarantees that Q_{out} is exactly N times of Q_{in}. From the view of zero-pole, the compensation network keeps the transfer function linear by canceling the additional zero produced by the reset network. The noise contribution of compensation network is negligible as it is N times smaller than the noise of reset network, N is usually much larger than 1.

3.4.3 Cascade CSA Structure

A high gain CSA stage can effectively reduce the noise contribution from pulse shaper. However, if the gain is too high, it's more likely to saturate the output and limit the maximum input charge and lower the dynamic range. As mentioned before, the input charge of proposed system is from 3K electron to 100K electron. A 100 times charge gain should be suitable for the system. The charge gain is achieved by the capacitance ratio between feedback capacitor and compensation capacitor. However, the area constrain prevents the implementation of large ca-

pacitor. Therefore, a cascade CSA is adopted in the proposed system as the following schematic: The structure of the second stage CSA is the same as the first stage.

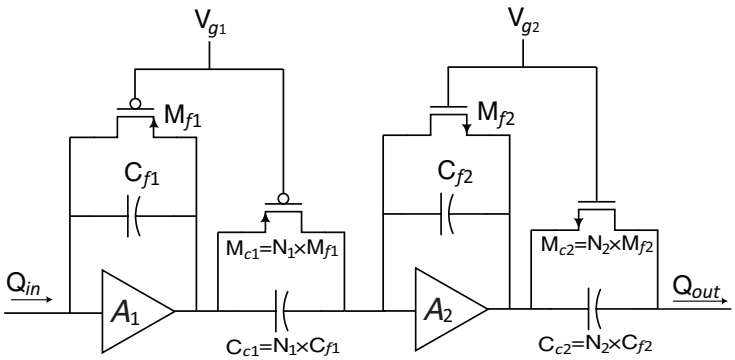


Figure 3.13: Schematic of the cascade CSA.

As the input capacitance of the second stage is nothing but parasitic capacitance, the size of the input transistor of second stage has to be reduced as well. The scale down voltage amplifier with the same W/L ratio is adopted to keep the virtual ground identical between stages. It is worth noting that the types of the transistors in reset and compensation network of two stages are decided by the direction of leakage current and they have to be different between stages. The purpose is to guarantee that M_f and its replica are always connected at their source nodes.

The charge gains of two stages are N_1 and N_2 respectively. The output noise of the cascade CSA is $N_1N_2 \times V_{n1} + N_2 \times Vn2$, V_{n1} and V_{n2} are the input referred noise of the first and second CSA stage. The output charge is $N_1N_2 \times Q_{in}$. To achieve small ENC, N_1 has to be as large as possible. The minimum value of feedback capacitor C_f is limited by the input charge loss. To assure the charge loss smaller than 1 persent, C_f is chosen to be 500 fF. Considering the area constrain, the acceptable largest capacitor is 10 pF. Then the maximum charge gain of one stage CSA is 20. As large N_1 decreases ENC, it is set to be 20. Accordingly, N_2 is 5 to realize the left charge gain in the second stage.

3.4.4 Noise Analysis

In the ENC optimization section, the noise from the input transistor are used to approximately represent the noise contribution of CSA in calculation. Since the architecture of entire CSA is decided, a more accuracy ENC estimation can be made to find the optimal value for shaper peaking time. The major modification of the current noise calculation includes that the shot noise becomes double due to the reset MOSFET and low frequency noise rises because of the existence of some small size transistors in the amplifier. On the other hand, the thermal noise just changes slightly as the transconductances of other transistors are much smaller than the input one. The relation between CSA ENC and shaper peaking time is re-simulated and shown in Figure 3.14. It can be observed that compared with the

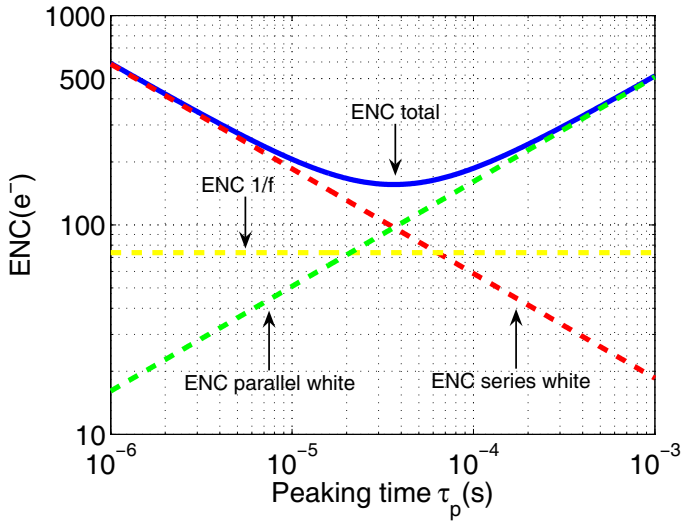


Figure 3.14: Simulated CSA ENC vs shaper peaking time.

result in Figure 3.9, the current parallel white noise increases faster with peaking time, while the series white noise almost keeps the same. Flicker noise is several decades bigger but still negligible. The optimal peaking time moves to 36 μs and the minimum ENC can be achieved is about 155 electron. ENC inflates about 10% from the result with just the input transistor.

3.5 RC Pulse Shaper

The pulse shaper is implemented as the filter in order to eliminate the noise outside the signal band and provide a voltage pulse whose height is proportional to the charge input. The proposed system adopts a third order shaper with real coincident poles. A shaper composed with resistors and capacitors is a simple and straightforward method to begin with.

3.5.1 Circuit Architecture

A third order RC pulse shaper structure is shown in Figure 3.15. The Op Amp

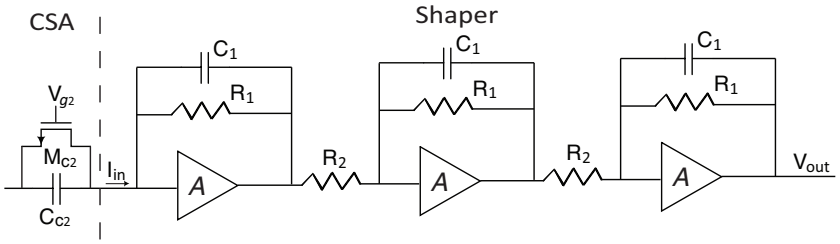


Figure 3.15: Schematic of pulse shaper.

used in the shaper is scaled-down version of the Op-Amp in CSA to keep the virtual ground voltage identical. Since the output signal of CSA stage is in the mode of charge or current, the shaper is configured as low input impedance and the input signal is in current mode. The transfer function of the RC shaper can be written as:

$$\frac{V_{out}}{I_{in}} = \frac{R_1^3}{R_2^2} \frac{1}{(R_1 C_1 S + 1)^3} \tag{3.32}$$

It is clear that the transfer function of shaper has three coincident poles. The position of poles can be controlled by the value of R_1 and C_1, the product of which is the time constant of the shaper. The gain of the shaper is adjusted by the value of R_2. The peaking time of the shaper is simulated in ENC optimization to equalize the white series noise and the white parallel noise. The optimal value for peaking

time is 36 μs. When the shaper order is three, its peaking time is about 1.9 times of its time constant. Therefore, the optimal time constant is about 19 μs. Due to the high area consumption for the implementation of large resistors and capacitors, a tradeoff has to be made. R_1 is chosen to be 1.2 MΩ and C_1 is 10 pF. The corresponding peaking time is 23 μs. Since it's relatively close to the optimum point, the simulated ENC is about 162 electron which means 1/3 area is saved at the cost of 7 electron ENC. R_2 is designed to be 200 KΩ to set the maximum output amplitude around 1.5 volt.

3.6 Gm-C Filter

Although RC filter has advantage in less complexity for implementation, the precious chip area is an important factor to limit its application. Performance has to be sacrificed to fit the filter into the ASIC. It is worth noting that according to Figure 3.14, if the system series white noise increases due to a even larger input capacitance or parallel white noise decreases due to a smaller leakage current, the least ENC point will be pushed to the right which means a bigger time constant is needed. Another solution has to be researched for the system with large time constant other than RC filter. Gm-C filter could be a suitable choice as it can reach very low cutoff frequency.

Gm-C filters are composed of operational transconductance amplifiers (OTA) and capacitors. The capacitors in the Gm-C filter are able to be fully integrated, because the OTA's transconductances can be realized in the order of nA/V or even less. However, irrespective of the frequency of operation, Gm–C filters suffer from limited linearity, small valid input range and offsets due to device mismatch. Therefore, to design a low transconductance OTA with high linearity and wide dynamic range is a major and significant topic in the Gm-C filter implementation.

3.6.1 Low Transconductance High Dynamic Range OTA

A very low transconductance OTA can be achieved using a five transistor OTA implementation with the input transistors biased in the weak inversion region of operation. The OTA achieves very low power consumption and small area [38]. However, 1% harmonic distortion limits the input peak to peak voltage to less than 15mV. As a result, the dynamic range can not exceed -45dB which is insufficient in the proposed system. Another option is to used the bulk as the input terminal [39], but in this case the performance strongly varies between processes and runs. Applying the techniques of source degeneration, current division and cancellation in design of OTA, a few large time constant subthreshold Gm-C filters are reported in the literature [40, 42] that achieve excellent performance in linearity

and dynamic range.

3.6.2 OTA Structure

The OTA structure adopted in the proposed system is shown in Figure 3.16. The structure uses two methods to improve the linearity, source degeneration and current division. The transistor M_R is biased in the triode region and acts as the source degeneration resistor. Source degeneration improves the OTA linearity as M_R realizes the voltage to current conversion instead of the input transistor biased in the saturation region. To achieve the high resistance, M_R has to be a long channel transistor. The currents flowing into transistors M_1 and M_M are divided by factor M which is the ratio of their sizes. Considering that only the current of M_1 contributes to the output current, the effective transconductance of the OTA, G_m, is reduced by the factor of M+1 compared to the OTA implemented without the current division. Therefore, G_m can be calculated as:

$$G_m = \frac{i_o}{v_{id}} = \frac{g_{m_{M1}}}{1 + (M+1)g_{m_{M1}}/g_{ds_{MR}}}, \tag{3.33}$$

where $g_{m_{M1}}$ is the transconductance of the input transistor M_1 and $g_{ds_{MR}}$ represents the small signal drain source conductance of M_R. We define the ratio of transconductances as

$$\alpha = \frac{(M+1)g_{m_{M1}}}{g_{ds_{MR}}}. \tag{3.34}$$

If α is much greater than 1, (3.33) can be further approximated as

$$G_m = \frac{i_o}{v_{id}} = \frac{g_{ds_{MR}}}{1+M}. \tag{3.35}$$

It is desirable to keep the α larger than 5. For a low power design, M_1, M_M and M_N operate in the moderate inversion. The moderate inversion operation leads to a high power efficiency compared to the strong inversion while it guarantees a larger input range than the weak inversion. The value of $g_{ds_{MR}}$ can be adjusted by

varying the V_{sg} voltage of M_R controlled by the current in the branch comprising M_2, M_3 and M_4 to tune the transconductance of OTA.

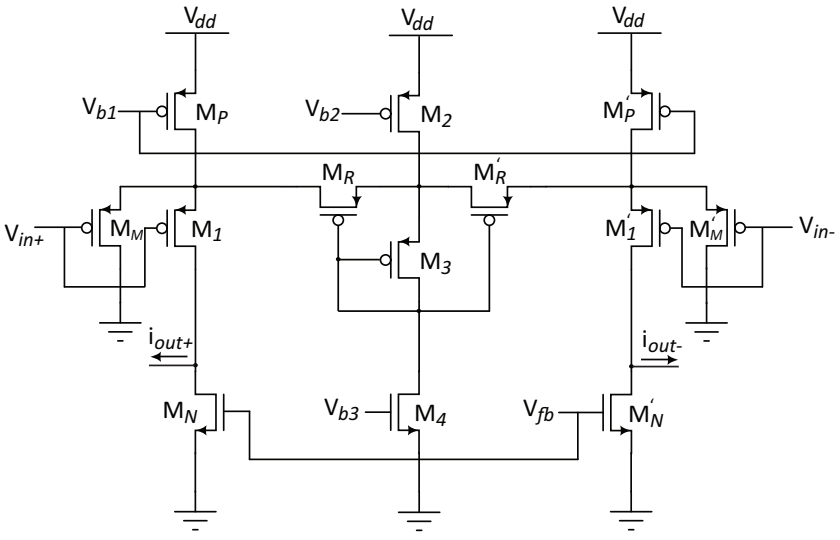


Figure 3.16: Implementation of a low transconductance OTA.

3.6.3 OTA Dynamic Range

The dynamic range of an OTA can be defined in several methods. One of the most common way is to specify total harmonic distortion (THD). Harmonic Distortion is simply the ratio of the rms value of the harmonic of interest (2nd, 3rd, etc.) to the rms signal level. In audio applications it is usually expressed as a percentage, while in communications applications it is more often expressed in dB. Total harmonic distortion is the ratio of the rmd value of all the harmonics to the rms signal level [41]. In many practical situations, there is negligible error if only the second and third harmonics are included, since the higher order terms most often are greatly reduced in amplitude because of components cutoff frequency.

The linearity of the OTA is mainly determined by the linearity of $g_{ds_{MR}}$, which is affected by the body effect. The third order harmonic distortion (HD_3) of the

OTA can be calculated as [42]:

$$HD_3 \cong \frac{\gamma \cdot v_{SD}^2}{96(v_{SG} - V_{th})(2\phi_F - v_{SB})^{\frac{3}{2}}}, \tag{3.36}$$

where γ is the body effect constant, ϕ_F is the Fermi potential and v_{SD} represents the same potential change as the input signal. From 3.36, the harmonic distortion is mainly determined by $v_{SG} - V_{th}$, which is just V_{DS_SAT} of the transistor M_R. By increasing V_{DS_SAT}, HD_3 can be improved. As M_R is biased in triode region, $v_{SG} - V_{th}$ can be computed as:

$$v_{SG} - V_{th} = \frac{g_{ds_{MR}}}{\mu_p C_{OX} \frac{W}{L}} = \frac{(M+1)G_m}{\mu_p C_{OX} \frac{W}{L}} \tag{3.37}$$

In the design of the proposed Gm-C filter, the transconductance of OTA can be given as:

$$G_m = \frac{2\pi f_c}{C_{max}} \tag{3.38}$$

f_c is the cutoff frequency of the filter and C_{max} is the largest capacitor can be integrated. The cutoff frequency can be calculated as 9 KHz according to 36μs peaking time in Figure 3.14, and due to area limitation, we choose C_{max} to be 5 pF. The requirement on the design of the OTA is that HD_3 is suppressed under -50 dB with 50 mV input amplitude. This means that the current division ratio, M, has to be greater than 10. The power consumption of the OTA increases linearly with M. Therefore, M is set to 10, which is the smallest value satisfying the linearity requirement and keeping the power consumption low at the same time.

The only constraint on g_m of transistor M_1 is to be 5 times bigger than the OTA transconductance. Therefore, when the G_m of OTA is tuned to fit the optimum shaper peaking time, the bias current of M_1 and M_M, can be varied simultaneously to decrease the power consumption of OTA.

The sizing of the OTA transistors in Figure 3.16 is shown in Table 3.2.

Table 3.2: Transistor sizing in the OTA

M_1	4.8μ/4.8μ
M_M	48μ/4.8μ
M_P	6.3μ/6μ
M_N	8.4μ/27μ
M_R	1.5μ/108μ
M_2	6.3μ/6μ
M_3	1.5μ/90μ
M_4	4.5μ/3μ

3.6.4 OTA Noise Performance

Due to the current division structure, the noise contributions of transistor M_M become negligible, as well as the contributions from M_P and M_R. Therefore, the output referred current noise density can be expressed as the sum of the noise contributions of M_1 and M_N. The white noise current density of a transistor operated in subthreshold is approximately:

$$S_{iw} = 2qI_b = 2kTng_m \tag{3.39}$$

where q is the charge of electron, the I_b is the biasing current, n is the subthreshold slope coefficient, k is the Boltzmann constant and T is the absolute temperature. For the moderate inversion transistor, $g_m = \frac{q}{nkT} I_D$. As the M_1 and M_N have the same biasing current, the total input referred white voltage noise of the OTA can be expressed as:

$$\begin{aligned} v_{in\_th}^2 &= \int_{BW} \frac{S_{iw}}{G_m^2} \,\mathrm{d}f \\ &\approx \int_{BW} \frac{4 \times 2kTng_m}{G_m^2} \,\mathrm{d}f = \frac{8kTng_m}{G_m^2} BW \end{aligned} \tag{3.40}$$

where g_m is the transconductance of M_1 and according to equation (3.35) can be expressed as:

$$g_m = \frac{g_{ds_{MR}} \times \alpha}{M} = \frac{\alpha(M+1)G_m}{M} \approx \alpha G_m \tag{3.41}$$

Therefore, the input white noise becomes:

$$v_{in\_th}^2 = \frac{8kTn\alpha}{G_m} BW \tag{3.42}$$

It can be observed that larger α guarantees less contribution of input transistor to the linearity of the OTA, at the cost of larger white noise. As a result, α is chosen to be 5 in order to trade off between linearity and white noise.

The input referred flicker noise can be computed as:

$$v_{in\_f}^2 \approx \frac{2}{C_{ox}G_m^2}(\frac{K_{Fp}}{W_1L_1} + \frac{K_{Fn}}{W_nL_n}) \log(BW) \tag{3.43}$$

where C_{ox} is the gate oxide capacitance per unit area, W_1, L_1, W_n and L_n are respectively the width and the length of transistor M_1 and the width and the length of transistor M_N. The flicker noise coefficient K_{Fn} is few times higher than K_{Fp}, which leads to a bigger transistor area of M_N than M_1 in order to lower the 1/f noise.

3.6.5 Gm-C Filter Design

The dynamic range of Gm-C filter is usually limited by the small linear input range of OTA. Capacitive attenuation can increase the linear range of the filter effectively by attenuating its input and feedback signals [43]. The input signals are attenuated to fit in the linear rang of OTA while the output signals are amplified in the filter to have the same amplitude as the input signal. Because the linear range of the transconductors is limited by their input swing, rather than their output swing.

To further analyze the characteristics of Gm-C filter, a fully differential Gm-C bandpass filter with capacitive attenuation is implemented using the designed

OTA, shown in Figure 3.17. The proposed implementation introduces additional OTA compared to the design reported in [44] to realize the fully differential structure for much lower second order harmonic distortion.

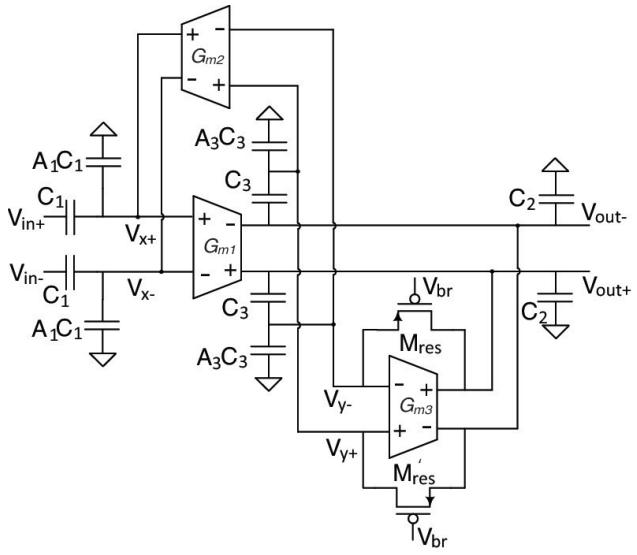


Figure 3.17: Implementation of a fully differential bandpass filter with capacitive attenuation.

The voltage gain in the pass band, center frequency and quality factor of the proposed implementation are

$$A_v = \frac{(A_3+1)G_{m1}}{(A_1+1)G_{m3}} \tag{3.44}$$

$$\omega_o^2 = \frac{G_{m1}G_{m2}}{(A_1+1)C_1[(A_3+1)C_2+A_3C_3]} \tag{3.45}$$

$$Q^2 = \frac{(A_3+1)C_2+A_3C_3}{(A_1+1)C_1}\frac{G_{m1}G_{m2}}{G_{m3}^2}. \tag{3.46}$$

By choosing the proper ratio of the transconductances and attenuation ratios, the output voltage can have the same amplitude as the input voltage. Meanwhile, the input voltages of OTAs are attenuated by the capacitive attenuation. The transistor M_{res} functions as a large resistor which provides the DC bias path for

OTA_2 and OTA_3. Higher Q factor indicates a lower rate of energy loss relative to the stored energy of the resonator which means harmonic distortion is more suppressed. Therefore, Q is chosen to be 4 for the bandpass filter with the voltage gain equals to 1.

The input voltage range of all the OTAs in the filter has to be the same, so that no single OTA limits the harmonic distortion. This introduces additional constraint in the selection of the filter parameters. The input voltages of OTAs can be expressed as:

$$V_x = \frac{sV_{out}[(A_3+1)C_2 + A_3C_3] + V_{out}G_{m3}}{(A_3+1)G_{m1}} \tag{3.47}$$

$$V_y = \frac{V_{out}}{A_3+1} \tag{3.48}$$

Assume that the resistance of M_{res} is large enough to make the current flow through the transistor negligible. In order to keep $|V_x| = |V_y|$, the transconductance of OTA1 and OTA3 can be calculated as:

$$G_{m1} = \sqrt{(Q^2+1)}G_{m3} \tag{3.49}$$

As the designed OTA can achieve -50dB HD3 with 50mV input voltage, A_3 is selected to be 4. As a result, A_1 has to be 19 to make Q equal to 4. To set gain to 1, we choose $G_{m1} = G_{m2}$ and $C_2 = 3C_1 = 2.4C_3$. The center frequency can be simplified as

$$\omega_c = \frac{G_{m1}}{20C_1} \tag{3.50}$$

3.6.6 Simulation Results

The proposed low transconductance OTA is simulated in Cadence Virtuoso. Because of the fully differential structure, the second order harmonic distortion is negligible. The overdrive voltage of M_R is set to be 350 mV as the worst case which is easy to reach in most OTA design. In Figure 3.18, the third order harmonic distortion (HD_3) of OTA is simulated as a function of input amplitude. It

can be observed that when the input peak to peak amplitude is 100mV, HD_3 of OTA is -55dB, less than 0.2%.

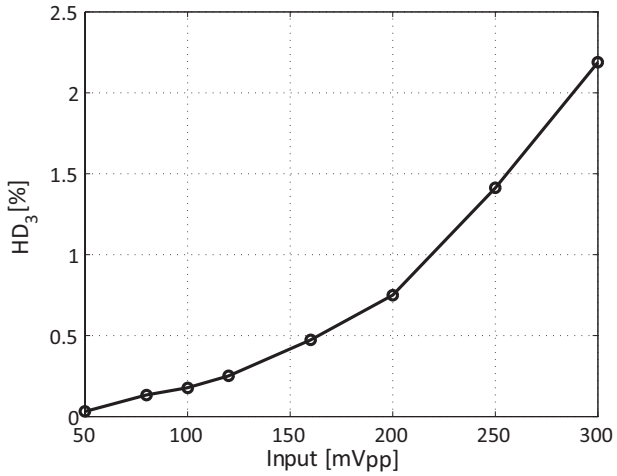


Figure 3.18: Simulated HD_3 of the designed OTA as a function of the amplitude of the input signal.

The input referred noise of the OTA is simulated and shown in Figure 3.19. The integrated input referred noise in the filter bandwidth is 50μV.

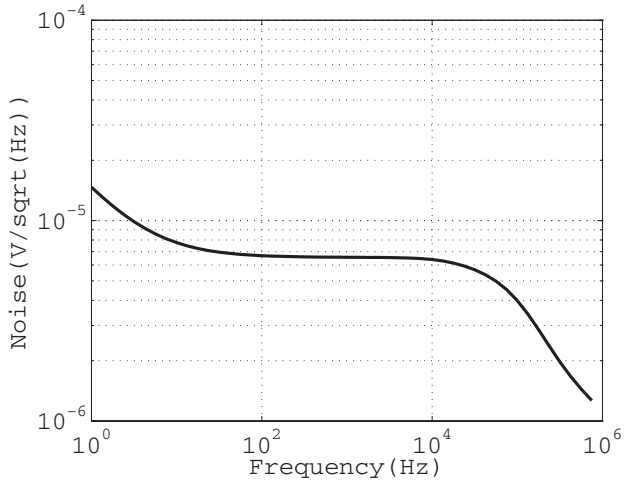


Figure 3.19: Simulated input referred noise of OTA.

A Simulink block diagram of the capacitive attenuation bandpass filter with center frequency at 9 KHz is simulated in Matlab shown in Figure 3.20. It is created based on the model of designed OTA with the parameters of OTA obtained from the Cadence simulation. The simulated input referred noise is added to the OTA. A 9 KHz sinusoidal wave with 1.92 V peak to peak amplitude is used as the input signal. The HD_3 of the bandpass filter is -61.3 dB with the dynamic range equal to 60.2 dB.

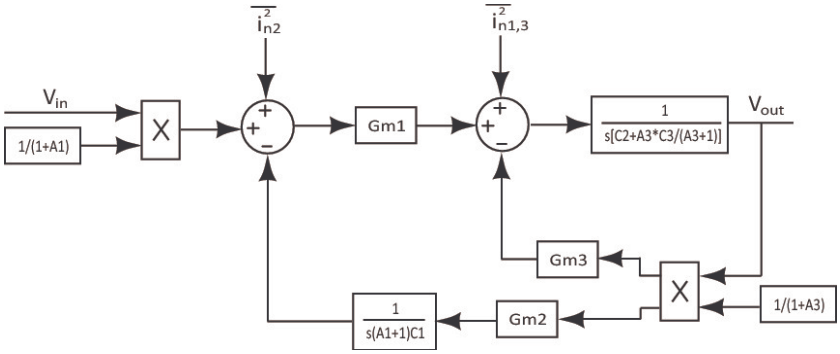


Figure 3.20: Simulink Block Diagram of Gm-C Bandpass Filter.

A fully differential Gm-C bandpass filter was then simulated in Cadence Spectre environment. The input signal is still 9 KHz sinusoidal wave with 1.92 V peak to peak amplitude. The output power spectrum is shown in Figure 3.21. From the Figure, we can observe that HD_3 is about -58 dB which is quite close to the result of Matlab simulation. Meanwhile, HD_2 is shown to be suppressed by the fully differential structure.

The output noise of the bandpass filter is simulated and shown in Figure 3.22. The integrated output noise is about 600μV

The transconductances of the OTAs are tuned to adjusted the center frequency of bandpass filter from 100 Hz to 10 KHz. The simulated frequency responses are shown in Figure 3.23. The transfer functions of the bandpass filer display uniformity among different center frequencies in the figure. The pass band gain

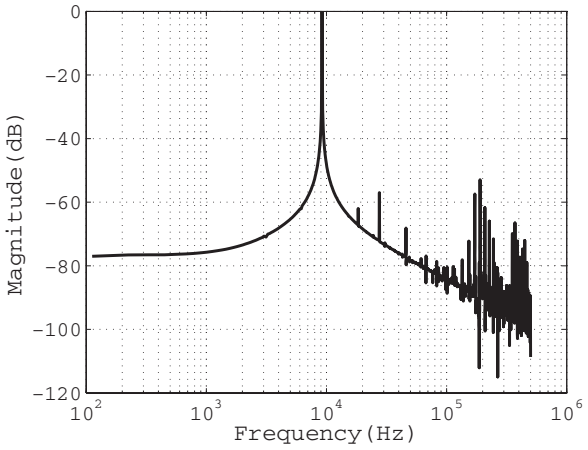


Figure 3.21: Simulated output power spectrum of Gm-C bandpass filter.

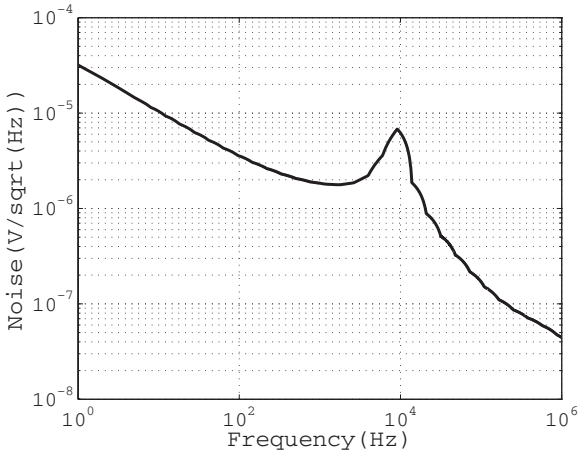


Figure 3.22: Simulated output noise of BPF.

can be seen as 0.8. Therefore, the signal-to-noise ratio can be calculated as:

$$SNR = 20log(\frac{Vin_{rms}}{V_{noise}}) = 20log(\frac{1.92 \times 0.8}{2\sqrt{2} \times 600e^{-6}}) = 59dB \tag{3.51}$$

It can be concluded that Gm-C filter is able to provide cutoff frequency much lower than RC filter. By proper design techniques, the linearity and signal-to-

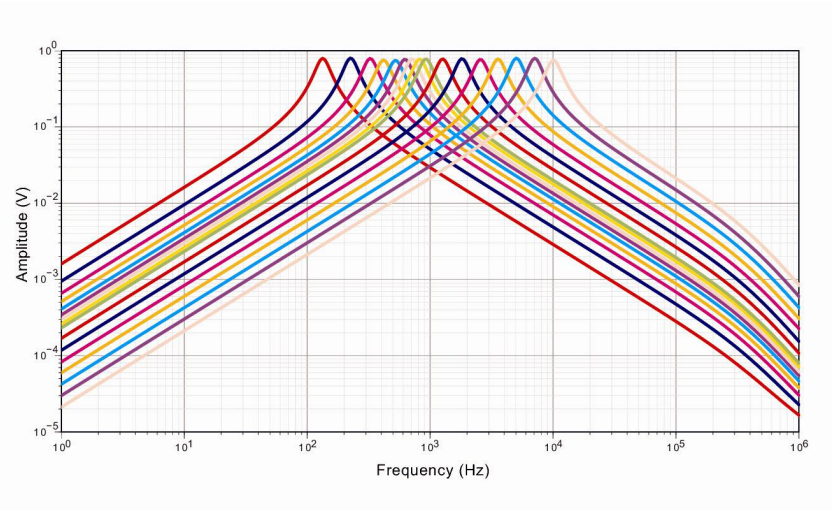


Figure 3.23: Simulated frequency responses of bandpass filter with center frequencies from 100 HZ to 10 KHz.

noise ratio of Gm-C filter can both be improved and close to 60 dB. Therefore, Gm-C filter is a superior solution to implement the pulse shaper in the charge amplification system.

3.7 Baseline Holder

In most cases, the readout circuit extracts the absolute amplitude of shaper output pulse which reflects the superposition of the signal as well as the baseline. As a result, any fluctuation in the output baseline may introduce an error in the measurement of the peak amplitude. However, as the charge amplifier and pulse shaper are based on dc coupling and unipolar shaping, the baseline of output voltage signal strongly depends on the sensor leakage current. Moreover, temperature change, power supply low frequency noise and non-recovery events cause the baseline instability as well. In order to maintain a stable output baseline in the whole operation band, a baseline holder (BLH) is necessary [45].

The BLH which functions as a low-frequency feedback loop around the shaper is composed of a differential amplifier, a non-linear dynamic buffer and a low-pass filter. The differential amplifier compares the output voltage with a reference voltage source. The nonlinear buffer dynamically reduces the gain of the feedback loop only in presence of large and fast signals. The low pass filter provides the dominant pole necessary for the stability of the loop. The simplified schematic of baseline holder is shown in Figure 3.24.

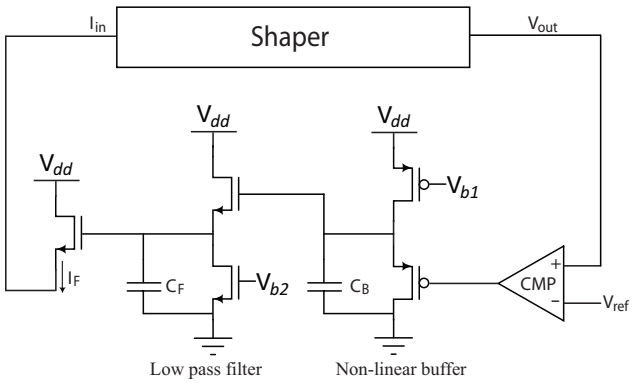


Figure 3.24: Simplified schematic of baseline holder.

For slow and small changes at the output of shaper, the differential amplifier compares the output with a fixed reference voltage. BLH functions as a nega-

tive feedback loop, a feedback current is generated to push the shaper's baseline voltage back to reference voltage. For large and fast signals, the slew rate of the output of differential amplifier is limited by the non-linear buffer. This gain attenuation results in a baseline much less sensitive to the event rate. The low pass filter is implemented with a very low cut off frequency. It has similar configuration as the buffer but with much smaller drain current and much larger capacitor C_F compared with C_B.

3.8 CSA and Shaper Simulation

The charge sensitive amplifier and RC shaper with baseline holder are designed under AMI 0.6μm CMOS technology, and simulated in the Cadence Spectre environment. The radiation detector is replaced with a current pulse generator parallel with a 50 pF capacitor and a 10 pA DC current source. First of all, the voltage outputs at two stages of CSA are simulated, the results are shown in Figure 3.25. The input charge is 30K electrons. The voltage output of the second stage is about

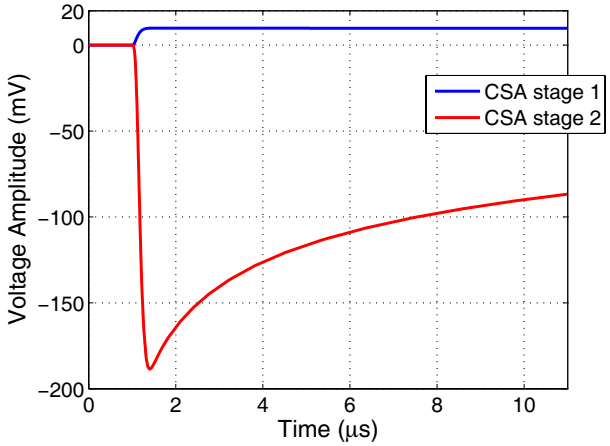


Figure 3.25: Simulated output of cascade CSAs with 30K input electrons.

20 times of the first stage. This elaborates the charge gain of the first stage. The gain of the second stage is not shown here because its output to the shaper which has a different integrating capacitor.

In the next step, different amount of charges are input in to the system, the outputs from the shaper is shown in Figure 3.42.

The performance of pulse shaper can be seen in the Figure 3.26. The peaking time of each pulse is identical and equals to the design value, 23 μs and the pulse width can be read as about 110 μs. Hence, τ_w/τ_p is around 5, which matches the theoretical coefficient for 3^{rd} semi-gaussian real shaper in Figure 3.6. The output amplitude for maximum input charge, 100K electron, is 1.4 volt. By extracting

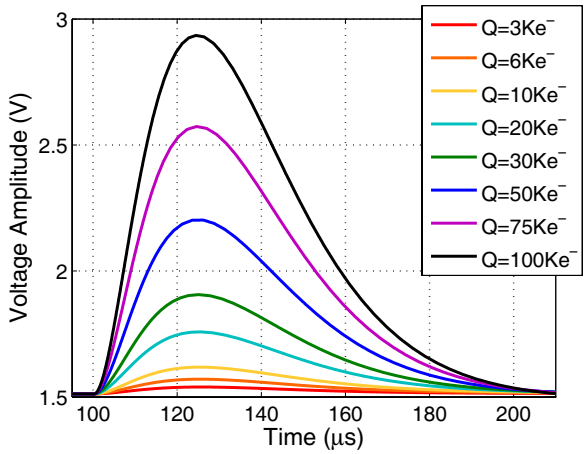


Figure 3.26: Simulated transient output of shaper with different input charges.

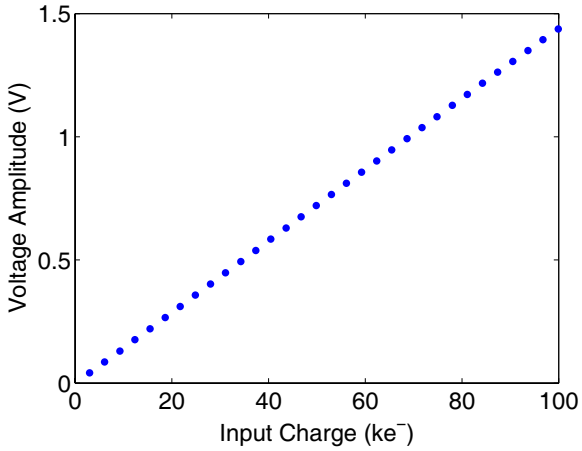


Figure 3.27: Output amplitude linearity with different input charge.

the voltage amplitude from the each pulse, the linearity of the output signal as a function of the input charge is shown in Figure 3.27. The system is proven to possess high linearity and the charge gain can also be found as 86.5 mV/fC.

By integrating the power spectre density in frequency domain, output noise power can be obtained. With the input charge and corresponding output amplitude, ENC for the system can be calculated. Sweeping the value of detector capacitance,

the relation between ENC and input detector capacitance can be obtained in Figure 3.28. It can be seen in the figure that ENC almost increases linearly with the

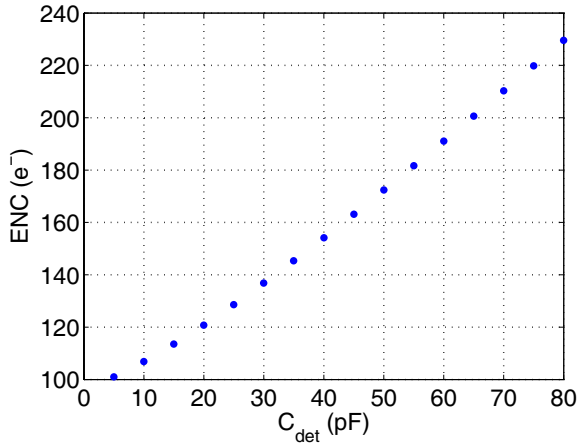


Figure 3.28: Simulated ENC with different detector capacitance.

detector capacitance. The approximate equation is $ENC = 87 + 1.7 \times C_{det}/pF$. When the detector has 50 pF capacitance in our case, ENC is about 172 electron in the simulation which is very close to 162 electron, the theoretical calculation result.

3.9 Peak Detector

The peak amplitude of the output pulse from the shaper is of interest because it contains information about the radiation intensity. However, the peak value doesn't last long enough for analog-to-digital conversion. Therefore, a peak detector module is essential to measure and store the peak voltage of the pulse for the ADC reading afterwards. In most cases, the peak detector also has to release a "peak-found" digital signal to trigger the conversion.

3.9.1 Circuit Architecture

The peak detector in Kruiskamp and Leenaerts configuration [46] is adopted in the proposed system. The simplified schematic of the peak detector is shown in Figure 3.29.

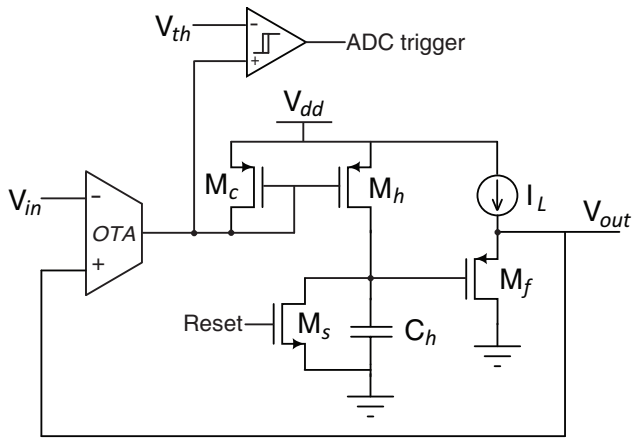


Figure 3.29: Simplified schematic of peak detector.

When the voltage pulse which enters the negative input of an OTA starts to rise, the output current of OTA feeds the diode connected transistor M_c. Its gate voltage drops and turns M_h on. The current flowing out of M_h charges the capacitor C_h. This charing current is proportional to the derivative of the input signal. The voltage on the capacitor is buffered and fed back to the positive input of OTA.

Because of the feedback loop and high gain, the feedback voltage tracks the input pulse. When the input signal approaches the peak, the charing current is very close to zero and the output of the peak detector reaches the peak as well. Right after the peak, the input signal begins to fall, M_h and M_c are turned off. Since there is no discharge path for C_h, it holds the peak value for the later readout. As the gate voltage of two shut down PMOS is larger than $V_{dd} - V_{thp}$ when the peak is hold, it can be used as the signal to indicate the completion of peak detection and trigger the conversion of ADC. When the conversion is over and system is ready to detect the next signal, the hold peak value can be reset by turning on M_s for a while to discharge the capacitor to the baseline voltage.

The error between the output of peak detector and the peak of the input pulse can be approximated as [47]:

$$\begin{aligned}\delta V_p \approx & \frac{2.5 V_{DD} L_h^2 V'_{imax}}{\mu_h (V_{DD} - V_{THh})^2} + V_{OFF} + \frac{V_{THh} - V_{A,CM}}{A_0} + \frac{V_{DD} - 2V_{ip}}{2CMRR_A} \\ & + \frac{V_{DD} C_{OX} W_A L_A}{1.4 C_h} + (V_{DD} - V_{THh}) \frac{V'_i}{V'_{g,max}}. \end{aligned} \tag{3.52}$$

The first term is caused by the parasitic capacitances and channel charge injection from M_h, where L_h is the gate length, μ_h is the mobility, V_{Thh} is the threshold voltage and $V'_{i,max}$ is the maximum slope of the input pulse. By using a small length transistor, it can be constrained within negligible percent of V_{DD}. All other terms come from non-ideal of the OTA. The second term is due to the offset at the input of the OTA. The third and fourth terms are due to the finite gain for the OTA, where $V_{A,CM}$ is the common-mode voltage reference, A_0 is the DC differential voltage gain and $CMRR_A$ is the common-mode rejection ratio. They can be negligible with a proper design of OTA. The fifth term is the error from OTA's input capacitances where W_A and L_A are the gate length and width of the OTA's input transistors. It can be limited by choosing small size input transistor. The last term is related to the slew-rate limit, $V'_{g,max}$ at the output of the OTA. Although the existence of the source follower may decrease the output range by raising the

lower-limit of output voltage, it has no effect on our system because only positive pulses are detected and hold.

3.9.2 Simulation Result

The peak detector module is simulated in the Cadence with the designed CSA and shaper. The input signal of the peak detector is the output pulse from shaper with 30K electrons as input charge. The profile of the peak detector output is shown in Figure 3.30. It can be seen in the figure the output of peak detector tracks

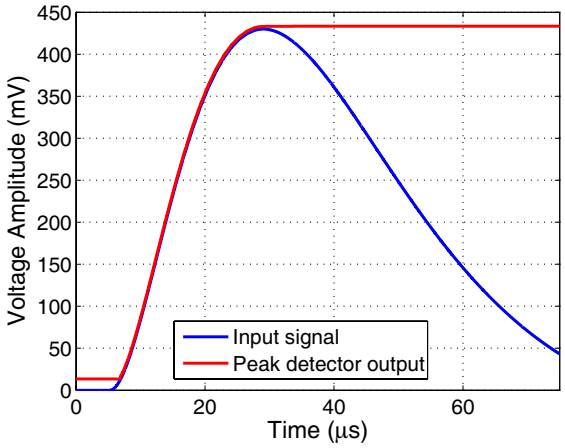


Figure 3.30: Simulated input and output of peak detector.

the input signal in the rising edge and holds the peak voltage long enough for the further process. The linearity of the peak detector is simulated with input pulse amplitude from 50 mV to 1.5 V which covers the output range of the shaper. The result shown in Figure 3.31 elaborates that peak detector has excellent linearity.

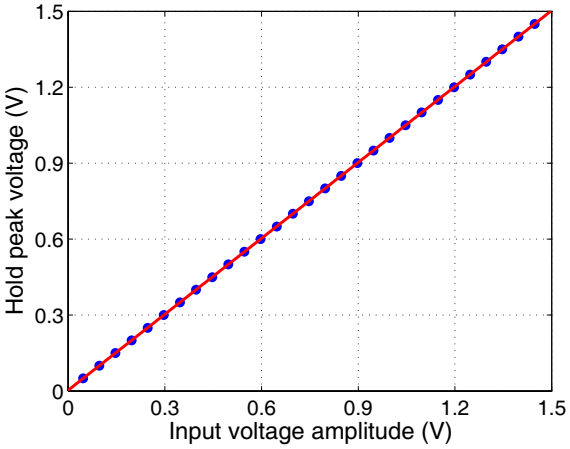


Figure 3.31: Simulated linearity of peak detector.

3.10 Clock-less ADC

In order to digitize the voltage output of the peak detector, an A/D converter is required in the system. A clock-less timebased A/D converter based on Wilkinson type ADC [48],[49] is implemented, as the presence of the clock in the system would interfere with the low-noise CSA.

3.10.1 Theory of Clock-less ADC

A typical Wilkinson ADC counts the number of clocks passed until one generated ramp hits the threshold. Since the slope of this ramp is decided by the input current, the number of clocks digitizes the analog charging current. However, an external clock is still inevitable in this configuration. In order to implement a complete clock-less analog to digital conversion, the proposed ADC is designed to count the number of ramps generated by a current integrator in a certain fixed period of time, T. Whenever the output voltage of the integrator reaches the threshold, a ramp is finished and the integrator is reset to start accumulating the input current again. Assume the input current is I, the output voltage threshold is V_{th}, the integrate capacitor is C, the time to finish a single ramp is $t_1 = (C \times V_{th})/I$.

The total number of generated ramps is added up by a counter as the digital output, $N = [T/t_1]$.

Although the ratio between the integrating time T and the input current determines what is number of bits (NOB) this ADC can achieve, the composition of the error sources of the ADC is more complicated and needs a careful analysis. Assume that the time consumed by the comparator to turn over is t_d, the input offset voltage of the amplifier in the comparator is ΔV, and the time for the integrator to reset and discharge to the baseline voltage is t_r, the non-ideal digital output of the ADC can be expressed as:

$$N = \frac{T - T_{res}}{\frac{C \times (V_{th} + \Delta V)}{I} + t_d + t_r}, \tag{3.53}$$

where T_{res} is the residue time for last uncompleted ramp. T_{res} is clearly the quantization error which is normal in ADC and always smaller than 1 LSB. The offset voltage of the comparator can be translated into a small drift of the threshold voltage which just affects the absolute output value of ADC and is negligible. However, the existence of t_d and t_r makes the total number of generated ramps nonlinearly proportional to the input current I. Compared with the reset time, the comparison delay is almost an order of magnitude smaller and can be suppressed by the proper design of a high gain comparator. Therefore, reset time error is the major system error for the ADC. To significantly reduce the effect of the reset time, non-overlapping dual integrators can be adopted. A pair of integrators take turns to integrate the input current. When one of them is charging, the other can finish discharge and prepare for the next cycle. At last, the binary counter provides the sum of the number of ramps from both integrators. In this way, the reset time t_r is no longer included in the integration time T, which improves the linearity of the ADC apparently. The only system error left is the comparator delay.

3.10.2 Circuit Architecture

The structure of clock-less ADC is shown in Figure 3.32. The output volt-

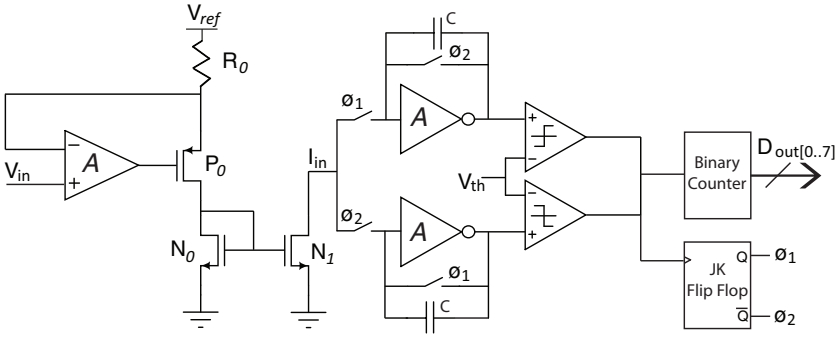


Figure 3.32: Simplified schematic of the clock-less A/D converter.

age signal of the peak detector is first converted to the current, with the resistor R_0 as the linear factor in the conversion. The negative feedback connection of a folded cascode high gain amplifier makes its inverting node track the input voltage at the non-inverting node. The current flowing through the resister R_0 equals to $(V_{ref} - V_{in})/R_0$ which is linearly proportional to the input voltage. However, it is worth noting that this linear relation is negative. The larger the input voltage, the smaller the output current. The current is mirrored and integrated on the feedback capacitor. When the first integrator reaches the threshold, the associated comparator makes the JK flip-flop toggle to activate the second integrator. Meanwhile, the capacitor of the first integrator starts discharging in preparation for the next integration cycle. A capacitor charged by a constant current is used as the timer which is triggered by the "peak-found" signal generated by the peak detector. At last, the binary counter provides the sum of the number of ramps from both of the integrators as the digital result. The comparator used in the proposed ADC is an open loop amplifier, with a regenerative loop introduced to speed up the response of the comparator. The schematic of the comparator is shown in Figure 3.33.

The input voltage of ADC is the the output voltage of the peak detector and it is in the range from 1.5 V to 3 V. The corresponding input current for the integrator after voltage to current conversion ranges from 150 nA to 5 μA. The integration capacitor is chosen to be 1 pF and the integration amplitude is 2 V. Since the gradual drop of input peak voltage caused by the leakage current of peak detector

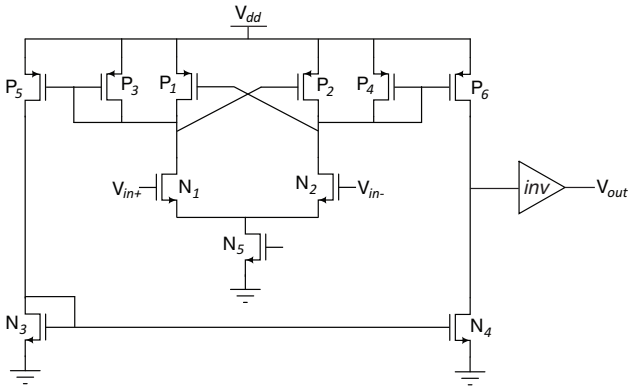


Figure 3.33: Simplified schematic of the comparator in ADC.

is no longer negligible if the integration time is too long, the fixed time period, T, is set as 100 μs. Therefore, the number of bit of ADC achieves 8 bit.

3.10.3 Simulation Result

The clock-less ADC connected with CSA, shaper and peak holder is simulated in Cadence. The outputs of two integrators are shown in Figure 3.34. The input

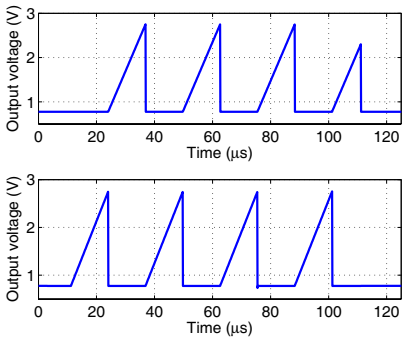


Figure 3.34: Simulated integrator outputs of ADC.

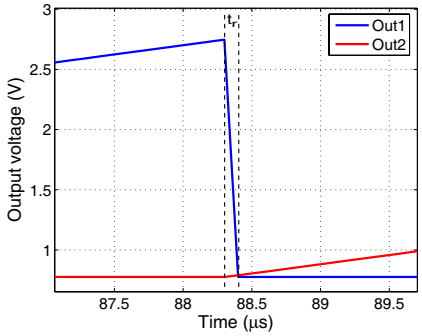


Figure 3.35: Simulated transition edge of ADC.

is a 100K electron charge which corresponds an approximate 3V voltage input into ADC. It can be seen the total integrate time is 100 μs and two integrators

are activated one after another. A small ramp is not finished in the end which means the quantization error of ADC. The transition edge of ADC is zoomed in and shown in Figure 3.35. It elaborates clearly in the figure that reset time of the integrator is eliminated because the second integrator starts to work right after the first integrator reaches the threshold voltage. The integral nonlinearity(INL) of ADC is simulated and shown in Figure 3.36. The input voltage ranges from 1.55V to 3V. It can be seen INL is approximately in the range of $\pm$ 0.5LSB.

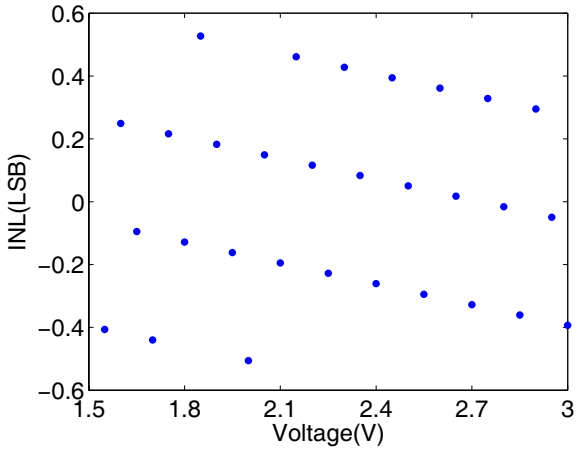


Figure 3.36: Simulated integral nonlinearity of clock-less ADC.

3.11 ASIC Implementation

3.11.1 ASIC Layout

The layout of the chip designed in 0.5 μm CMOS technology with three channels of the radiation detection readout system is completed as shown in Figure 3.37. The purpose of inclusion of three channels is to observe the performance of the

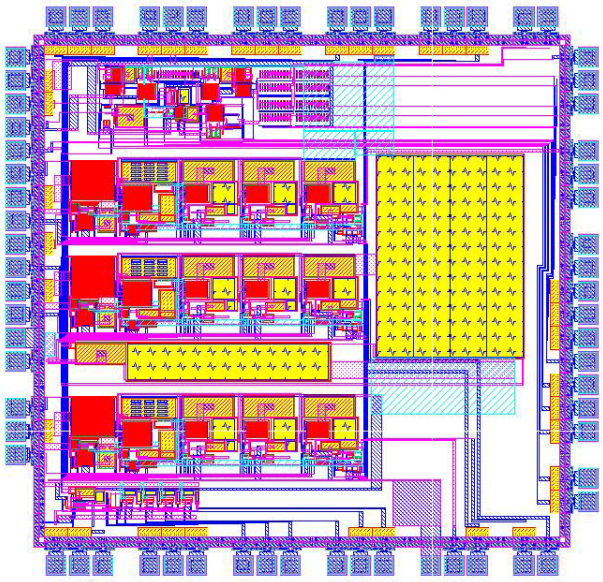


Figure 3.37: ASIC layout of radiation detection readout chip in 0.5 μm technology.

readout circuit under different circumstances such as with on chip capacitance or off chip capacitance, with or without digital processing circuit connection and etc. The area of the chip that one channel comprising CSA and shaper without ADC occupies is 0.42 mm^2, while the area of ADC is 0.25 mm^2. The chip is submitted for fabrication, and the micro-photo of implemented ASIC is shown in Figure 3.38.

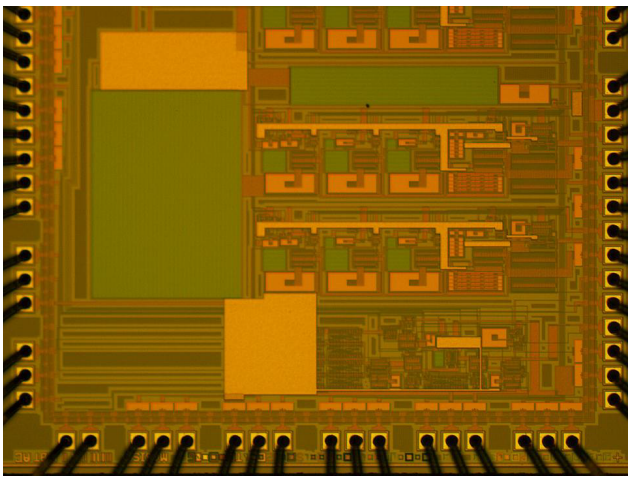


Figure 3.38: Micro-photo of implemented radiation detection readout chip.

3.11.2 ASIC Test Setup

A printed circuit board (PCB) is designed and fabricated as the test board of radiation detection ASIC. To eliminate the parasitic capacitance introduced by the chip package and socket, The chip-on-board technique was employed to wire-bond the chip die directly on the printed circuit board. The Figure 3.39 shows a photo shot of the test board with ASIC on it. It can be seen that the chip die is directly mounted on the board with the pins of the chip connected to the pads by thin golden wires. The negligible parasitic capacitance makes the input capacitance of the CSA precisely controllable and measurable. The test board also provides 3.3V power supplies for the chip as well as connects chip with PC through a data acquisition (DAQ) card, $NI\_PCI6259$. This DAQ card includes analog input and analog output with 16 bits resolution and up to 48 ports of digital I/Os. The maximum sampling rate of the DAQ card is 1 MHz.

For the purpose of test accuracy, leakage current of the radiation detector was modeled by a constant voltage potential across a fixed large resistor and the input charge is represented as an adjustable voltage step across an ac coupling capacitor to the readout circuit. The input capacitance is implemented as an external

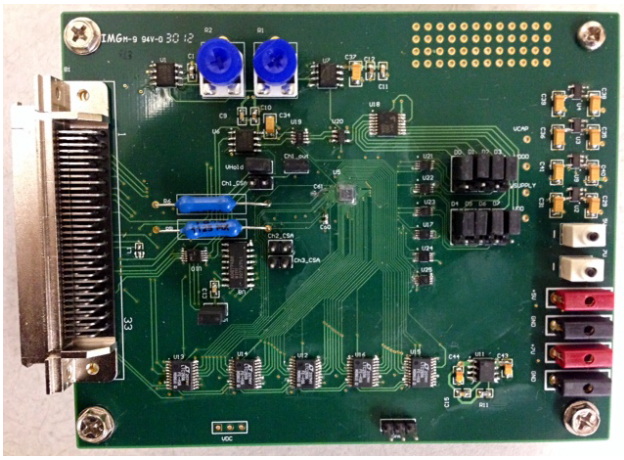


Figure 3.39: Photo of ASIC test PCB.

capacitor connected between the input node and ground. Capacitors with different values can be attached to test system equivalent noise charge with different input capacitance.

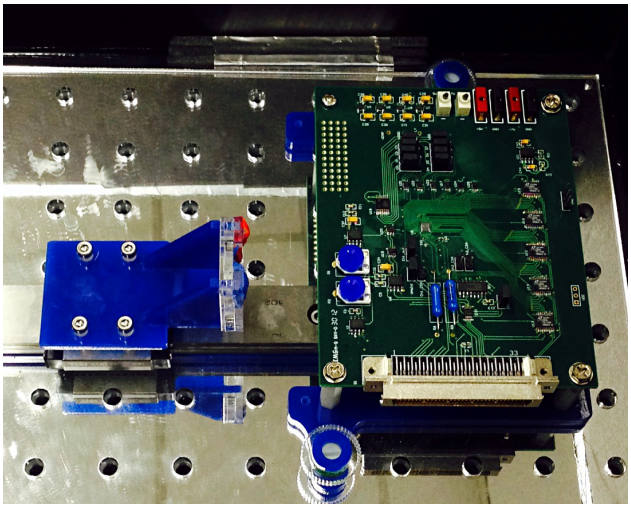


Figure 3.40: Photo of radiation detection system test station.

To shield the sensitive CSA stage from the interference in the air, a test box with mental coating is fabricated. The PCB to be measured is fixed in the box and

the radiation source which emits alpha or gamma particles can move along the track to adjust the scale of the input charge. The set up of the experiment station is shown in Figure 3.40.

3.11.3 ASIC Test result

Linearity

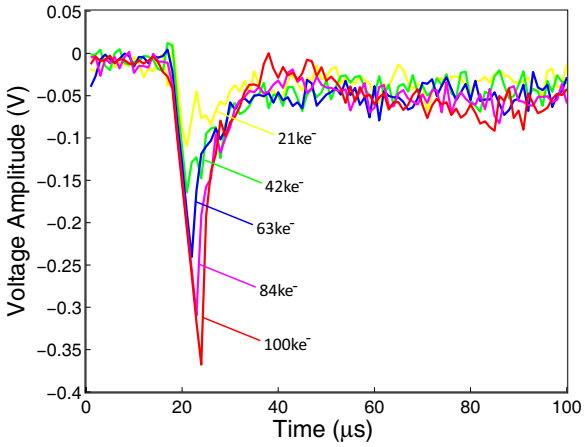


Figure 3.41: Measured output voltage of CSA for different input charge.

The responses of CSA for different injected charge are shown in Figure 3.41. Since they are actually the voltage output of the first amplification stage of CSA, the charge gain by far is 20 times and the output polarity is opposite to the eventual output. It can be seen that the signals have fast falling edge and obvious noise because they are output without passing through the shaper.

Figure 3.42. shows the measured output voltage of pulse shaper for different input charge. An approximate 23 μs peaking time can be observed in the figure for all the curves. The relationship between the injected charge and the output voltage is shown in Figure 3.43. from 3 ke^- to 100 ke^-. The measured charge gain is 94.4 mV/fC. The typical integral linearity error (INL) of the shaper output is shown in Figure 3.44. The INL is measured to be less than 1% in the entire input range.

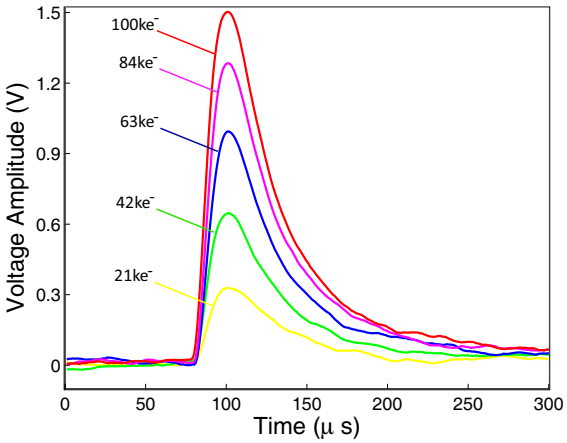


Figure 3.42: Measured output voltage of pulse shaper for different input charge.

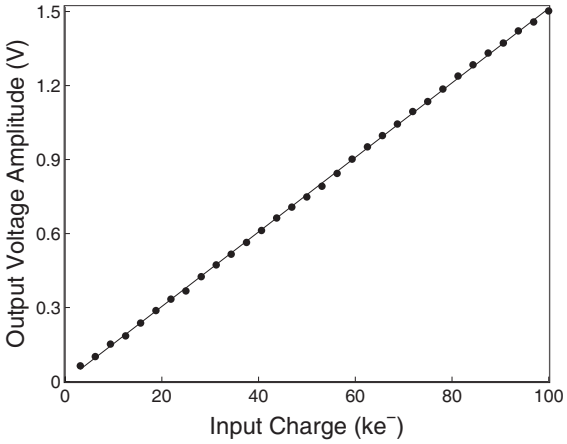


Figure 3.43: Measured output voltage of the pulse shaper as a function of the input charge.

Equivalent Noise Charge

The output noise spectrum density was sampled with different external load capacitance at the input node of the CSA. After Fourier Transform, the output noise can be obtained by integration in the frequency domain. The output signal amplitude is provided in the Figure 3.42. The corresponding ENC were calculated

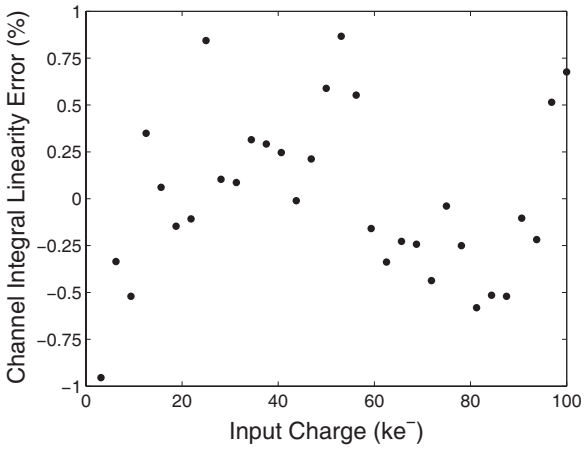


Figure 3.44: Measured shaper output integral linearity error.

based on equation 3.3. The plot of the equivalent noise charge as the function of input capacitance is shown in Figure 3.45.

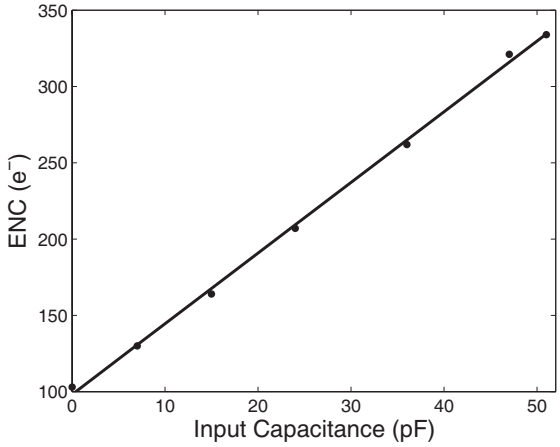


Figure 3.45: Measured ENC versus external input capacitance.

When there is no load capacitance connected at the input node, the ENC is measured to be 103 electrons. With a 51 pF input capacitance, the measured rms ENC is 334 electrons. According to the plot, ENC can be expressed as: $ENC =$

$103 + 4.5e^-/pF$. The slight increase of the measured ENC from the theoretical value is estimated to be caused by the existence of the parasitic capacitance and the thermal noise generated by the resistor providing the leakage current.

The power consumption of one channel of CSA and shaper is measured to be 2.2mW. Table 3.3 displays a comparison of this work with other recent related works. This work possesses relatively low ENC when there is no input capacitance connected and exhibits very slow ENC increment with the increasing of the detector capacitance. On the other hand, the achievement of low power consumption can also be seen from the table.

Table 3.3: Comparison with Related Work.

Reference	ENC	Linearity	Power
[24]	185e^- + 14e^-/pF	$\pm 1\%$	10 mW
[25]	400e^- @ 5.8pF	N/A	198 mW
[22]	200e^- @ 30pF	$\pm 0.25\%$	5 mW
[20]	275e^- + 10e^-/pF	$< 1\%$	13 mW
[21]	89e^- + 7.5e^-/pF	N/A	3 mW
[26]	139e^- + 18.9e^-/pF	N/A	3.5 mW
This work	103e^- + 4.5e^-/pF	$< \pm 1\%$	2.2 mW

A/D Converter

To assure the accuracy, the performance of the proposed 8-bit clock-less A/D converter is tested individually. An external voltage potential is directly used as the input of the ADC. Figure 3.46 shows the integral nonlinearity of the ADC. It can be observed that INL is less than 0.7 LSB in the entire input range. The major error source is estimated to be the the deviation of the fixed time period generation.

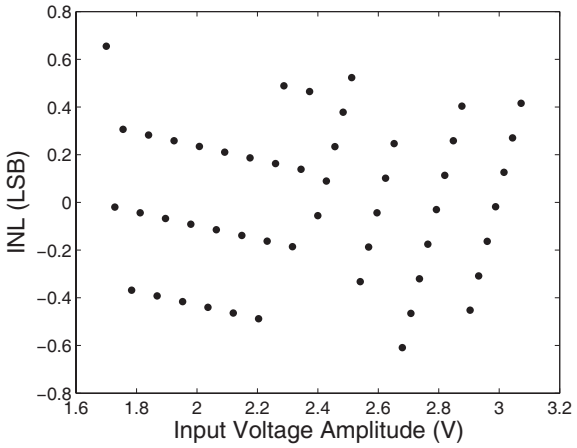


Figure 3.46: Measured INL of the 8 bit clock-less A/D converter.

Chapter 4

Conclusions and Future Work

This work presents the design of the integrated readout circuits for sensory microsystems. The specialities in low noise and low power are emphasized as the key requirements in the system implementation. A gas sensing system and a radiation detection system are analyzed as two examples of microsystems.

4.1 Gas Sensing System

In the gas sensing system, the metal-oxide gas sensor indicates the concentration of the target gas by the variation of its own resistance. The proposed readout IC system is able to compensate for the deviation of large baseline resistance across sensors and reduce the necessary resolution of ADC without sacrificing any accuracy. The design principle of the system is illustrated and two operation modes are introduced. The readout circuit is designed to be compatible to the sensor baseline resistance from 1 kΩ to 100 MΩ and guarantee error rate less than 0.045 %.

The architecture of the segmented current-steering D/A converter is analyzed. Comparison is made between the binary coded and thermometer coded architecture. The sizes of the transistors are optimized to reduce the error caused by the fabrication mismatch.

The design of 13-bit current mode incremental delta-sigma A/D converter is

presented including integrator, 1-bit feedback DAC, comparator and decimator. The parameters of components are theoretically calculated to meet with the requirements on the dynamic range and power consumption. The system is simulated to achieve $\pm$0.4 LSB INL and low power consumption on the order of 400 μW by limiting the current flowing through the resistive sensor.

Gas sensing system based on the board level is designed and provides accurate measurement with the gas sensor as input, which verify the feasibility of the system architecture. The ASIC layout was implemented with AMI 0.5 μm CMOS process and fabricated through MOSIS.

A complete test of the gas sensor readout ASIC will be the next step. The linearity of the current steering DAC and Delta-Sigma ADC is going to be recorded separately. Experiments are going to be conducted on the entire system to measure its sensitivity to the minimum resistance change, the detectable range of the sensor baseline resistance and the output signal linearity.

Based on the verification of the system performance, long time measurement with the gas sensor and concealed gas chamber can be conducted to witness the stability of the system. The implementation of an impact and portable breath analyzer which can measure the target gas concentration under room temperature is the final stage of the work.

4.2 Radiation Detection System

In the radiation detection system, a semiconductor scintillator with large area epitaxial photodiode is able to detect the emission of radiation particles and generate input electric charge to the front-end readout circuit. The high sensitivity of the detector has advantage at its big input load capacitance up to 50 pF. The proposed readout circuits are composed with a two-stage charge sensitive amplifier, a third order semi-Gaussian RC pulse shaper with baseline holder, a peak detector and a clock-less A/D converter.

By optimizing the size of the charge amplifier input transistor as well as the

peaking time of the pulse shaper, an optimal equivalent noise charge can be achieved with a relatively large input load capacitance. The accurate model of the moderate inverted input transistor and its white noise and flicker noise calculation are discussed.

This work also presents the circuit design of CSA including voltage amplifier, feedback network and charge gain distribution. Due to its low complexity, RC filter is used as the pulse shaper. However, peaking time has to be compromised to reduce the excessive area consumption of the RC filter. As a competent solution, the design of Gm-C filter is analyzed. Source degeneration and current division techniques are adopted to lower the transconductance of OTAs in the Gm-C filter. With capacitance attenuation, Gm-C filter is proven to achieve large time constant, high linearity and signal-to-noise ratio.

The implementation theory of the 8-bit clock-less time-based A/D converter is elaborated. Operated in continuous time, the ADC minimizes the switch noise interference on the low-noise CSA stage. Dual integrators and high speed comparator are introduced to eliminate the error sources of the ADC and improve the linearity.

After the simulation of each module in the readout circuits, the designed front-end readout system is implemented with AMI 0.5 μm CMOS process and the prototype chip is taped out. The chip die of the ASIC is directly mounted on the test PCB to assure the smallest parasitic capacitance at the input node. Based on the experiments result, the optimum equivalent noise charge level reaches 103 e^- without detector connected and increases 4.5 e^- every pF of input capacitance. With the semiconductor scintillator connected, the measured ENC is 334 electrons. The non-linearity of the system is smaller than $\pm 1\%$ for the entire input charge range from 3 ke^- to 100 ke^-. The power consumption of one channel of ASIC is 2.2 mW.

Since the Gm-C filter has been analyzed to possess advantage in large time constant shaper implementation and the improvement of its linearity and SNR is worth further research, a radiation detection system with Gm-C filter as the pulse

shaper could be a direction of future work. Moreover, based on the tuning technique of the OTA transconductance, the peaking time of the Gm-C shaper can be adjusted as well. A shaper with adaptable or programmable peaking time is able to search for the minimum system output noise in real time, according to the present input capacitance and leakage current of the detector.

On the other hand, how to generate a fixed time period which is independent on the temperature and fabrication process will be the next step of the clock-less ADC design. A portable and hand-held structure of the system is still the target to be achieved.

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