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Design Methodologies to Manage Switching Noise with Applications to Biomedical Acoustic Systems

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Abstract of the Dissertation

Design Methodologies to Manage Switching Noise with Applications to Biomedical Acoustic Systems

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Noise and power efficiency are two critical issues in modern integrated circuits (ICs) that highly impact the system performance. Due to the high density of circuits, different circuit modules are integrated on the same die. Specifically, in a mixed-signal environment, switching noise due to substrate coupling propagates from digital circuits to analog parts. Furthermore, analog circuits also suffer from the intrinsic device noise such as thermal, flicker and shot noise. Thus, a challenging issue during the design process of analog circuits is the evaluation of the dominant noise source. An analysis flow is proposed to understand the dominance characteristics of switching noise and device noise in two commonly used amplifiers. The frequencies at which the input device and switching noise are equal have been determined to provide guidelines for signal isolation process.

Power supply noise is known as a primary source of switching noise. Voltage regulators are typically used to ensure stable power supply voltage with tolerable noise. A buck voltage regulator with 87% power efficiency is introduced in this thesis. Typical buck converters with on-chip inductors have high switching frequency to reduce the stringent inductor size. In this research, the voltage regulator consists of spiral inductors that are embedded within the flip-chip package structure. Inductors with relatively high quality factors are built by utilizing the flexibility of the package space, enabling a relatively low switching frequency of the buck converter. Low switching frequency reduces the dynamic loss, thereby increasing the overall conversion efficiency of the regulator.

The proposed methodologies to manage noise are utilized while developing ultrasound transducers with application to bone density diagnosis and treatment. Furthermore, these methodologies can also serve as a framework to minimize the undesirable artifacts during the ultrasound B-mode imaging process. Several research studies related to ultrasound transducer development and front-end circuit design are introduced in the second part of this thesis. Ultrasound scanning is noninvasive compared to other medical imaging techniques such as computerized tomography (CT) and magnetic resonance imaging (MRI) scan. Ultrasound therefore can be applied to human beings on a daily basis for bone density treatment.

A software controlled flexible ultrasound system with two-dimensional (2-D) dual array transducer is proposed for noninvasive bone density diagnosis and bone loss treatment. Transmitting (Tx) transducer elements are divided into sub-blocks to excite ultrasound signals in sequence to significantly decrease the system complexity while maintaining beam pattern properties through signal processing at receiving (Rx) side. Apodization is also applied to reduce side lobes and to make the resolution in the field of view (FOV) more uniform.

A 5 by 5 phased array low intensity pulse ultrasound system is developed for therapeutic purpose to prevent bone density loss as well as enhance nonunion bone fracture. Electrical pulses generated from the embedded system based electrical control box are converted into ultrasound signals and are excited in a certain time sequence to reach the focal point simultaneously. Sufficient energy intensity is achieved with an ultrasound pulse that has a duty cycle less than 12%. Dynamic targets are realized to accumulate energy to a specific area. The proposed methodologies in this thesis enable robust ultrasound transducers that can be used for enhanced bone density diagnosis and treatment.

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Chapter 1

Introduction

In the past several decades, noise, power consumption and dense integration have been some of the primary concerns during IC design process. These challenges are summarized in Section 1.1. Some of the methodologies to alleviate these challenges are also applicable to the development of robust ultrasound transducers to be used in a microgravity environment. Some of the challenges on developing ultrasound transducers are reviewed in Section 1.2. The outline of this thesis is provided in Section 1.3.

1.1 Primary Challenges in Mixed-Signal Integrated Circuits

In mixed-signal ICs, substrate coupling noise has long been a critical issue due to dense and monolithic integration of analog/RF and digital components on the same die. Switching (also referred to as induced) noise caused by a transition of

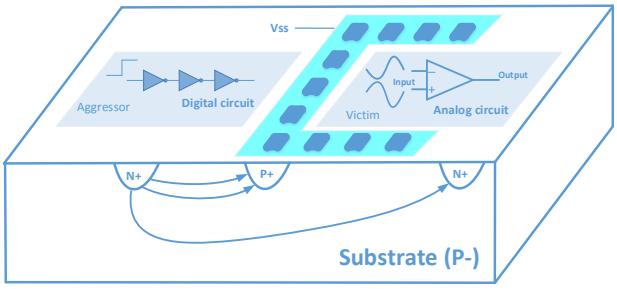


Figure 1.1: **Switching noise coupling from a digital block to a sensitive analog circuit in the presence of guard rings.**

a digital signal propagates through the substrate and reaches an analog/RF circuit, degrading important performance specifications such as signal-to-noise ratio, gain, and bandwidth, as shown in Fig. 1.1 [1–4].

Heterogeneous integration and faster transition times exacerbate the issue of switching noise in sensitive analog/RF blocks. In addition to induced noise, analog/RF circuits also suffer from intrinsic device noise such as thermal [5], flicker [6], and shot noise [7]. Traditional analog design flows typically focus on intrinsic noise since extensive analysis and simulation methods exist [8,9]. Alternatively, the analysis of switching noise and substrate coupling is challenging due to prohibitive computational complexity. Accurate estimation of the substrate noise at the bulk node of an analog/RF transistor requires simultaneous consideration of the digital switching activity, power/ground networks, and the substrate network [10].

Significant effort has been made to characterize and efficiently analyze substrate noise coupling. For example, in [11] and [12], experimental circuits have been used to model substrate noise in a mixed-signal environment and several isolation strategies have been introduced. In [13], a simplified equivalent circuit has been developed to model switching noise and its effects on analog-to-digital converter

and voltage-controlled oscillator. Specific logic gates have been used in [14] to model and detect switching noise in digital circuits. In [15], a voltage comparator has been designed as a noise detector to measure the equivalent substrate noise waveforms. The uniformity of the voltages on the ground distribution network is exploited in [16] to efficiently analyze substrate noise coupling.

These research works primarily focus on the estimation of switching noise at the victim circuits. For analog design flows, it is also important to evaluate the significance of switching noise and understand the conditions under which switching noise starts to be dominant. This evaluation is important since conventional noise mitigation techniques (such as guard rings [17], deep-N well [18], slew/skew control [19], power network optimization [20]) typically aim at reducing switching noise amplitude at the expense of area and power consumption. It is therefore critical to determine the required reduction in switching noise amplitude to minimize the overhead. The analytic expressions provided in this thesis are utilized to determine the peak amplitude of switching noise (in the time domain) that makes the input-referred switching and device noise the same in the frequency domain. This criterion is used to evaluate the significance of switching noise.

An important circuit module that has significant impact on switching noise is the voltage regulator. An AC signal is first converted to DC voltage through an AC-DC regulator. The power management system then converts the single DC voltage to multiple different DC values through DC-DC converters. The power efficiency of a DC-DC voltage regulator is a significant design parameter. There are primarily three types of voltage converters: 1) linear converters such as low-dropout (LDO) regulators, 2) switched-capacitor based DC-DC converters, and 3) switching buck converters. LDO regulators are cost effective and have relatively fast transient re-

sponse, but these regulators suffer from low power efficiency, less than 60% in most of the cases [21]. This limitation is exacerbated as the conversion ratio increases or output voltage decreases. Switched-capacitor converters exhibit enhanced power efficiency, but suffer from poor regulation capability since the switching frequency should be modified to regulate the output. This process is slow since a voltage controlled oscillator is needed to vary the switching frequency, increasing the response time. Finally, switching buck converters can achieve high efficiency and large output current at the expense of a high quality inductor. Since integrating a high quality inductor on-chip is highly costly, buck regulators typically consist of an external, discrete inductor. Existing work has also investigated the feasibility of increasing switching frequency to reduce the required inductance. In this case, however, the dynamic loss increases, thereby reducing the power efficiency [22]. Thus, it is challenging to develop a high efficiency DC - DC voltage converter while still considering other design characteristics such as area and transient response.

Another important research objective in this thesis is to develop two ultrasound systems that include the ultrasound transducer as well as control system. Ultrasound signals are converted from electrical pulse signals. In order to fire desired ultrasound signals, reliable high voltage and high frequency electrical signals should be first obtained. Noise and power efficiency are two primary design parameters during this process. The proposed methodologies to manage noise and enhance power efficiency can be applied in a practical ultrasound system, as shown in Fig. 1.2.

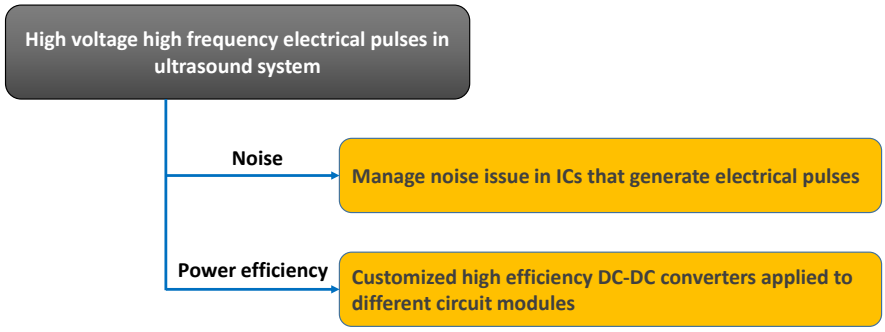


Figure 1.2: **The applicability of low noise and high power efficiency in ultrasound transducers.**

1.2 Challenges in Developing Ultrasound Transducer Systems

This thesis provides design solutions for two types of phased array ultrasound transducers to be used in a micro-gravity environment as well as for clinical purposes. Astronauts who live and study in international space station (ISS) typically lose 2% bone mass each month due to the micro-gravity environment [23]. Furthermore, astronauts are under the risk of extensive bone loss during long term space trip due to the radiation exposure. As indicated in Fig. 1.3, bone density loss is approximately 20% in 15 months in micro-gravity environment. This bone loss places astronauts in high threat of bone fracture. Alternatively, osteopenia and osteoporosis are two critical problems in aging population and in functional disuse conditions. Osteoporosis diminishes both the structure and strength of bone, and each is considered critical for resistance to fracture [24, 25]. Ultrasound transducer is thus applied as a noninvasive scanning acoustic method for bone density loss treatment as well as bone architecture diagnosis. Ultrasound could accelerate healing of fresh fractures and influence various stages of the healing process (inflammation, repair,

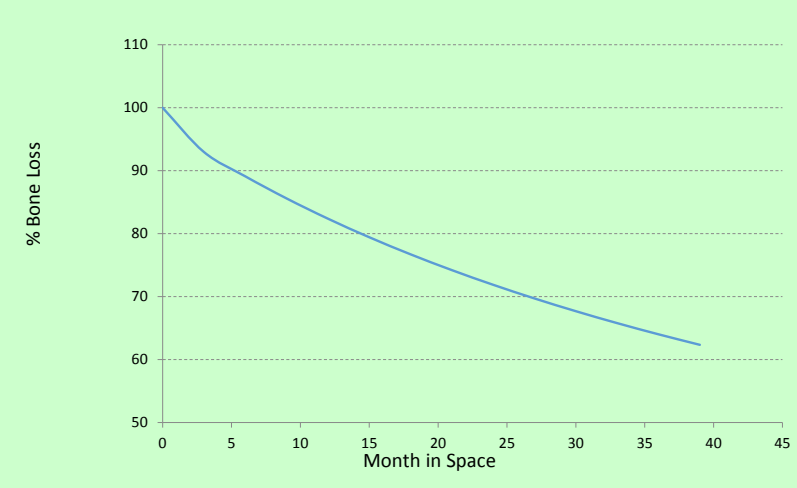


Figure 1.3: Prediction of percent bone loss in microgravity [23].

and remodeling) via enhancement of angiogenic, chondrogenic and osteogenic activity [26, 27]. Ultrasound transducers are devices that convert electrical energy to ultrasound waves through piezoelectric crystals and are widely applied in medical field for diagnosis and therapeutics. The most significant contribution of ultrasound transducer to medical imaging is its noninvasive characteristics as compared to magnetic resonance imaging (MRI) and X-ray computed tomography (CT) scan.

It is widely accepted that quantitative ultrasound (QUS) can serve as a noninvasive modality to characterize tissue quantity for fracture risk [28–30] and predict fracture risk [31]. Recent studies describe the interaction between trabecular bone structural alignment and ultrasound waves [32–34]. While traditional QUS measurement, particularly of the human calcaneus, is performed in medial-lateral orientation through parallel wave propagation, the results of previous work indicate that confocal based QUS measurement can determine the structural alignment of trabecular bone and correlate strongly with mechanical properties of the trabecular bone density and strength using either mechanical scan or 1-D linear array

scan [34]. However, QUS meets the problem of relatively low scan quality and long scan time. Also, software-based ultrasound is preferred over conventional systems as this is a more radiation tolerant approach for outer space. A new flexible ultrasound system (FUS) is introduced to meet the requirements and improve the performance based on QUS. It has been demonstrated that phased-array ultrasound can be used for configuring spatial focal zone and perform noninvasive characterization of trabecular bone quality. Such sensor configuration can also be integrated into existing ultrasound triggering, data analysis, demultiplexer and imaging system in a flexible ultrasound platform. The primary goal of the study introduced in Chapter 5 is focused on the unique dual 2-D array transducer kit design and simulation of a flexible ultrasound system for trabecular bone assessment. Transmission (Tx) and receiving (Rx) transducers are designed as two identical 2-D array sensors, with elements arrayed in 27 by 27 within a square. Tx elements are divided into sub-blocks to excite ultrasound signal in sequence to decrease the system complexity while maintaining beam pattern properties by the signal processing procedure at Rx side. The results suggest that the reduced array size (27 by 27) highly simplifies the design and manufacturing, but maintains the image/signal resolution.

The design and development of a 5 by 5 low intensity pulsed ultrasound system (LIPUS) is also introduced in this thesis in order to check the therapeutic possibility of the low intensity ultrasound energy device, particularly with application to bone fracture prevention and nonunion fracture enhancement. The largest advantage of this device is the portable characteristics. Unlike FUS which is based on *GE* Vivid E95 ultrasound machine, LIPUS electrical signal control box is only half the size of a piece of letter paper and provides ease of daily use. Also, the ultrasound wave intensity is adjustable based on specific treatment requirement.

1.3 Outline

In this thesis, research results on switching noise in analog circuits and in-package voltage converter are presented. Design and development of FUS and LIPUS are also described. In Chapter 2, statistical noise characteristics and different noise types are summarized to provide background. Voltage regulator characteristics and a detailed introduction to switching buck converters are also provided. Ultrasound signal characteristics as well as ultrasound transducer principles are then introduced.

In Chapter 3, an analysis flow is proposed to determine the significance of induced (switching) noise in analog circuits. The proposed flow is exemplified through two commonly used amplifier topologies. Specifically, *input-referred switching noise* is introduced as the first figure-of-merit and compared with the well-known equivalent input device noise through analytic expressions. Furthermore, time domain switching noise amplitude (at the bulk node) at which the input device and switching noise magnitude are equal (in the frequency domain) is determined as the second figure-of-merit, providing guidelines for the signal isolation process. Reverse body biasing is also proposed to alleviate the effect of switching noise by weakening the bulk-to-input transfer function as opposed to reducing the switching noise amplitude at the bulk nodes. It is demonstrated that this method has negligible effect on primary design objectives of the victim circuit while reducing the input-referred switching noise by up to 10 dB. As a case study, the proposed flow is applied to a potentiostat circuitry where input sensitivity is of primary importance.

In Chapter 4, the design and characterization process of a package-embedded spiral inductor is investigated via comprehensive electromagnetic simulations. A realistic, multi-layer flip-chip package is considered and modeled in a full wave elec-

tromagnetic simulator, *ANSYS HFSS*. At constant package area, parasitic resistance of a given inductance is minimized. In the next step, the applicability of the proposed package-embedded spiral inductor to a DC-DC switching buck converter is demonstrated. The flexibility of the package is exploited to obtain a relatively high inductance, enabling a reduced switching frequency. Lower switching frequency minimizes the dynamic loss, thereby increasing the power efficiency. Finally, an interleaved multi-phase buck regulator with an *array of package-embedded spiral inductors* is developed.

In Chapter 5, a software controlled flexible ultrasound system with 2-D dual array transducer is proposed for noninvasive bone density diagnosis and bone loss treatment. Tx transducer elements are divided into sub-blocks to excite ultrasound signal in sequence to decrease the system complexity while maintaining beam pattern properties by the signal processing procedure at Rx side. Appropriate delay modules are inserted into the process of signal exciting. The gray-scale images are simulated by using *FIELD II* program, acoustic resolution and side lobes are analyzed. Apodization is also applied to reduce side lobes as well as to make the resolution in the field of view (FOV) more uniform. The sub-block structure hardware design which includes the circuit schematic to distribute the analog signals from *GE* adaptor to transducer elements is also proposed.

In Chapter 6, the design and development of a low intensity pulsed ultrasound system is proposed. An embedded system based control box is designed and programmed to generate electrical pulse signals. The electrical pulses are converted to ultrasound pulses through a 5 by 5 transducer. Each element has a certain delay module to ensure that all of the 25 ultrasound signals reach the focal point in phase so that the maximum intensity is achieved for each focal point. Intensity can be

changed for specific treatment purpose by adjusting the pulse duration as well as pulse repetition frequency.

Finally, the thesis is concluded in Chapter 7. Possible future research directions are discussed.

Chapter 2

Background

To investigate the primary noise issues in mixed-signal ICs and develop methodologies to evaluate and reduce the dominant noise effect, noise characteristics as well as different noise types should be understood. The statistical characteristics of device and switching noise are introduced in Section 2.1. DC-DC converter is a critical module for power and noise management. Energy efficiency of the DC-DC converters highly depends on the converter topology and determines the converter quality. Several DC-DC converter module parameters and primary topologies are provided in Section 2.2. Developing robust acoustic ultrasound transducers with application to medicine is another research direction in this thesis. Ultrasound transducers are widely applied in medical field to help the process of therapeutic and diagnosis. Ultrasound transducer characteristics, beam-forming and imaging properties are discussed in Section 2.3.

2.1 Electronic Noise

Electronic noise refers to the random unwanted electrical signal that limits the performance and precision of circuits. As noise is represented by random fluctuations, average power (rather than instantaneous power) is typically characterized. Statistical methods applied to analyze noise are discussed in Section 2.1.1. Two primary categories of noise, device and switching noise, are introduced in Section 2.1.2 and Section 2.1.3.

2.1.1 Statistical characteristics

Since noise is a random signal, instantaneous values cannot correctly represent the real power of noise. Thus, average power and average power spectral density are calculated to analyze noise.

The average power of a sinusoidal signal can be calculated as the sum of the instantaneous power of a cycle and over the period [35]

$$Average\ power\ consumption = \frac{1}{T}\int_0^T \frac{V_p^2 \sin^2(2\pi\frac{t}{T})}{R}dt, \tag{2.1}$$

where V_p is the amplitude of the sinusoidal signal and R is the resistance. Mean square voltage thus equals to average power consumption multiplied by R,

$$Mean\ square\ voltage = \frac{1}{T}\int_0^T V_p^2 \sin^2(2\pi\frac{t}{T})dt = \frac{V_p^2}{2}, \tag{2.2}$$

where the unit of mean squared voltage is v^2. Root mean square (RMS) value is the square root of mean square voltage value and represents DC voltage with the

resistor R that has the power dissipation calculated above.

Power spectral density (PSD) is used to measure the power intensity in the frequency domain with the unit of W/Hz and is widely used to quantify the value of noise. The expression of PSD is

$$PSD = \frac{mean\ squared\ voltage}{R \times frequency}, \tag{2.3}$$

where the unit V^2 / Hz and A^2 / Hz are used, respectively, for voltage and current source [35].

2.1.2 Device Electronic Noise

Device noise refers to the random intrinsic noise observed in electrical devices. Due to the random characteristics, device noise should be analyzed by statistical methods such as mean and variance values instead of the instantaneous value. Power spectral density is a typical parameter that represents the strength of the noise as a function of frequency, as discussed previously. Three primary types of device noise are thermal, flicker and shot noise, as provided below. Flicker noise is reduced as frequency increases while the other two are frequency independent.

2.1.2.1 Thermal Noise

Thermal noise, or Johnson - Nyquist noise, originates from random thermal motion of electrons in a conductor regardless of average current. The resistor thermal noise is modeled as a voltage source connected in series which has the power spectral density

$$S_v(f) = 4kTR, \tag{2.4}$$

where k is the Boltzmann constant and is equal to $1.38 \times 10^{-}23$ J/K, T is the temperature in Kelvin and R is the resistor [36]. Note that the bandwidth is 1 Hz. As indicated by the equation, thermal noise is proportional to the temperature. Note that thermal noise is a white noise as noise spectral density is independent of frequency.

Thermal noise also exists in a MOS transistor channel. This noise is modeled as a current source from drain to source and is equal to

$$S_v(f) = 4kT\gamma g_m, \tag{2.5}$$

where γ is the coefficient that is approximately equal to 2/3 for long channel transistors, g_m is the transconductance of the transistor.

2.1.2.2 Flicker Noise

Flicker noise, also referred to $1/f$ noise, is another device noise that is present in MOS transistors. Flicker noise is caused by the fact that the charge carriers are trapped and released by the energy coming from the bonds located at the silicon surface. Flicker noise can be modeled as a voltage source connected in series with the transistor gate node and is inversely proportional with the frequency

$$S_v(f) = \frac{K}{C_{ox}WLf}, \tag{2.6}$$

where K is a process-dependent constant, C_{ox} is gate capacitance per unit area, W and L are, respectively, width and length of a transistor [36]. Due to the frequency dependent characteristics, flicker noise is considered as the primary device noise

source at relatively low frequencies. MOS transistor device noise is therefore dominated by flicker noise at relatively low frequencies and thermal noise dominates after the cross-over frequency.

2.1.2.3 Shot Noise

Shot noise is generated by the discrete nature of electric charge that causes nonuniform current flow. This noise increases as the average current flow increases. Shot noise has a constant power spectral density at a fixed current [4]

$$S_v(f) = 2qI, \tag{2.7}$$

where q is the electrical charge and I is the bias current.

2.1.3 Switching Noise

Switching noise is generated by the switching activity of digital signals. Three primary switching noise types are interconnect, power / ground and substrate coupling noise.

2.1.3.1 Interconnect Noise

As the device and interconnect sizes are down to sub-micron level, interconnect coupling noise becomes one of the major issues. Two categories of interconnect noise are capacitive and inductive coupling.

Two types of capacitances among interconnects are parallel plate capacitance and coupling capacitance. Parallel plate interconnect capacitance depends upon the

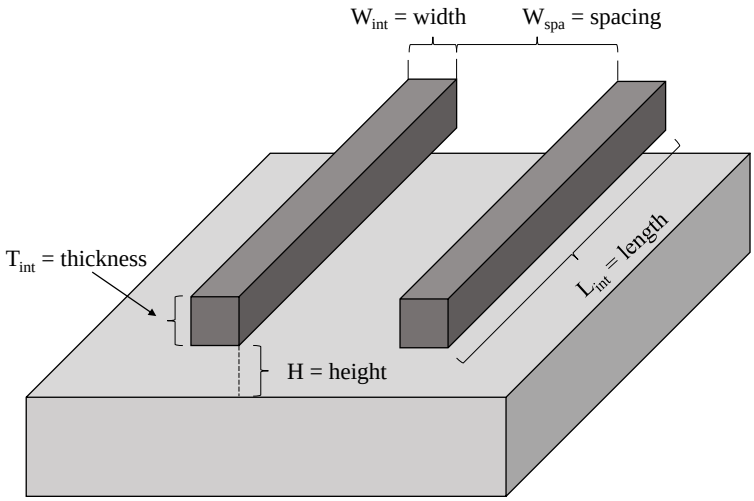


Figure 2.1: **Two parallel conductors located above a substrate layer.**

overlapping area as well as the spacing between two adjacent metal lines. For a metal line to the substrate as shown in Fig. 2.1, the parallel plate capacitance is

$$C_{pp} = \frac{\varepsilon L_{int} W_{int}}{H}, \tag{2.8}$$

where ε is insulator dielectric constant [4].

Coupling capacitance between two interconnects is proportional to the overlapping area and inversely proportional to the spacing between the metal lines. The coupling capacitance is determined by

$$C_c = \frac{\varepsilon L_{int} T_{int}}{W_{spa}}. \tag{2.9}$$

For two long parallel transmission lines, as shown in Fig. 2.2, total interconnect capacitance depends on the value of C_c, C_{pp} as well as the signal switching direction in both of the lines. With two transmission lines switching in the same direction,

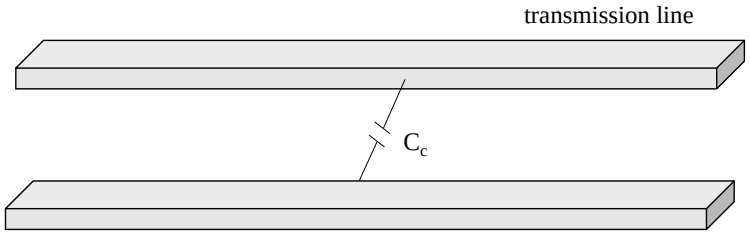


Figure 2.2: **Capacitively coupled interconnects.**

total capacitance is C_{pp}, whereas if the interconnects carry out-of-phase signals, the capacitance increases to $2 \times C_c + C_{pp}$.

2.1.3.2 Power Supply Noise

Power supply noise (PSN) refers to voltage fluctuations along the power / ground distribution network. PSN limits the performance and reliability of the circuit by causing delay uncertainty and logical failure [4]. Power / ground distribution network is resistive and inductive in nature. Two types of noise exist in the power / ground network: *IR* drop and *Ldi / dt* noise. Switching signal in high frequency causes the switching current to flow through the power / ground network. Power supply voltage drops as this current flows through the network resistance and can produce delay uncertainty and degrades the system reliability.

Circuits with increasingly higher speed also lead to *Ldi / dt* noise. *Ldi / dt* noise therefore increases with switching speed and current load.

2.1.3.3 Substrate Coupling Noise

To reduce the overall fabrication cost, digital circuits typically share the same die with analog / RF blocks in mixed-signal ICs. Switching noise from digital

circuits may propagate through the monolithic substrate and affect the performance of analog / RF circuits. Digital circuits behave as aggressor circuit while analog / RF circuits are the victim blocks. Two different types of substrate exist. Bulk type substrate is lightly doped and with high resistivity, while an *epi* type substrate includes a high resistivity layer above the low resistivity substrate [4]. Due to the high impedance characteristics of the bulk type substrate, current flow throughout the substrate is near the surface. Alternatively, in *epi* type substrates, current flows deeper to reach the low resistivity bulk. Since the bulk potential fluctuates due to current flow, body effect causes the transistor threshold voltage to change.

2.2 DC-DC Voltage Regulator

Voltage regulator is a circuit block to generate and maintain a constant electrical DC voltage and distribute this regulated DC voltage to the circuit. A system may include multiple circuit modules with a different power supply voltage. In order to satisfy the power supply for various circuit modules, multiple DC-DC converters are used. Voltage regulators also isolate the circuit from system level power fluctuations.

There are two kinds of DC-DC converters, boost and buck converters. Boost converter steps up the voltage producing an output voltage that is higher than the input voltage. Alternatively, buck converter is used to step down the voltage. Primary DC-DC converter characteristics are introduced in Section 2.2.1, two DC-DC converter topologies are discussed in Sections 2.2.2 and 2.2.3.

2.2.1 DC-DC Converter Characteristics

The quality of a DC-DC converter affects the performance of other circuits. Ideally, the output voltage should remain constant regardless of the output load current and input voltage. DC-DC converter load regulation efficiency is expressed as

$$\beta_{load} = \frac{V_o^{max,load} - V_o^{min,load}}{V_{o,ref}}, \tag{2.10}$$

where $V_o^{max,load}$ and $V_o^{min,load}$ are, respectively, the output voltage when the load current reaches maximum and minimum values, $V_{o,ref}$ is the reference output voltage. Small β_{load} indicates that the effect of load current on output voltage is small [4].

Power efficiency is a significant parameter for a DC-DC converter and is expressed as

$$\eta = \frac{P_o}{P_{in}} = \frac{V_o I_o}{V_{in} I_{in}}, \tag{2.11}$$

where P_o and P_{in} are output and input power, respectively. An ideal DC-DC converter should reach 100% efficiency even at full load, however, DC-DC converter has parasitic impedances that degrade converter efficiency. DC-DC converters dissipate internal power and the amount of power loss highly depends upon the topology and the size of the components.

2.2.2 Linear Regulators

A linear regulator consists of power transistor and a control circuit module, as shown in Fig. 2.3. Control circuit is typically an error amplifier. The regulated output voltage is fed back to the error amplifier and compared with the reference voltage. Power transistor works as a variable resistor and the value depends on the

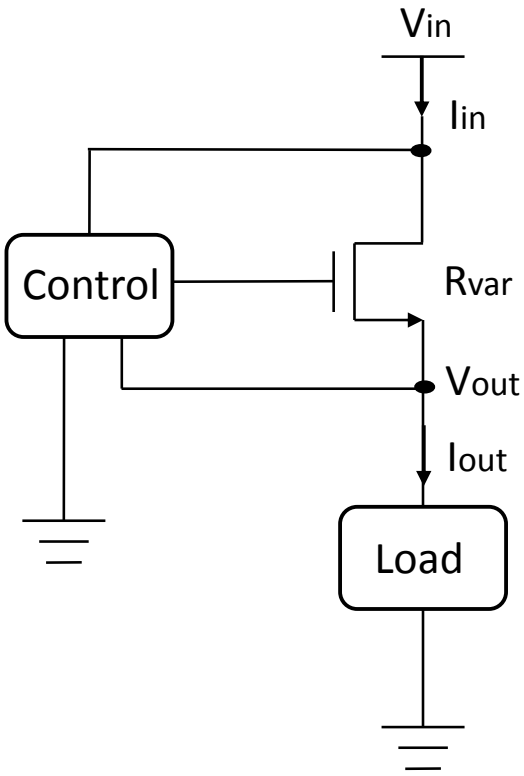


Figure 2.3: **Conceptual schematic of a linear regulator.**

output of the control circuits.

Linear regulator is built without any inductors and thus the consumed area is relatively small. However, linear regulators suffer from low power efficiency. Input current partly flows through the control circuits and the output current is not equal to the input current. Thus, the current efficiency is relatively low. Both control circuit module and power transistor consume power and the overall power efficiency is relatively low compared to other DC-DC converter topologies. Also, the output voltage is not adjustable as the control circuit has a fixed reference voltage.

2.2.3 Switching Buck DC-DC Converters

Switching buck converter is a step down DC-DC converter to supply power to various circuit modules such as CPU core, memory core, or accelerator module. A typical single-phase buck converter consists of 1) a switch network that generates an AC signal $V_s(t)$, 2) a second order low pass filter that passes the DC component of the AC signal to the output, and 3) feedback path that regulates the output voltage by changing the duty cycle of the AC signal. The schematic is shown in Fig. 2.4, where the drain of NMOS is the AC signal $V_s(t)$ which is operated in two phases as shown Fig. 2.5 [4]. During phase one, $V_s(t)$ is equal to the value of V_{in} as the PMOS power transistor is on. This phase lasts for DT_s, where D is the duty cycle and T_s is the switching period. When NMOS turns on during phase two, the $V_s(t)$ is connected to ground and is equal to zero. $V_s(t)$ then passes through a low pass filter and leaves the DC component to the output node which is indicated as

$$V_{out} = \frac{1}{T_s}\int_0^{T_s} V_s(t)dt = DV_{in}. \tag{2.12}$$

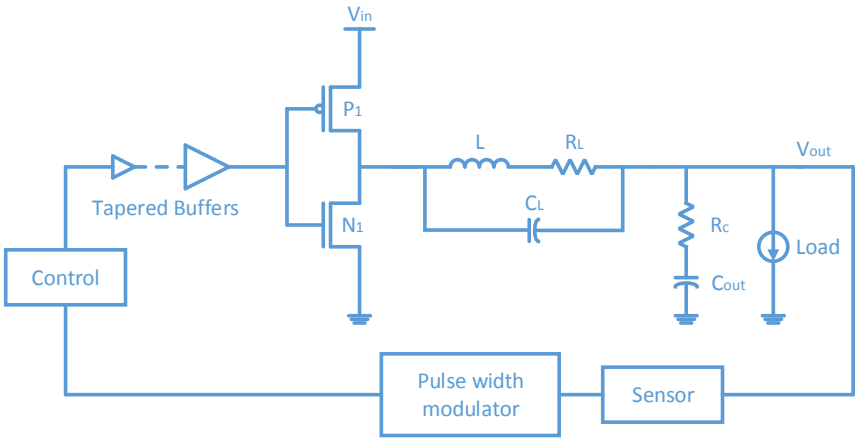


Figure 2.4: **Conceptual schematic of a switching buck converter.**

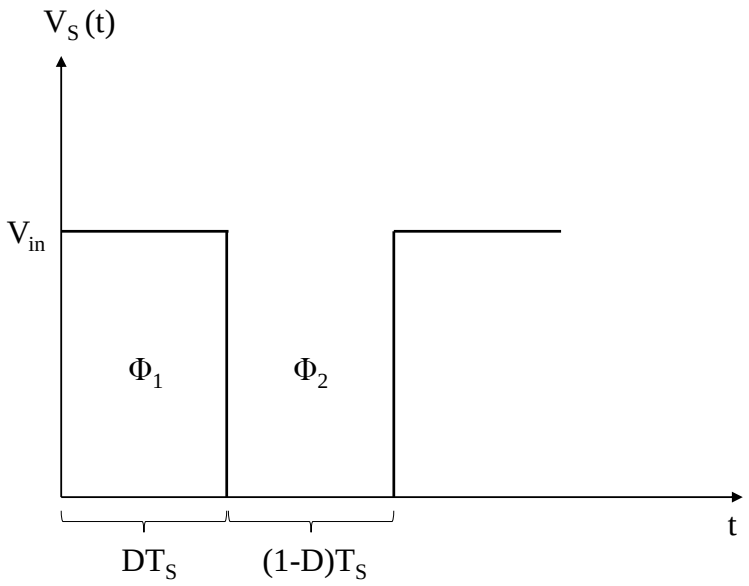


Figure 2.5: **Voltage $V_s(t)$ value in two phases where T_s is switching period and D is duty cycle.**

Note that the filter cutoff frequency is much smaller than the switching frequency in order to block the AC part of $V_s(t)$. Since the duty cycle cannot be larger than one, this DC-DC converter topology cannot boost the input voltage. A small amount of ripple voltage due to nonideal low pass filter is superimposed on the DC component and the final V_{out} is

$$V_{out}(t) = V_{out} + V_{ripple}(t). \tag{2.13}$$

The procedure to determine the inductor and capacitor of the low pass filter is as follows. Voltage across the inductor is the difference between input and output voltages. V_L equals to V_{in} - V_{out} in phase one, and since $V_s(t)$ is connected to ground in phase two, V_L is - V_{out}. Thus, inductor current slope in two phases are

$$\frac{dI_{L\phi 1}}{dt} \approx \frac{V_{in} - V_{out}}{L}, \tag{2.14}$$

$$\frac{dI_{L\phi 2}}{dt} \approx \frac{-V_{out}}{L}, \tag{2.15}$$

and the peak-to-peak current is equal to

$$\Delta I_{Lp-p} = 2 \times \Delta I_L = \frac{V_{in} - V_{out}}{L} DT_s. \tag{2.16}$$

ΔI_L is then equal to

$$\Delta I_L = \frac{V_{in} - V_{out}}{2L} DT_s. \tag{2.17}$$

This ripple current flows through the capacitor and causes capacitor voltage fluctuations. This is the output ripple voltage indicated in (2.13).

The capacitor voltage fluctuation is shown in Fig. 2.6. The capacitor is charged when the current is positive and discharged when the current is negative. The overall

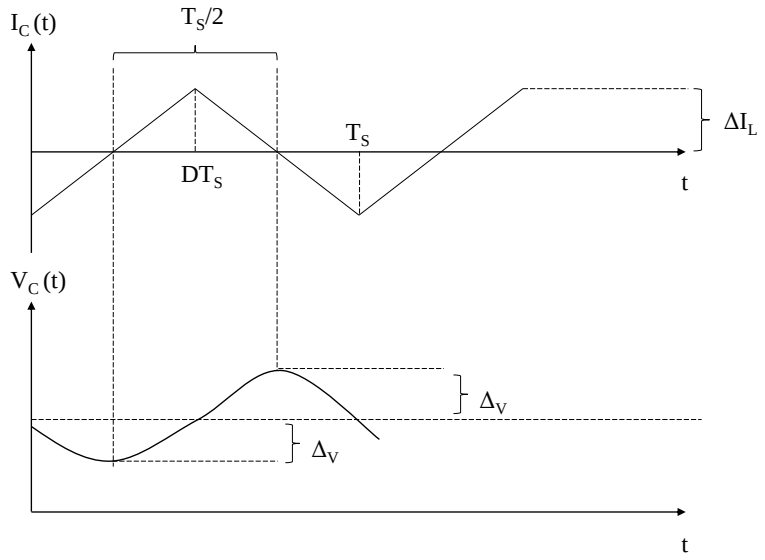


Figure 2.6: **Current and voltage waveform of capacitor in time domain.**

charge q is

$$q = C \times 2\Delta v = \frac{1}{2}\frac{T_s}{2}\Delta I_L. \tag{2.18}$$

The output ripple is extracted and is expressed as

$$\Delta v = \frac{\Delta I_L}{8Cf_s}. \tag{2.19}$$

Typical design specifications of a switching buck converter include the power efficiency, output current, voltage ripple, and transient response. The low pass filter, consisting of an inductor and capacitor, is a critical element within the the buck converter since the output voltage characteristics depend upon the quality of this filter. The parasitic effective series resistance (ESR) of the inductor plays an important role in the resistive loss and the overall performance of the buck converter. A larger inductance (required to reduce ripple) typically produces a larger ESR, which

in turn increases the resistive loss and causes a non-negligible voltage drop at the output, particularly if the load current is sufficiently high.

2.3 Acoustic Ultrasound Transducer

Ultrasound transducer is an energy converting device that converts electrical pulse signal into ultrasound signal and transmits the ultrasound waves. The transducer can also work in a reverse manner to receive ultrasound echoes and convert the echoes back to electrical signals. Different types of ultrasound transducers have been widely applied in medical field to better support clinical decisions. Ultrasound waveform characteristics are introduced in Section 2.3.1. Transducer physics, types and the corresponding beam forming principle are discussed in Section 2.3.2. Ultrasound imaging formation and properties are provided in Section 2.3.3.

2.3.1 Ultrasound Waveform Characteristics

Ultrasound waveform refers to acoustic waveform with frequency above 20 kHz, which exceeds the audible range for humans. Ultrasound waveforms are longitudinal waves where the particles move back and forth along the same direction as the waveform propagation. High pressure of the wave appears at the places where particles move towards each other while low pressure appears at the places where particles move apart from each other. Note that the particles do not move along with the propagation of the waveform but keep oscillating backward and forward.

Ultrasound wavelength can be calculated as

$$\lambda = c/f, \tag{2.20}$$

Medium	Speed of sound (m/s)
Air	333
Water	1480
Bone	3190-3406
Average tissue	1540
Fat	1430
Liver	1578
Muscle	1585

Table 2.1: Speed of sound in medium.

where λ is wavelength, c is speed of sound and f is frequency. As seen from the equation, with a fixed speed of sound, wavelength is inversely proportional to frequency. The speed that sound travels through highly depends on the density and stiffness of the medium material and is expressed as

$$c = \sqrt{k/\rho}, \tag{2.21}$$

where k is stiffness and ρ is density. Table 2.1 shows various speed of sound values in some typical mediums. Three important characteristics can be seen from the table: 1) different human tissues have similar speed of sound and thus an average tissue speed of sound can be used for all the human tissues for simplicity; 2) ultrasound waves can hardly pass through air due to the high compressibility; 3) ultrasound signal wavelength changes according to the medium. In addition to speed of sound, acoustic impedance z is another important physical property of the medium. Acoustic impedance is a function of density and speed of sound

$$z = \rho c. \tag{2.22}$$

The equation indicates that the impedance increases with the increasing of density or speed of sound. Table 2.2 shows the acoustic impedance in some typical

Medium	Acoustic impedance (kg$m^{-2}s^{-1}$)
Air	430
Water	1.48×10^6
Bone	6.47×10^6
Fat	1.33×10^6
Liver	1.65×10^6
Muscle	1.71×10^6

Table 2.2: Acoustic impedance in medium.

mediums. In B-mode ultrasound imaging, acoustic impedance affects the ability of the ultrasound wave transfer through different medium (tissue) types. As the ultrasound waves travel through different mediums, not all of the waves can propagate forward, part of the waves reflect back at the medium interface. Reflection fraction coefficient R_i is used to define the amount of reflection as ultrasound wave transfers through different mediums,

$$R_i = (\frac{Z_2 - Z_1}{Z_2 + Z_1})^2, \tag{2.23}$$

where Z_1 and Z_2 are acoustic impedance of medium (tissue) 1 and 2, respectively. As can be seen from the equation, when two mediums have similar acoustic impedance, reflection fraction coefficient reaches a relatively small value meaning that most of the ultrasound wave is able to propagate through the interface. Alternatively, when ultrasound wave passes through the interface with two mediums that have large difference of acoustic impedance, a large amount of ultrasound intensity is reflected. Note that acoustic impedance in the air is much smaller than that in the tissue. Thus, the ultrasound signal can hardly propagate through the interface between air and human tissue. Coupling gel is therefore typically applied between the surface of ultrasound transducer and patient skin as a type of conductive medium to minimize the reflection of the ultrasound signal.

Another physical property of ultrasound signal is the attenuation of the intensity. Intensity is defined as the energy transmitted per unit time and per unit area with the unit Wcm^{-2}. As the ultrasound signal propagates through tissue, the intensity gradually decreases. The attenuation factor is typically calculated in logarithm scale with the unit $dBcm^{-1}MHz^{-1}$. The unit indicates that with higher transducer frequency and longer propagation distance, ultrasound wave intensity is gradually reduced. Specifically, when the transmit transducer (TX) also serves as receiving transducer (RX), the distance is twice the distance from the transducer to target. The receiving echo therefore is too weak to detect if the frequency is high. In medical applications, high frequency is applied only to superficial targets such as thyroid. When the target is located deeper in human body, low frequency transducer is desirable to avoid the fast attenuation with distance.

2.3.2 Transducer Physics and Beam Forming Principle

Ultrasound transducers have different sizes and shapes to meet the requirement of various clinical applications. There are primarily three common types: single element, linear-array and phased-array transducers. These three types of transducers have the same features and physics. The beam forming and target steering principles however are different. Each type of the transducer is discussed in the following sections.

2.3.2.1 Single Element Transducer

A simple single element ultrasound transducer structure including a piezoelectric crystal, matching layer and backing layer is shown in Fig. 2.7. These three

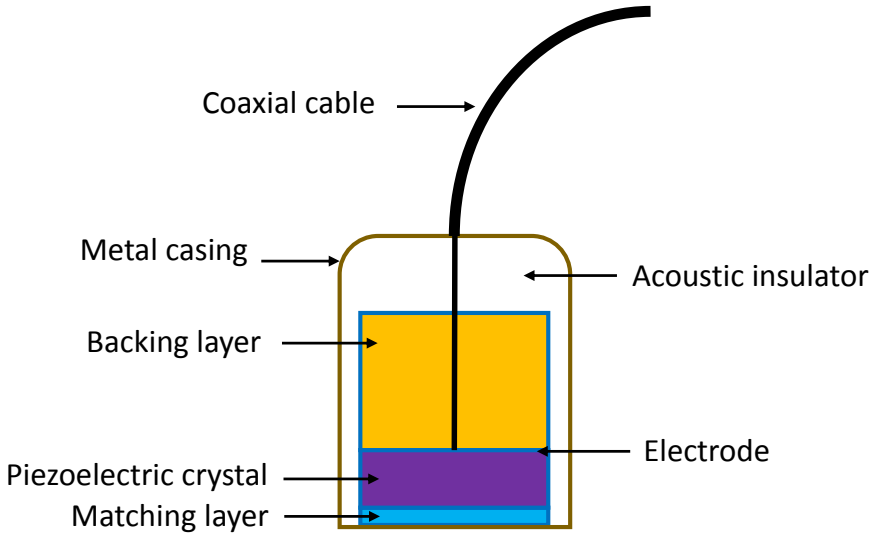


Figure 2.7: **Single element transducer structure.**

components are manufactured in a metal casing surrounded by acoustic insulator. Positive electrode is on the rear side of piezoelectric crystal and is connected to the control circuits by a coaxial cable. Piezoelectric material (PZT) is the key component of the transducer which converts electrical energy to sound energy. The front electrode of PZT is typically grounded for safety of the patient and the voltage is applied to the rear electrode. When a certain voltage pulse is applied to the electrodes, PZT structure is physically deformed. With the mechanical expansion and contraction of the PZT, the front side of PZT sends ultrasound waves to the object through matching layer. The thickness of the PZT is dependent on the required frequency which is typically equal to half of the wavelength to ensure that the reflected wave is in phase with the original wave. Note that the medium for sound is assumed to be PZT instead of human tissue.

Due to the large difference in the acoustic impedance of PZT and human tissues, only a small amount of ultrasound waves can be transmitted to the object, whereas

the rest is reflected back to PZT. An appropriate matching layer is therefore inserted between PZT and human tissues as an intermediate material to maximize the ultrasound wave transmission. The matching layer impedance is equal to

$$Z_{matching} = \sqrt{(Z_{PZT} \times Z_T)}, \tag{2.24}$$

where Z_{PZT} and Z_T are the acoustic impedance of PZT and human tissue, respectively. The matching layer thickness is typically 1/4 of wavelength in order to have the reflected waves in matching layer combined in-phase with each other, thereby generating a stronger wave. Matching layer however also has some issues. Due to the fixed thickness, matching layer can only work at a single optimal frequency, the ultrasound wave cannot be in-phase inside the entire bandwidth. Also, if the target point deviates from axial direction with an angle, the matching layer is no longer 1/4 of wavelength which also affects the superposition of wave.

The common problem of piezoelectric materials is that the ultrasound wave that reflects back from the interface between PZT and matching layer may produce reverberations within PZT even after the electrical voltage pulses have finished. A backing layer is thus located behind PZT to absorb this excessive reverberations. With the backing layer inserted, the ultrasound pulse length is shorter and axial resolution is improved. However, the absorbed energy is converted to heat, and the transducer sensitivity is also reduced. The backing layer material acoustic impedance is therefore lower than PZT to adjust the tradeoff between the axial resolution and sensitivity.

A typical ultrasound pulse fired by a transducer is shown in Fig. 2.8. The pulse duration typically includes multiple pulse periods. The pulse is repeated based on

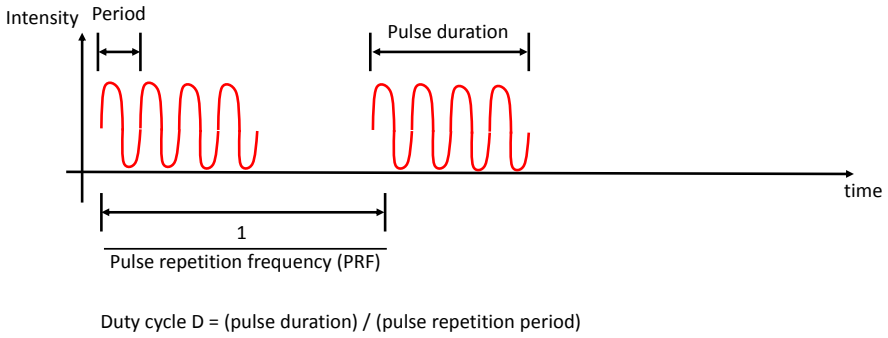


Figure 2.8: **Ultrasound pulse waveform parameters.**

the pulse repetition frequency (PRF). In pulse-echo setting, transducer switches from TX to RX to receive the echo from the target during the idle time in every cycle. Both PRF and duty cycle are directly related to each other and are regulated by the electrical signal.

2.3.2.2 Linear Array Transducer

Linear array transducers can realize dynamic focusing. Linear transducer consists of a set of narrow, rectangular elements with identical size. All of the elements share the front electrodes as ground node but have separate electrical lead on the rear side. Linear array transducer can have as few as 32 elements and as many as 256 elements. The size of the element highly depends on the center frequency of the transducer (and therefore wavelength). Linear array transducer elements are sub-grouped to fire ultrasound waves instead of simultaneous activation. Focal points move back and forth by activating different sub-grouped elements while the probe remains in the same position. The principle of the linear array transducer is shown in Fig. 2.9. Note that only 16 elements are included in this probe for simplicity. Initially, elements 1 to 5 are grouped together to form the ultrasound beam and

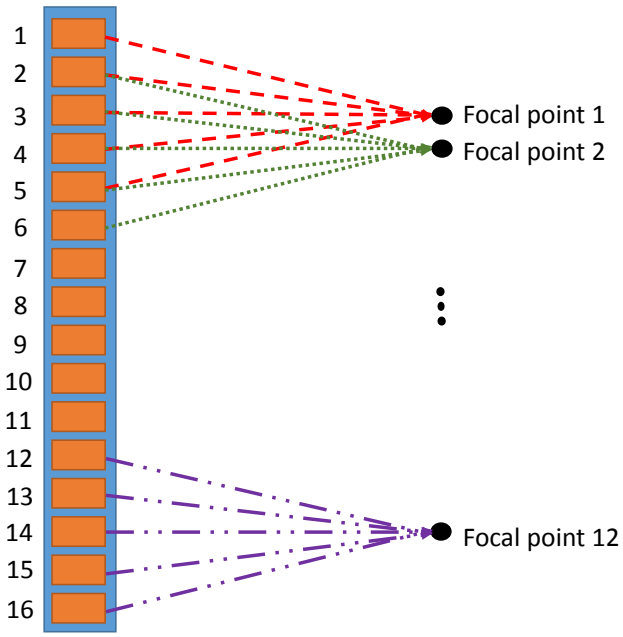


Figure 2.9: **Linear array transducer beam forming principle.**

transmit ultrasound beams to focal point 1. As shown in the figure, element 3 is in the center of the group and thus has the shortest distance to focal point 1 while elements 1 and 5 have the longest path lengths. Since all of the ultrasound pulses should arrive at focal point 1 at the same time to reach maximum intensity, certain delay modules are inserted to element 2, 3 and 4 accordingly. The delay modules are controlled by electrical control signal where the elements on the side of the group transmit ultrasound signals earlier than the center element. Once the ultrasound waveforms are transmitted, the transducer is switched to receiving mode to receive the reflected ultrasound echoes within the region of interest. Electronic delay modules are calculated by the ultrasound control machine to ensure that all of the reflected echoes reach the summer in-phase.

Once the transmission of group 1 is finished, element 1 is dropped from the

group and element 6 is activated. Group 2 is then formed and consists of elements from 2 to 6. By dropping the very left side element and adding a new element on the right side, total 12 sub-groups are combined and thus total 12 focal points are scanned. The number of activated elements in the sub-group depends on the distance between the transducer and focal points, steering angle of the element as well as the required amount of energy for focal targets. Compared to single element transducer, linear array transducer has a wider aperture and the amount of energy each focal point receives from the transducer is therefore significantly increased due to multiple elements beam forming.

Although linear array transducer transmits stronger ultrasound signal to focal point as compared to single element transducer, linear array transducer suffers from grating lobes which can be considered as unwanted noise. Grating lobes occur when the received ultrasound echoes in two elements have one period delay. Two peaks from these two echoes are summed and cause a large signal as grating lobe. The grating lobe can be avoided if the element pitch is smaller than half of the wavelength.

2.3.2.3 Phased Array Transducer

Phased array transducer is another widely applicable type of transducer with dynamic focusing. Unlike linear array transducer where only a group of elements is selected at a time, all of the elements of phased array transducer are activated together to form the beam steering. An example of phased array transducer beam steering is shown in Fig. 2.10. Note that only five elements are included in this example for simplicity. As indicated in the figure, element 5 has the longest distance to focal point while element 1 has the shortest distance. In order to have ultrasound

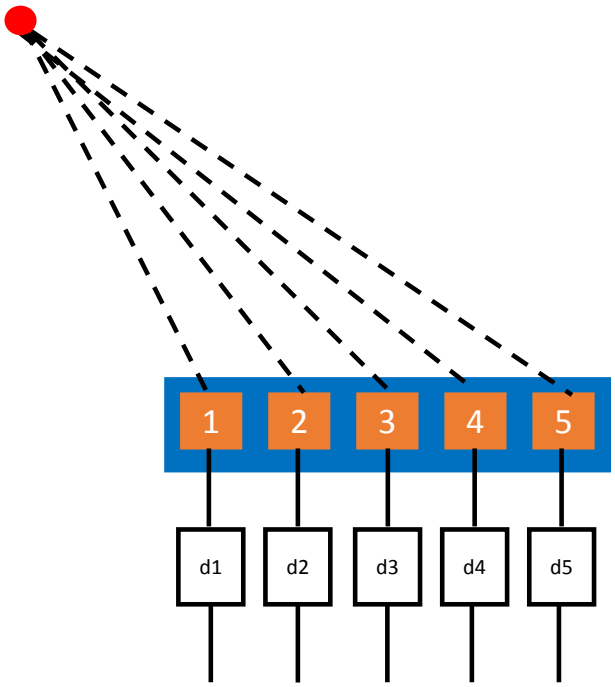


Figure 2.10: **Phased array transducer beam forming principle.**

waves from all the elements to reach the focal point simultaneously, different electronic delay modules $d1$ to $d5$ are calculated based on the distance difference. In this specific case, $d1$ is the longest and $d5$ is the shortest delay module.

Similar to linear array transducer, phased array transducer also suffers from grating lobe issue. Another disadvantage of phased array transducer is that the electronic complexity increases significantly with larger number of transducer elements as the electronic delay modules need to be calculated precisely. Also, with the increasing number of transducer elements, a large bundle of electrical coaxial cables exhibits another issue. Sub-block transducer controlled by de-multiplexer is an option to reduce the phased array transducer complexity, as introduced in Chapter 5.

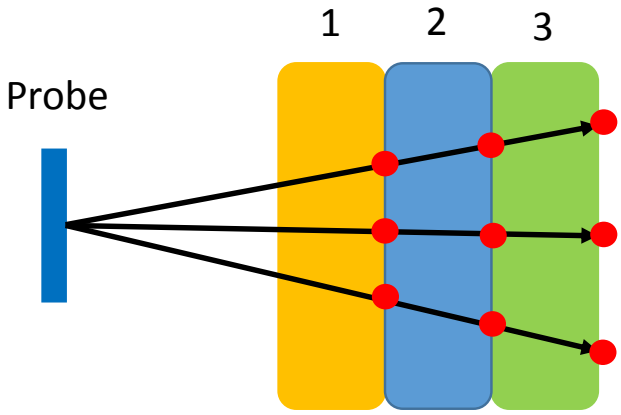


Figure 2.11: **B-mode imaging principle.**

2.3.3 B-mode Ultrasound Imaging Formation and Properties

B-mode (brightness) ultrasound imaging is one of the most widely used imaging method for clinical purposes. It is a two dimensional grey-scale imaging that can reflect the physical properties of tissues. B-mode imaging is formed by sweeping a set of scan lines where the amplitude of the signal is represented by the dots of brightness. The principle of B-mode imaging is shown in Fig. 2.11. When the scan line reaches the boundary between medium 1 and 2, part of the wave keeps moving forward, while part of the wave is reflected back and appears as a bright dot on the B-mode imaging. The wave that moves forward is also partly reflected at the boundary of medium 2 and 3. With a series of dots on the boundary of different mediums, the organ or tissue contour is shown. B-mode imaging has played a crucial role in the diagnosis process in cardiology, gynecology, etc [37]. The B-mode imaging requires a series of digital signal processing at the receiving side and the imaging quality can be described by imaging resolution such as lateral and axial resolution. The details are discussed in Chapter 5 of this thesis.

Chapter 3

Figures-of-Merit to Evaluate the Significance of Switching Noise in Analog Circuits

In this chapter, the analysis method to determine the significance of induced (switching) noise in analog circuits is investigated. An introduction is provided in Section 3.1. The proposed analysis flow to determine the significance of induced noise in analog circuits is described in Section 3.2. The significance of switching noise is evaluated and dominance noise regions are identified in Section 3.3. Reverse body biasing to alleviate switching noise is investigated in Section 3.4. A case study example is described in Section 3.5.

3.1 Introduction

As mentioned in Chapter 1, both intrinsic device noise and the switching noise that propagates from digital circuits impact the performance of the analog circuits. In order to mitigate the noise, a fair comparison between these two noise sources and better understanding of the dominance noise region is significant.

The primary contributions of this project are as follows: (1) *input-referred switching noise* is introduced as a figure-of-merit to determine the significance of induced noise, (2) an analysis flow is proposed to analytically compare input-referred switching noise with equivalent input device noise, (3) dominance regions for both switching noise and device noise are identified as a function of time domain switching noise characteristics such as the peak amplitude, period, oscillation frequency within each period, and damping coefficient, (4) time domain peak amplitude that leads to equal input-referred switching and device noise in the frequency domain is characterized and used as the second figure-of-merit, (5) a method based on body biasing is introduced to reduce the effect of switching noise by weakening the transfer function from bulk node to input node of an analog circuit, and (6) the proposed flow is applied to a sensitive potentiostat circuitry as a case study.

3.2 Proposed Analysis Flow

The proposed flow is summarized in Fig. 3.1. Time domain switching noise profile at the bulk node of the transistors is modeled as a decaying sine wave. Existing techniques can also be utilized to estimate switching noise profile for a specific circuit. Corresponding transfer functions are used to transfer switching noise from the bulk node to the input node of the circuit. This noise is referred to as input-referred

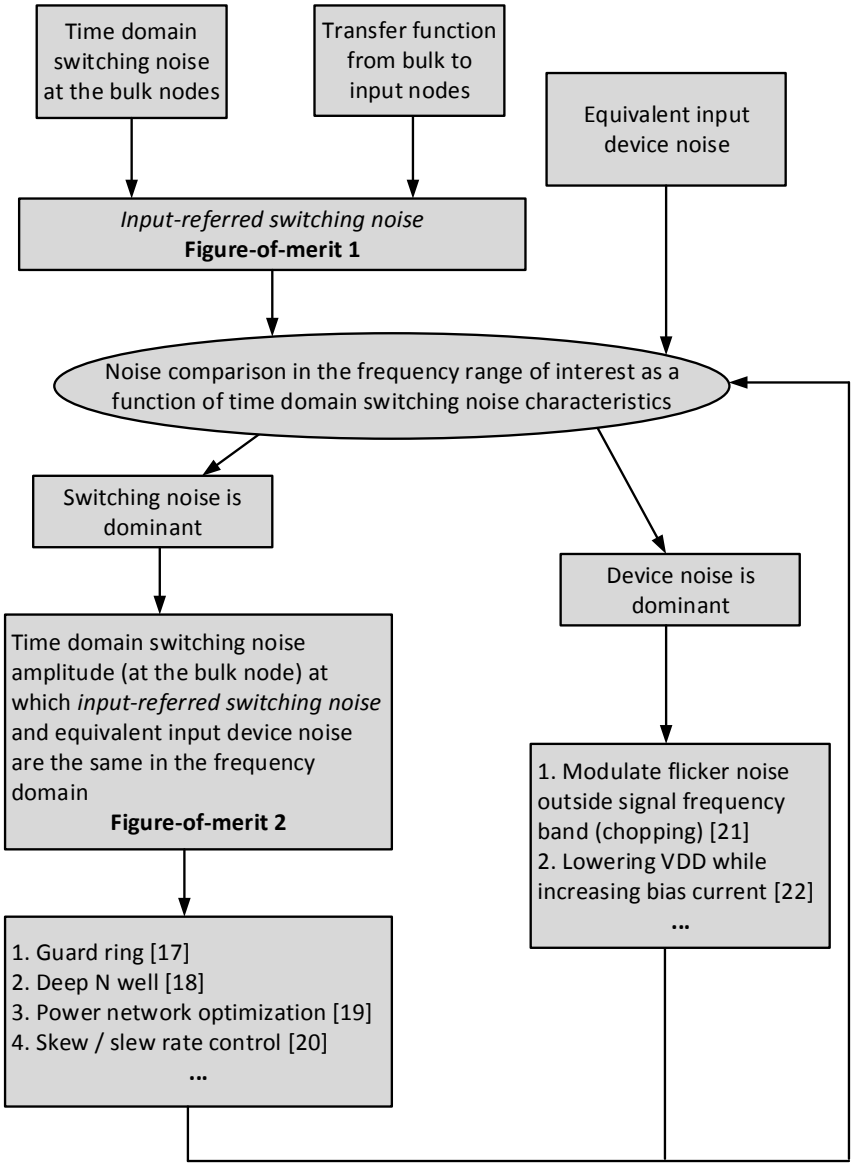


Figure 3.1: **Proposed flow and the concept of *input-referred switching noise* to determine the significance of induced noise in analog circuits.**

switching noise and used as a primary figure-of-merit to determine the significance of switching noise. By comparing the input-referred switching noise with the equivalent input device noise, dominant noise source in the frequency range of interest is determined. Note that the noise analysis at the input eliminates the effect of gain, providing a more fair comparison framework. Once the dominant noise is determined, applicable noise reduction techniques can be applied. Furthermore, time domain switching noise amplitude (at the bulk node) that leads to equal switching and device noise at the input node (in the frequency domain) is characterized and used as a guideline while applying switching noise reduction techniques.

Two commonly used amplifier topologies, two-stage common source with a differential input pair and folded cascode, are chosen as analog victim circuits to illustrate the proposed flow. Both amplifiers are designed in a 0.5 μm AMI CMOS technology with a VDD of 3 V. All of the simulations are achieved with Spectre using AMI device models [38]. Brief background information on these amplifier topologies is provided in Section 3.2.1. The model used to represent switching noise generated by digital blocks is described in Section 3.2.2. Input-referred switching noise and equivalent input device noise are quantified in, respectively, Section 3.2.3 and Section 3.2.4.

3.2.1 Background on Amplifier Topologies

Two-stage common source with a differential input pair (see Fig. 3.2) and a folded cascode amplifier (see Fig. 3.3), are used as analog victim circuits. Both topologies utilize a current mirror to obtain a single output. Some related specifications of these two amplifiers and the operating points are listed in Table 3.1. Note that the DC gain and phase margin of both amplifiers are comparable.

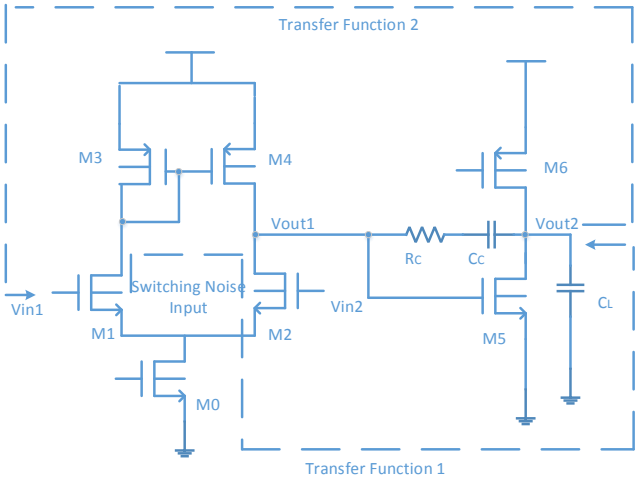


Figure 3.2: **Schematic of a two-stage amplifier used to evaluate the significance of switching noise.**

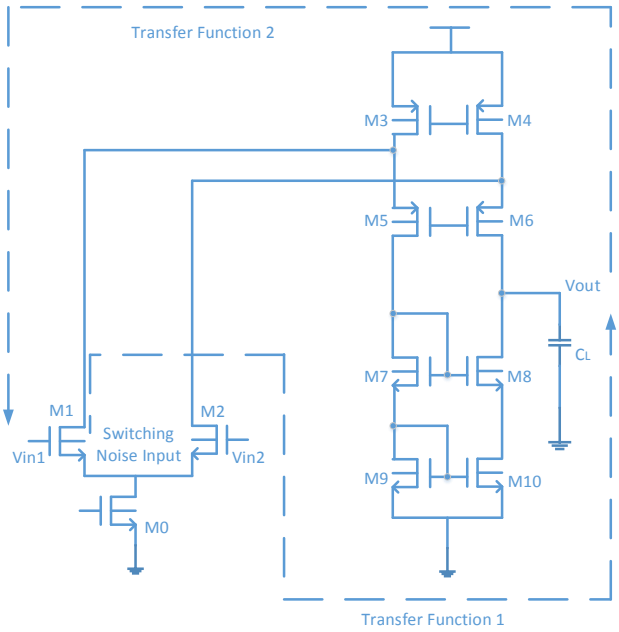


Figure 3.3: **Schematic of a folded cascode amplifier used to evaluate the significance of switching noise.**

	Two-stage	Folded cascode
DC gain	72 dB	75 dB
Phase margin	56°	60°
Location of dominant pole	17.62 kHz	10.83 kHz
Flicker and thermal noise at 1 Hz	-114 dB	-104.5 dB
Input bias voltage	1.6 V	1.5 V
Load capacitance	1 pF	1 pF

Table 3.1: Amplifier specifications and operating points

Each transistor within the amplifiers suffers from both thermal and flicker noise. The resistance R_C between the first and second stage in the two-stage amplifier is used to adjust the location of the pole/zero for frequency compensation. In addition to device noise, the transistors suffer from switching noise that is generated by the digital circuitry and propagates to the bulk nodes through the substrate.

3.2.2 Switching Noise Modeling at the Bulk Node

A periodic decaying sine wave is used to represent the switching noise generated by the digital circuit. Decaying sine wave is an appropriate function for switching noise, as shown in [11, 39, 40]. Peak amplitude, oscillation frequency, period of the decaying sine wave, and damping coefficient are the primary parameters of the decaying sine wave and are used to model noise characteristics. These parameters are illustrated in Fig. 3.4. Since dominant noise identification is achieved in the frequency domain, Laplace transform is used. The decaying sine wave time and

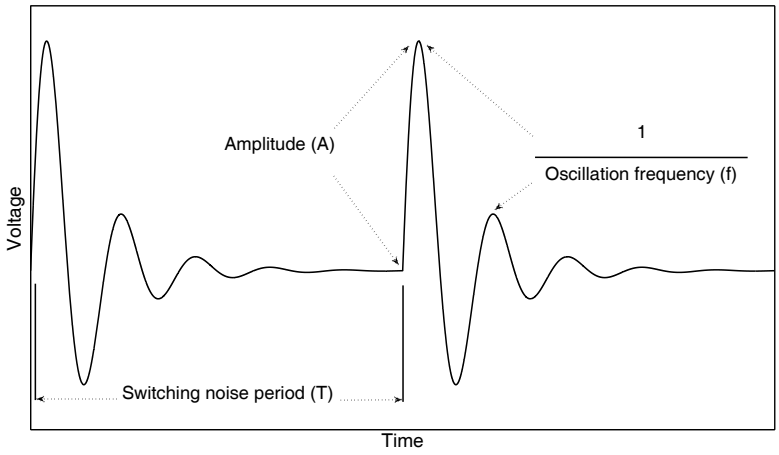


Figure 3.4: **Characteristics of decaying sine wave used to model time domain switching noise at the bulk node of a transistor.**

frequency domain expressions are, respectively,

$$\begin{aligned} V_{swi}(t) &= Ae^{-(\alpha t)}sin(\omega t)u(t)u(T-t) \\ &\quad +Ae^{-(\alpha(t-T))}sin(\omega(t-T))u(t-T)u(2T-t) \\ &\quad +...+Ae^{-(\alpha(t-(n-1)T))} \\ &\quad sin(\omega(t-(n-1)T))u(t-(n-1)T)u(nT-t), \end{aligned} \tag{3.1}$$

$$\begin{aligned} V_{swi}(s) &= \frac{1}{(1-e^{-Ts})} \times A \times \\ &\quad \frac{e^{-(s+\alpha)T} \times (-(s+\alpha)sin\omega T - \omega cos\omega T) + \omega}{\omega^2 + (s+\alpha)^2}, \end{aligned} \tag{3.2}$$

where A is the peak amplitude, T is the period of the decaying sine wave, α is the damping coefficient to determine how fast the sine wave decays, ω is the oscillation frequency within a period, which is $2\pi f$, and $u(t)$ is the unit function.

A greater damping coefficient α results in reduced settling time (faster damping), thereby producing smaller noise magnitudes in the frequency domain, particularly at low frequencies. Similarly, noise magnitude in the frequency domain is linearly proportional to the peak amplitude A in the time domain, as indicated by (3.2). For example, decreasing the peak amplitude from 80 mV to 30 mV reduces the switching noise by approximately 9 dB over the entire frequency range. Higher oscillation frequency ω in time domain corresponds to a smaller settling time. In the frequency domain, switching noise with a larger ω has a smaller amplitude at low frequencies. For example, if oscillation frequency is increased from 5 MHz to 10 MHz in time domain, the frequency domain magnitude decreases by approximately 7 dB at DC. Finally, an increase in the period T of the switching noise in time domain shifts the fundamental frequency and reduces the noise magnitude in the frequency domain, particularly at low frequencies. For example, if the period increases from 1 μs to 10 μs, noise magnitude in the frequency domain is reduced by approximately 20 dB at DC. These four parameters are utilized to model different switching noise characteristics.

3.2.3 Quantification of Input-Referred Switching Noise

Switching noise generated by a digital circuit couples to the substrate and reaches the bulk node of NMOS transistors in analog blocks. Note that switching noise observed at the PMOS transistors is typically lower due to the capacitive isolation of N-WELL and is therefore ignored in this analysis [4].

Transfer functions are obtained to transmit each noise source from the bulk

node of a transistor to the input node of the amplifiers, as shown by the dashed lines in Figs. 3.2 and 3.3. The overall input-referred switching noise is determined by the superposition of these noise sources and used as a primary figure-of-merit to evaluate the significance of switching noise.

Noise sources at the bulk nodes are first transferred to the output of the amplifiers through the transfer function V_{out}/V_{bulk}. This noise at the output is then transferred to the input of an amplifier through the transfer function V_{out}/V_{in}, which represents the gain of the amplifier. Thus, switching noise at the bulk node of the NMOS transistors is transferred to the input node of the amplifier by utilizing these two transfer functions,

$$V_{in}^{swi} = \frac{V_{out}/V_{bulk}}{V_{out}/V_{in}} \times V_{swi} = \frac{V_{in}}{V_{bulk}} \times V_{swi}, \tag{3.3}$$

where V_{in}^{swi} is the input-referred switching noise, V_{out} is the amplifier output voltage, V_{bulk} is the voltage at the bulk node of an NMOS transistor, V_{in} is the amplifier input voltage, and V_{swi} is the switching noise at the bulk node.

In the two-stage amplifier (see Fig. 3.2), the ratio of these two transfer functions for each NMOS transistor in the second stage is approximately 50 times weaker as compared to the input NMOS transistors due to the gain of the first stage. Thus, for the two-stage amplifier, switching noise is critical primarily for the two input transistors (M_1 and M_2), as also verified by SPICE analysis. Hence, switching noise is applied only to the bulk nodes of M_1 and M_2. The ratio of the transfer functions

for the two-stage amplifier is determined by

$$\frac{V_{in}}{V_{bulk}} = \frac{V_{out2}/V_{bulk}}{V_{out2}/V_{in}} = \frac{V_{out1}/V_{bulk}}{V_{out1}/V_{in}}, \tag{3.4}$$

since the gain of the second stage (V_{out2}/V_{out1}) is canceled. The DC transfer function V_{out1}/V_{bulk} is given by

$$\begin{aligned} \left.\frac{V_{out1}}{V_{bulk}}\right|_{2stg} &= \frac{g_{mb1}(g_{m2}+g_{mb2})}{g_{m1}+g_{mb1}} \times (r_{o2} \parallel r_{o4}) \\ &= g_{mb1} \times (r_{o2} \parallel r_{o4}), \end{aligned} \tag{3.5}$$

where g_m and g_{mb} are, respectively, the transconductance of the gate and bulk nodes of a transistor, and r_o is the channel resistance. DC transfer function V_{out1}/V_{in} is calculated in a similar fashion,

$$\left.\frac{V_{out1}}{V_{in}}\right|_{2stg} = g_{m1} \times (r_{o2} \parallel r_{o4}). \tag{3.6}$$

By dividing (3.5) by (3.6), the DC transfer function V_{in}/V_{bulk} for each input transistor of the two-stage amplifier is

$$DCTF|_{2stg} = \frac{\left.\frac{V_{out1}}{V_{bulk}}\right|_{2stg}}{\left.\frac{V_{out1}}{V_{in}}\right|_{2stg}} = \frac{g_{mb1}}{g_{m1}}. \tag{3.7}$$

Note that since the two input transistors are sized the same, $g_{m1} = g_{m2}$.

A similar procedure is followed for the folded cascode amplifier, yielding the

following two expressions,

$$\left.\frac{V_{out}}{V_{bulk}}\right|_{FC} = g_{mb1}\{[(g_{m3}+g_{mb3})r_{o3}(r_{o1} \parallel r_{o5})] \parallel [(g_{m7}+g_{mb7})r_{o7}r_{o9}]\}, \tag{3.8}$$

$$\left.\frac{V_{out}}{V_{in}}\right|_{FC} = g_{m1}\{[(g_{m3}+g_{mb3})r_{o3}(r_{o1} \parallel r_{o5})] \parallel [(g_{m7}+g_{mb7})r_{o7}r_{o9}]\}. \tag{3.9}$$

Thus, the DC transfer function V_{in}/V_{bulk} for each input transistor of the folded cascode amplifier is determined by dividing (3.8) by (3.9),

$$DCTF|_{FC} = \frac{\left.\frac{V_{out}}{V_{bulk}}\right|_{FC}}{\left.\frac{V_{out}}{V_{in}}\right|_{FC}} = \frac{g_{mb1}}{g_{m1}}. \tag{3.10}$$

The final transfer function from the bulk node of the input transistor to the input node is

$$\frac{V_{in}}{V_{bulk}} = DCTF \times \frac{(1+\frac{s}{\omega_{z1}})(1+\frac{s}{\omega_{z2}})...(1+\frac{s}{\omega_{zn}})}{(1+\frac{s}{\omega_{p1}})(1+\frac{s}{\omega_{p2}})...(1+\frac{s}{\omega_{pn}})}, \tag{3.11}$$

where ω_{z1}^m to ω_{zn}^m and ω_{p1}^m to ω_{pn}^m are, respectively, the magnitude of zeros and poles.

Expression (3.11) is used to transmit the switching noise from the bulk node to the input node for both two-stage and folded cascode amplifiers. These transfer functions are shown in Figs. 3.5 and 3.6 for both amplifiers.

According to these figures, the analytic expressions match SPICE simulations.

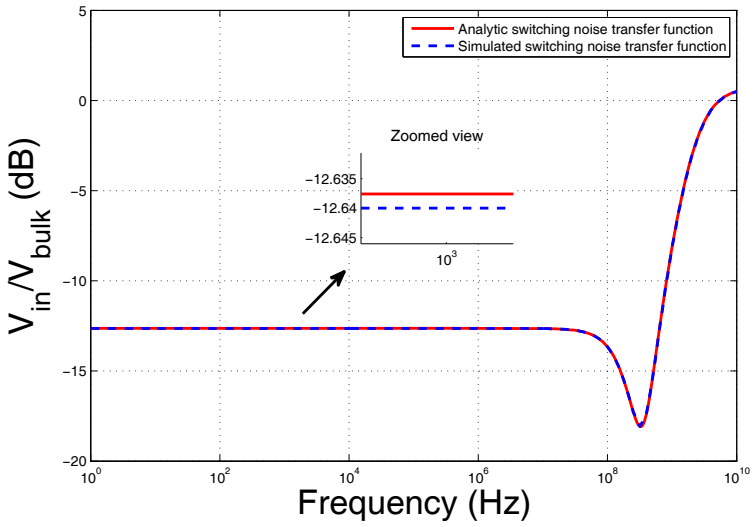


Figure 3.5: **Comparison of analytic and simulated transfer function V_{in}/V_{bulk} used to transmit switching noise from bulk node to the input node in the two-stage amplifier.**

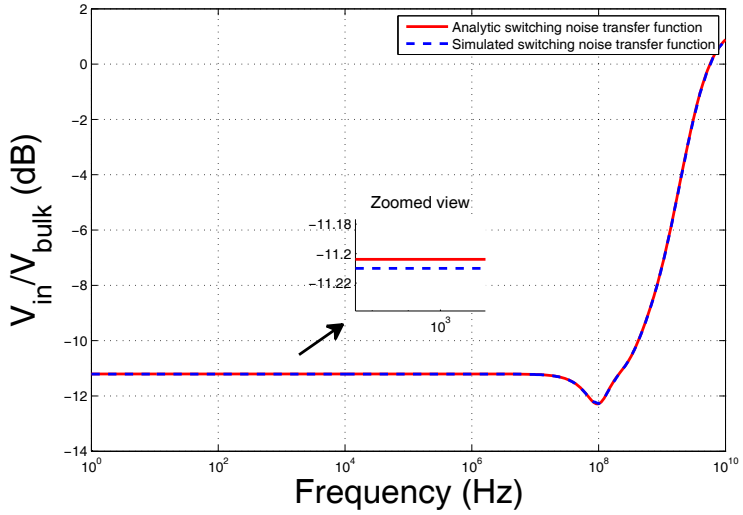


Figure 3.6: **Comparison of analytic and simulated transfer function V_{in}/V_{bulk} used to transmit switching noise from bulk node to the input node in the folded cascode amplifier.**

Finally, overall input-referred switching noise V_{in}^{swi} due to two input transistors is determined by

$$V_{in}^{swi} = 2 \times \frac{V_{in}}{V_{bulk}} \times V_{swi}. \tag{3.12}$$

3.2.4 Quantification of Equivalent Input Device Noise

As mentioned previously, flicker and thermal noise are considered to determine the inherent noise. The overall device noise at the input node is the superposition of each noise source. For the two-stage amplifier, even though the device noise in the first stage affects the overall noise significantly more than the second stage (since the noise in the second stage is divided by the gain of the first stage to reach amplifier input), transistors M_1 to M_6 are included in the analysis.

The DC flicker noise $V_{flicker}^2$ and thermal noise $V_{thermal}^2$ of the two-stage amplifier at the input node are, respectively,

$$\begin{aligned} V_{flicker}^2\Big|_{2stg} &= \frac{2K_N}{C_{ox}WL_{M1}f} + \frac{2K_P g_{m3}^2}{g_{m1}^2 C_{ox}WL_{M3}f} \\ &\quad + \frac{\frac{K_N}{C_{ox}WL_{M5}f} + \frac{K_P g_{m6}^2}{g_{m5}^2 C_{ox}WL_{M6}f}}{g_{m1}^2 (r_{o1} \parallel r_{o3})^2}, \end{aligned} \tag{3.13}$$

$$\begin{aligned} V_{thermal}^2\Big|_{2stg} &= \frac{8kT\gamma}{g_{m1}} + \frac{8kT\gamma g_{m3}}{g_{m1}^2} \\ &\quad + \frac{4kT\gamma}{g_{m1}^2 g_{m5} (r_{o1} \parallel r_{o3})^2} \\ &\quad + \frac{4kT\gamma g_{m6}}{g_{m1}^2 g_{m5}^2 (r_{o1} \parallel r_{o3})^2}, \end{aligned} \tag{3.14}$$

where k is Boltzmann's constant, T is temperature in Kelvin, γ is thermal noise coefficient, K_N and K_P are process-dependent constants for, respectively, NMOS and PMOS transistors, C_{ox} is gate oxide capacitance per unit area, W and L are, respectively, width and length of a transistor. Thus, the overall DC device noise for the two-stage amplifier is

$$V_{in,DC}^{dev}\Big|_{2stg} = \sqrt{V_{flicker}^2\Big|_{2stg} + V_{thermal}^2\Big|_{2stg}}. \tag{3.15}$$

For the folded cascode amplifier, the device noise analysis is achieved as follows. The thermal and flicker noise of each transistor are modeled by an AC current source I_s between the source and drain terminals of each transistor (M_1 to M_{10}). This current source is transmitted to the input node by utilizing the transfer function V_{in}/I_s. Thus, the DC device noise at the input node is

$$V_{in,DC}^{dev}\big|_{FC} = \sqrt{(\frac{V_{out}/I_{s1}}{V_{out}/V_{in}})^2 \times I_{s1}^2 + ... + (\frac{V_{out}/I_{s10}}{V_{out}/V_{in}})^2 \times I_{s10}^2}, \tag{3.16}$$

where I_s is

$$I_s^2 = 4kT\gamma g_m + \frac{K_{N/P}}{C_{ox}WLf} g_m^2. \tag{3.17}$$

The DC gain V_{out}/V_{in} is equal to (3.9). V_{out}/I_s, however, varies for each transistor M, as provided below,

$$\frac{V_{out}}{I_s}\Big|_{M3,4} = \frac{ab - r_{o5}b}{a+b}, \tag{3.18}$$

$$\frac{V_{out}}{I_s}\Big|_{M5,6} = \frac{br_{o5}}{a+b}, \tag{3.19}$$

$$\frac{V_{out}}{I_s}\Big|_{M7,8} = \frac{ar_{o7}}{-a-b}, \tag{3.20}$$

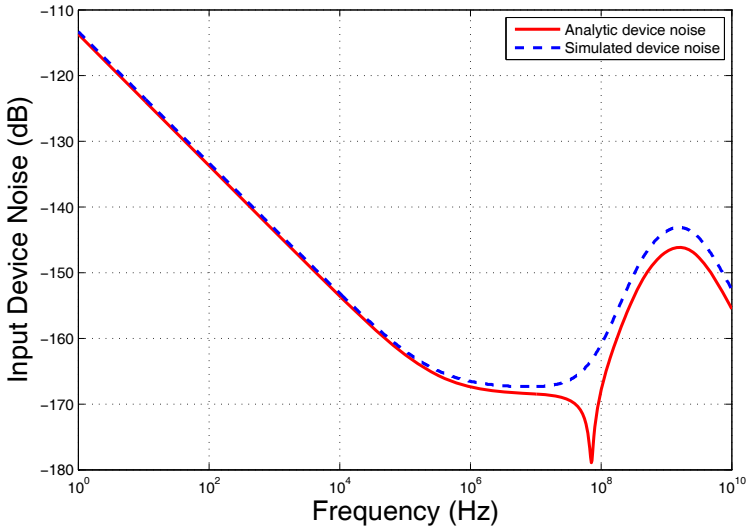


Figure 3.7: **Comparison of analytic and simulated equivalent input device noise for the two-stage amplifier.**

$$\frac{V_{out}}{I_s}\Big|_{M9,10} = \frac{-ab + ar_{o7}}{a+b}, \tag{3.21}$$

where

$$a = r_{o5} + (r_{o1} \parallel r_{o3}) + g_{m5} r_{o5} (r_{o1} \parallel r_{o3}), \tag{3.22}$$

$$b = r_{o7} + r_{o9} + g_{m7} r_{o7} r_{o9}. \tag{3.23}$$

The overall equivalent input device noise (including both thermal and flicker) for both amplifiers is determined by

$$V_{in}^{dev} = V_{in,DC}^{dev} \times \frac{(1+\frac{s}{\omega_{z1}^m})(1+\frac{s}{\omega_{z2}^m})...(1+\frac{s}{\omega_{zn}^m})}{(1+\frac{s}{\omega_{p1}^m})(1+\frac{s}{\omega_{p2}^m})...(1+\frac{s}{\omega_{pn}^m})}, \tag{3.24}$$

where ω_{z1}^m to ω_{zn}^m and ω_{p1}^m to ω_{pn}^m are, respectively, the magnitude of zeros and poles. Note that the location of poles and zeros are different for each transistor m.

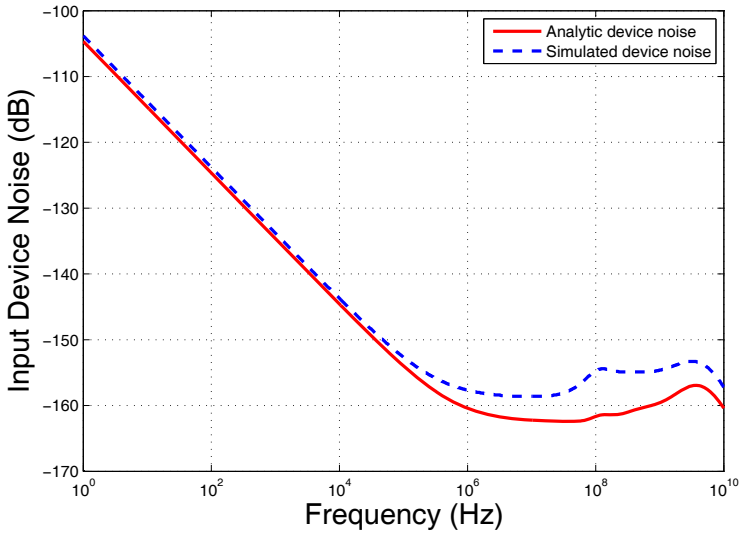


Figure 3.8: **Comparison of analytic and simulated equivalent input device noise for the folded cascode amplifier.**

Equivalent input device noise for the two-stage amplifier is plotted in Fig. 3.7. Noise exhibits an approximately linear decrease at low frequencies due to flicker noise. The device noise becomes constant at approximately 1 MHz due to the dominance of thermal noise. Since the DC gain decreases at higher frequencies, equivalent input device noise slightly increases after 10 MHz. Similarly, equivalent input device noise for the folded cascode amplifier is plotted in Fig. 3.8. For both amplifiers, analytic expressions reasonably approximate SPICE simulations.

3.3 Identification of Dominance Noise Regions

Input-referred device and switching noise are compared to identify dominant noise source as a function of multiple parameters. Eqns. (3.12) and (3.24) are utilized to determine the dominance regions. As an example, these noise sources are

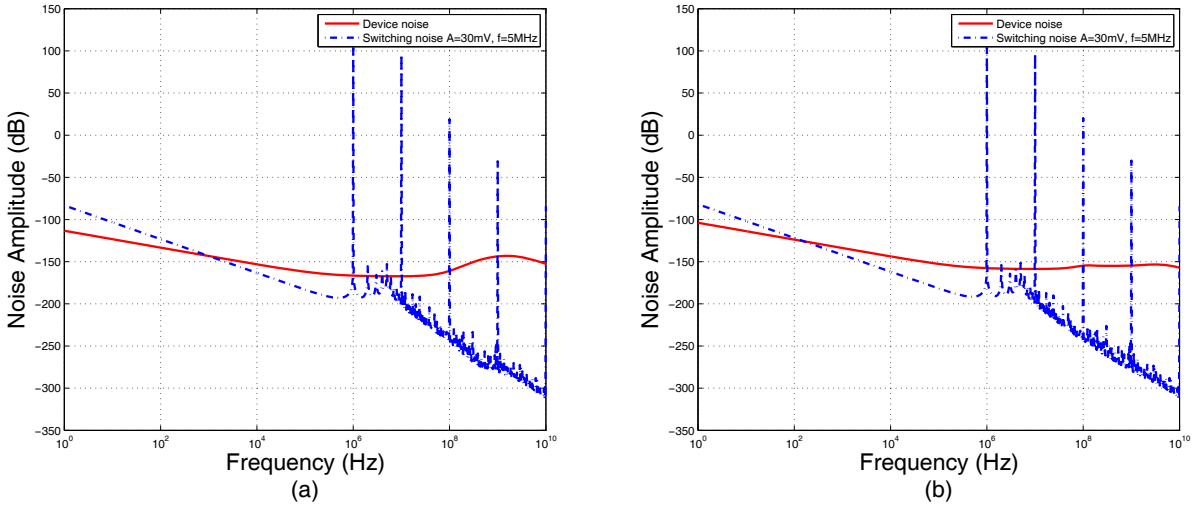


Figure 3.9: **Comparison of input-referred switching noise and equivalent input device noise: (a) two-stage amplifier, (b) folded cascode amplifier.**

plotted as a function of frequency in Fig. 3.9 for both amplifiers. Solid line represents equivalent input device noise. Dotted dash line is the input-referred switching noise when the time domain characteristics are as follows: peak amplitude A is 30 mV (1% of V_{DD}), period T is 1 μs, oscillation frequency f within each period is 5 MHz, and damping coefficient α is 4×10^6. Note that the peak amplitude of 30 mV is comparable to the measured substrate noise in [12] and [41]. Specifically, the time domain noise amplitude in [41] is approximately 3% of V_{DD}. For a V_{DD} of 3 V, peak-to-peak substrate noise of up to 190 mV has been reported [41].

According to Fig. 3.9, switching noise is dominant at low frequencies despite high flicker noise. Specifically, in the two-stage amplifier, switching noise is dominant over device noise until approximately 1 kHz. For the folded cascode amplifier, the crossover frequency is 158 Hz. Also note that at DC, input-referred switching

noise is 30 dB and 22 dB higher than equivalent input device noise in, respectively, two-stage and folded cascode amplifier. Both noise sources decrease with increasing frequency, but switching noise decreases with a faster pace. Thus, device noise starts to be dominant after the crossover point except the fundamental and harmonic frequencies that are determined by the period of the switching noise (modeled as a decaying sine wave) in time domain. Note that the dominant noise analysis illustrated in Fig. 3.9 is not affected by temperature variations since flicker noise dominates thermal noise at low frequencies. Alternatively, at high frequencies, device noise proportionally increases with temperature due to thermal noise. This increase (approximately 5 dB at 10 MHz when temperature rises from 27°C to 165°C), however, is negligible since the overall noise is sufficiently low.

3.3.1 Effect of Time Domain Switching Noise Period

To better investigate the effect of the switching noise period, frequency domain dominance region is illustrated in Fig. 3.10 for the two-stage amplifier. The y axis represents the frequency, while the switching noise period varies from 1 μs to 10 μs (x axis). The remaining parameters of the decaying sine wave are maintained constant at $A = 30$ mV, $\alpha = 4 \times 10^6$, and $f = 5$ MHz. The black line with square markers and dotted black lines represent the operating points where equivalent input device noise and input-referred switching noise are equal. Switching noise is dominant in the shaded region whereas the blank region represents the operating points where device noise is dominant. As the period of the switching noise increases in the time domain, the dominance region of the switching noise is reduced.

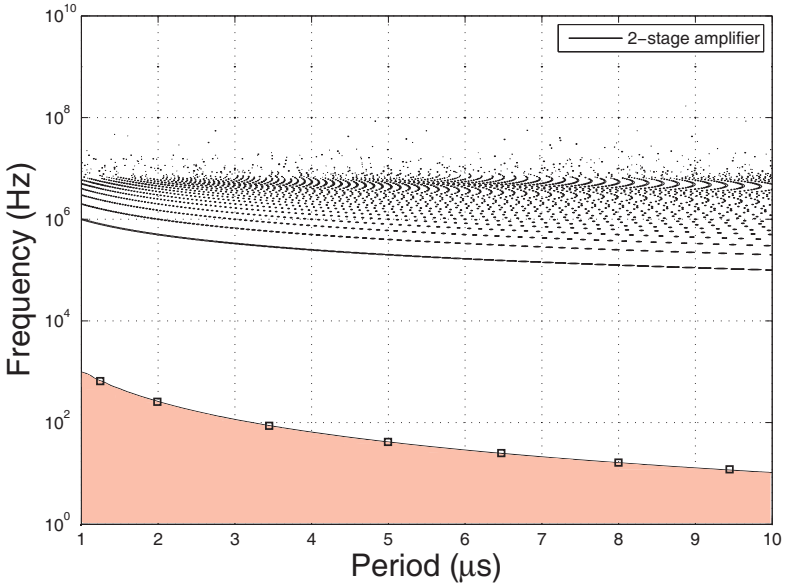


Figure 3.10: **Noise dominance regions for the two-stage amplifier. The black lines and dots represent the operating points where equivalent input device noise and input-referred switching noise are equal. Switching noise is dominant in the shaded region whereas the blank region represents the operating points where device noise is dominant.**

Note that at constant period, switching and device noise become equal at multiple frequencies, as indicated by the black line with square markers and the black dots at higher frequencies. These crossover points can also be observed in Fig. 3.9 at a constant period of 1 μs. In the immediate vicinity of the black dots, switching noise dominates due to fundamental and harmonic frequencies. Thus, if the amplifier bandwidth of interest coincides with these points, switching noise significantly affects circuit operation. Alternatively, in the blank region, emphasis should be placed on reducing device noise. Note that a similar noise dominance region is also obtained for the folded-cascode amplifier, exhibiting similar characteristics. The switching noise dominance region is slightly smaller for the folded cascode

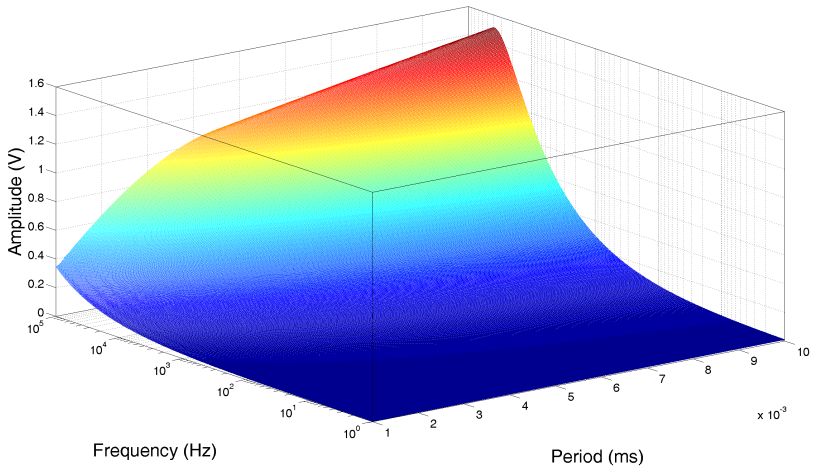


Figure 3.11: **Time domain amplitude of switching noise at which input-referred device and input-referred switching noise (in the frequency domain) are equal (for two stage amplifier).**

amplifier due to greater device noise, as can be seen in Fig. 3.9.

3.3.2 Effect of Time Domain Switching Noise Amplitude

The noise dominance region illustrated in Fig. 3.10 is obtained at a constant switching noise amplitude ($A = 30$ mV) in the time domain. Existing switching noise mitigation techniques typically aim at reducing this amplitude. It is however difficult to determine an acceptable level of switching noise since no reliable figures-of-merit exist. Thus, (3.12) and (3.24) are utilized to numerically solve for the peak amplitude A of switching noise (in the time domain) that makes the input-referred switching noise and equivalent input device noise the same in the frequency domain. This computation is performed as a function of frequency and period of the switching noise. Results for the two-stage amplifier are illustrated in Fig. 3.11. The z axis represents the switching noise amplitude in the time domain at which

	Period = 1 μs				Period = 5 μs				Period = 10 μs			
	Two-stg	FC	Two-stg BB	FC BB	Two-stg	FC	Two-stg BB	FC BB	Two-stg	FC	Two-stg BB	FC BB
1Hz	0.9	2.4	1.3	3.4	4.7	11.7	6.5	16.9	9.3	23.4	13	33.7
100Hz	9.5	23.8	13.3	34.3	46.6	117	65.2	168.6	93.1	234	130.4	337.2
1kHz	30	75.5	42.1	108.8	147.5	370.5	206.5	534	294.9	740.9	413	1067.8
10kHz	96.5	242	135.1	348.8	472	1245.7	660.7	1705.4	932.4	2337.5	1305.1	3368.7
100kHz	344.3	846.8	479.3	1221.8	1097.8	2699.8	1528. 2	3895.4	Negligible			

Table 3.2: Time domain switching noise amplitude (in millivolts) at which input-referred switching and input-referred device noise are equal in the frequency domain.

Two-stage common source amplifier								
V_B (V)	I_D (μA)	DC gain (dB)	g_{mb}/g_m	V_{GS} (V)	V_{th} (V)	Output swing (V)	Phase margin	Bandwidth (kHz)
0	89.58	72.3	0.23	941.6 m	807.6 m	1.71	56.1°	17.62
-0.8	87.73	73.4	0.17	1.072	941.1 m	1.70	56.4°	15.48
-1	87.23	73.2	0.15	1.099	969 m	1.70	56.5°	15.80
-2	84.23	68.6	0.11	1.213	1.085	1.68	56.4°	25.39
-3	79.75	59.1	0.08	1.298	1.172	1.66	56.3°	63.16
Folded cascode amplifier								
V_B (V)	I_D (μA)	DC gain (dB)	g_{mb}/g_m	V_{GS} (V)	V_{th} (V)	Output swing (V)	Phase margin	Bandwidth (kHz)
0	54.84	75.2	0.28	1.024	773.9 m	1.56	44.85°	11.87
-0.65	51.66	73.8	0.20	1.139	898.9 m	1.53	48.09°	13.83
-1	49.1	72.5	0.17	1.189	954.3 m	1.51	50.38°	15.80
-2	39.18	68.0	0.12	1.295	1.082	1.44	57.95°	24.51
-3	28.52	62.8	0.09	1.367	1.178	1.39	64.87°	37.78

Table 3.3: The effect of reverse body biasing on primary design objectives for both amplifiers.

input-referred switching and device noise are equal in the frequency domain. The remaining parameters of the switching noise (decaying sine wave) are constant at $\alpha = 4 \times 10^6$ and $f = 5$ MHz.

At constant period, A increases with frequency since input-referred switching noise is reduced as frequency increases (except the fundamental and harmonic frequencies). Some specific amplitude values are listed in Table 3.2 for both amplifiers.

For example, when the period of the switching noise is 1 μs, at 100 Hz, the

peak switching noise amplitude in the two-stage amplifier should be 9.5 mV to satisfy equal input-referred switching and device noise. This value increases to 23.8 mV for the folded cascode amplifier. Note that if the period of the switching noise is equal to 10 μs, the fundamental frequency is 100 kHz. At this frequency, the switching noise amplitude that produces equal input-referred switching and device noise is sufficiently small since the effect of switching noise is highly strong at the fundamental frequency. This figure-of-merit provides a guideline on the acceptable level of switching noise, assuming that the time domain characteristics of the switching noise (at the bulk node) are known. Last two columns for each period in Table 3.2 represent the effect of body biasing on dominant noise analysis and this figure-of-merit, as described in the following section.

3.4 Reverse Body Biasing to Alleviate Switching Noise

As mentioned previously, existing noise mitigation techniques (such as guard rings, deep N-well, power network optimization, skew/slew rate control) typically focus on reducing the peak noise amplitude. In this paper, an alternative approach is described where the magnitude of the transfer function from a bulk node (where switching noise is present) to the input node of a victim circuit is reduced, thereby reducing input-referred switching noise even though the switching noise at the bulk node remains the same. Note that in low voltage operational transconductance amplifiers, bulk node has been properly biased and utilized as the input node since threshold voltage has not scaled proportionally with the power supply volt-

age [42, 43]. Alternatively, in this paper, bulk node is reverse biased to reduce noise coupling from bulk node to the input node, as described in this section. Also note that device noise is relatively insensitive to reverse body biasing, as shown in existing work [44].

In (3.7) and (3.10), decreasing g_{mb} while maintaining g_m constant reduces the magnitude of the transfer function V_{in}/V_{bulk}, thereby alleviating the effect of switching noise at the input of the two-stage and folded cascode amplifiers.

According to the following expression, bulk transconductance g_{mb} of the input NMOS transistors can be decreased by applying reverse body bias to these transistors [36],

$$g_{mb} = g_m \frac{\gamma}{2\sqrt{2\varphi + V_{SB}}}, \tag{3.25}$$

where γ is the body effect coefficient and φ is the surface potential. When body bias decreases, the threshold voltage increases, the current that flows through input NMOS transistors also decreases due to a higher threshold voltage. Less current causes the source voltage of transistors M_1 and M_2 to decrease. However, the change in the source voltage is relatively smaller as compared to the body bias. Thus, V_{SB} increases and g_{mb} decreases. Since both V_{GS} and threshold voltages simultaneously increase, the g_m of the input NMOS transistor remains approximately constant, which is highly important to maintain the primary design objectives of the amplifiers.

The effect of reverse body bias on g_m and g_{mb} is illustrated in Fig. 3.12 for the two-stage common source amplifier.

As the body bias changes from 0 to -3 V (up to -V_{DD}), g_m changes only from

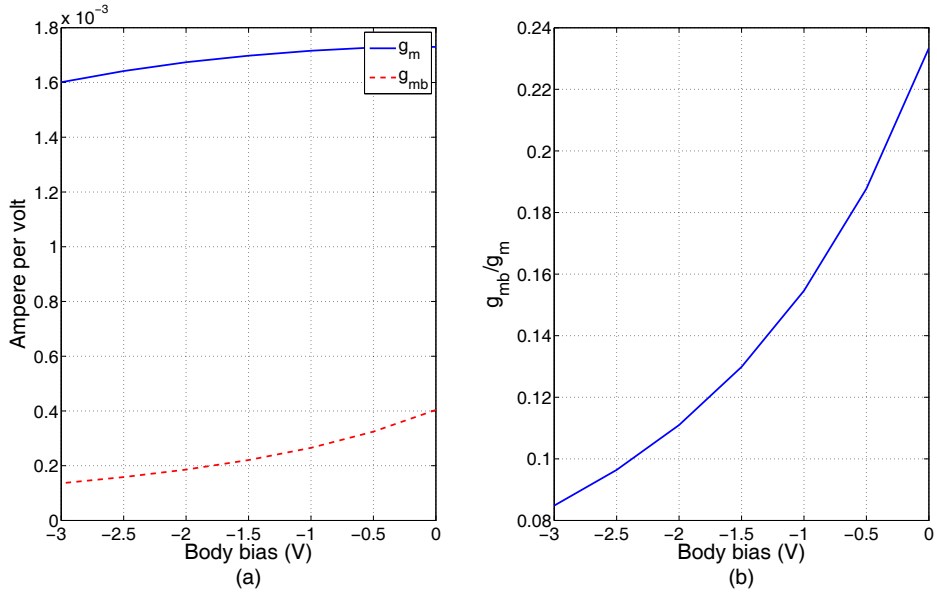


Figure 3.12: **Effect of reverse body bias on (a) transconductance and bulk transconductance, (b) ratio of bulk transconductance to transconductance for two-stage common source amplifier.**

V_B (V)	Temperature (°C)	Two-stage CS amplifier			Folded cascode amplifier		
		g_{mb}	g_m	g_{mb}/g_m	g_{mb}	g_m	g_{mb}/g_m
0	-40	657.5μ	2.745m	0.24	199.2μ	711.4μ	0.28
	27	403.8μ	1.73m	0.23	140.1μ	508.9μ	0.28
	165	178.1μ	806.1μ	0.22	74.72μ	281.9μ	0.27
-1	-40	437.8μ	2.737m	0.16	121.7μ	694.4μ	0.18
	27	265.3μ	1.716m	0.15	83.38μ	489.1μ	0.17
	165	114.4μ	798.2μ	0.14	42.59μ	265.4μ	0.16
-3	-40	230μ	2.565m	0.09	54.18μ	561.8μ	0.1
	27	135.8μ	1.601m	0.08	35.18μ	382.9μ	0.09
	165	56.08μ	752μ	0.07	16.89μ	204.9μ	0.08

Table 3.4: Effect of temperature on the proposed reverse body biasing technique to reduce input-referred switching noise.

1.73 mA/V to 1.601 mA/V (7.5% reduction) whereas g_{mb} decreases from 403.8 μA/V to 135.8 μA/V (more than 66% reduction) Thus, as shown in Fig. 3.12(b), the ratio g_{mb}/g_m significantly decreases as the body bias changes from 0 to -3 V, thereby weakening the bulk-to-input transfer function and reducing input-referred switching noise.

The effect of reverse body biasing on primary design objectives is listed in Table 3.3 for both two-stage common source and folded cascode amplifiers. DC gain, output swing, phase margin, and bandwidth remain approximately the same until a body bias of -1 V. Note that the increase in the threshold voltage is compensated by an increase in the gate-to-source voltage (due to a reduction in the drain current). Also note that when applying reverse body bias, it is important to ensure that the input transistors remain in the saturation region.

As an example, body bias voltages of -0.8 V and -0.65 V (both smaller than -1 V) are applied to the bulk nodes of the input transistors in, respectively, two-stage and folded cascode amplifiers. With these body voltages, the peak switching noise amplitude (in time domain) at the bulk node that leads to equal input-referred switching and device noise magnitude (in frequency domain), *i.e.*, the second figure-of-merit, is characterized, as illustrated in Fig. 3.13 for the two-stage amplifier. Some specific values are listed in Table 3.2. According to the figure and the table, the peak switching noise amplitude that satisfies equal noise at the input increases with body biasing. For example, when the period of the switching noise is 1 μs, at 1 kHz, the peak amplitude increases from 30 mV to 42.1 mV for a two-stage amplifier, indicating that approximately 40% more switching noise can

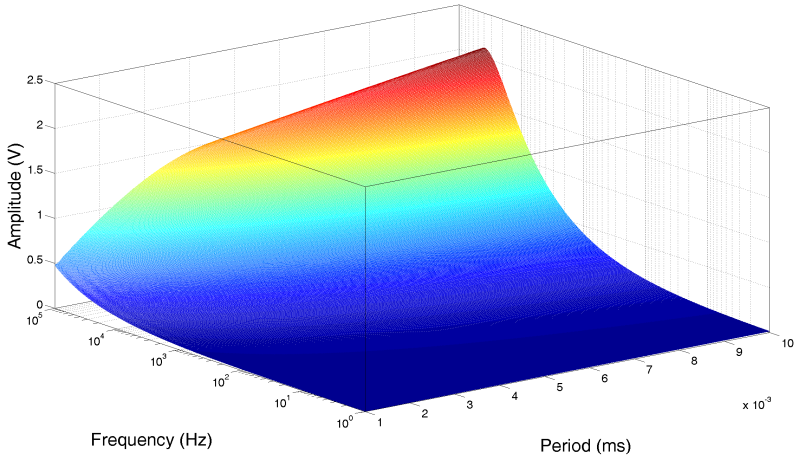


Figure 3.13: **Effect of body biasing on the time domain amplitude of switching noise that leads to equal input-referred device and switching noise (for two-stage amplifier).**

be tolerated. For a folded cascode amplifier, the peak amplitude increases from 75.5 mV to 108.8 mV, thereby tolerating 44% higher switching noise at the bulk node. Note that based on the simulation results, device noise is nearly independent of the reverse body bias. This characteristic is also described in [44], as mentioned earlier in this section.

Another important characteristic of the proposed reverse body biasing technique is temperature insensitivity. Both g_m and g_{mb} are affected by the temperature, but the ratio g_{mb}/g_m remains approximately constant. To illustrate the effect of temperature, g_m, g_{mb}, and the ratio g_{mb}/g_m are listed in Table 3.4 at three reverse body voltages (0 V, -1 V, and -3 V) and at three different temperatures (-40° C, 27° C, 165° C). As shown in this table, at constant body bias, the effect of temperature on g_{mb}/g_m is negligible.

3.5 Case Study

The proposed flow to evaluate the significance of switching noise and reverse body biasing to reduce input-referred switching noise are applied to a potentiostat circuitry as a case study. The potentiostat array architecture is introduced in Section 3.5.1. Application of the proposed analysis flow is described in Section 3.5.2. Reverse body bias is applied to reduce input-referred switching noise, as discussed in Section 3.5.3.

3.5.1 Potentiostat Array Architecture

A 16-channel potentiostat, integrated with microfabricated sensor array, is used for real time and sensitive detection of neurotransmitter concentration [45,46]. This potentiostat array measures the redox current proportional to the concentration of electroactive neurotransmitters, while keeping the potential of the sensor electrode at specific redox potential [47]. The detection of the neurotransmitters is critical for neural pathways and the etiology of neurological diseases like epilepsy and stroke.

The primary challenges in the design process of a potentiostat are high input sensitivity and wide dynamic range. Input noise should be minimized to enhance these design objectives. It is therefore of primary importance to identify the dominant component of the input noise and evaluate the significance of switching noise.

A single channel of a potentiostat consists of a first order single-bit delta-sigma modulator as the analog-to-digital converter, a counter for decimation, and a shift register, as depicted in Fig. 3.14. The delta-sigma modulator consists of a current

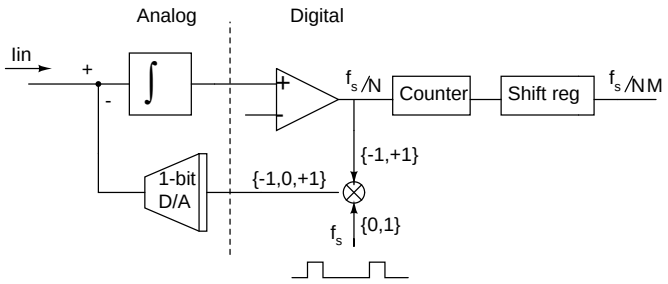


Figure 3.14: **System level diagram of a single channel of the potentiostat.**

integrator, comparator, and switched-current 1-bit digital-to-analog converter in the feedback loop. Sense amplifier in the current integrator is the primary victim block that is highly sensitive to both induced and intrinsic noise. Alternatively, the counter is the primary aggressor that generates high switching noise. Note that the sense amplifier is a single stage cascode amplifier with feedback, designed in 0.5 μm CMOS technology, as shown in Fig. 3.15. The input DC current is 1 pA and the load capacitance of the amplifier is 1 pF.

3.5.2 Application of the Proposed Analysis Flow

The switching noise generated by the counter (aggressor) propagates throughout the substrate and reaches the bulk nodes of the NMOS transistors in the sense amplifier. Thus, the first step in quantifying the input-referred switching noise is to determine the switching noise profile at the bulk node of these transistors. This step is achieved by discretizing the physical structure of the substrate into unit cells and modeling each unit cell with lumped parasitic impedances (consisting of resistance and capacitance), as further described in [48]. The overall network is then simu-

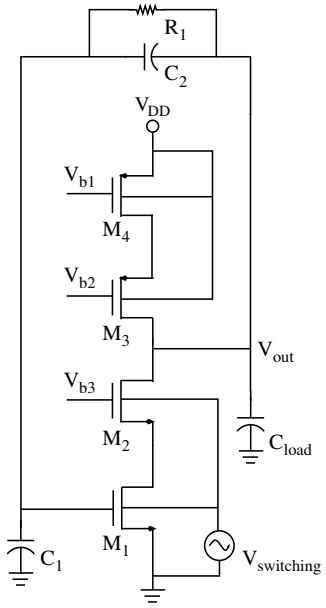


Figure 3.15: **Schematic of the sense amplifier where switching noise is inserted at the bulk nodes of NMOS transistors.**

lated in SPICE to determine noise profiles at the bulk nodes. Also referred to as three-dimensional transmission line matrix (3D-TLM) method [49], the accuracy of this technique has been previously verified by comparing the results with 3-D field solvers [50] and experimental data [51]. A conceptual representation of the overall model (based on 3D-TLM) to determine the switching noise profile at the bulk nodes is depicted in Fig. 3.16. Note that other existing techniques (such as finite difference method or boundary element method) can also be used in this step.

The noise profile V_{swi} obtained in the first step is illustrated in Fig. 3.17 in time domain. The peak noise is in the range of five to ten millivolts whereas the RMS noise is approximately 230 μV.

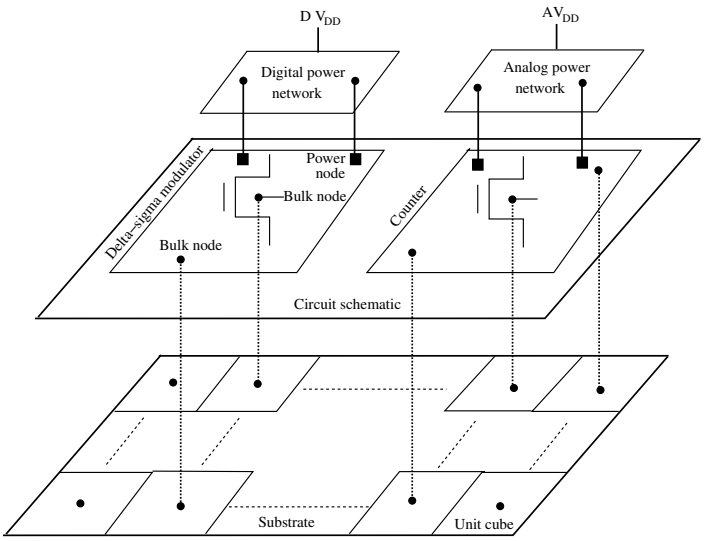


Figure 3.16: **Conceptual representation of the overall model to analyze noise profile at the bulk nodes of the victim transistors.**

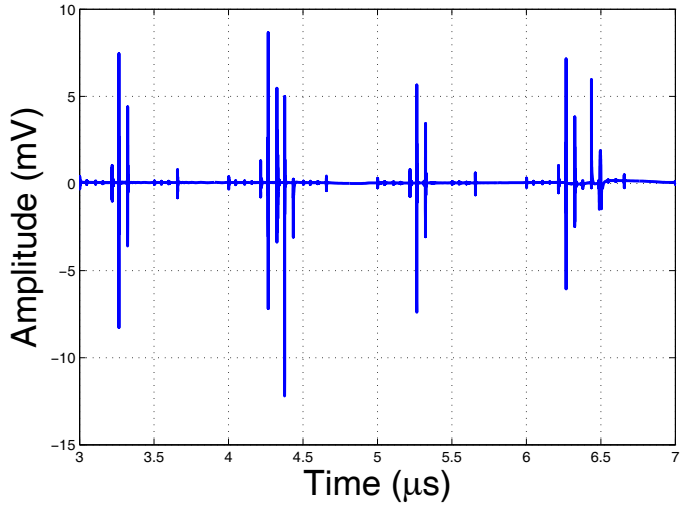


Figure 3.17: **Switching noise profile at the bulk node of the NMOS transistors in time domain.**

V_B (V)	I_D (nA)	DC gain (dB)	g_m	g_{mb}	g_{mb}/g_m	V_{GS} (V)	V_{th} (V)	Output swing (V)	Phase margin	Bandwidth (Hz)
0	956.5	179.9990	24.8 μ	9.752 μ	0.393	660 m	643.2 m	2.4643	86.93°	159.147
-1.2	956.4	179.9992	26.5 μ	5.384 μ	0.203	995.3 m	981.3 m	2.4639	86.92°	159.152
-2.4	956.4	179.9993	26.8 μ	3.480 μ	0.129	1.19	1.176	2.4637	86.94°	159.152
-3	956.4	179.9993	26.9 μ	2.887 μ	0.107	1.26	1.247	2.4637	86.98°	159.153

Table 3.5: Effect of reverse body biasing on primary performance characteristics of the sense amplifier within the potentiostat.

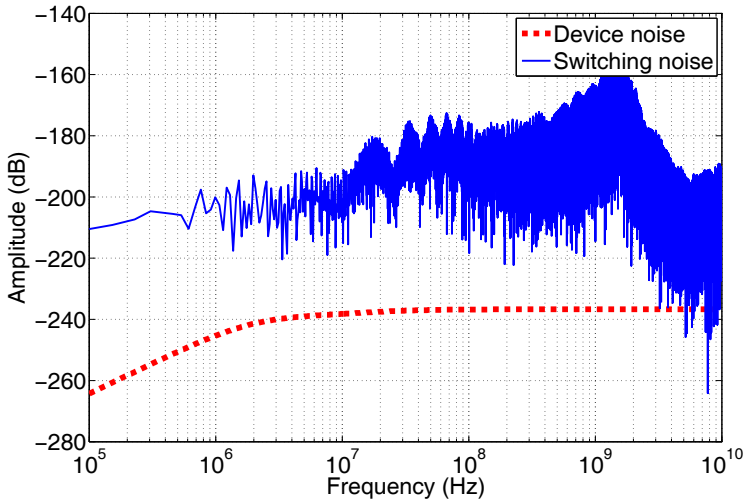


Figure 3.18: **Comparison of input-referred switching noise and equivalent input device noise in the sense amplifier of the potentiostat.**

By utilizing the proposed analysis flow, both equivalent input device noise and input-referred switching noise (first figure-of-merit proposed in this paper) are quantified in the frequency domain. The overall input-referred switching noise due to digital activity and equivalent input device noise due to both active and passive devices are compared in Fig. 3.18. As illustrated in this figure, at low frequencies, switching noise dominates device noise, where the difference is approximately 40 dB. As the frequency is increased, this difference is initially reduced to approximately 20 dB at 10 MHz. As the frequency increases further, however, switching noise increases whereas device noise remains constant. This result is accurate until approximately 1 GHz, beyond which switching noise starts to decrease. According to this analysis, switching noise dominates device noise within the frequency range of interest. Thus, to increase the input sensitivity of the potentiostat, the counter (primary digital block with high switching activity) should be sufficiently isolated

from the sense amplifier (primary victim block). Note that the switching noise analysis is performed when the counter and sense amplifier have separate power/ground networks. Substrate, however, remains as the primary medium for the transmission of switching noise. The noise that couples to the bulk nodes of the transistors significantly contributes to the input-referred current noise.

3.5.3 Application of Reverse Body Bias

Reverse body biasing is applied to the input NMOS transistor within the sense amplifier to alleviate input-referred switching noise. The effect of reverse body biasing on g_m, g_{mb}, amplifier gain, output swing, phase margin, and bandwidth are listed in Table 3.5 for different bias voltages. It is shown that, up to -3 V, g_m, DC gain, output swing, bandwidth, and phase margin remain approximately the same while g_{mb} is significantly reduced, weakening the bulk-to-input transfer function. Note that as opposed to the two-stage and folded cascode amplifiers discussed in the previous section, the sense amplifier in this case study operates in a closed-loop with a large feedback resistance. Thus, gain, bandwidth, and output swing are not affected by the reverse body bias.

Reduction in input-referred switching noise is illustrated in Fig. 3.19 when -3 V is applied as the reverse body bias. The *y* axis on the right hand side shows the dB reduction in input-referred switching noise as a function of frequency. More than 10 dB reduction is demonstrated up to 1 MHz. The noise reduction decreases to 4 dB and 1.5 dB at, respectively, 100 MHz and 1 GHz. The *y* axis on the left hand side shows the increase in the noise tolerance as a function of frequency. Specifically,

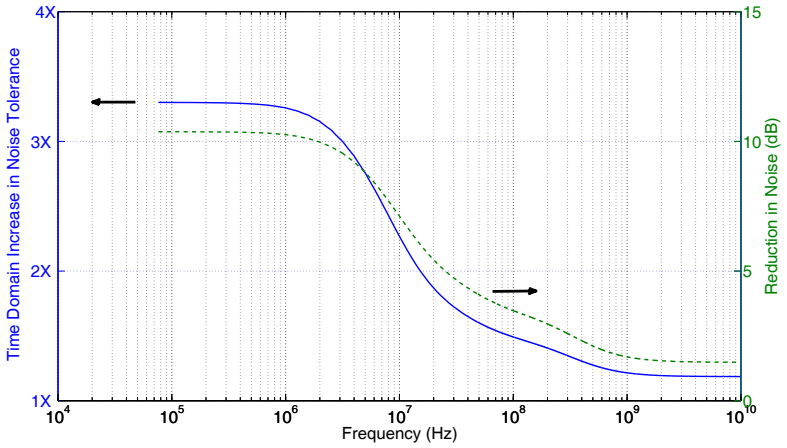


Figure 3.19: **Noise reduction and time domain increase in noise tolerance when -3 V is applied as the reverse body bias.**

when -3 V is applied as the reverse body bias, the peak amplitude of the time domain switching noise at the bulk nodes can be increased by more than three times (from 8 mV when bulk bias is zero to 26 mV when bulk bias is at -3 V) while maintaining the input-referred switching noise constant. Thus, significantly more substrate noise can be tolerated through reverse body biasing.

3.6 Summary

An analysis flow has been proposed to evaluate the significance of switching noise in analog circuits. Switching noise at the bulk node of a transistor (modeled as a decaying sine wave) is first transmitted to the input node by utilizing the corresponding transfer functions to obtain *input-referred switching noise*. Input-referred switching noise is used as a figure-of-merit and compared with equivalent input device noise (thermal and flicker) to identify the dominance regions as a function of

time domain switching noise characteristics such as amplitude and period. A two-stage and folded cascode amplifier are used to demonstrate the proposed flow. For both amplifiers, the time domain switching noise amplitude that leads to equal input device and switching noise is determined as the second figure-of-merit. Knowing this amplitude is helpful to gain intuition on the required reduction in switching noise since existing noise reduction techniques typically increase physical area and power consumption. It is also demonstrated that reverse body biasing weakens the bulk-to-input transfer function, thereby alleviating the effect switching noise without affecting the remaining design specifications such as gain, bandwidth, output swing, and phase margin. A case study is described to apply the proposed flow and reverse body biasing to a potentiostat circuitry where input sensitivity is critical. Noise dominance regions are identified and up to 10 dB reduction in input-referred switching noise is demonstrated through reverse body biasing.

Chapter 4

Package-Embedded Spiral Inductor Characterization with Application to Switching Buck Converter

In this chapter, design and characterization of built-in package-embedded spiral inductors with application to switching buck converter are investigated. Background on switching buck converters is provided in Section 4.1. Proposed method to develop high efficiency switching buck converter is discussed in Section 4.2.

4.1 Background on DC-DC Buck Converter

Efficient voltage regulation and conversion are essential mechanisms in modern IC design process due to power management and heterogeneous computing. Most

of the existing low power design methods such as multi-voltage design, dynamic voltage frequency scaling, and low swing clocking require high efficiency and low cost regulators.

As mentioned in Chapter 1, for a switching buck converter, in order to decrease the size of the inductor, the switching frequency should be increased. Higher switching frequency, however, increases the dynamic loss and thus decreases the power efficiency. An intermediary solution (between a fully on-chip inductance and an off-chip discrete inductance) is investigated in this project where the inductor is built within a flip-chip package in a spiral fashion whereas all of the other components are integrated on-chip. Note that this approach is different from discrete inductors integrated into a package (common practice in literature) since in the proposed case, the inductor is built using existing metal interconnects within the package layers and fabricated at the same time as the package. Package-embedded inductors have been previously discussed in [52]. The primary emphasis has been on experimental characterization. The applicability of this approach to switching buck converters has not been discussed.

A higher inductance with a reasonable quality factor can be achieved by exploiting the greater flexibility of package area as compared to die area, as demonstrated in this chapter. This package-embedded spiral inductor is connected to the die via low resistance controlled collapse chip connection (C4) bumps. Thus, the switching frequency of the buck regulator can be reduced to minimize dynamic power loss and enhance power efficiency. Furthermore, package flexibility can be further utilized to develop an *array of package-embedded spiral inductors* for an interleaved

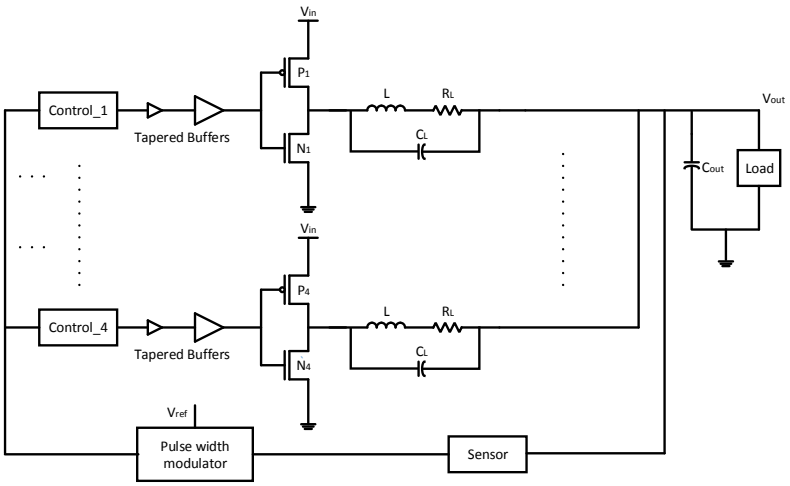


Figure 4.1: **An interleaved multi-phase switching buck regulator architecture.**

multi-phase buck regulator architecture (see Fig. 4.1). Thus, power efficiency and output ripple can be further enhanced.

4.1.1 Background of Switching Buck Converter

The one phase schematic is discussed in Chapter 2. An interleaved multi-phase architecture has been commonly used to reduce the size of the individual inductors (and therefore ESR) without increasing the output ripple, as shown in Fig. 4.1. In this case, multiple buck converters operate in a parallel fashion, but at a different phase. Each regulator has an individual inductor, but share the same capacitor. Thus, the high ripple across each inductor is partially canceled at the output. Package-embedded spiral inductors provide a unique opportunity for interleaved architecture since an array of spiral inductors can be built using the package metal layers and fabricated as part of the package fabrication process.

4.2 Proposed Method

4.2.1 Package-Embedded Spiral Inductor Characterization

A multi-layer flip-chip package is assumed. Cross-section of the package illustrating each layer is shown in Fig. 4.2 [52,53]. Three copper metal layers exist with two different thicknesses. The top metal (F3) is 35 μm thick whereas the bottom two metal layers (F1 and F2) are 15 μm thick. There is an aluminum pad layer with 15 μm thickness. The dielectric layers (D1 and D2) are 30 μm thick and consist of flame retardant (FR4) epoxy. The inductor is built on layer F3 and is connected to the C4 bumps located at the bottommost layer filled with epoxy with 75 μm thickness [54]. The C4 bumps connect the inductor terminals to the on-chip components (power transistors and capacitance).

This package structure is modeled using a commercial finite element method (FEM) based full wave electromagnetic field solver ANSYS HFSS (high frequency structural simulator). The DC and low frequency characteristics are analyzed using ANSYS Q3D Extractor. A conventional spiral inductor is illustrated in Fig. 4.3(a) where the important physical characteristics are highlighted such as the number of turns T, internal diameter D_{in}, external diameter D_{out}, width w, and spacing s. The following relationship holds among these parameters, assuming that the number of turns T is an integer,

$$D_{in} = D_{out} - 2 \times (T+1) \times w - 2 \times T \times s. \tag{4.1}$$

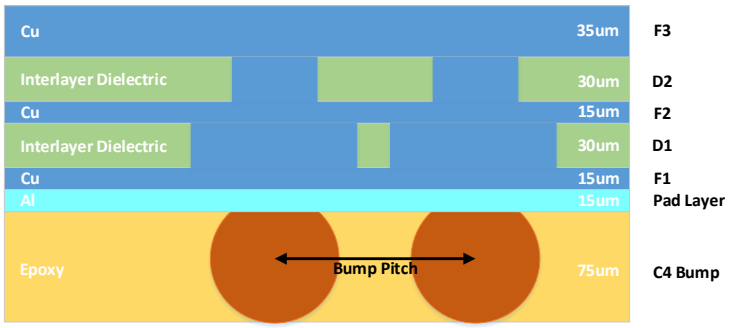


Figure 4.2: **Cross-section of the multi-layer flip-chip package where spiral inductors are built.**

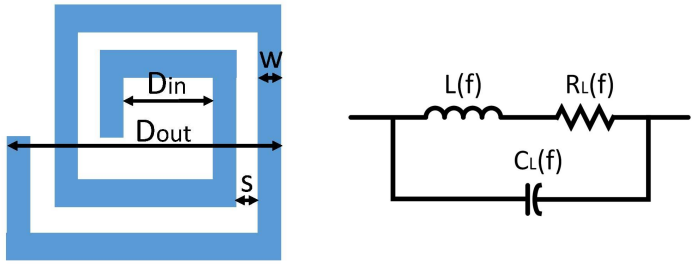


Figure 4.3: **Typical spiral inductor: (a) physical characteristics, (b) equivalent electrical circuit.**

An electrical equivalent circuit is shown in Fig. 4.3(b) assuming a one-terminal, two-port extraction [55]. The frequency dependent $L(f)$, $C_L(f)$, and $R_L(f)$ refer, respectively, to the extracted inductance, capacitance, and ESR. These frequency dependent components are extracted by analyzing the Y parameters from HFSS. Specifically, Y_{11} is

$$Y_{11}(f) = \frac{1}{R_L(f) + j\omega L(f)} + j\omega C_L(f). \tag{4.2}$$

Assuming the series capacitance $C_L(f)$ varies only marginally with frequency [55],

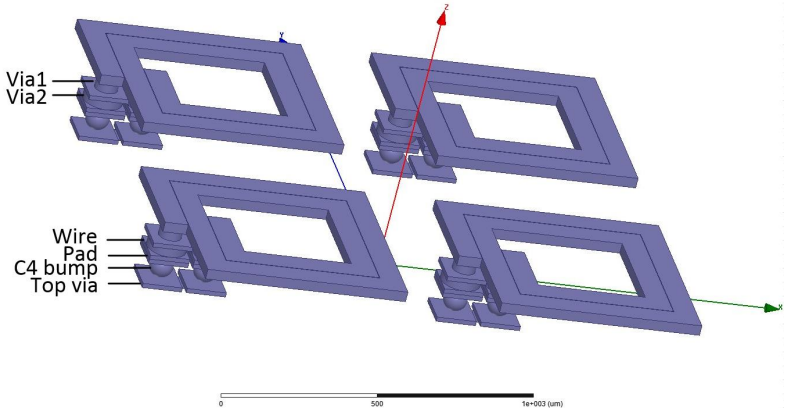


Figure 4.4: **Array of package-embedded spiral inductors modeled in full wave electromagnetic simulator HFSS.**

this component is extracted from Q3D Extractor at a low frequency. The admittance $j\omega C_L(f)$ is then subtracted from Y_{11} and the reciprocal of the remaining term is the impedance

$$Z(f) = R_L(f) + j\omega L(f). \tag{4.3}$$

$R_L(f)$ and $L(f)$ are determined from, respectively, the real and imaginary parts of the Z parameter, extracted from HFSS at the frequency of interest.

An array of four inductors modeled in HFSS considering the package structure described above is shown in Fig. 4.4. In this example, each inductor occupies an area of 1 mm $\times$ 1 mm. Two analysis modes are considered to determine the physical characteristics of the inductor and maximize the quality factor [56]:

- D_{in} based model: D_{in} is kept constant at 50 μm. The width is progressively increased (with a step size of 1 or 4 μm, depending on required accuracy) until D_{out} reaches 1 mm, the available dimension for the package area.

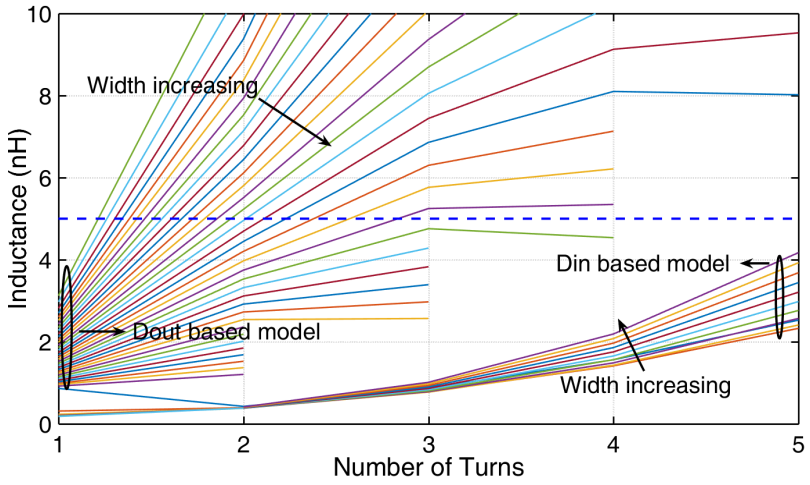


Figure 4.5: **Design space of the package-embedded spiral inductor as a function of number of turns and width at constant spacing, thickness, and frequency.**

- D_{out} based model: D_{out} is constant at 1 mm. The width is progressively increased (with a step size of 1 or 4 μm) until D_{in} reaches the minimum allowable value. Note that according to (4.1), as width is increased, D_{in} is reduced.

For both analysis modes, spacing is constant at 2 μm to maintain the tight coupling of the magnetic field. Note that these analysis are achieved at different number of turns, producing a large design space, as illustrated in Fig. 4.5. Also note that the frequency is constant at 50 MHz. From this design space, the inductors that satisfy the required inductance can be extracted (for example, see the dashed horizontal line at 5 nH). Here, every design point that intersects with the horizontal line satisfies the required inductance. Thus, the point that achieves the highest quality factor (minimum ESR) can be chosen. It is important to note that for inductors in the range of several nano henry and above, the minimum ESR occurs within the D_{out}

based model since the D_{in} based model requires a large number of turns to reach the required inductance, which increases the ESR. Thus, for minimum ESR, a good design practice is to choose a small number of turns at a sufficiently high width that can achieve the required inductance.

4.2.2 Application to Interleaved Switching Buck Converter

Package-embedded spiral inductors designed and characterized in the previous section are used for a switching DC-DC converter, designed in 45 nm technology. The converter converts an input voltage of 1.2 V to an output voltage of 0.9 V while supplying 1 A of load current. Referring to Fig. 4.1, P_1 and N_1 are two large power transistors driven by a 5-stage tapered buffer, followed by a low pass filter. The switching frequency is 50 MHz (lower than existing buck regulators with on-chip inductor [22, 57–59]) since the flexibility of the package is utilized. Duty cycle is 0.79 that is slightly larger than the conversion ratio (0.75) to compensate for the voltage drop across the ESR of the inductor [60].

For a single phase buck converter, the required inductor is determined by [4],

$$L = \frac{(V_{in} - V_{out})D}{2\Delta I_L f_s}, \tag{4.4}$$

where V_{in} and V_{out} are, respectively, input and output voltages, D is duty cycle, ΔI_L is the current ripple (half of the peak-to-peak current), and f_s is switching frequency. Substituting the values, L is determined as 7.9 nH. Assuming the output voltage ripple cannot exceed 5% of the output voltage, the minimum required capacitor

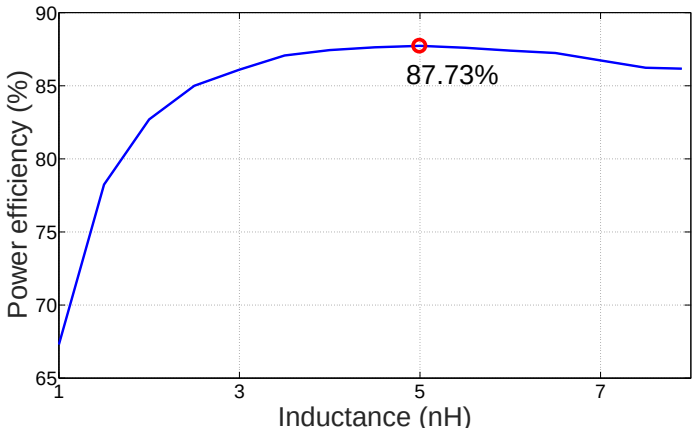


Figure 4.6: **Power efficiency of an interleaved four-phase buck converter as a function of inductance (of a single phase).**

C_{out} is determined by [4]

$$C_{out} \geq \frac{5(V_{in} - V_{out})D}{4V_{out}Lf_s^2}, \tag{4.5}$$

which is calculated as 16.7 nF, taking approximately 0.5 mm^2 on-chip area in 45 nm technology. If 7.9 nH of inductance is characterized and extracted by HFSS (within an area of 1 mm^2), the output voltage of the converter exhibits a significant drop due to relatively large ESR. Thus, an interleaved four-phase buck converter is developed to reduce the inductor and therefore ESR without increasing the output ripple. The power efficiency of the converter as a function of inductor in a four-phase buck converter is shown in Fig. 4.6. The highest efficiency of 87.73% is achieved when each inductor in the interleaved topology is approximately 5 nH. Thus, *an array of package-embedded spiral inductors* is characterized in HFSS where each of the four inductors is 5 nH and occupies 1 mm^2 area (see Fig. 4.4). The overall area consumed in the package by spiral inductors is 4.076 mm^2. To determine the physical characteristics of the inductors, the procedure described in

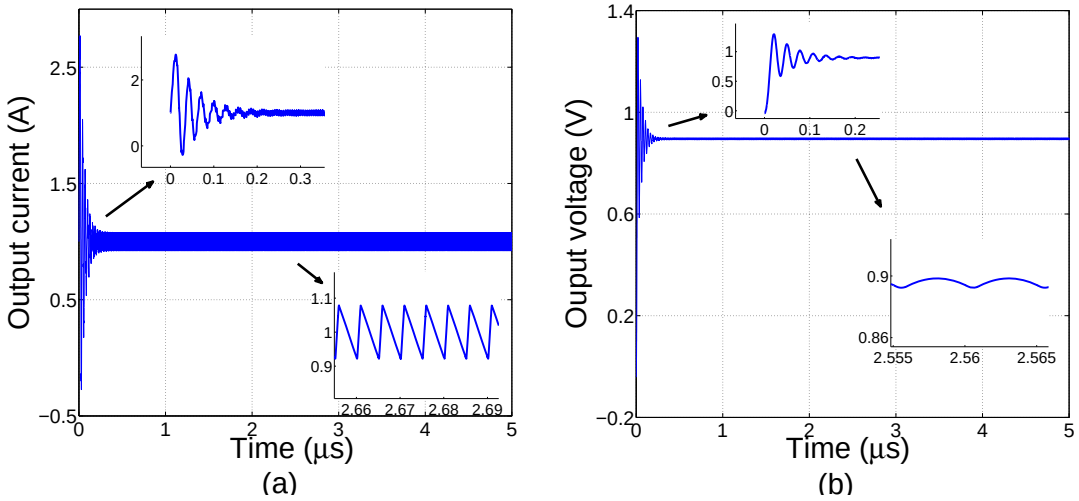


Figure 4.7: **Simulation results of the interleaved, four-phase buck converter with package-embedded spiral inductors: (a) output current, (b) output voltage.**

Parameter	[57]	[58]	[59]	[61]	This work
Inductor type	glass epoxy inductor, on chip	stacked, on chip	stacked, on chip	air-core, in package	spiral, in package
Conversion ratio	0.7	0.75	0.73	0.785	0.75
Output load	70 mA	190 mA	125 mA	0.4 A	1 A
Switching frequency	200 MHz	170 MHz	300 MHz	233 MHz	50 MHz
Power efficiency	62%	77.9%	74.5%	84.5%	87.73%
Voltage ripple	10%	4.4%	1.17%	5%	0.33%

Table 4.1: Comparison of the proposed buck converter with existing approaches.

the previous section is followed. After the entire design space is obtained, as shown in Fig. 4.5, the number of turns and widths that produce the required inductance are analyzed for quality factor.

The highest quality factor of 11.8 is achieved (at the switching frequency of 50 MHz) with a 2-turn spiral inductor and 64 μm width. The D_{in} is 608 μm and D_{out} is 1 mm. The ESR and series capacitance are extracted, respectively, as 132 mΩ and 50.7 fF.

The four-phase interleaved buck converter is simulated in SPICE with the elec-

trical model of the package-embedded spiral inductors. The current ripple on each phase is 398 mA. The maximum and minimum output current in steady state are, respectively, 1.078 A and 0.922 A. Thus, the output current ripple is 78 mA, 7.8% of the output current, as depicted in Fig. 4.7(a). Note that the output current ripple is much smaller than the ripple on each phase due to the interleaved multi-phase topology.

The transient response time when current abruptly changes from 0 to 1A is 0.2 μs, as shown in Fig. 4.7(a). The corresponding output voltage is plotted in Fig. 4.7(b). The overshoot when the load current abruptly falls to zero is 0.3 V. The output voltage ripple in the steady state is only 3 mV.

The simulation results are compared with several prior work, as listed in Table 4.1. At comparable conversion ratios, this work achieves the highest power efficiency while supplying a load current of 1 A. The switching frequency is lowest due to the package-embedded spiral inductors. These results demonstrate the applicability and advantages of built-in, package-embedded spiral inductors for DC-DC switching buck converters.

4.3 Summary

Design and characterization of built-in package-embedded spiral inductors have been investigated in this chapter through comprehensive electromagnetic field simulations using HFSS. A detailed and realistic flip-chip package has been considered. An array of spiral inductors have been characterized with application to an interleaved switching buck converter. The greater flexibility of the package area has

been utilized to lower the switching frequency, thereby increasing power efficiency. The proposed buck converter outperforms existing buck converters, demonstrating the benefits of package-embedded spiral inductors for switching regulators.

Chapter 5

Design and Simulation of a 2-D Array Flexible Ultrasound System for Tissue Characterization

The flexible ultrasound system (FUS) is introduced in Section 5.1. Dual array transducer sub-block structure design simulation and verification are proposed in Section 5.2. FUS hardware design is discussed in Section 5.3 and the chapter is concluded in Section 5.4.

5.1 Flexible Ultrasound System Structure

FUS is an integrated ultrasound system with the combination of software-based signal controlling and dual transducer design that focuses on bone density and ar-

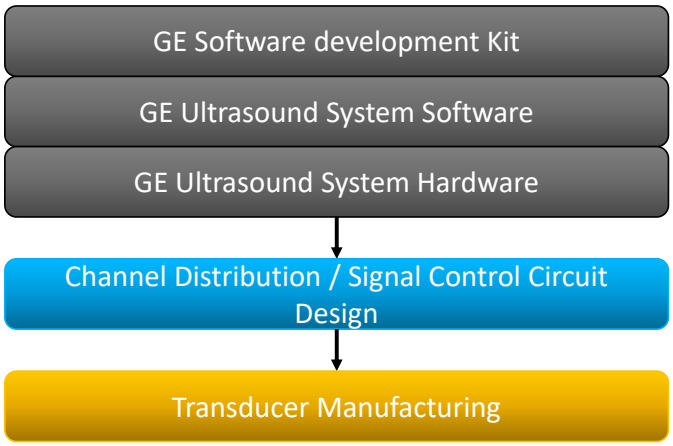


Figure 5.1: **Flexible ultrasound system block diagram.**

chitecture diagnosis as well as bone loss treatment. FUS block diagram is shown in Fig. 5.1. The system primarily consists of 1) *GE* C++ or MATLAB software development kit (SDK) which includes researcher applications for research user, 2) *GE* ultrasound system software that can switch the mode from research user to clinical user, 3) *GE* ultrasound hardware which includes the extension cable, dual probe adaptors and high power module, 4) printed circuit board (PCB) to regulate transducer sub-block signal distribution and 5) a 32 by 32 two dimensional phased array transducer. A significant advantage of the FUS is the software based design. The parameters such as beam forming, scanning, focusing and data acquisition are all regulated by software instead of a fixed hardware design. The system complexity is therefore greatly reduced due to less hardware components.

5.2 Dual Array Transducer Designing Simulation and Verification

Dual array transducer kit is a critical part of the entire system. Two identical probes that work as transmitting (Tx) and receiving (Rx) transducers respectively are designed. Due to the large number of elements of the probe, a sub-block structure is proposed. The dual array transducer kit design simulation as well as multiple tradeoffs are analyzed in this section to verify that sub-block structure can meet the design requirement. The design specifications as well as sub-block structure are introduced in Section 5.2.1. The lateral resolution and apodization are discussed, respectively, in Sections 5.2.2 and 5.2.3.

5.2.1 Dual Array Transducer Specification

Tx and Rx transducers are two identical 2-D flat surface aperture transducers working in the phased array mode. Note that this simulation work is based on total 729 elements for each transducer. These elements are arrayed in 27 by 27 as a square.

The center element of Tx transducer is located at [0, 0, 0] along lateral (x axis), elevational (y axis) and axial (z axis) directions respectively. Primary related parameters of the transducer in this work are listed in Table 5.1. Dual array transducer working diagram is shown in Fig. 5.2. In this diagram, 65 by 65 focal points wait for scanning in a frame parallel with the transducer aperture are used to model bone and tissue. The gap between two adjacent focal point is 1 mm and the total size of

Parameter	Value
Center frequency	1 MHz
Sampling frequency	100 MHz
Wavelength (λ)	1.54 mm
Element width (a)	1.05 mm
Element height (h)	1.05 mm
Element kerf (k)	0.2 mm
Size of probe aperture	$33.55 \times 33.55\ mm^2$
Target frame size	$64 \times 64\ mm^2$

Table 5.1: Parameters of dual-probe and simulation setting.

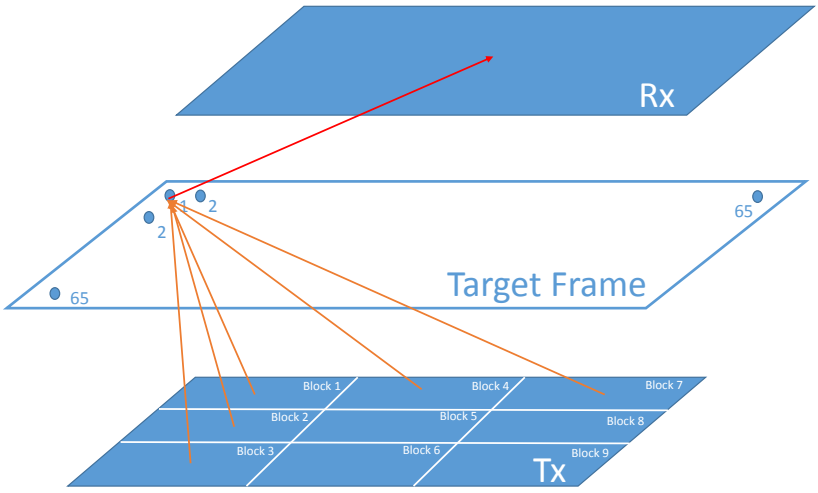


Figure 5.2: **Operation of the Tx and Rx transducers.**

this frame is 40.96 cm^2. This target frame is located in the middle of two transducers parallel with two apertures that has 60 mm distance to both Tx and Rx transducers along axial axis.

Since both transducers work in phased array mode, ultrasound signal emitted from each element steers angle and travels through each desired focal point without moving of the transducers. Thus the challenges in adjusting the transducer position and orientation is avoided. Each individual element is expected to be narrow so that the ultrasound signal can cover a relatively large area at far field and thus contribute more energy to focal points. The maximum beam angle that can be covered by single element is [62]

$$\theta = \arcsin(0.514 \times \frac{\lambda}{a}), \tag{5.1}$$

where λ is wavelength and a is element width. The theoretical maximum angle that can be covered by each element in this case is 48.9°. In order to guarantee enough energy be propagated to all the targets, each element should have the ability to direct to every target in the frame. In other words, any target beyond the range of this element angle cannot receive enough energy from that specific element. Note that the longest distance between the element and the target is along the diagonal line that equals to 91.4 mm. The distance between the element and the propagation target is 60 mm. Thus the largest angle needed is equal to arccos (60 / 91.4), exactly matches 48.9°.

Narrow elements have the advantage of more beam spreading while inevitably result in small overall aperture size and thus sacrifice lateral and elevational resolution. Note that lateral and elevational resolution are the same in FUS due to the

symmetric structure. This tradeoff has been balanced by providing a relatively large area of the aperture while dividing the aperture into 729 elements. By considering the above two criteria, the width of each element is set as 1.05 mm, slightly larger than half of the wavelength.

Another tradeoff is the system complexity and the number of elements. As the number of elements to improve the performance of transducers increases, the control signal as well as the hardware design get more complicated. This issue has been solved by using sub-blocks in Tx transducer. On Tx side, 729 elements are divided into 9 identical square blocks, each of which contains 81 elements. During the transmission, these blocks are activated in sequence and analog signals coming from the software kit are distributed to each element in one of the block. While on the Rx side, all elements are enabled.

Tx transducer works based on block activation as described above and the sub-block structure is shown in Fig. 5.2. Block 1 is activated first while the rest are deactivated. 81 elements in block 1 target the same focal point and excite ultrasound signal, the signals are then be received by Rx transducer. Appropriate delay modules are inserted into the process of exciting signal based on the distance to the focal point to ensure that the signals reach the Rx side simultaneously. These 81 elements then steer at next focal point until all the desired points in the frame have been scanned. Same procedure is repeated for all the other 8 blocks. Radio frequency (RF) data received from all those blocks are summed at the receiving side as a beamformed RF data. In this way, the system complexity is reduced by emitting only 81 ultrasound signals at one time, and the small activated size of Tx

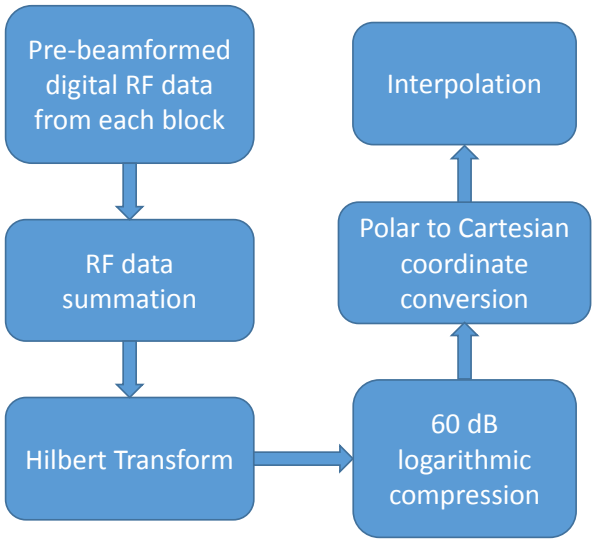


Figure 5.3: **Flowchart illustrating the beamforming and image processing at the receiving side.**

aperture is compensated by the superposition of RF data obtained from all blocks. Fig. 5.3 is the flow diagram of the entire beamforming and image process. Typical delay-and-sum is applied to the the received RF data from each block and filtered for bone imaging, proper apodization is applied, the summed RF data is then Hilbert-transformed to get the envelop of each scan line, the log compression and scan-conversion is applied to generate a sector image.

The above transducer design and working procedure is simulated by *FIELD II* [63, 64]. Specifically, Tx and Rx transducers are 12 cm away from each other along the axial direction. The target frame is located in the middle which is 6 cm away from both Tx and Rx transducers. Note that since the 2-D focal points are symmetric to the center, only one row of focal points located at [x, 0, 60] mm along lateral direction are simulated for convenience.The gray-scale simulation is

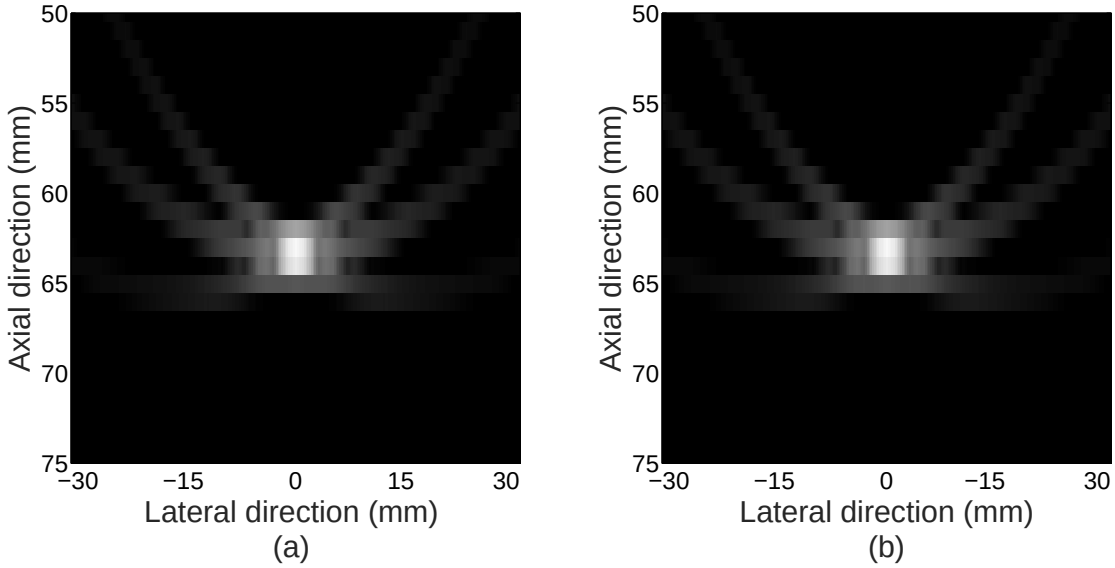


Figure 5.4: **Gray-scale analytical simulation: (a) all Tx elements are activated simultaneously, (b) Tx elements are activated block by block.**

shown in Fig. 5.4. One target is located at [0, 0, 60] mm to model human tissue, which is the brightest spot in the figure. The lobes located closely around the target are side lobes. The simulation results of activating all 729 elements of Tx and activating elements block by block have only slight difference, which implies that using 81 analog signals instead of 729 can significantly decrease the complexity of the system while still maintaining the sharpness of the gray-scale figure. The disadvantage of smaller aperture area is compensated by the superposition of the RF data of each block.

Scanning time is another concern since each focal point now needs to be scanned 9 times. For the total distance of 12 cm from Tx to Rx and 1540 m/s media velocity, the time cost from transmission to receiving for the ultrasound signal from one ele-

ment is approximately 78 μs, assuming that the time on delay module is neglected. This is also the time cost for a single block of Tx transducer as the elements in the same block are emitting together. Thus the time for the entire Tx transducer targeting a single focal point and be received by Rx transducer is 702 μs. The total time to scan the entire two dimensional 65 by 65 focal points frame is approximately 2.97 s. Compared to 0.33 s when all elements are transmitted and received together, the block transmittion method needs 2.64 s more but with a huge advantage of reducing the number of electrical signal and corresponding hardware cost.

5.2.2 Lateral Resolution

Lateral resolution (LR) is a crucial specification to be considered in design procedure that reflects the ability of the system to distinguish two adjacent points. LR is defined as the spacing in the transverse plane at which the points are just separately resolvable [65]. For a rectangular aperture, LR is calculated at the points where power intensity value is reduced to half, which is 3 dB down from the peak point of main lobe in terms of decibel [66]. LR is determined by beam directional factor, size of the aperture and the focal length. The analytic expression of directional factor is [65]

$$H_r(\Phi_x, \Phi_y) = [\frac{\sin[(kb\sin\Phi_x)/2]}{(kb\sin\Phi_x)/2}\frac{\sin[(kh\sin\Phi_y)/2]}{(kh\sin\Phi_y)/2}], \tag{5.2}$$

where Φ_x and Φ_y are the divergence along the lateral and elevational direction respectively, b and h are the width and height of the probe aperture respectively. The

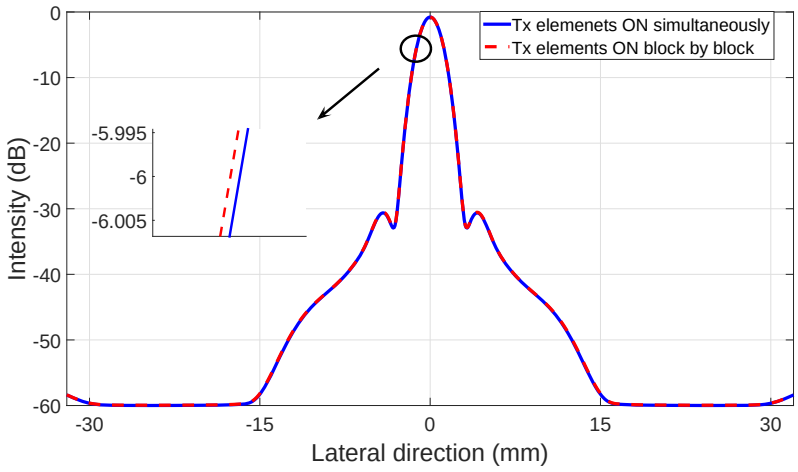


Figure 5.5: **Lateral resolution comparison between all elements activated (solid line) and elements are activated block by block (dash line).**

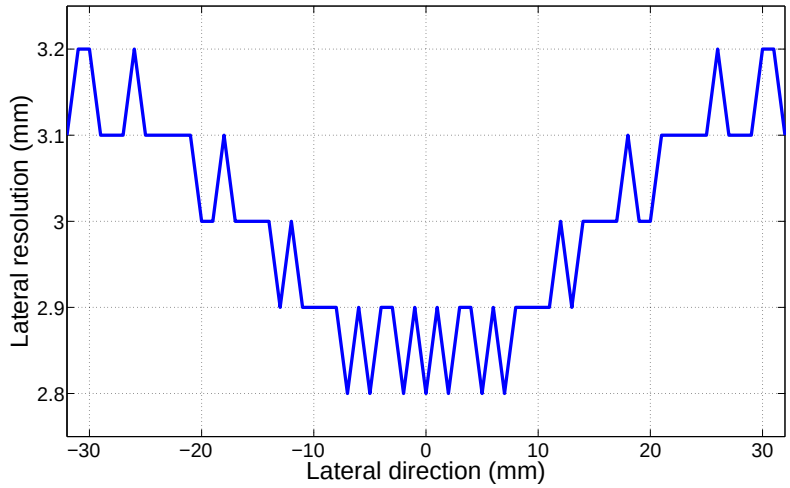


Figure 5.6: **Lateral resolution along lateral direction.**

calculated value of $\sin\Phi_x$ is 0.0203 when $H_r(\Phi_x)$ equals to $1/\sqrt{2}$, 3 dB down from the maximum pressure. The pressure attenuation at this divergent angle is then 6 dB as Rx also introduces 3 dB loss. For a focus system, the transformation from far-field angular distribution into focal plane spatial distribution is

$$\sin\Phi_x = \frac{x_1}{l_f}, \tag{5.3}$$

where x_1 is the half 3 dB focused spot size and l_f is focal length. Thus the theoretical lateral resolution is

$$LR = 2 \cdot x_1 = 2 \cdot l_f \cdot \sin\Phi_x. \tag{5.4}$$

The theoretical LR value when all 27 $\times$ 27 elements of Tx are excited is 2.436 mm. In simulation process, LR is measured at the point of full width at half maximum (FWHM) of the power. The pattern in Cartesian coordinate is shown in Fig. 5.5, this target gives the lateral resolution when it is located at the center of the aperture along propagation direction. As the figure shows, the LR of the system equals to 2.8 mm when all elements are enabled and is 0.364 mm poorer than theoretical value. When elements are enabled block by block, LR reaches almost the same value. The LR has not been sacrificed by the smaller size of aperture because the RF data are added together to compensate the loss area.

In order to verify the lateral resolution of the system, 65 targets are put in sequence along the lateral direction from -32 mm to 32 mm at 6 cm along axial direction, with 1 mm gap between adjacent target. The simulation step is set as 0.1 mm for precise result. Lateral resolution for all 65 phantoms is depicted in Fig. 5.6.

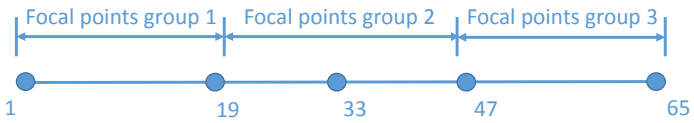


Figure 5.7: **Categorization of focal points for apodization application.**

The best lateral resolution is in the middle point since more energy is propagated and the points on the side have poorer LR up to 3.2 mm.

5.2.3 Apodization

Apodization is a common filtering technique to suppress unwanted side lobe intensity. Various window functions as well as coefficient ranges are available based on system specifications and application [66].

In FUS, Hann window is applied. Since focal points cover a wide range along lateral direction, these points are categorized into three groups, as illustrated in Fig. 5.7. When Tx scan the focal points located at group 1, right half of the Hann window is applied to the left 14 columns of the Tx elements matrix. The right 13 columns of elements have no weights distributed since the distance between these elements and focal points are relatively far and the energy these elements contribute to the beam forming is limited. When Tx steers to group 2, the entire aperture is covered by a full Hann window. For the focal points located at group 3, left half of Hann window is applied to the right 14 columns of the Tx elements. Alternatively, Rx transducer has been applied a full Hann window on all the elements at all time. Note that 9 blocks of Tx transducer are still activated in sequence but following the way of apodization regulated above when steering scanning angle.

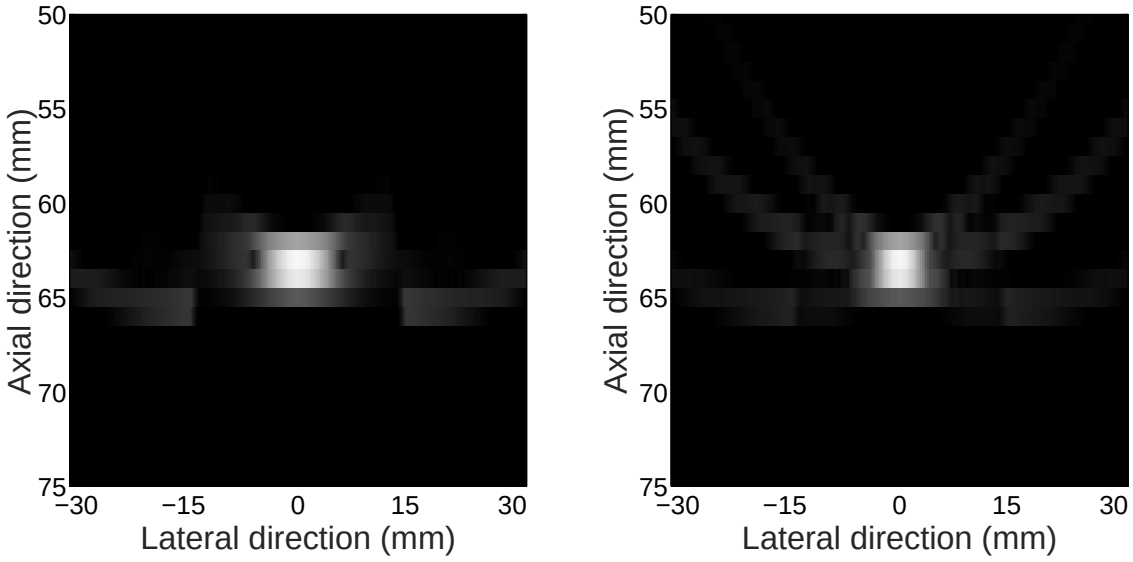


Figure 5.8: **Gray-scale analytical simulation: (a) apodization by Hann window weights 0 to 1, (b) apodization by Hann window weights 1 to 2.**

The gray-scale figure after apodization is shown in Fig. 5.8 (a). Compared to Fig. 5.4 (b), side lobes located around the target has been reduced significantly. The corresponding voltage trace signal intensity is shown by red dashed line in Fig. 5.9. As depicted in the figure, side lobes with no apodization have intensity up to -31 dB. This value decreases to -47 dB after applying apodization.

The primary drawback of apodization is the reduction in lateral resolution due to smaller area of the aperture. Various apodization coefficients can be applied to reach the optimum balance between side lobes and lateral resolution. In order to compensate the loss of lateral resolution and reduction in the side lobes, apodization weights are adjusted to be in the range of 1 to 2 instead of 0 to 1. The gray-scale is shown in Fig. 5.8 (b), side lobes have higher intensity than apodization weights from 0 to 1 but still be suppressed compared to no apodization case.

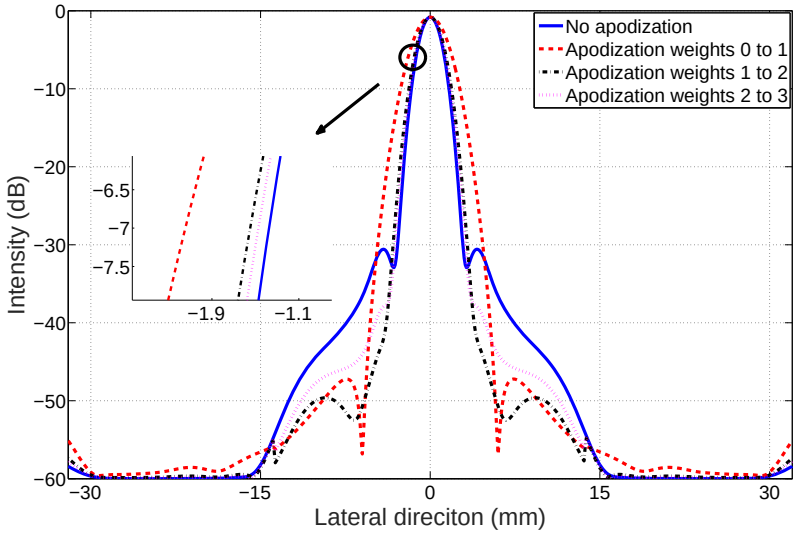


Figure 5.9: **Voltage trace signal intensity with different apodization weights.**

Apodization weights	LR (mm)	Side lobe max intensity (dB)
No apodization	2.8	-30.58
Weights 0 to 1	4.4	-47.28
Weights 1 to 2	3.2	-42
Weights 2 to 3	3	-37.5

Table 5.2: Comparison of lateral resolution and side lobes at different apodization weights.

Fig. 5.9 shows the voltage intensity with different apodization weights and the values are summarized in Table 5.2. The imaging without apodization has the highest intensity of side lobes but best lateral resolution is equal to 2.8 mm. The Hann window with apodization coefficients from 0 to 1 gives lowest side lobes but sacrifice the LR for approximately 1.6 mm. Apodization weights between 1 to 2 gives 3.2 mm LR. The application for the specific combination should be determined by tissue specifics. For example, higher resolution imaging may help for soft tissue characterization while less side lobe may be needed for hard tissue evaluation.

5.3 FUS Hardware Design

FUS hardware design includes the layout of transducer as well as the circuit board schematic. The number of transducer elements in the FUS system is extended from 27 by 27 to 32 by 32 which is 1024 elements in total. The transducer elements layout as well as analog signal distribution are given in Section 5.3.1 and the circuit schematic design is discussed in Section 5.3.2.

5.3.1 Transducer Elements Layout and Analog Signals Distribution

FUS transducer element array layout is shown in Fig. 5.10. In order to reduce the system complexity, 32 by 32 elements are divided into 16 identical blocks labeled from (1,1) to (4,4), and each block is an 8 by 8 square. Therefore total 64 analog signals are required in order to activate an entire block.

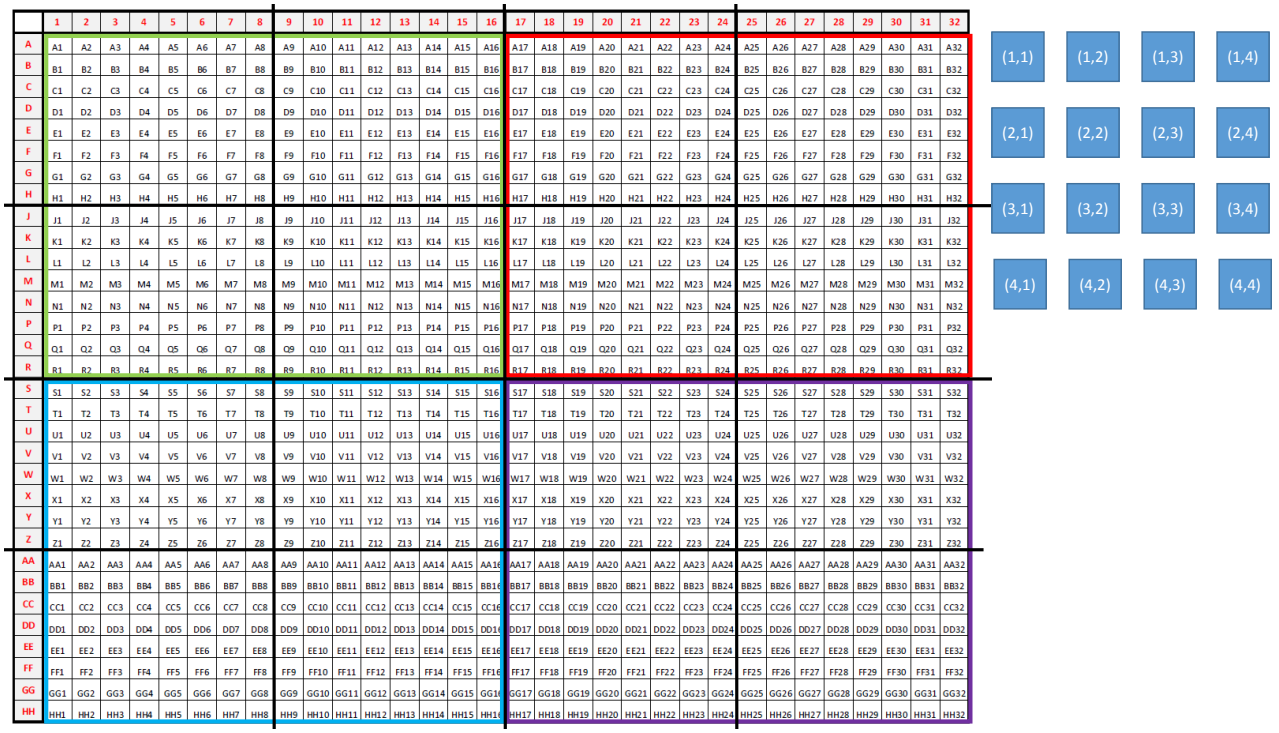


Figure 5.10: **Probe element array view.**

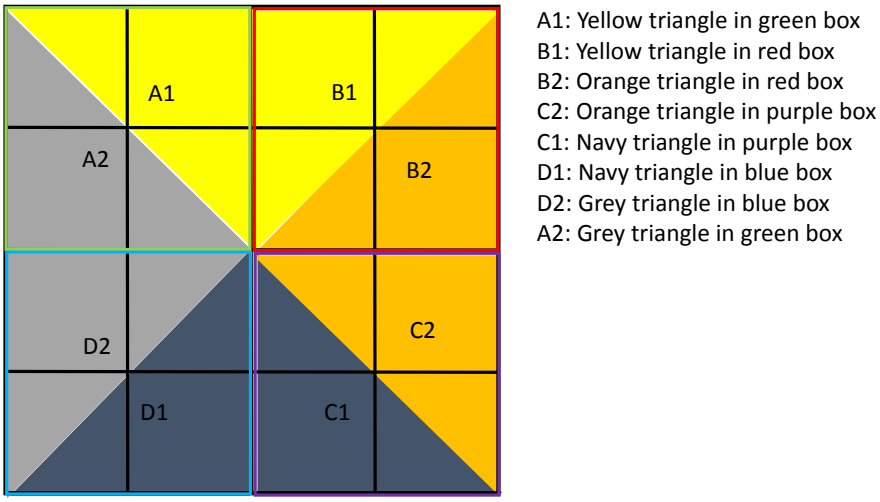


Figure 5.11: **Probe connector layout.**

The probe receives electrical pulses from PCB via 8 probe connectors. The connector layout is shown in Fig. 5.11, 16 squares in this figure represent 16 sub-blocks. Connector A1 is connected to the elements located in the yellow triangle in the green large block. For example, connector A2 is connected to the elements located in the grey triangle in the green large block. Each of four big blocks marked in Fig. 5.11 needs two probe connectors to cover all the elements. If Block (3,3) needs to be activated for example, then the analog signals are distributed to the element through connector C1 and C2. If Block (1,2) needs to be activated, the analog signals are sent to the element through connector A1 only.

The PCB that is integrated on the back side of the transducer serves as the intermediate stage to distribute the analog electrical signals to the specified transducer elements. The PCB structure is shown in Fig. 5.12. Board E serves as the motherboard and is directly connected to *GE* dual probe adaptor to receive 64 analog

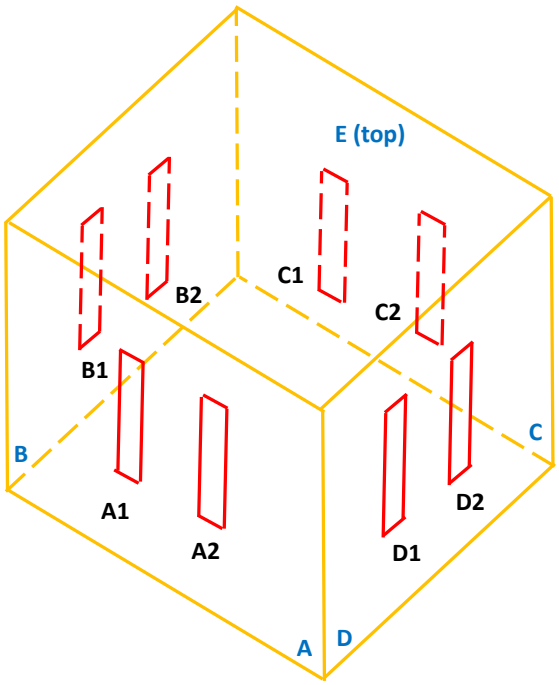


Figure 5.12: **4-stage customized high voltage DeMUX structure.**

input signals, ground signals as well as control signals. Boards A, B, C and D are identical and linked to Board E through board-to-board connector. As mentioned previously, the sub-block structure requires the entire surface to be divided into 16 identical 8 by 8 square blocks. This is realized by connecting the Boards A, B, C and D to appropriate probe connectors which are listed in Table 5.3. The corresponding element blocks that are controlled are also listed in the table. Each board is in charge of one fourth of the elements. For example, probe connector A1 and A2 are connected to Board A to control the element in green block.

PCB	Probe Connector	Block
Board A	A1 and A2	(1,1), (1,2), (2,1), (2,2)
Board B	B1 and B2	(1,3), (1,4), (2,3), (2,4)
Board C	C1 and C2	(3,1), (3,2), (4,1), (4,2)
Board D	D1 and D2	(3,3), (3,4), (4,3), (4,4)

Table 5.3: Connection between PCB and probe connectors.

5.3.2 Circuit Schematic Design

As mentioned in the previous section, 64 analog signals received from *GE* adaptor need to be distributed to different sub-blocks and each time only one of the sub-blocks is activated. This is realized by using *Supertex* HV2809 high voltage analog switching IC which is served as the demux. HV2809 works with 3V power supply voltage. The positive (VPP) and negative (VNN) high bias voltages are +100V and -100V, respectively. HV2809 is a 32-channel switch that can be configured as a 1:2 demux, the combination of two chips results a 1:4 demux. In order to create a signal transmission structure with 64 inputs and 1024 outputs, a total of 60 chips are used. These 60 chips are divided into four stages as shown in Fig. 5.13. Stage 1 consists of 4 chips (S1-1, S1-2, S1-3 and S1-4), each of which has 16 input signals. Every time either odd or even outputs are selected based on first stage select signal *Sel1*. Stage 2 has total 8 chips, the input of stage 2 is connected to the output of stage 1. 64 inputs are therefore distributed to 256 outputs after first two stages. Note that these two stages with a total of 12 chips are all mounted on Board E. Stages 3 and 4 have 16 and 32 chips, respectively. S3-1 to S3-4 and S4-1 to S4-8 are on Board A, S3-5 to S3-8 and S4-9 to S4-16 are on Board B, S3-9 to S3-12 and S4-17 to S4-24 are on Board C, S3-13 to S3-16 and S4-25 to S4-32 are on Board D. Each

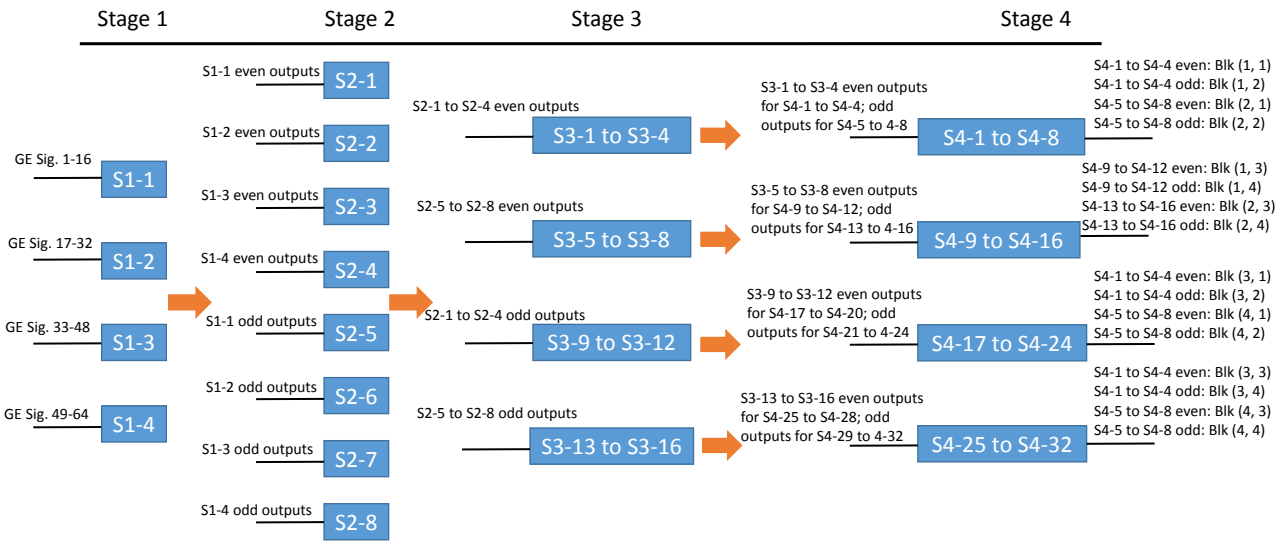


Figure 5.13: **Analog signals distribution through HV2809 chips.**

stage has a select signal to regulate whether even or odd output is chosen and thus which element block is activated. These four select signals are named as Sel1, Sel2, Sel3 and Sel4, respectively. When the chips are enabled, even outputs are on when select signal is logic high and odd outputs are on when select signal is logic low. If block (1,1) should be picked for example, then all four select signals are logic high. If block (2, 2) should be picked on the other hand, Sel1 and Sel2 are logic high and Sel3 and Sel4 are logic low. The rest of the conditions are shown in the figure.

As the motherboard, board E not only receives 64 analog signals but also gets all low voltage differential signaling (LVDS) control signals, 5V, +100V, -100V power signals from *GE* dual probe adaptor. In addition to 12 HV2809 chips and connectors for both GE side and Board A to D, Board E also includes an 8-bit micro-controller (MCU), four LVDS to transistor transistor logic (TTL) converters,

a 5V to 3.3V linear voltage regulator and connectors. The MCU has four inputs TTLA, TTLB, TTLC and TTLD, these four inputs are derived from the outputs of LVDS to TTL converters. The MCU also has four output *enable* signals for LVDS and TTL converters and four output *select* signals for each stage of demultiplexer. Alternately, each of the board A, B, C and D has 12 HV2809 chips, three connectors to receive signals from Board E as well as two probe connectors to the transducer elements. By combining all five circuit boards, analog signals from *GE* adaptor can be distributed to transducer sub-block properly.

5.4 Conclusion

In this work, the sub-block structure of Tx transducer is evaluated using simulation program *Field II* for dual array transducer of the flexible ultrasound system. The system complexity has been significantly reduced when exciting the ultrasound signal from Tx transducer block by block while maintaining the properties of beam pattern. Apodization is also applied to reduce side lobes of the bone imaging. Multiple apodization coefficients can be chosen based on the specific application of the system. Such reduction of side lobes via apodization may contribute to increase the sensitivity of the measurement of hard tissues. Although the resolution of approximately 2.5 mm is incapable to identify single trabeculae, the obtained ultrasound image may provide localized characterization of the tissue density and quality as a potential diagnostic modality. A 32 by 32 phased array transducer layout is designed to realize sub-block structure, total 16 identical blocks with 64 elements are

regulated. Circuit schematic is also created to distribute the analog signal from *GE* adaptor to probe elements. Proper connector pinouts for both *GE* and transducer manufacturing sides are regulated.

Chapter 6

Design and Implication of a Two-dimensional Phased Array Low Intensity Pulsed Ultrasound Transducer System

The development of a low intensity pulsed ultrasound (LIPUS) transducer system is discussed in Section 6.1. Ultrasound pulsing programming is analyzed in Section 6.2. The test results are shown in Section 6.3 and the chapter is concluded in Section 6.4.

6.1 LIPUS System Hardware Design

As indicated by the name, LIPUS works at a relative low intensity, commonly refers to the intensity at or below 50 mW/cm^2. Compared to high intensity focused ultrasound (HIFU) transducer that is widely applied for the destruction of cancerous tumors in different organs, LIPUS is mostly known for enhancing nonunion bone fracture healing process, specifically for femur as well as cartilage in knee. LIPUS can also be used to mitigate bone density loss in micro-gravity environment. Due to the low intensity characteristics, LIPUS should have low to no damage on tissue while stimulating bone. LIPUS device is shown in Fig. 6.1, which includes a phased array transducer and a front-end embedded system based control box which is used to trigger electrical pulses for transducer. The control box is powered by a 36 V medical grade AC-DC converter and a 36 V to 9 V buck DC-DC converter. The control box is only half the size of a piece of letter paper which is highly portable and easy for daily use. LIPUS probe design is introduced in Section 6.1.1 and the electrical control box is investigated in Section 6.1.2.

6.1.1 LIPUS Probe Design

The transducer is a 2-D flat surface aperture transducer working in the phased array mode with a total of 25 elements. As shown in Fig. 6.2 (a), these elements are arrayed in 5 by 5 as a square with a width of 6 cm and a kerf of 1 cm. Fig. 6.2 (b) is the surface of the LIPUS probe, Fig. 6.2 (c) shows the probe with the extensive cable and the connector. Primary related parameters of the transducer in this work are

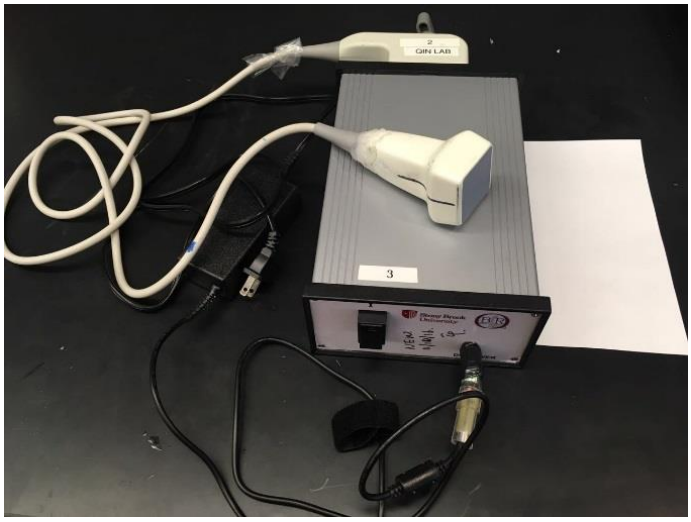


Figure 6.1: **LIPUS device.**

Parameter	Value
Center frequency	1 MHz
Sampling frequency	adjustable
Wavelength (λ)	1.54 mm
Element width (a)	6 mm
Element height (h)	6 mm
Element kerf (k)	1 mm
Size of probe aperture	$34 \times 34\ mm^2$

Table 6.1: Parameters of dual-probe and simulation setting.

listed in Table 6.1. Note that since LIPUS is designed for therapeutic purpose and ultrasound imaging is not required, the transducer therefore works in transmission mode only. Echo receiving mode is not considered in this design. Also note that this device is built to stimulate the bone for 20 minutes a day. The element size is relatively wide to make the transducer more robust.

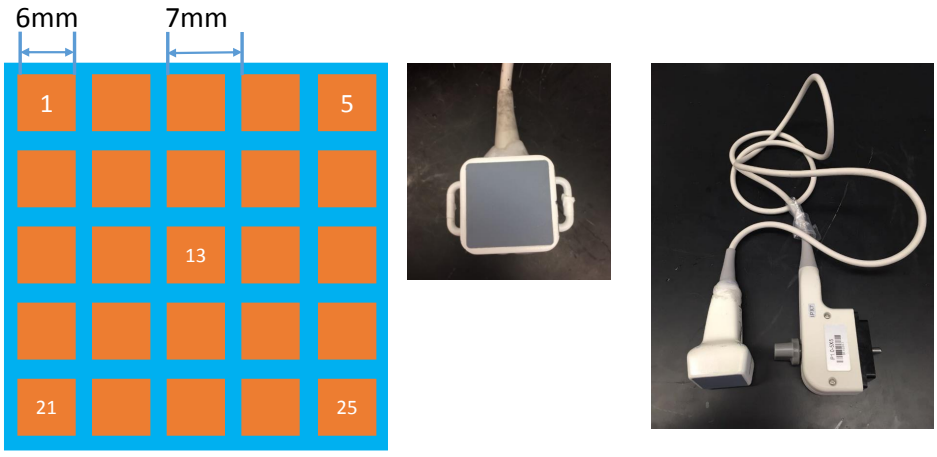


Figure 6.2: **(a) LIPUS probe element layout, (b) Probe surface, (c) Probe with connector.**

6.1.2 LIPUS Electrical Control Box Design

As mentioned in Chapter 2, ultrasound signal is a mechanical signal that is converted from electrical pulse through PZT. LIPUS electrical pulses are generated through the PCB inside the control box. The circuit block diagram and the PCB are shown in Fig. 6.3. Primary components on the board include three 8-bit *Microchip* MCUs, three first-in-first-out (FIFO) memories, 13 TC4467 logic gates, 25 channel CMOS pulsers and a connector board on the left side of the figure. Each channel is connected to one element of the transducer. MCU is programmed through *Microchip MPLAB* ICD3 debugger. One of the MCUs is served as the master MCU and the other two are slaved MCUs. Master MCU as well as the first slave MCU control 9 elements each and the second slave MCU controls 7 elements. Each MCU is connected to a FIFO for saving data. Logic gates work as a buffer to drive

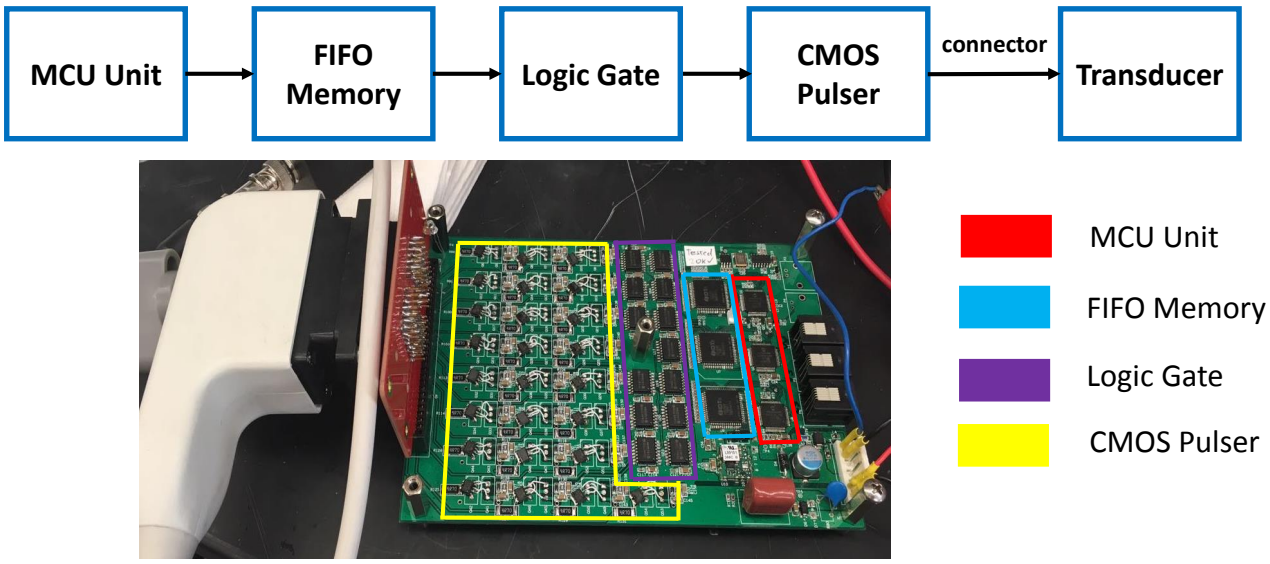


Figure 6.3: **LIPUS block diagram and control printed circuit board.**

MOSFET and are also good for signal isolation. The MCU and FIFO connections are shown in Fig. 6.4 including the data and control signals. Note that only main control signals are included in this figure, other outputs are neglected for simplicity. $TXDA1 - TXDA9$ are data signals that are programmed to MCU and saved in FIFO. These data are then read out to one of the inputs of TC4467 and finally the inversed signals reach the gate of PMOS. Similarly, $TXDB1 - TXDB9$ are sent to the other input of TC4467 and the inversed signals are connected to the gate of NMOS.

During the write process, $FIFOMRS$ is connected to FIFO MRS and is used to clear the whole memory before writing in new data. $FIFOWEN$ is connected to WEN of FIFO. When $FIFOWEN$ is enabled, FIFO is write-enabled and is ready to have data written in. Every time when a pulse is generated on $FIFOWCLK$, one

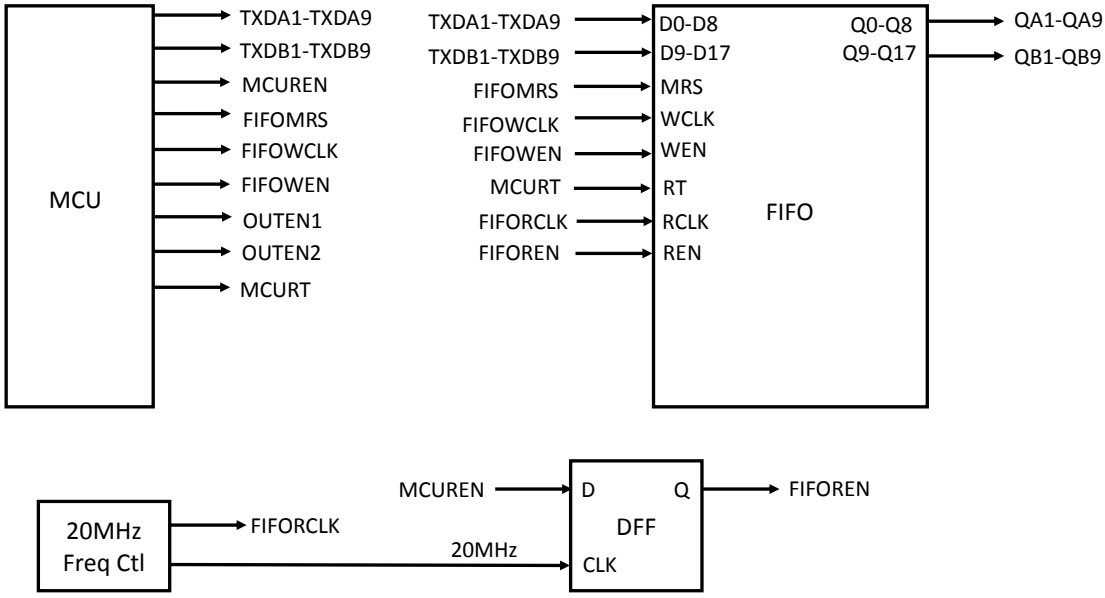


Figure 6.4: **Main control signals in schematic.**

bit of $TXDA1 - TXDA9$ and $TXDB1 - TXDB9$ are written and saved into FIFO. $FIFOWEN$ is set to disabled when writing process is completed. When slaved MCUs finish writing in data to their FIFO, both of these two MCUs need to send a signal to master MCU to notify master MCU that they finished writing data and the corresponding FIFO is ready for reading out data. Master MCU keeps checking the ready signal from slaved MCUs. Once the master MCU receives ready signal from both of slaved MCUs, a LED light is turned on to indicate that writing process is complete and the reading process is about to start.

In reading process, an oscillating signal at 20 MHz is obtained from a control chip and is applied to generate 20 MHz FIFO clock pulse, as shown in Fig. 6.4. One of the outputs of this frequency chip is connected to the clock pin of a D flip-

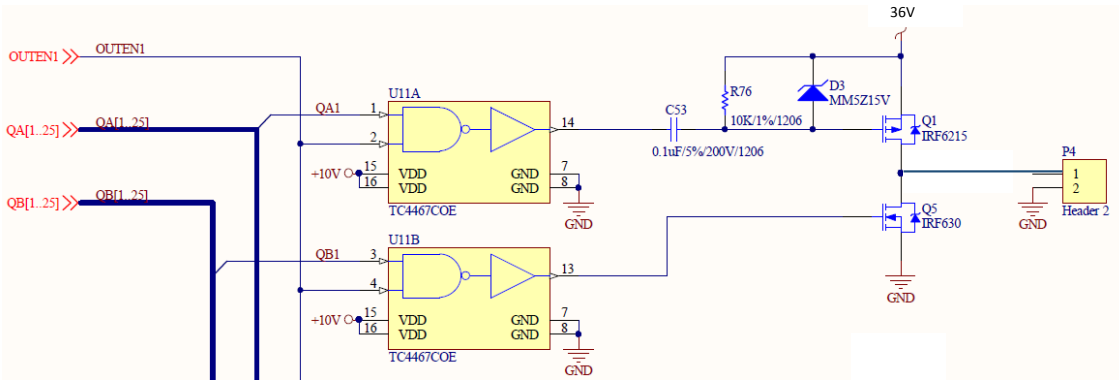


Figure 6.5: **One channel schematic of LIPUS.**

flop (DFF). *MCUREN* is connected to Data pin of this DFF. The output of DFF is *FIFOREN* and this output is connected to *REN* of FIFO. When *MCUREN* is enabled, *FIFOREN* is enabled through DFF and data is read out from FIFO. Each bit lasts for 50 ns (1/ 20 MHz). These data are sent out from the output of FIFO directly to the input of logic gates. *OUTEN*1 and *OUTEN*2 are used to enable TC4467, this should be done before reading out data from FIFO. *MCURT* is the retransmit signal. Each time *MCURT* is enabled, FIFO has the point back to the first bit of the data array.

One of 25 channels that consists of a TC4467 chip and a CMOS pulser is shown in Fig. 6.5. TC4467 includes two NAND gates both followed with a buffer. When *OUTEN*1 and *OUTEN*2 are enabled, data is transferred to one of the input of NAND and the inversed signals are transmitted to the output node. These two signals are then sent to the gate of PMOS and NMOS, respectively, of one channel. A 36 V VDD is connected to the source of PMOS. Based on the signal at the gate of CMOS, the output is a square pulse signal between 36 V and ground.

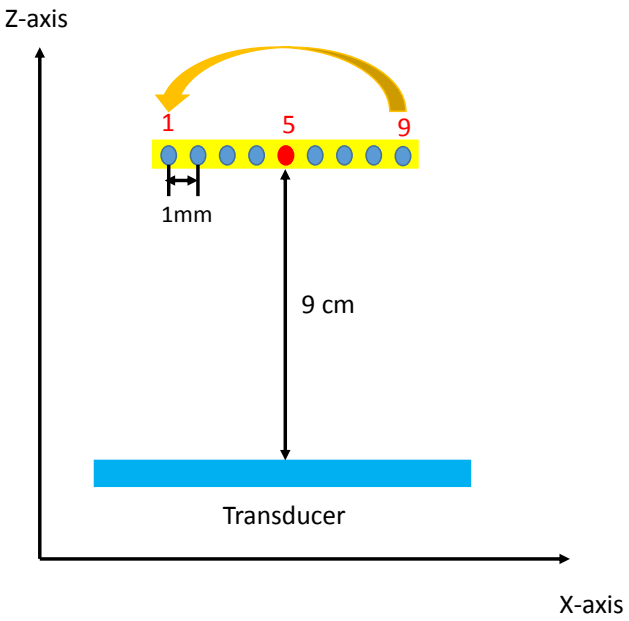


Figure 6.6: **Target focal points.**

6.2 LIPUS Pulsing Programming

LIPUS pulse programming is discussed in this section. As shown in Fig. 6.6, in order to mimic the deepness of hip bone, the focal point is set at 9 cm away from probe surface. For a single focal point setup, the MCUs are programmed to permit all 25 elements simultaneously reach the center focal point 5, which is the red point in the figure. $TXDA1 - TXDA9$ and $TXDB1 - TXDB9$ are then programmed to generate electrical pulses to trigger the ultrasound transducer. One of 25 channels waveform is shown in Fig. 6.7. As mentioned before, each bit in the FIFO represents 50 ns, the numbers shown in this figure represent the number of bit that is maintained at certain logic value. For example, 14 at the beginning of QB means 14 bits are at logic high, which lasts 700 ns. QA and QB are the input of two

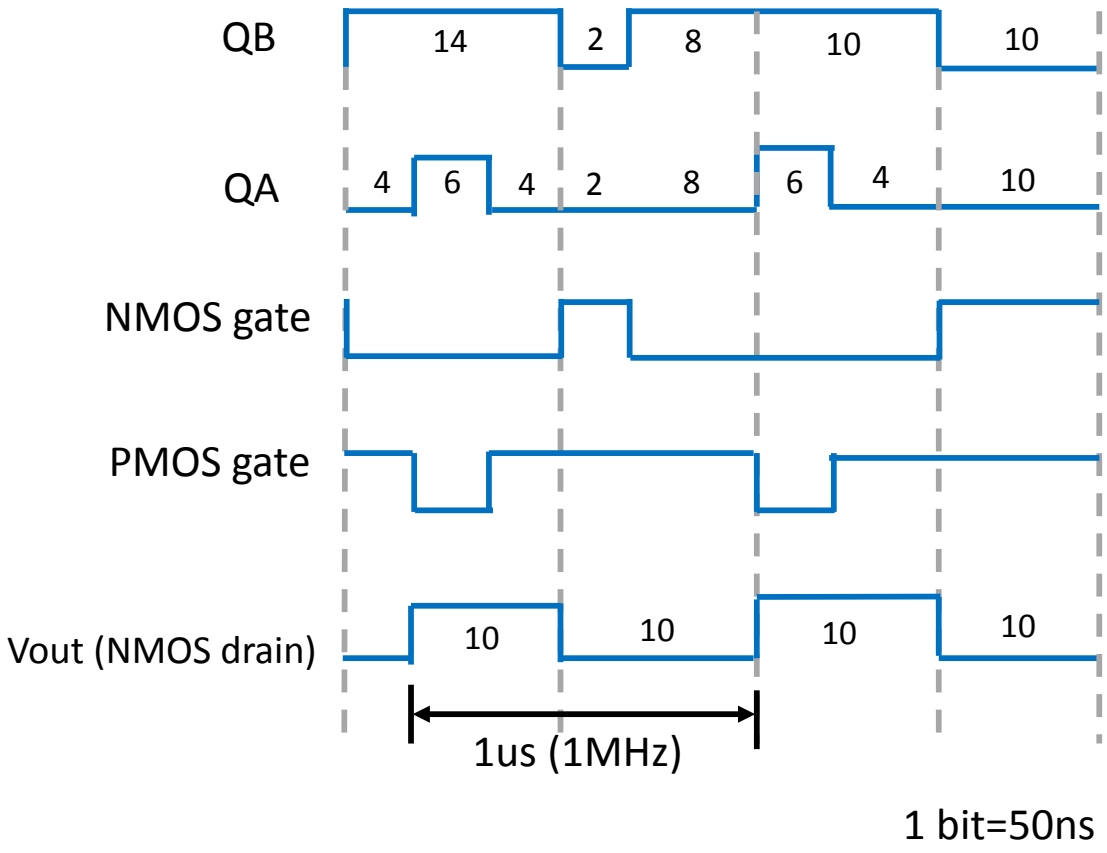
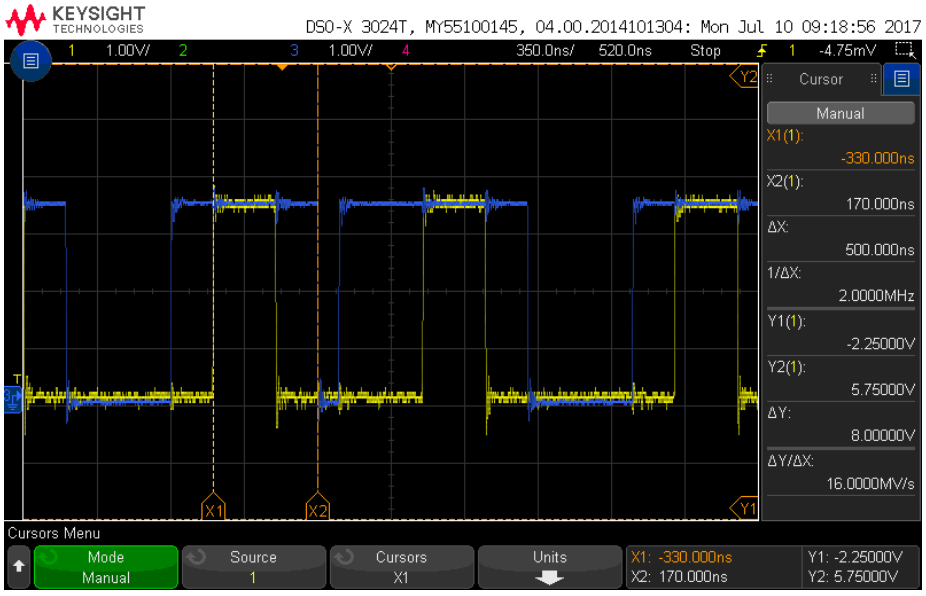


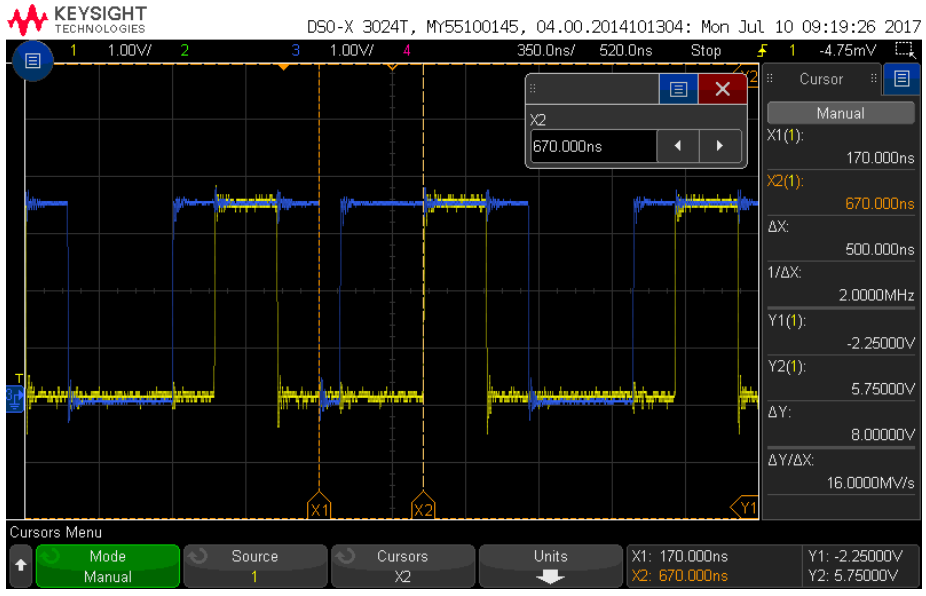
Figure 6.7: **Channel electrical signal waveform.**

NAND gates of TC4467, the other input of these two NAND gates is connected to $OUTEN1$ and $OUTEN2$ respectively. The output of the NAND gate is the inverted input with enabled $OUTEN1$ and $OUTEN2$, therefore, the NMOS gate is the inverted QB and PMOS gate is the inverted QA. Both are shown in the figure. Since LIPUS center frequency is 1 MHz, the electrical pulse period is expected to be 1 μs. This is realized by adjusting the gate of NMOS and PMOS. Note that PMOS and NMOS should not be turned on at the same time in order to avoid a short circuit path from VDD to ground. As shown in the figure, when PMOS gate is turned on at 5th bit, NMOS gate is still off, Vout is therefore connected to VDD. When PMOS is turned off after 6 bits, NMOS is off for another 4 bits to avoid the short circuit path. Vout is then connected to ground when NMOS is ON. Note that the Vout waveform in this figure is only 2.2 μs for simplicity. In practice, Vout waveform lasts for 200 μs. The measured input waveforms of TC4467 chip from oscilloscope are provided in Fig. 6.8. Blue waveform is QB and yellow waveform is QA. As shown in this figure, the blue and yellow waveforms match the waveform shown in Fig. 6.7 as expected. The cursors indicate 500 ns in (a) logic high of Vout, in (b) the logic low of Vout. The measured electrical output signal waveforms at the drain of NMOS are shown in Fig. 6.9 which is a square wave from 36 V to GND. As shown in this figure, each scaled box on the screen is 250 ns, both logic high and logic low occupy 500 ns time in (a) results a 1 MHz frequency, the same as the center frequency of the transducer.

After the single channel pulse waveform is verified, the delay time module is considered for the phased array transducer focusing. The flowchart of single fo-

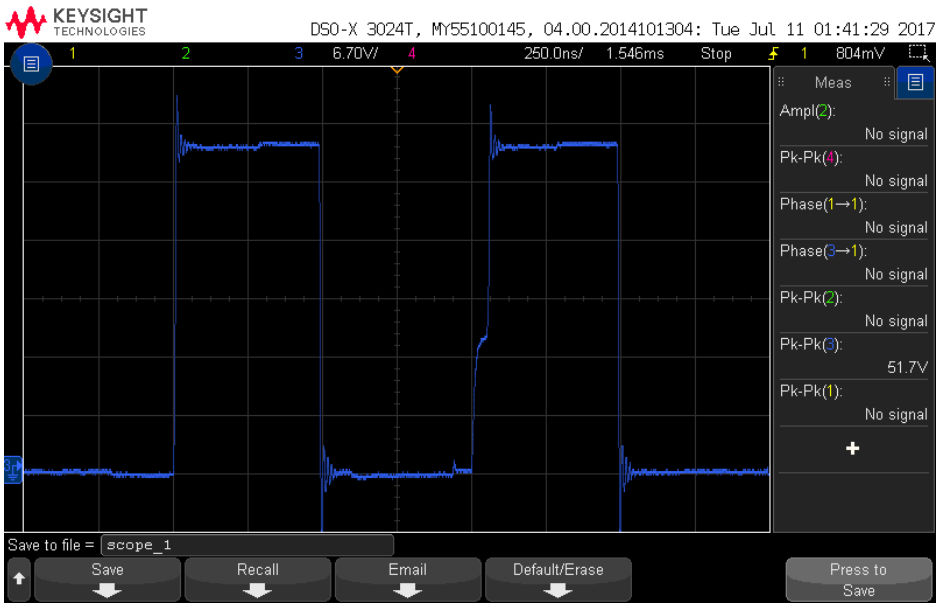


(a)

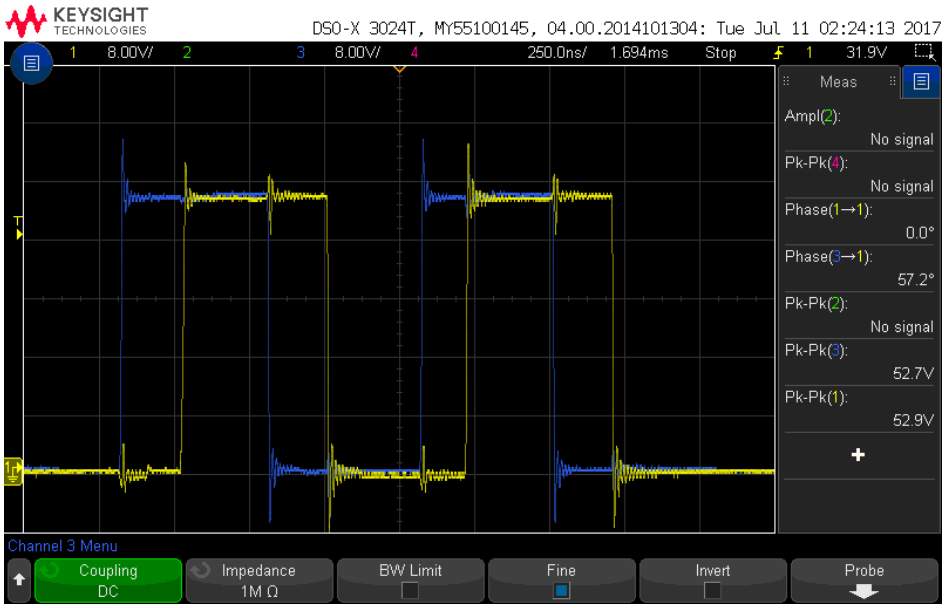


(b)

Figure 6.8: **Measured channel electrical signal waveform: (a) first half period of pulse; (b) second half period of pulse.**



(a)



(b)

Figure 6.9: **(a) measured electrical output signal, (b) two channel measured electrical output signals.**

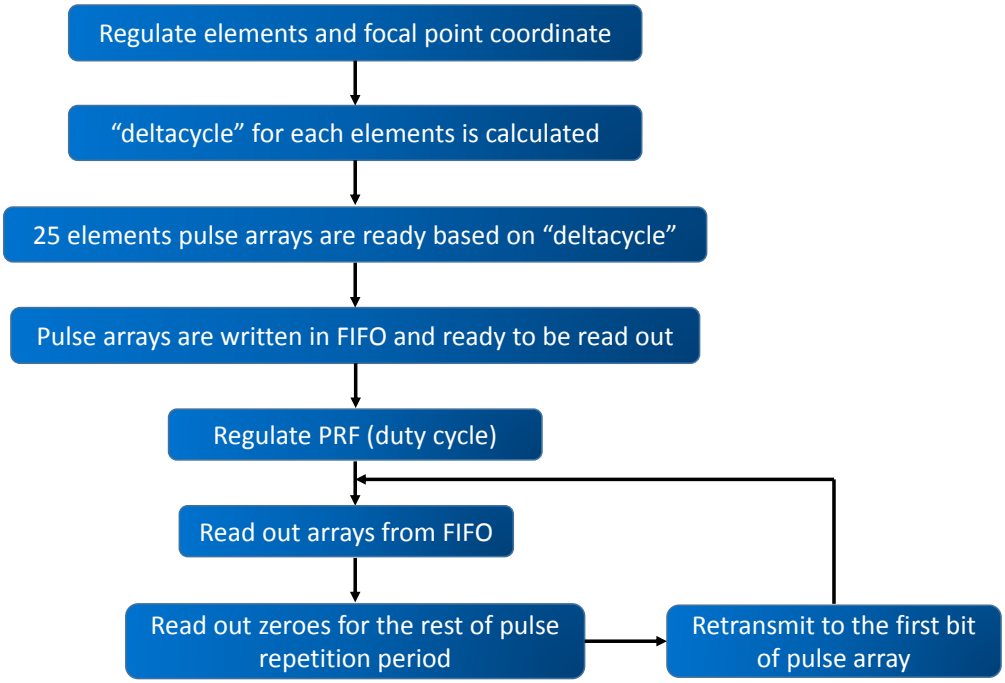


Figure 6.10: **Single focal point flowchart.**

cal point programming is shown in Fig. 6.10. The coordinate of all elements and the focal point are regulated based on the actual physical sizes and distances. The longest distance from probe to center is the distance from the elements at four corners. In order to have the ultrasound waves fired from all 25 elements in phase to reach the maximum intensity at the focal points, these four elements should fire the ultrasound signal first and the rest of the elements need to wait for a certain delay time ”deltadelay” to fire based on the distance difference. As expected, the center element 13 has the longest delay time due to the shortest distance. Since each bit in FIFO lasts 50 ns, the ”deltadelay” is calculated and then divided by 50 ns and represented by ”delaycycle”. This ”delaycycle” refers to how many idle bits need

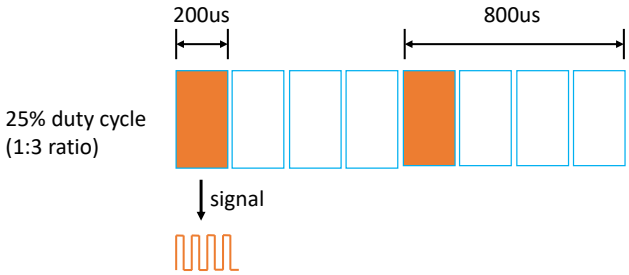
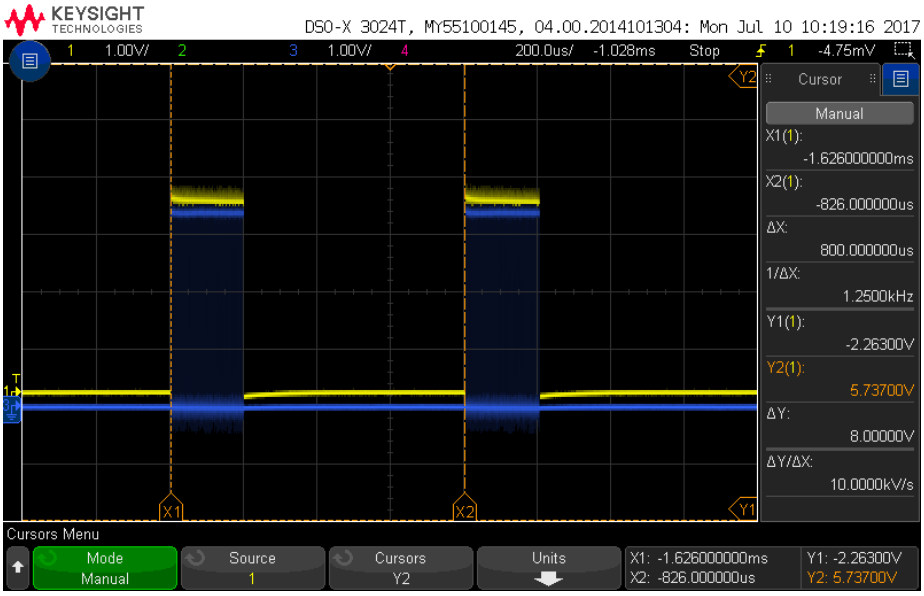
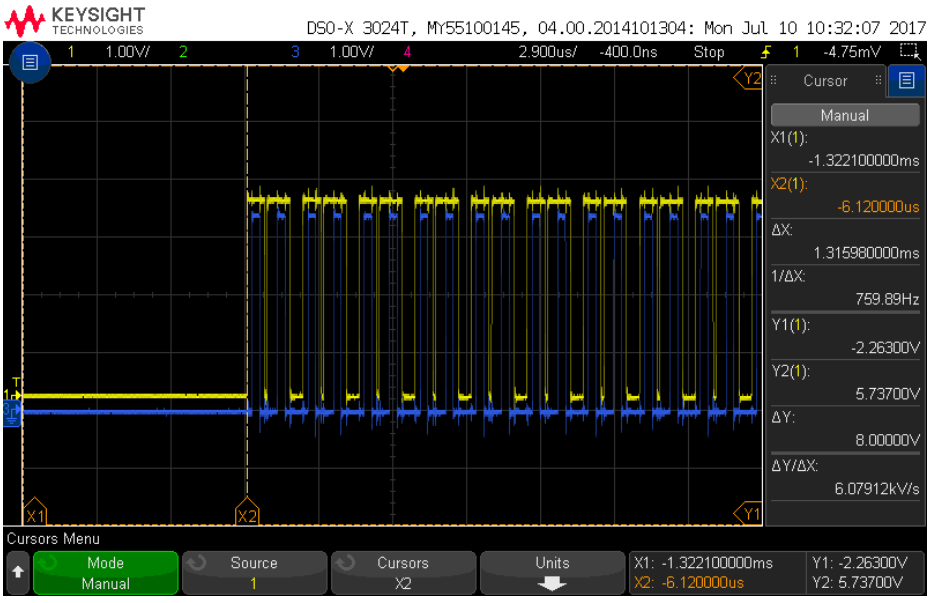


Figure 6.11: **Pulse duty cycle.**

to be inserted before starting the pulse signal. 25 different ”delaycycle” signals are then inserted to each of the elements at the front of the electrical signal so that all signals are in phase. These electrical pulses are then written into three FIFO memories. Two channels are selected and the electrical outputs are measured together, as shown in Fig. 6.9 (b). There is a certain time delay between these two signals due to the distance difference from these two elements to the focal point. Next, the pulse repetition frequency is regulated based on the requirement of the application. For example, with a 25% duty cycle as shown in Fig. 6.11, the pulse duration is set as 200 μs and the idle time is 600 μs, the pulse repetition period is 800 μs. A timer is set to count the idle time after the pulse duration time. When pulse array is read from FIFO, the timer starts working until the goal waiting time is reached, then the FIFO is retransmitted to the first bit of pulse array and restart reading out data. This process is repeated as long as the power is on. The measured 25% duty cycle waveform at the input of TC4467 is provided in (a) of Fig. 6.12. Pulse duration occupies the entire box on the screen which is 200 μs. The cursors show that the pulse repetition period is exactly 800 μs. Fig. 6.12 (b) is the zoomed in figure which is the repetition of the waveform shown in Fig. 6.7. Blue waveform is QA



(a)



(b)

Figure 6.12: **(a) TC4467 input duty cycle measured from oscilloscope, (b) zoomed in result of (a).**

and yellow waveform is QB.

This ultrasound transducer can work on trabecular bone and large tissue, which are typically in the range of centimeters instead of one spot. Single focal point is therefore extended to multiple focal points. As indicated in Fig. 6.6, s total of 9 focal points are set along lateral direction, where the gap between two adjacent focal points is 1 mm. Initially, all elements target to focal point 1 on the very left. After 10 ms stimulation, the target is switched to focal point 2. It takes 90 ms to cover 9 focal points. Once the stimulation on focal point 9 is done, the target is switched back to focal point 1 and the process is repeated. Note that the pulse duration, pulse repetition frequency as well as the stimulation time on each focal point are all adjustable based on the need of the application.

6.3 Test Results

LIPUS probe test setup is shown in Fig. 6.13. LIPUS probe and hydrophone are set in the water tank filled with degassed water. The probe is set on a motor and can be moved back and forth to adjust the position, hydrophone is fixed on the other side as the receiving side. The distance between probe and hydrophone is 9 cm to mimic the distance from skin to hip bone. The receiving ultrasound signal is converted back to electrical signal through hydrophone and can be observed on oscilloscope.

The transducer elements focus on focal point 1 located at (-4, 0, 90) mm. All elements are transmitted with different delay time and reach the focal point simul-

Figure 6.13: **Test setup for LIPUS: (a) Probe and hydrophone setup, (b) Board, oscilloscope setup and connection.**

taneously. The electrical pulse duration is set as 200 μs with a pulse repetition frequency (PRF) of 800 μs. The duty cycle is calculated as pulse duration over PRF, which is 25% in this case. The measured ultrasound pulse receiving from hydrophone is shown in Fig. 6.14, the ultrasound pulse duration is 200 μs with 800 μs PRF, which is the same as the electrical pulse. Next, the pulse duration is maintained at 200 μs, while the duty cycle is adjusted as 12%, 15% and 19% separately. The corresponding PRF is 1.5 ms, 1.3 ms and 1.06 ms respectively. The measurement results are shown in Fig. 6.15 (b). X-axis is along lateral direction, y-axis is axial direction and z-axis is the ultrasound signal intensity. With the focal point fixed at 1, five points along lateral direction with x-axis coordinate of -4, -3, -2, -1 and 0 mm are measured. As shown in this figure, the highest intensity appears at the focal point, and the intensity starts decreasing gradually when the measuring points get farther away from the focal point. For example, when duty cycle is set

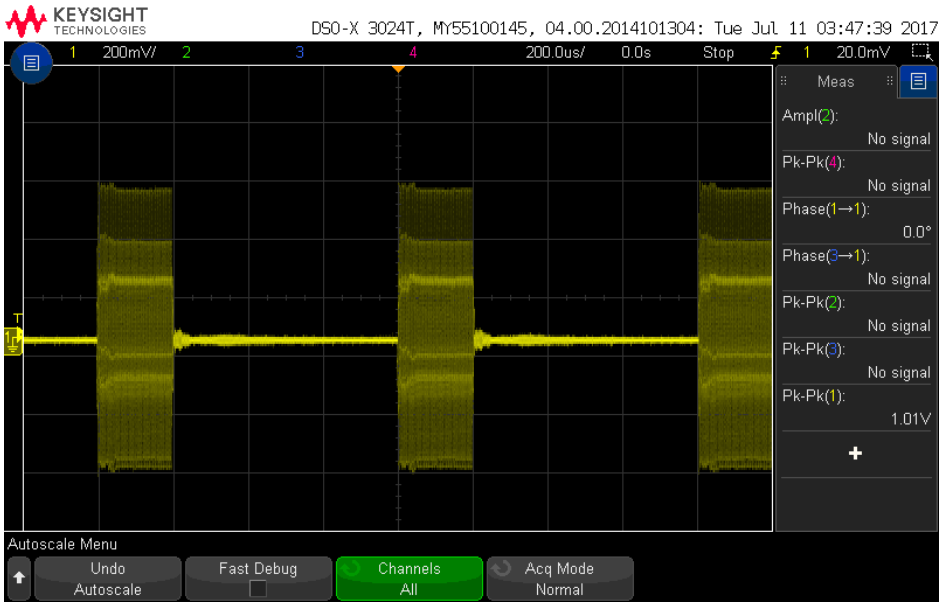


Figure 6.14: **LIPUS testing ultrasound signal with elements focus on focal point 1.**

as 25%, the intensities along x-axis from -4 to 0 mm are 397, 329, 187, 61 and 38 mW/cm^2 respectively. The highest measured intensity is located at focal point (-4, 0, 90) cm with 25% duty cycle, and the intensity equals to 397 mW/cm^2, the lowest intensity appears at (0, 0, 90) cm when the duty cycle is 12%, the intensity is 20 mW/cm^2. The focal point is then switched to (0, 0, 90) mm located at the center of lateral and axial direction, which is focal point 5 in Fig. 6.6. The intensity is then measured at the same locations and the results are shown in Fig. 6.15 (a). Similar to focal point 1, the center point in all duty cycles reaches the highest intensity and the value starts decreasing as the measurement position gets farther away. The highest intensity is 349 mW/cm^2 at the center point with 25% duty cycle and the lowest intensity is 20 mW/cm^2 appears at the side point with 12% duty cycle. The comparison of these intensity values from (a) and (b) of Fig. 6.15 shows that there is no

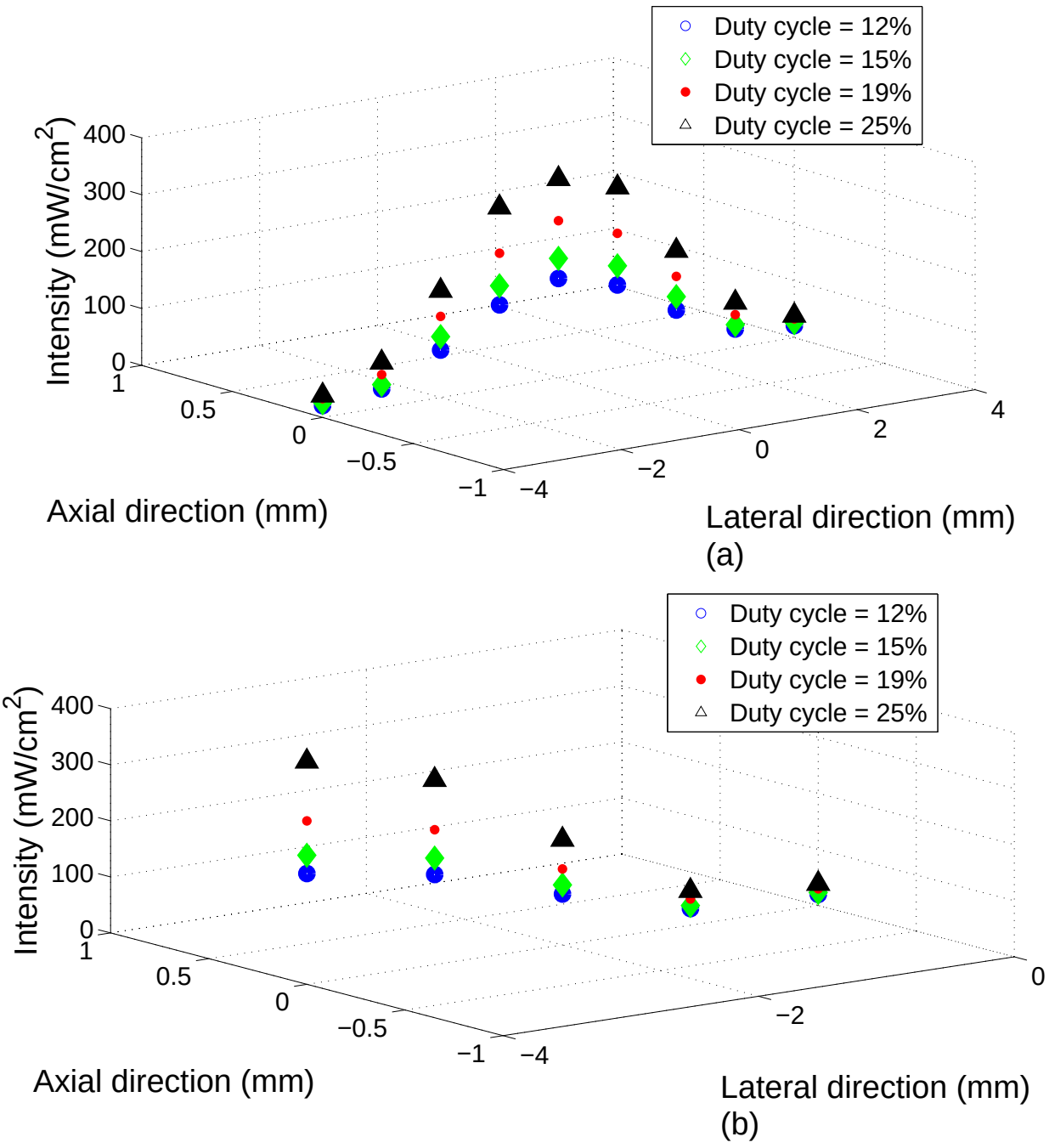


Figure 6.15: **Intensity measurement: (a) all elements focus on focal point 5, (b) all elements focus on focal point 1.**

significant difference between the focal point 1 and focal point 5. Theoretically, the intensity at center point 5 should be higher than point 1 because the longest distance from the element to this target is shorter. In real measurement, both of them have very similar intensity values, the intensity at point 1 is even slightly higher than that of point 5, primarily due to measurement error.

The intensity results measured at 25% duty cycle are almost twice higher than the intensity with 12% duty cycle. In order to reach the low intensity for the application of this device, duty cycle should be set lower than 15%. In addition to the adjustment of duty cycle, the intensity can also be controlled by the pulse voltage, this voltage value can be reduced from 36 V to further decrease the intensity.

6.4 Conclusion

An embedded system based control box with a low intensity 5 by 5 2-D phased array transducer is investigated in this chapter. The electrical signal control box has 25 channels to trigger 25 transducer elements. These 25 electrical signals are triggered in a certain time sequence to reach the focal point in phase with the maximum intensity. The pulse duration as well as pulse repetition frequency are adjustable for specific application. Both electrical signal and ultrasound signal waveforms with different duty cycle from 12% to 25% are tested and measured. The intensities can be controlled by adjusting pulse voltage as well as pulse repetition frequency.

Chapter 7

Conclusion and Future Work

Switching noise and energy efficiency are two primary design constraints for dense mixed-signal ICs. In this thesis, figures-of-merit to evaluate the significance of switching noise in analog circuits are proposed to determine the dominant noise source. A package embedded buck DC-DC converter with high power efficiency is also presented. These methodologies are helpful in the design of biomedical transducers where highly dense PCBs with DC-DC converters are developed. The second part of this thesis is on front-end two dimensional phased array ultrasound transducer system. A flexible ultrasound system gray-scale imaging simulation as well as hardware design are discussed. An embedded system based 5 by 5 low intensity ultrasound system for therapeutic purpose is developed. The contributions of this thesis are summarized in Section 7.1. Several future directions are discussed in Section 7.2.

7.1 Thesis Summary

Two resesarch studies have been described in the first part of this thesis: 1) the estimation of input-referred switching noise in analog/RF circuits, 2) investigation of a package-embedded spiral inductor with application to switching buck converter. With higher and heterogenous integration, sensitive analog / RF circuits suffer from switching noise which degrades the system performance and may cause functional failure. Alternatively, analog circuits also have intrinsic device noise. The first research study in this thesis provides a methodology on how to determine and mitigate the most significant noise source, as described in Chapter 3. Switching noise is first transferred from MOS transistor bulk node to the amplifier output and then transferred to the amplifier input node. Also, the equivalent input device noise that includes thermal and flicker noise is quantified at the input node. By determining the input-referred switching noise in the analog circuit blocks and comparing with the intrinsic device noise, dominance noise regions for both noise sources are developed in frequency domain. This comparison is achieved as a function of multiple parameters that characterize switching noise in the time domain such as peak amplitude, period, oscillation frequency within each period, and damping coefficient. These results provide guidelines for the signal isolation process. A noise mitigation approach, reverse body biasing, is also proposed to alleviate the effect of switching noise by weakening the bulk-to-input transfer function as opposed to reducing the switching noise amplitude at the bulk nodes.

Chapter 4 focuses on a package-embedded spiral inductor with application to switching buck converter. Passive components such as inductors and capacitors are

highly costly for on-chip integration, while these passive components are crucial to satisfy several performance criteria such as power efficiency and output noise. The second research study of this thesis thus focuses on the package embedded DC-DC converter and provides a methodology to save on-chip area while achieving high power efficiency. By utilizing spirals inductors embedded within a flip-chip package, significant on-chip area is saved without implementing an off-chip inductor. Also, the switching frequency of the DC-DC converter is 50 MHz since a larger inductance can be achieved by exploiting the flexibility of the package structure. Thus more than 87% conversion efficiency is achieved.

The second part of this thesis focuses on ultrasound transducer system design and simulation where noise and power efficiency are important design considerations. In Chapter 5, a novel 2-D array ultrasound research instrument, named Flexible Ultrasound System (FUS), is discussed. The system is integrated into existing advanced ultrasound imaging system with a specified interface of clinical diagnostic imaging capability. The sub-block structure is proposed and simulated for a 27 by 27 phased array transducer. The system divides 729 elements into 9 square blocks with 9 by 9 elements in each block. The block is activated in sequence and the receiving signal is summed up at the Rx side for digital image processing. This procedure is simulated in *FIELD II*, the results verify the transducer design specifications by checking the target imaging and lateral resolution. The apodization is also simulated by applying a Hann window. The system hardware is significantly less complicated as compared to traditional phased array transducer where only 81 electrical signals are required instead of 729. Furthermore, the B-mode imaging

quality as well as the lateral resolution are maintained without any degradation. Also, challenges in adjusting the position and orientation of transducer are avoided by this highly flexible phased array design. The sub-block hardware design is realized by applying high voltage analog switch ICs that serve as demultiplexer. These chips are located on five boards to select the appropriate elements to be activated.

Astronauts who live and work in the international space station (ISS), a microgravity environment, exhibit a bone density loss of 2% per month as compared to 1.5% per year on earth. Astronauts need to have two hour long workouts to enhance bone density. Ultrasound transducer is applied as the treatment for bone density loss. In Chapter 6, a portable phased array low intensity pulsed ultrasound system that includes 25 elements is developed and proposed for therapeutic purpose. This transducer is controlled by an embedded electrical control box which includes microcontrollers (MCU), followed by FIFO memories, logic gates and MOSFET drivers. Each element is controlled by individual channel and can be focused on various target points. Pulse repetition frequency and duty cycle are adjustable and thus the intensity of the ultrasound signal can be changed based on specific therapeutic purposes. By programming the MCU, 25 elements can be triggered in a specific time sequence to simultaneously reach the same target without moving the transducer. These elements can also be split into groups and excite group by group as a linear transducer.

7.2 Future Work

The future work is primarly related to the ultrasound transducer system. For FUS, future steps are necessary for both hardware and software tasks. Hardware task includes the printed circuit boards (PCBs) design and manufacturing. These circuit boards will be integrated on the back side of the transducer. The transducer with integrated PCB will then be combined with *GE* Vivid E95 ultrasound machine through the probe adaptor as an entire flexible ultrasound system. Software task includes the Matlab and C++ programming by using *GE* research user SDK to control the electrical signals that are transmitted to the transducer. LIPUS is currently used for the first animal experiment. Two turkeys are having their luna bone fractured and are under treatment for 20 minutes a day, 5 days a week for 6 weeks. The LIPUS will also be applied for rat study. The experiments are expected to have low damaged tissue, low pain data and low serum pain biomarkers after the treatment. The successful animal studies will bring LIPUS to FDA clinical trial and eventually have the device be applied to human beings for nonunion fracture enhancement as well as bone density loss prevention.

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